```
{'wire_C1': ['INPUT', 'wire_C1', True, '0'], 'wire_C0': ['INPUT', 'wire_C0', True, '1'], 'wire_X0': ['INPUT', 'wire_X0', True, '0'], 'wire_X1': ['INPUT', 'wire_X1', True, '1'], 'wire_X2': ['INPUT', 'wire_
X2', True, '1'], 'wire_X3': ['INPUT', 'wire_X3', True, '0'], 'wire_c': ['NOT', ['wire_C1'], False, 'U'], 'wire_f': ['NOT', ['wire_C0'], False, 'U'], 'wire_g': ['AND', ['wire_f', 'wire_c', 'wire_X0'], Fals
e, 'U'], 'wire_h': ['AND', ['wire_c', 'wire_C0', 'wire_X1'], False, 'U'], 'wire_i': ['AND', ['wire_C1', 'wire_f', 'wire_X2'], False, 'U'], 'wire_j': ['AND', ['wire_C0', 'wire_C1', 'wire_X3'], False, 'U'],
 'wire_M': ['OR', ['wire_g', 'wire_h', 'wire_i', 'wire_j'], False, 'U'], 'INPUT_WIDTH': ['input width:', 6], 'INPUTS': ['Input list', ['wire_C1', 'wire_C0', 'wire_X0', 'wire_X1', 'wire_X2', 'wire_X3']], '
OUTPUTS': ['Output list', ['wire_M']], 'GATES': ['Gate list', ['wire_c', 'wire_f', 'wire_g', 'wire_h', 'wire_i', 'wire_j', 'wire_M']]}
Progress: updating wire_c = 1 as the output of NOT for:
wire_C1 = 0

Press Enter to Continue...

Progress: updating wire_f = 0 as the output of NOT for:
wire_C0 = 1

Press Enter to Continue...

Progress: updating wire_g = 0 as the output of AND for:
wire_f = 0
wire_c = 1
wire_X0 = 0

Press Enter to Continue...

Progress: updating wire_h = 1 as the output of AND for:
wire_c = 1
wire_C0 = 1
wire_X1 = 1

Press Enter to Continue...

Progress: updating wire_i = 0 as the output of AND for:
wire_C1 = 0
wire_f = 0
wire_X2 = 1

Press Enter to Continue...

Progress: updating wire_j = 0 as the output of AND for:
wire_C0 = 1
wire_C1 = 0
wire_X3 = 0

Press Enter to Continue...

Progress: updating wire_M = 1 as the output of OR for:
wire_g = 0
wire_h = 1
wire_i = 0
wire_j = 0

Press Enter to Continue...


 *** Finished simulation - resulting circuit:

{'wire_C1': ['INPUT', 'wire_C1', True, '0'], 'wire_C0': ['INPUT', 'wire_C0', True, '1'], 'wire_X0': ['INPUT', 'wire_X0', True, '0'], 'wire_X1': ['INPUT', 'wire_X1', True, '1'], 'wire_X2': ['INPUT', 'wire_
X2', True, '1'], 'wire_X3': ['INPUT', 'wire_X3', True, '0'], 'wire_c': ['NOT', ['wire_C1'], True, '1'], 'wire_f': ['NOT', ['wire_C0'], True, '0'], 'wire_g': ['AND', ['wire_f', 'wire_c', 'wire_X0'], True,
'0'], 'wire_h': ['AND', ['wire_c', 'wire_C0', 'wire_X1'], True, '1'], 'wire_i': ['AND', ['wire_C1', 'wire_f', 'wire_X2'], True, '0'], 'wire_j': ['AND', ['wire_C0', 'wire_C1', 'wire_X3'], True, '0'], 'wire
_M': ['OR', ['wire_g', 'wire_h', 'wire_i', 'wire_j'], True, '1'], 'INPUT_WIDTH': ['input width:', 6], 'INPUTS': ['Input list', ['wire_C1', 'wire_C0', 'wire_X0', 'wire_X1', 'wire_X2', 'wire_X3']], 'OUTPUTS
': ['Output list', ['wire_M']], 'GATES': ['Gate list', ['wire_c', 'wire_f', 'wire_g', 'wire_h', 'wire_i', 'wire_j', 'wire_M']]}

 *** Summary of simulation:
011010 -> 1 written into output file.
```

```
X2', True, '1'], 'wire_X3': ['INPUT', 'wire_X3', True, '1'], 'wire_c': ['NOT', ['wire_C1'], False, 'U'], 'wire_f': ['NOT', ['wire_C0'], False, 'U'], 'wire_g': ['AND', ['wire_f', 'wire_c', 'wire_X0'], Fals
e, 'U'], 'wire_h': ['AND', ['wire_c', 'wire_C0', 'wire_X1'], False, 'U'], 'wire_i': ['AND', ['wire_C1', 'wire_f', 'wire_X2'], False, 'U'], 'wire_j': ['AND', ['wire_C0', 'wire_C1', 'wire_X3'], False, 'U'],
 'wire_M': ['OR', ['wire_g', 'wire_h', 'wire_i', 'wire_j'], False, 'U'], 'INPUT_WIDTH': ['input width:', 6], 'INPUTS': ['Input list', ['wire_C1', 'wire_C0', 'wire_X0', 'wire_X1', 'wire_X2', 'wire_X3']], '
OUTPUTS': ['Output list', ['wire_M']], 'GATES': ['Gate list', ['wire_c', 'wire_f', 'wire_g', 'wire_h', 'wire_i', 'wire_j', 'wire_M']]}
Progress: updating wire_c = 0 as the output of NOT for:
wire_C1 = 1

Press Enter to Continue...

Progress: updating wire_f = 0 as the output of NOT for:
wire_C0 = 1

Press Enter to Continue...

Progress: updating wire_g = 0 as the output of AND for:
wire_f = 0
wire_c = 0
wire_X0 = 1

Press Enter to Continue...

Progress: updating wire_h = 0 as the output of AND for:
wire_c = 0
wire_C0 = 1
wire_X1 = 1

Press Enter to Continue...

Progress: updating wire_i = 0 as the output of AND for:
wire_C1 = 1
wire_f = 0
wire_X2 = 1

Press Enter to Continue...

Progress: updating wire_j = 1 as the output of AND for:
wire_C0 = 1
wire_C1 = 1
wire_X3 = 1

Press Enter to Continue...

Progress: updating wire_M = 1 as the output of OR for:
wire_g = 0
wire_h = 0
wire_i = 0
wire_j = 1

Press Enter to Continue...


 *** Finished simulation - resulting circuit:

{'wire_C1': ['INPUT', 'wire_C1', True, '1'], 'wire_C0': ['INPUT', 'wire_C0', True, '1'], 'wire_X0': ['INPUT', 'wire_X0', True, '1'], 'wire_X1': ['INPUT', 'wire_X1', True, '1'], 'wire_X2': ['INPUT', 'wire_
X2', True, '1'], 'wire_X3': ['INPUT', 'wire_X3', True, '1'], 'wire_c': ['NOT', ['wire_C1'], True, '0'], 'wire_f': ['NOT', ['wire_C0'], True, '0'], 'wire_g': ['AND', ['wire_f', 'wire_c', 'wire_X0'], True,
'0'], 'wire_h': ['AND', ['wire_c', 'wire_C0', 'wire_X1'], True, '0'], 'wire_i': ['AND', ['wire_C1', 'wire_f', 'wire_X2'], True, '0'], 'wire_j': ['AND', ['wire_C0', 'wire_C1', 'wire_X3'], True, '1'], 'wire
_M': ['OR', ['wire_g', 'wire_h', 'wire_i', 'wire_j'], True, '1'], 'INPUT_WIDTH': ['input width:', 6], 'INPUTS': ['Input list', ['wire_C1', 'wire_C0', 'wire_X0', 'wire_X1', 'wire_X2', 'wire_X3']], 'OUTPUTS
': ['Output list', ['wire_M']], 'GATES': ['Gate list', ['wire_c', 'wire_f', 'wire_g', 'wire_h', 'wire_i', 'wire_j', 'wire_M']]}

 *** Summary of simulation:
111111 -> 1 written into output file.
```

```
{'wire_C1': ['INPUT', 'wire_C1', True, '0'], 'wire_C0': ['INPUT', 'wire_C0', True, '1'], 'wire_X0': ['INPUT', 'wire_X0', True, '0'], 'wire_X1': ['INPUT', 'wire_X1', True, '1'], 'wire_X2': ['INPUT', 'wire_
X2', True, '0'], 'wire_X3': ['INPUT', 'wire_X3', True, '1'], 'wire_c': ['NOT', ['wire_C1'], False, 'U'], 'wire_f': ['NOT', ['wire_C0'], False, 'U'], 'wire_g': ['AND', ['wire_f', 'wire_c', 'wire_X0'], Fals
e, 'U'], 'wire_h': ['AND', ['wire_c', 'wire_C0', 'wire_X1'], False, 'U'], 'wire_i': ['AND', ['wire_C1', 'wire_f', 'wire_X2'], False, 'U'], 'wire_j': ['AND', ['wire_C0', 'wire_C1', 'wire_X3'], False, 'U'],
 'wire_M': ['OR', ['wire_g', 'wire_h', 'wire_i', 'wire_j'], False, 'U'], 'INPUT_WIDTH': ['input width:', 6], 'INPUTS': ['Input list', ['wire_C1', 'wire_C0', 'wire_X0', 'wire_X1', 'wire_X2', 'wire_X3']], '
OUTPUTS': ['Output list', ['wire_M']], 'GATES': ['Gate list', ['wire_c', 'wire_f', 'wire_g', 'wire_h', 'wire_i', 'wire_j', 'wire_M']]}
Progress: updating wire_c = 1 as the output of NOT for:
wire_C1 = 0

Press Enter to Continue...

Progress: updating wire_f = 0 as the output of NOT for:
wire_C0 = 1

Press Enter to Continue...

Progress: updating wire_g = 0 as the output of AND for:
wire_f = 0
wire_c = 1
wire_X0 = 0

Press Enter to Continue...

Progress: updating wire_h = 1 as the output of AND for:
wire_c = 1
wire_C0 = 1
wire_X1 = 1

Press Enter to Continue...

Progress: updating wire_i = 0 as the output of AND for:
wire_C1 = 0
wire_f = 0
wire_X2 = 0

Press Enter to Continue...

Progress: updating wire_j = 0 as the output of AND for:
wire_C0 = 1
wire_C1 = 0
wire_X3 = 1

Press Enter to Continue...

Progress: updating wire_M = 1 as the output of OR for:
wire_g = 0
wire_h = 1
wire_i = 0
wire_j = 0

Press Enter to Continue...


 *** Finished simulation - resulting circuit:

{'wire_C1': ['INPUT', 'wire_C1', True, '0'], 'wire_C0': ['INPUT', 'wire_C0', True, '1'], 'wire_X0': ['INPUT', 'wire_X0', True, '0'], 'wire_X1': ['INPUT', 'wire_X1', True, '1'], 'wire_X2': ['INPUT', 'wire_
X2', True, '0'], 'wire_X3': ['INPUT', 'wire_X3', True, '1'], 'wire_c': ['NOT', ['wire_C1'], True, '1'], 'wire_f': ['NOT', ['wire_C0'], True, '0'], 'wire_g': ['AND', ['wire_f', 'wire_c', 'wire_X0'], True,
'0'], 'wire_h': ['AND', ['wire_c', 'wire_C0', 'wire_X1'], True, '1'], 'wire_i': ['AND', ['wire_C1', 'wire_f', 'wire_X2'], True, '0'], 'wire_j': ['AND', ['wire_C0', 'wire_C1', 'wire_X3'], True, '0'], 'wire
_M': ['OR', ['wire_g', 'wire_h', 'wire_i', 'wire_j'], True, '1'], 'INPUT_WIDTH': ['input width:', 6], 'INPUTS': ['Input list', ['wire_C1', 'wire_C0', 'wire_X0', 'wire_X1', 'wire_X2', 'wire_X3']], 'OUTPUTS
': ['Output list', ['wire_M']], 'GATES': ['Gate list', ['wire_c', 'wire_f', 'wire_g', 'wire_h', 'wire_i', 'wire_j', 'wire_M']]}

 *** Summary of simulation:
101010 -> 1 written into output file.
```

```
OUTPUTS': ['Output list', ['wire_M']], 'GATES': ['Gate list', ['wire_c', 'wire_f', 'wire_g', 'wire_h', 'wire_i', 'wire_j', 'wire_M']]}
Progress: updating wire_c = 0 as the output of NOT for:
wire_C1 = 1

Press Enter to Continue...

Progress: updating wire_f = 1 as the output of NOT for:
wire_C0 = 0

Press Enter to Continue...

Progress: updating wire_g = 0 as the output of AND for:
wire_f = 1
wire_c = 0
wire_X0 = 1

Press Enter to Continue...

Progress: updating wire_h = 0 as the output of AND for:
wire_c = 0
wire_C0 = 0
wire_X1 = 0

Press Enter to Continue...

Progress: updating wire_i = 1 as the output of AND for:
wire_C1 = 1
wire_f = 1
wire_X2 = 1

Press Enter to Continue...

Progress: updating wire_j = 0 as the output of AND for:
wire_C0 = 0
wire_C1 = 1
wire_X3 = 0

Press Enter to Continue...

Progress: updating wire_M = 1 as the output of OR for:
wire_g = 0
wire_h = 0
wire_i = 1
wire_j = 0

Press Enter to Continue...


 *** Finished simulation - resulting circuit:

{'wire_C1': ['INPUT', 'wire_C1', True, '1'], 'wire_C0': ['INPUT', 'wire_C0', True, '0'], 'wire_X0': ['INPUT', 'wire_X0', True, '1'], 'wire_X1': ['INPUT', 'wire_X1', True, '0'], 'wire_X2': ['INPUT', 'wire_
X2', True, '1'], 'wire_X3': ['INPUT', 'wire_X3', True, '0'], 'wire_c': ['NOT', ['wire_C1'], True, '0'], 'wire_f': ['NOT', ['wire_C0'], True, '1'], 'wire_g': ['AND', ['wire_f', 'wire_c', 'wire_X0'], True,
'0'], 'wire_h': ['AND', ['wire_c', 'wire_C0', 'wire_X1'], True, '0'], 'wire_i': ['AND', ['wire_C1', 'wire_f', 'wire_X2'], True, '1'], 'wire_j': ['AND', ['wire_C0', 'wire_C1', 'wire_X3'], True, '0'], 'wire
_M': ['OR', ['wire_g', 'wire_h', 'wire_i', 'wire_j'], True, '1'], 'INPUT_WIDTH': ['input width:', 6], 'INPUTS': ['Input list', ['wire_C1', 'wire_C0', 'wire_X0', 'wire_X1', 'wire_X2', 'wire_X3']], 'OUTPUTS
': ['Output list', ['wire_M']], 'GATES': ['Gate list', ['wire_c', 'wire_f', 'wire_g', 'wire_h', 'wire_i', 'wire_j', 'wire_M']]}

 *** Summary of simulation:
010101 -> 1 written into output file.


 *** Now resetting circuit back to unknowns...
```

```
e, 'U'], 'wire_h': ['AND', ['wire_c', 'wire_C0', 'wire_X1'], False, 'U'], 'wire_i': ['AND', ['wire_C1', 'wire_f', 'wire_X2'], False, 'U'], 'wire_j': ['AND', ['wire_C0', 'wire_C1', 'wire_X3'], False, 'U'],
 'wire_M': ['OR', ['wire_g', 'wire_h', 'wire_i', 'wire_j'], False, 'U'], 'INPUT_WIDTH': ['input width:', 6], 'INPUTS': ['Input list', ['wire_C1', 'wire_C0', 'wire_X0', 'wire_X1', 'wire_X2', 'wire_X3']], '
OUTPUTS': ['Output list', ['wire_M']], 'GATES': ['Gate list', ['wire_c', 'wire_f', 'wire_g', 'wire_h', 'wire_i', 'wire_j', 'wire_M']]}
Progress: updating wire_c = 1 as the output of NOT for:
wire_C1 = 0

Press Enter to Continue...

Progress: updating wire_f = 1 as the output of NOT for:
wire_C0 = 0

Press Enter to Continue...

Progress: updating wire_g = 0 as the output of AND for:
wire_f = 1
wire_c = 1
wire_X0 = 0

Press Enter to Continue...

Progress: updating wire_h = 0 as the output of AND for:
wire_c = 1
wire_C0 = 0
wire_X1 = 0

Press Enter to Continue...

Progress: updating wire_i = 0 as the output of AND for:
wire_C1 = 0
wire_f = 1
wire_X2 = 0

Press Enter to Continue...

Progress: updating wire_j = 0 as the output of AND for:
wire_C0 = 0
wire_C1 = 0
wire_X3 = 0

Press Enter to Continue...

Progress: updating wire_M = 0 as the output of OR for:
wire_g = 0
wire_h = 0
wire_i = 0
wire_j = 0

Press Enter to Continue...


 *** Finished simulation - resulting circuit:

{'wire_C1': ['INPUT', 'wire_C1', True, '0'], 'wire_C0': ['INPUT', 'wire_C0', True, '0'], 'wire_X0': ['INPUT', 'wire_X0', True, '0'], 'wire_X1': ['INPUT', 'wire_X1', True, '0'], 'wire_X2': ['INPUT', 'wire_
X2', True, '0'], 'wire_X3': ['INPUT', 'wire_X3', True, '0'], 'wire_c': ['NOT', ['wire_C1'], True, '1'], 'wire_f': ['NOT', ['wire_C0'], True, '1'], 'wire_g': ['AND', ['wire_f', 'wire_c', 'wire_X0'], True,
'0'], 'wire_h': ['AND', ['wire_c', 'wire_C0', 'wire_X1'], True, '0'], 'wire_i': ['AND', ['wire_C1', 'wire_f', 'wire_X2'], True, '0'], 'wire_j': ['AND', ['wire_C0', 'wire_C1', 'wire_X3'], True, '0'], 'wire
_M': ['OR', ['wire_g', 'wire_h', 'wire_i', 'wire_j'], True, '0'], 'INPUT_WIDTH': ['input width:', 6], 'INPUTS': ['Input list', ['wire_C1', 'wire_C0', 'wire_X0', 'wire_X1', 'wire_X2', 'wire_X3']], 'OUTPUTS
': ['Output list', ['wire_M']], 'GATES': ['Gate list', ['wire_c', 'wire_f', 'wire_g', 'wire_h', 'wire_i', 'wire_j', 'wire_M']]}

 *** Summary of simulation:
000000 -> 0 written into output file.


 *** Now resetting circuit back to unknowns...
```