Field Programmable Gate Array

Designing a configurable fabric

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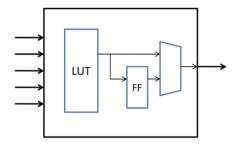
INTRODUCTION

We were to design a configurable fabric that can be used as any combinational/sequential digital circuit configured by a single memory file. It is designed using multiple instances of Logic tiles as LookUp tables and Switch boxes to connect input wires to any of the output wires.

THEORY

Logic Tiles:

Logic tile is used as a lookup table which is hot encoded for different inputs. We implemented a five input logic tile which has a choice for synchronous and non

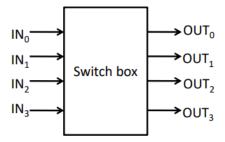


Configuration Data: 32 bit for LUT, 1 bit for MUX control

synchronous output.

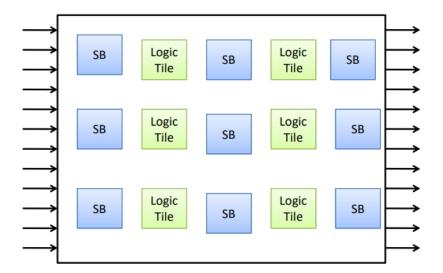
Switch Box:

Switch boxes were used to rearrange the input wires according to the input configuration file. A 4X4 switch box was used for the purpose.



Configurable Fabric:

By using the combination of Logic tiles and Switch boxes, a configurable Fabric is designed which can serve purposes just by giving different configuration files as input.FPGAs can be reprogrammed for desired application and functionality requirements.



PROCEDURE

- 1. We were to design a configurable fabric which could serve the purpose of more than one combinational/ sequential circuit by changing the input configuration file.
- 2. The circuits which I were to implement were :
 - 8 to 1 multiplexer
 - BCD Adder
 - Shift Register
- 3. Maximum input count was for 8 to 1 multiplexer (11 inputs) which include 8 input bits and 3 control bits.
- 4. Maximum Output count was for 8 bit shift register.
- 5. Multiple Instances of Switch boxes were used to map all inputs to only the required inputs.
- 6. Logic tiles were used as 5 input lookup tables configured through memory file with a clock input to the flip flop.
- 7. Corresponding to the design, many configurations were made, hot encoded for each input and output.

CONFIGURATION FILES

Out of many different configurations, some of the configuration files made were:

0 0 0 1 1 0 1 0 10 0 1 0 11 1 0 0 100 0 1 1 101 0 0 1 110 0 0 1 111 1 1 0 1000 0 0 0 1001 0 0 0 1010 0 0 0 1011 1 1 1				
10 0 1 0 11 1 0 0 100 0 1 1 101 0 0 1 110 0 0 1 111 1 1 1 1000 0 0 0 1001 0 0 0 1010 0 0 0	0	0	0	1
11 1 0 0 100 0 1 1 101 0 0 1 110 0 0 1 111 1 1 0 1000 0 0 0 1001 0 0 0 1010 0 0 0	1	0	1	0
100 0 1 1 101 0 0 1 110 0 0 1 111 1 1 0 1000 0 0 0 1001 0 0 0 1010 0 0 0	10	0	1	0
101 0 0 1 110 0 0 1 111 1 1 1 0 1000 0 0 0 0 1001 0 0 0 0 1010 0 0 0 0	11	1	0	0
110 0 0 1 111 1 1 1 0 1000 0 0 0 0 1001 0 0 0 0 1010 0 0 0 0	100	0	1	1
111 1 1 0 1000 0 0 0 1001 0 0 0 1010 0 0 0	101	0	0	1
1000 0 0 0 1001 0 0 0 1010 0 0 0	110	0	0	1
1001 0 0 0 1010 0 0 0	111	1	1	0
1010 0 0 0	1000	0	0	0
	1001	0	0	0
1011 1 1 0	1010	0	0	0
	1011	1	1	0

1100	1	0	1
1101	1	1	0
1110	1	1	1
1111	1	1	0

1	0	1
1	0	0
1	0	0
1	0	0
1	0	0
1	0	1
1	0	0
1	0	0
1	0	0
1	0	0
1	0	0
1	0	0
1	0	0
1	0	0
1	0	0
1	0	0
	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0

RESULTS

Here ,using different instances of memory file and different input configurations, the designed configurable fabric could be used as any of the three circuits which include combinational as well as sequential ones.

REFERENCES

1. Dr. Neeraj Goel, IIT Ropar