

REALIZATION OF COMBINATIONAL SYSTEMS AT

(i) LOGIC LEVEL:

GATES + CONNECTIONS.

(ii) CIRCUIT LEVEL:

GATES MADE OF TRANSISTORS

+ WIRES + PACKAGING + POWER SUPPLY

NEED TO UNDERSTAND THE CIRCUIT LEVEL

BECAUSE PHYSICAL CHARACTERISTIC OF
GATES & WIRES (SPEED, COST, POWER) AFFECT
THESE CHARACTERISTIC OF COMBINATIONAL
NETWORKS

- WE CONSIDER ONLY ELECTRIC CIRCUIT LEVEL ABSTRACTIONS — NO SOLID-STATE PHYSICS AND ELECTRONICS
- SUFFICIENT TO OBTAIN COMBINATIONAL NETWORK CHARACTERISTICS:
I/O DELAY, COST, (POWER)

COMBINATIONAL ICs

- REPRESENTATION OF BINARY VARIABLES AT THE PHYSICAL LEVEL
- BASIC SWITCH. STRUCTURE OF GATES AND THEIR OPERATION
- REALIZATION OF GATES USING CMOS CIRCUITS
- CHARACTERISTICS OF CIRCUITS: LOAD FACTORS AND FANOUT FACTORS, PROPAGATION DELAYS, TRANSITION TIMES, AND EFFECT OF LOAD

- THREE-STATE GATES (DRIVERS) AND BUSES
- NOISE AND NOISE MARGINS
- EVOLUTION OF ICs. VLSI CIRCUIT-LEVEL DESIGN STYLES
- PACKAGING LEVELS: CHIPS, BOARDS AND CABINETS.

REPRESENTATION OF BINARY VARIABLES

- REPRESENTATION OF 0 AND 1 BY ELECTRICAL SIGNALS
 - VOLTAGES
 - CURRENTS
 - ELECTRICAL CHARGES
- REALIZATION OF CIRCUITS THAT OPERATE ON THESE SIGNALS TO IMPLEMENT DESIRED SWITCHING FUNCTIONS

TYPICAL VALUES FOR A 3.3V CMOS TECHNOLOGY

$$\begin{array}{ll} V_{Hmax} & 3.3V \\ V_{Hmin} & 2.0V \end{array} \quad \begin{array}{ll} V_{Lmax} & 0.8V \\ V_{Lmin} & 0.0V \end{array}$$

VOLTAGE REGIONS

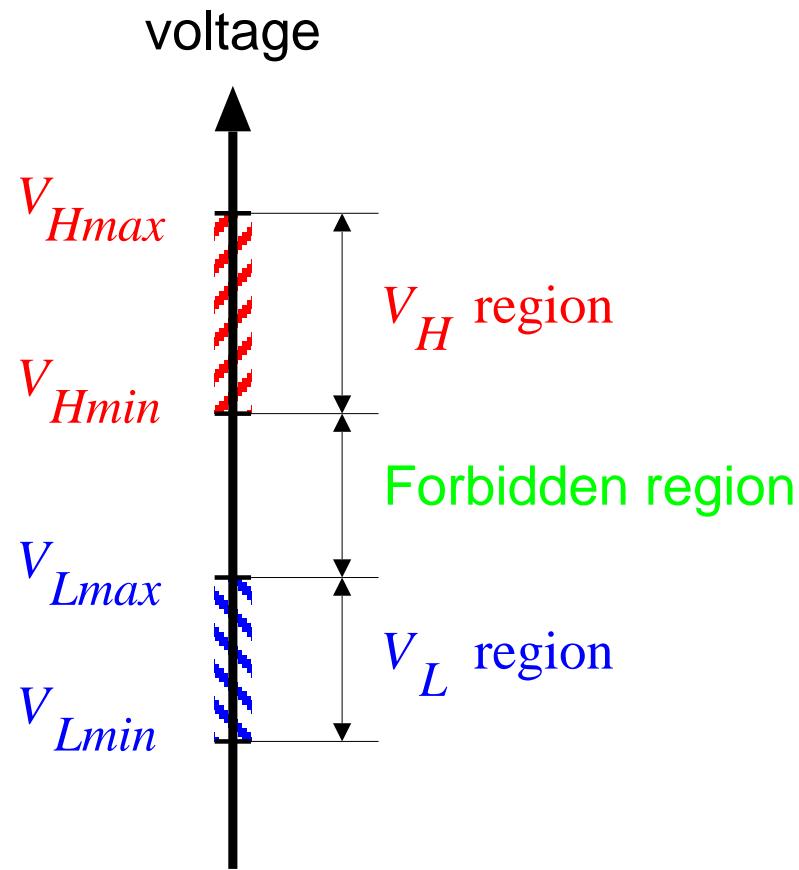


Figure 3.1: VOLTAGE REGIONS.

POSITIVE AND NEGATIVE LOGIC

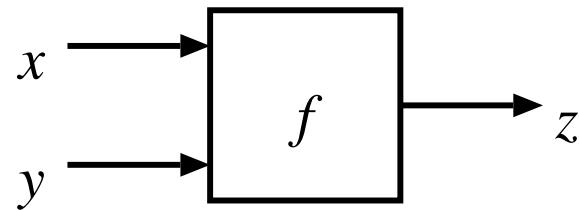


Figure 3.2:

POSITIVE LOGIC

$$V_H \longleftrightarrow 1$$

$$V_L \longleftrightarrow 0$$

NEGATIVE LOGIC

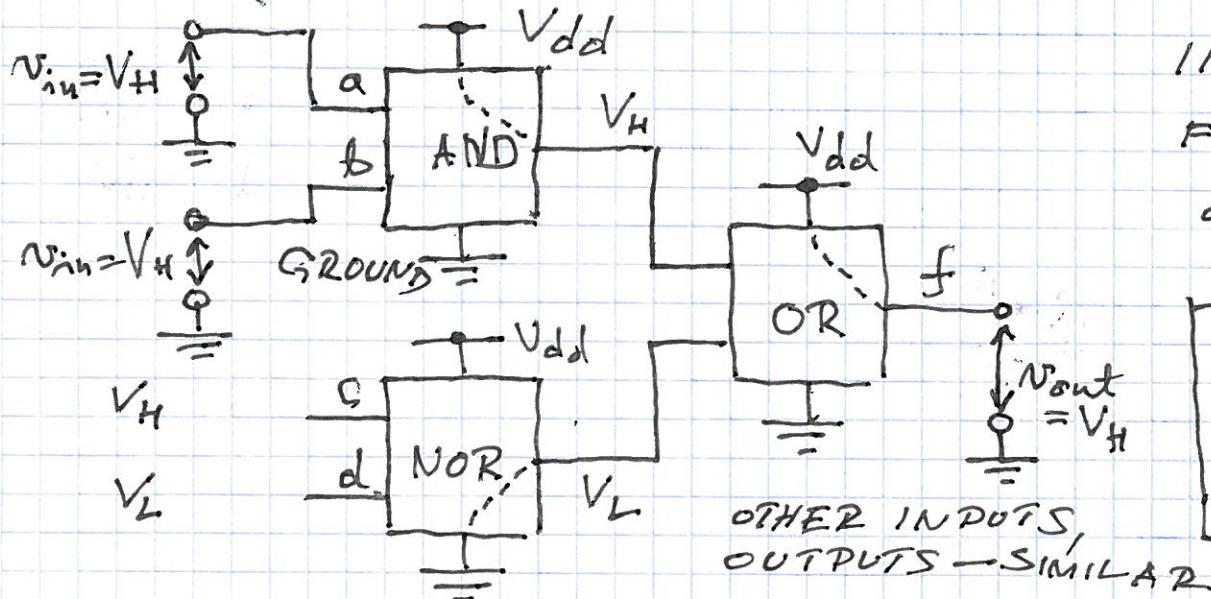
$$V_H \longleftrightarrow 0$$

$$V_L \longleftrightarrow 1$$

Input voltages		Output voltage	Positive logic			Negative logic		
x	y	z	x	y	z	x	y	z
V_L	V_L	V_L	0	0	0	1	1	1
V_L	V_H	V_L	0	1	0	1	0	1
V_H	V_L	V_L	1	0	0	0	1	1
V_H	V_H	V_H	1	1	1	0	0	0
			$f = \text{AND}$			$f = \text{OR}$		

$$f = ab + c'd' = OR(AND(a,b), NOR(c,d))$$

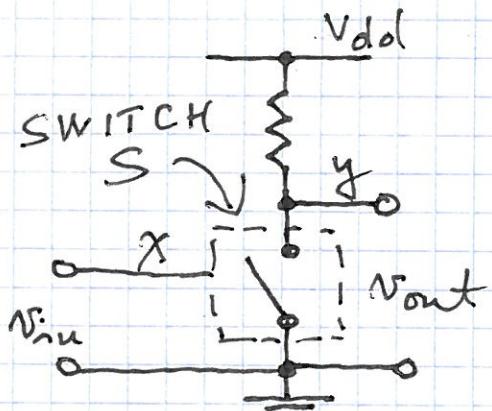
POWER SUPPLY VOLTAGE



INPUTS, OUTPUTS SWITCH
FROM V_L TO V_H
OR V_H TO V_L

$V_{dd} \sim V_H (1)$
$GND \sim V_L (0)$

A SIMPLE PHYSICAL GATE (NOT)

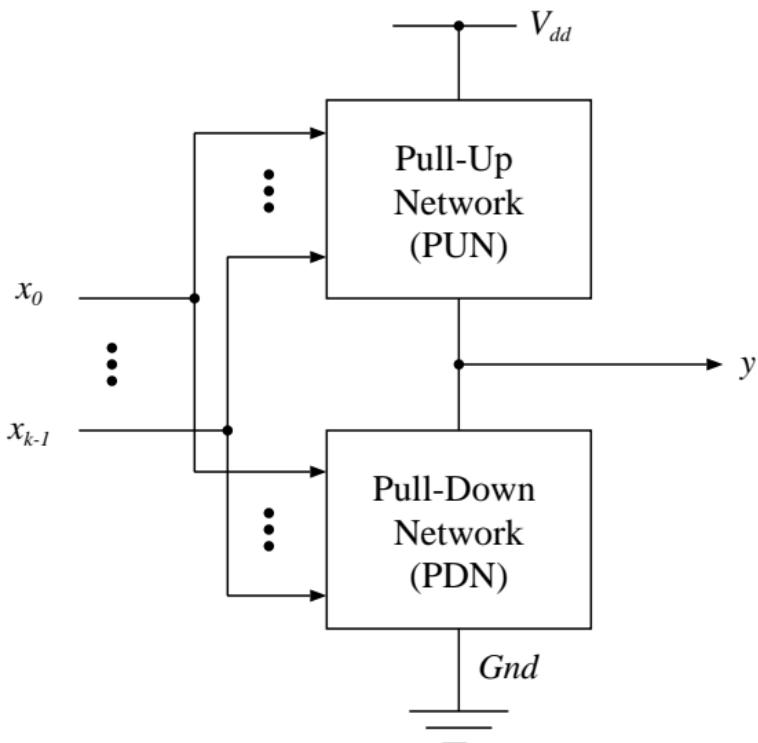


V_{in}	S	V_{out}
V_L	OPEN	$V_H (\sim V_{dd})$
V_H	CLOSED	$V_L (\sim 0 \leftrightarrow GROUND)$

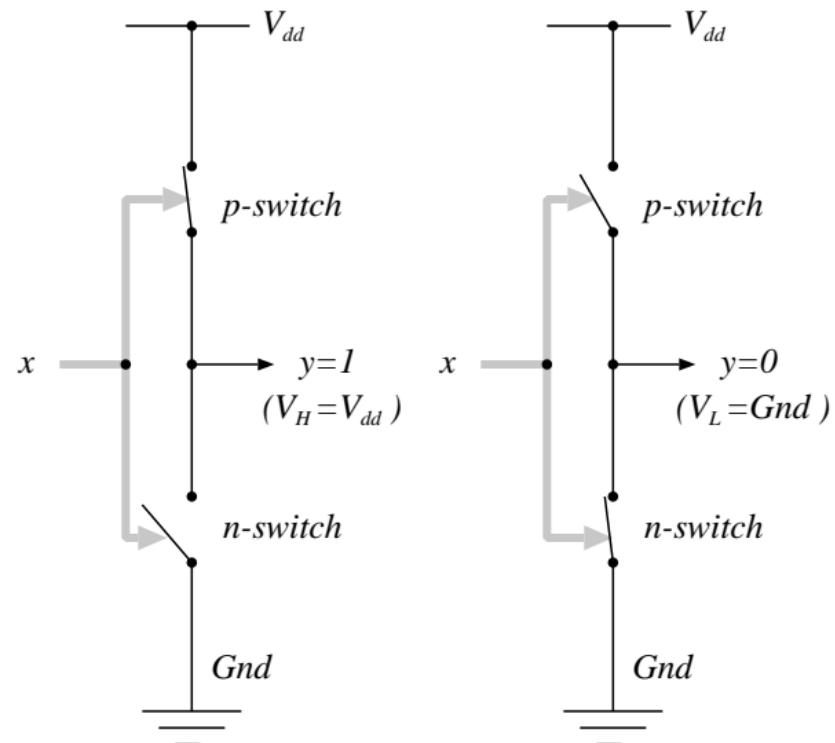
X	S	V_{out}
0	OPEN	1
1	CLOSED	0

\Rightarrow NOT function

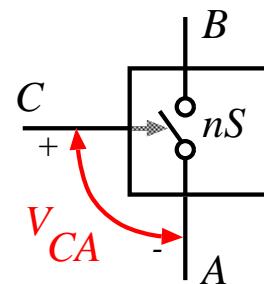
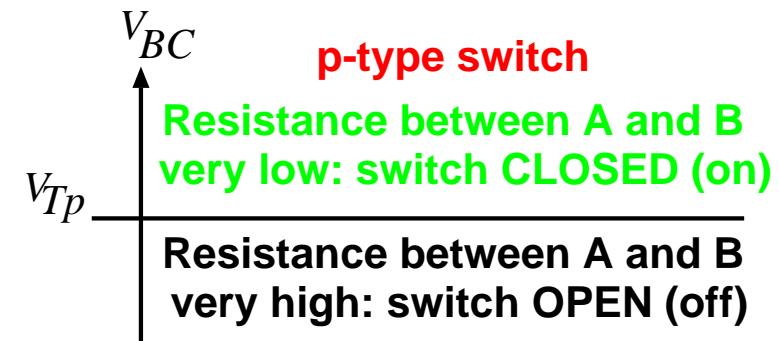
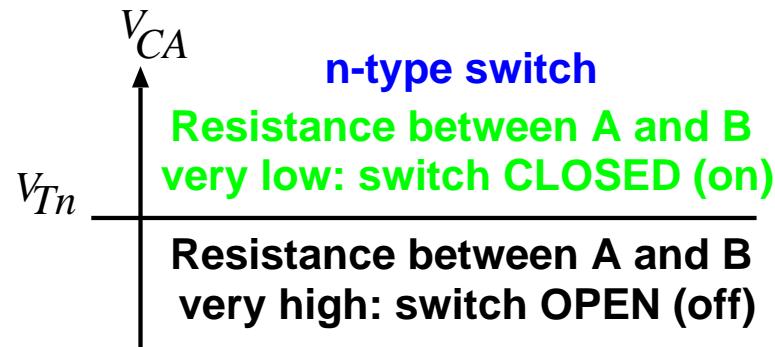
COMPLEMENTARY LOGIC



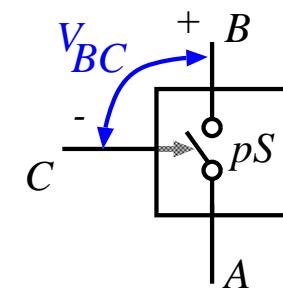
STABLE SITUATIONS



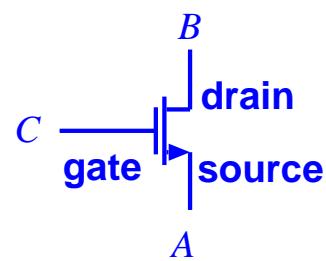
- ° no static current in stable state
=> low power dissipation
- ° faster transitions



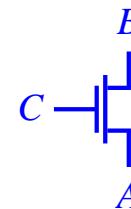
(a)



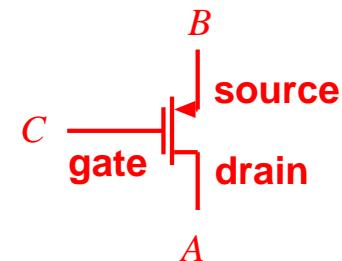
NMOS transistor



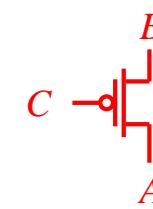
logical symbol



PMOS transistor



logical symbol



(b)

Figure 3.3: a) N-TYPE AND P-TYPE CONTROLLED SWITCHES. b) NMOS AND PMOS TRANSISTORS.

STRUCTURE AND OPERATION OF GATES

SWITCH AND MOS TRANSISTORS

N-TYPE:

OPEN (OFF) if $V_{CA} < V_{Tn}$

CLOSED (ON) if $V_{CA} > V_{Tn}$

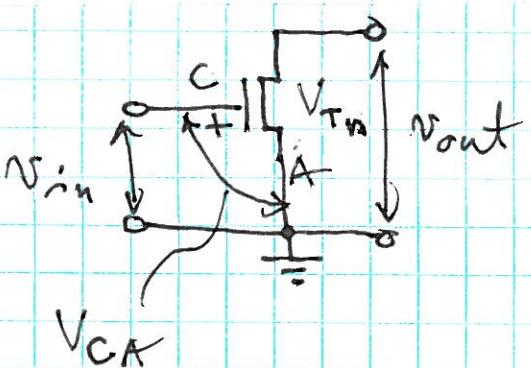
V_{Tn} – THE THRESHOLD VOLTAGE FOR N-TYPE SWITCH

P-TYPE:

OPEN (OFF) if $V_{BC} < V_{Tp}$

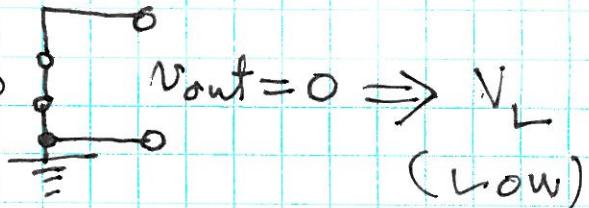
CLOSED (ON) if $V_{BC} > V_{Tp}$

V_{Tp} – THE THRESHOLD VOLTAGE FOR P-TYPE SWITCH



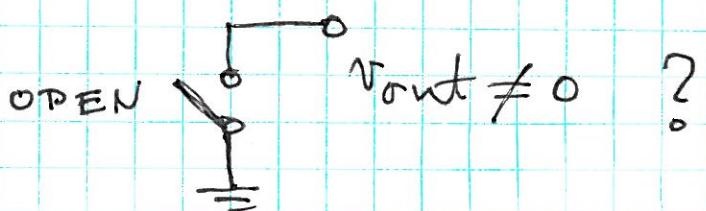
nMOS SWITCH

IF $V_{CA} = V_H > V_{Tn}$

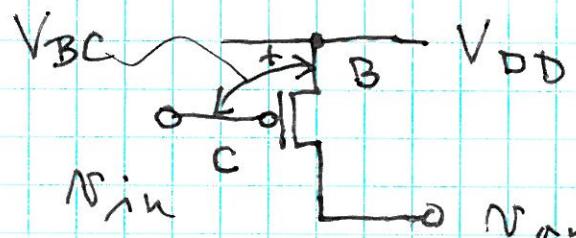


(Low)

IF $V_{CA} = V_L < V_{Tn}$



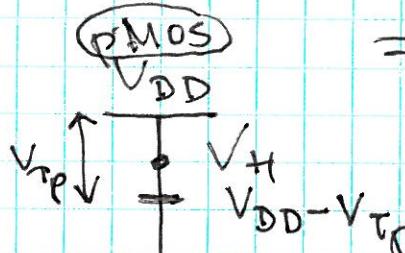
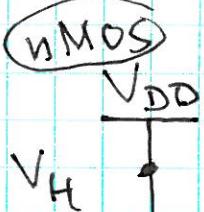
pMOS SWITCH



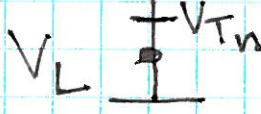
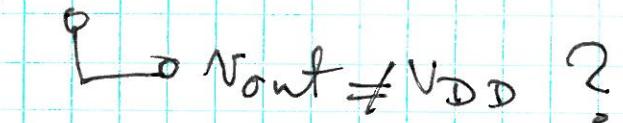
IF: $V_{BC} = V_H > V_{DD} - V_{Tp}$
 $< V_{Tp}$



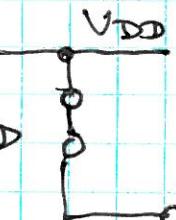
nMOS



\Rightarrow OPEN



IF $V_{BC} = V_L < V_{DD} - V_{Tp}$
 $> V_{Tp}$



CLOSED

$V_{out} = V_{DD} \Rightarrow V_H$ (HIGH)

CMOS NOT GATE

- COMPLEMENTARY MOS CIRCUIT

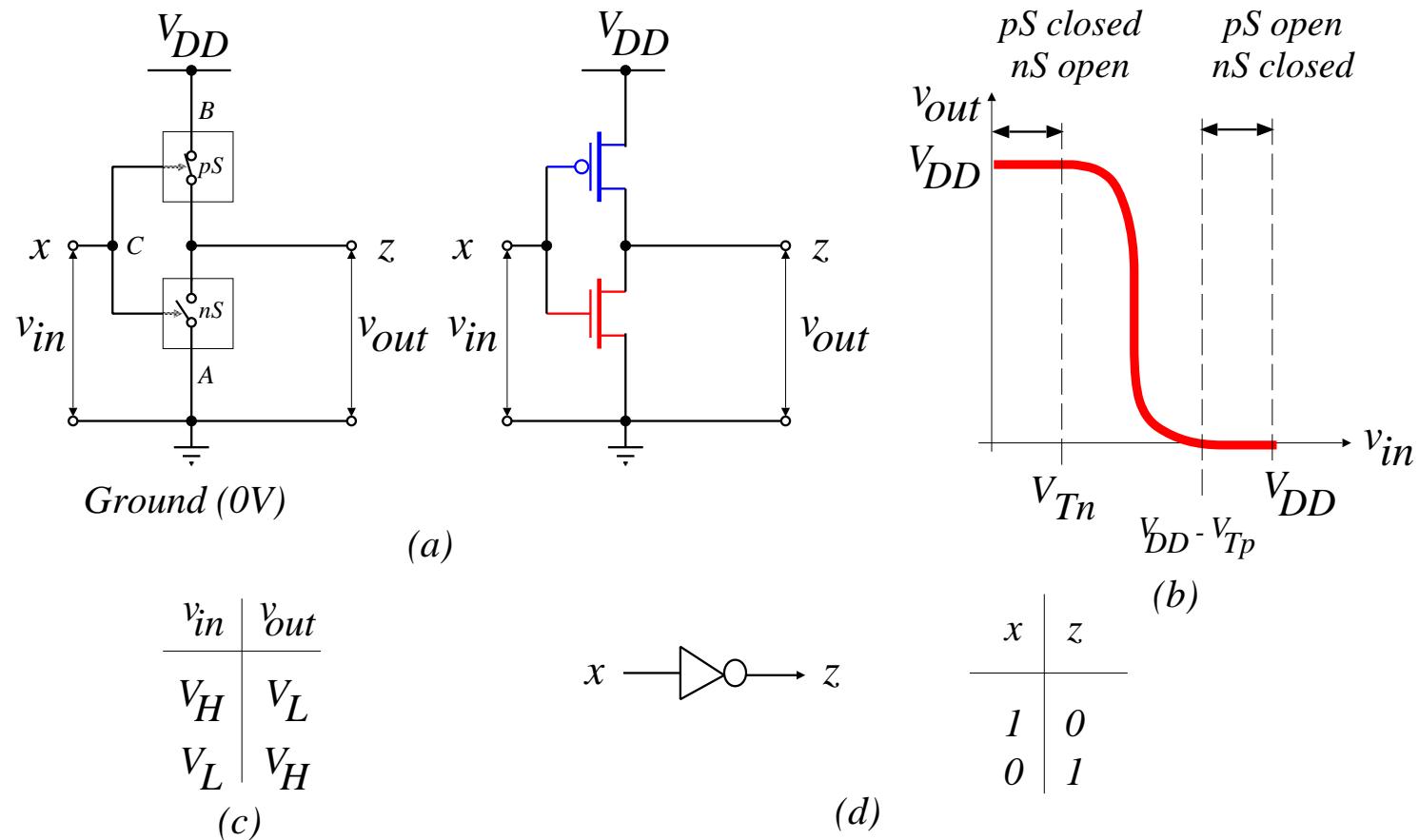


Figure 3.4: CIRCUIT, I/O CHARACTERISTIC, AND SYMBOL

OPERATION OF NOT GATE

$$V_{BC} = V_{DD} - v_{in} \quad (V_{DD} = V_{BC} + v_{in})$$

1. $v_{in} < V_{Tn} \implies V_{CA} < V_{Tn}$

N-SWITCH OPEN

If $V_{DD} > V_{Tn} + V_{Tp}$ then $V_{BC} > V_{Tp}$

P-SWITCH CLOSED AND $v_{out} = V_{DD}$

2. $v_{in} > V_{DD} - V_{Tp} \implies V_{BC} < V_{Tp}$

P-SWITCH IS OPEN

If $V_{DD} > V_{Tn} + V_{Tp}$ then $V_{CA} > V_{Tn}$

N-SWITCH IS CLOSED AND $v_{out} = 0$

OPERATION (cont.)

CIRCUIT OPERATES AS NOT GATE IF

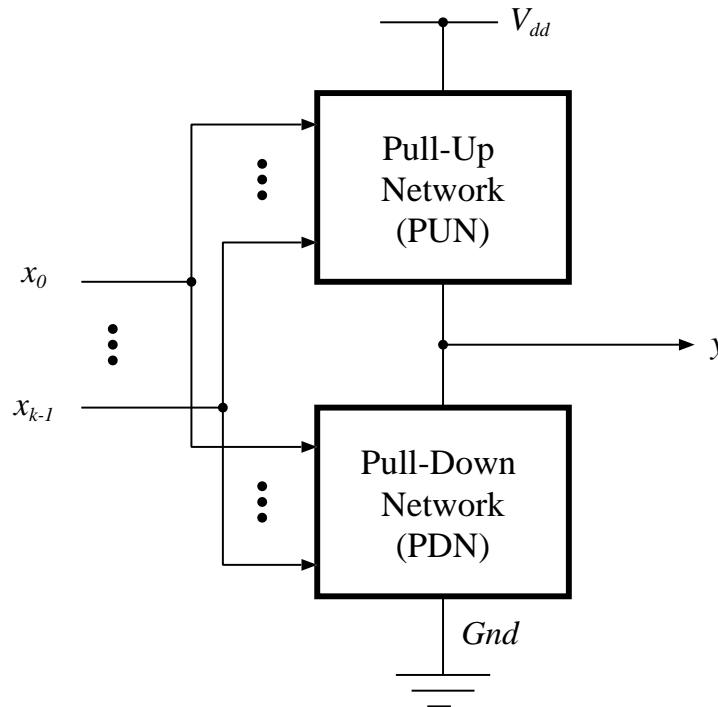
$$V_{Lmax} < V_{Tn}$$

$$V_{Hmin} > V_{DD} - V_{Tp}$$

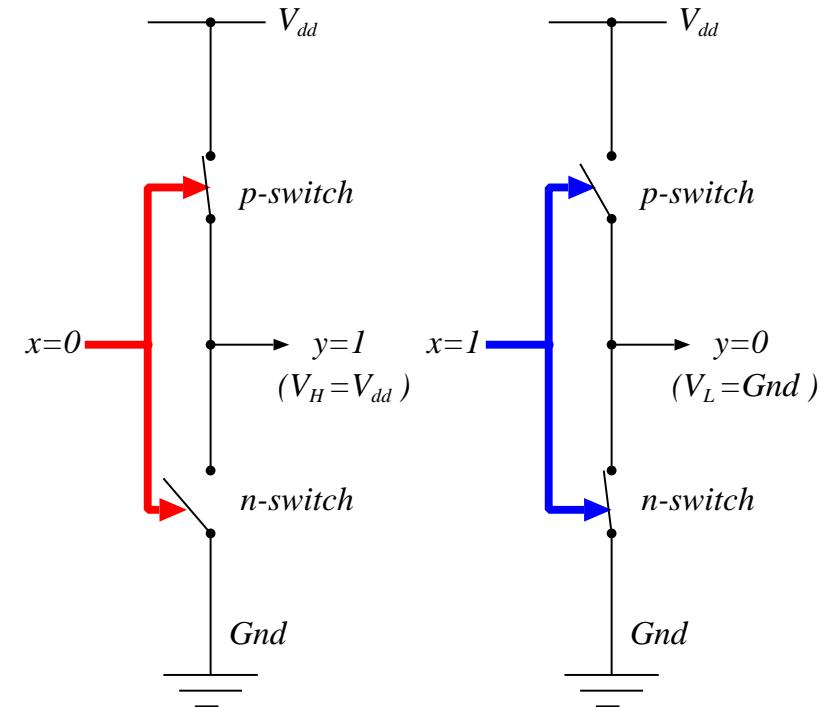
$$V_{DD} > V_{Tn} + V_{Tp}$$

COMPLEMENTARY LOGIC

COMPLEMENTARY LOGIC



STABLE SITUATIONS

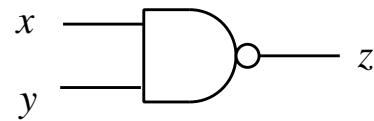


- no static current in stable state
=> low power dissipation
- faster transitions

Figure 3.5:

NAND and NOR GATES

Circuit 1: NAND



Circuit 2: NOR

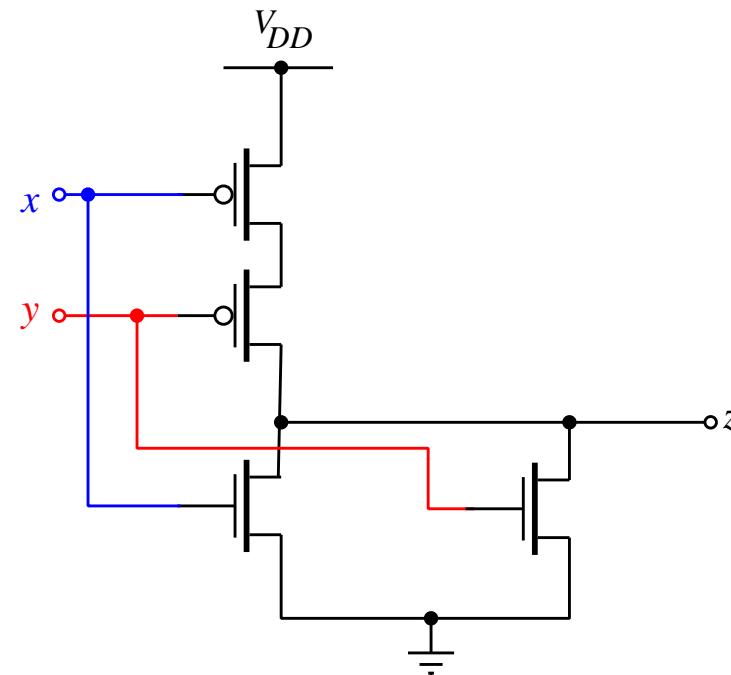
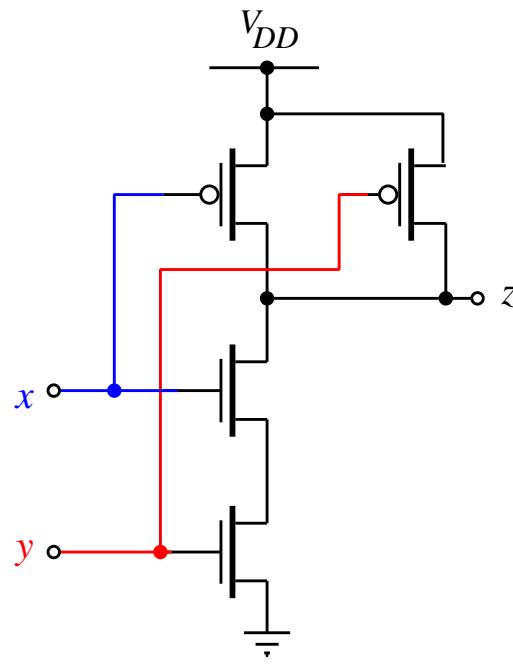
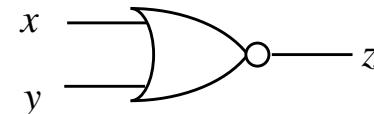


Figure 3.5: CIRCUITS FOR NAND and NOR GATES.

NAND and NOR GATES (cont.)

x	y	Circuit 1	Circuit 2
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

AND and OR GATES

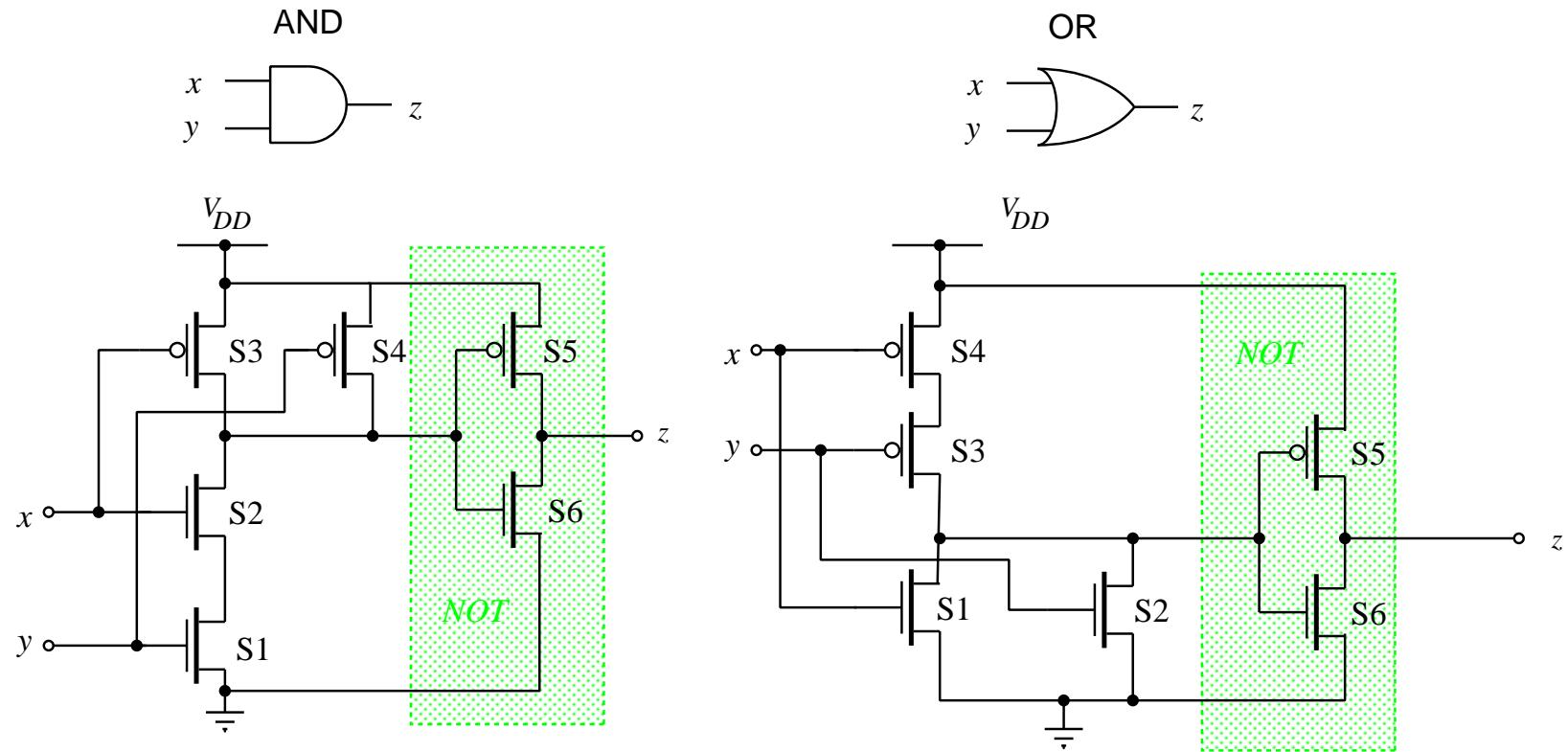
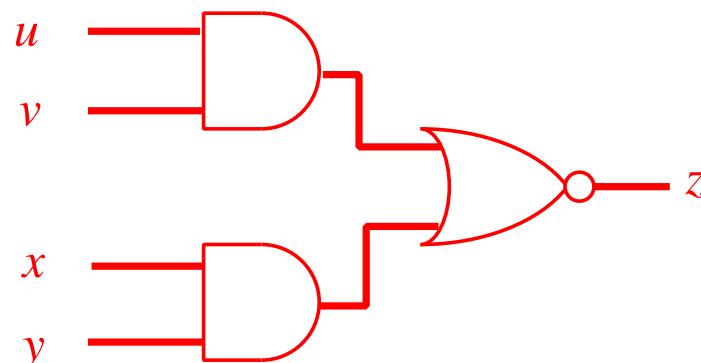


Figure 3.6: CIRCUITS FOR AND and OR GATES.

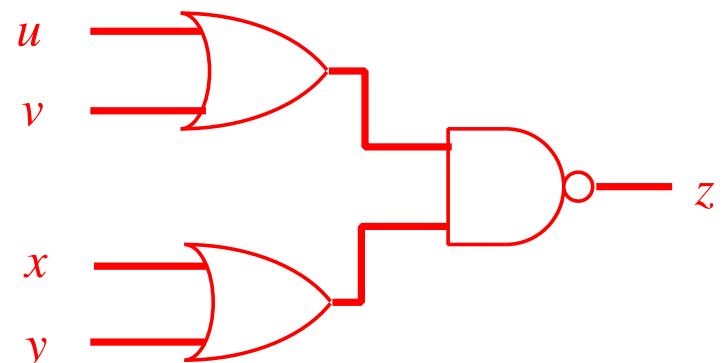
COMPLEX GATES

AND-OR-INVERT (AOI)



$$z = (uv + xy)'$$

OR-AND-INVERT (OAI)



$$z = [(u+v)(x+y)]'$$

Figure 3.7: COMPLEX GATES.

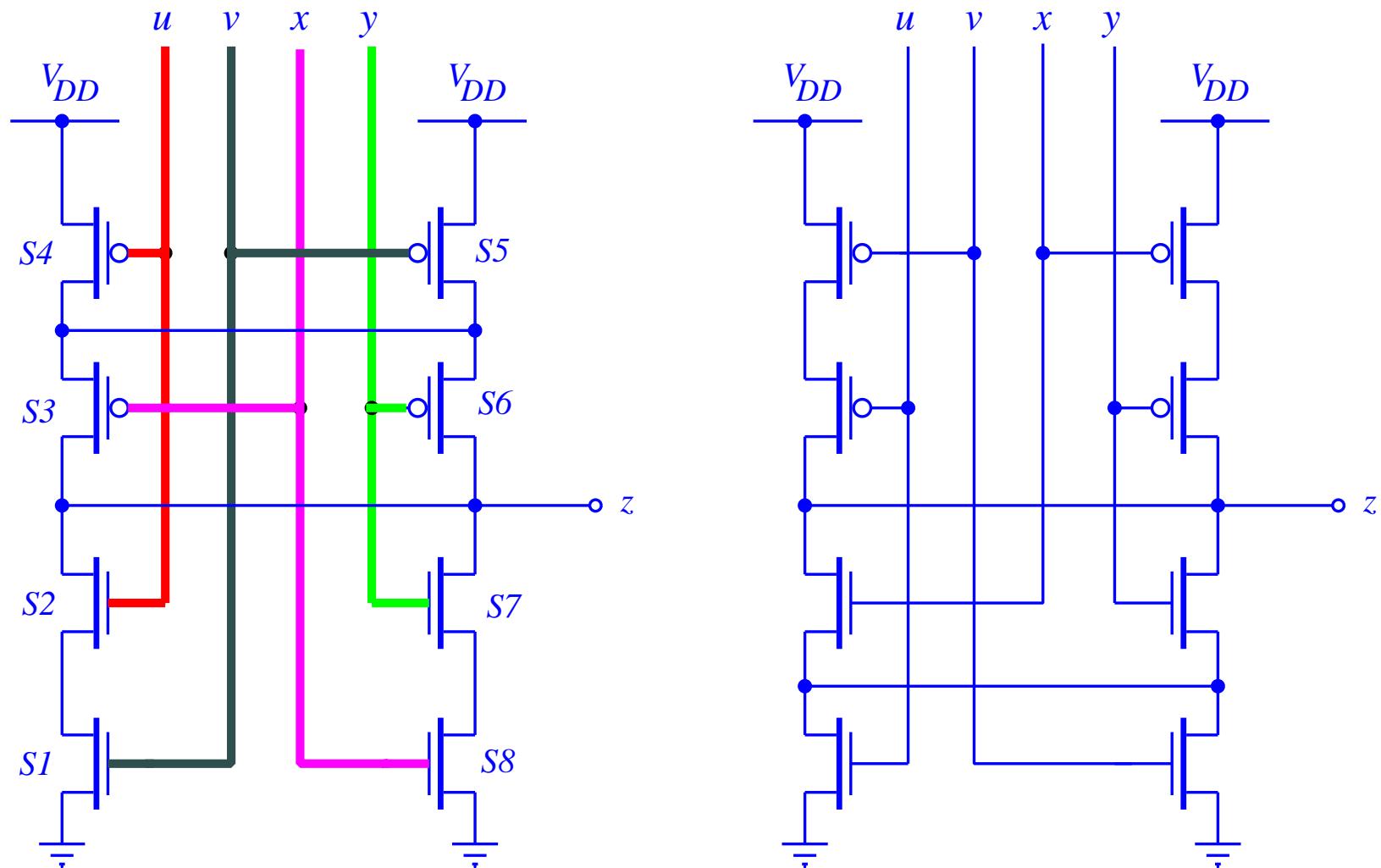


Figure 3.7: EXAMPLES OF COMPLEX GATES.

$$Z = (UN + XY)'$$

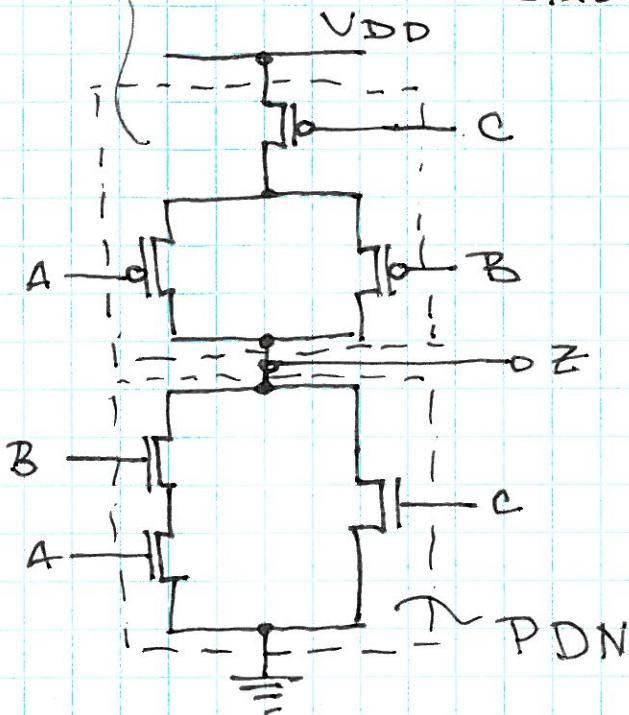
PULL-DOWN NET: $Z' = UN + XY$

PULL-UP NET:

$$\begin{aligned} Z &= (UN + XY)' \\ &= (UN)' \cdot (XY)' \\ &= (U' + N')(X' + Y') \\ &= U'X' + N'Y' + U'Y' + N'X' \Rightarrow 4 \text{ PATHS!} \end{aligned}$$

EXAMPLE: DETERMINE THE SWITCHING FUNCTION OF THE FOLLOWING CMOS CIRCUIT

PUN



$$Z = f(A, B, C)$$

FROM THE PD NETWORK:

$$Z' = AB + C$$

$$Z = (AB + C)' = (A' + B')C'$$

FROM THE PU NETWORK

$$Z = (A' + B')C' \Rightarrow \text{CHECKS!}$$

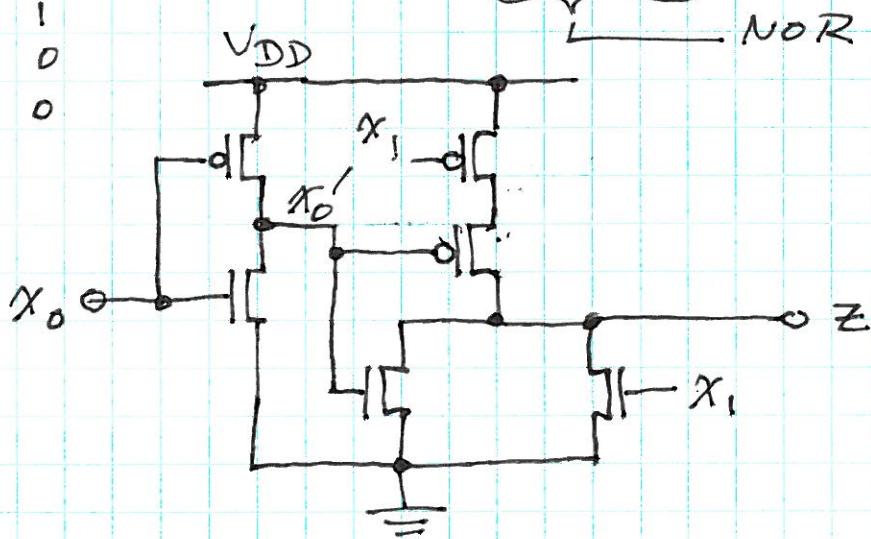
EXERCISE 3,4: SHOW A CMOS CIRCUIT THAT IMPLEMENTS THE FOLLOWING FUNCTION (FOR POSITIVE LOGIC)

X_1	X_0	Z
0	0	0
0	1	1
1	0	0
1	1	0

$$Z = X_1' X_0 = (X_1 + X_0')'$$

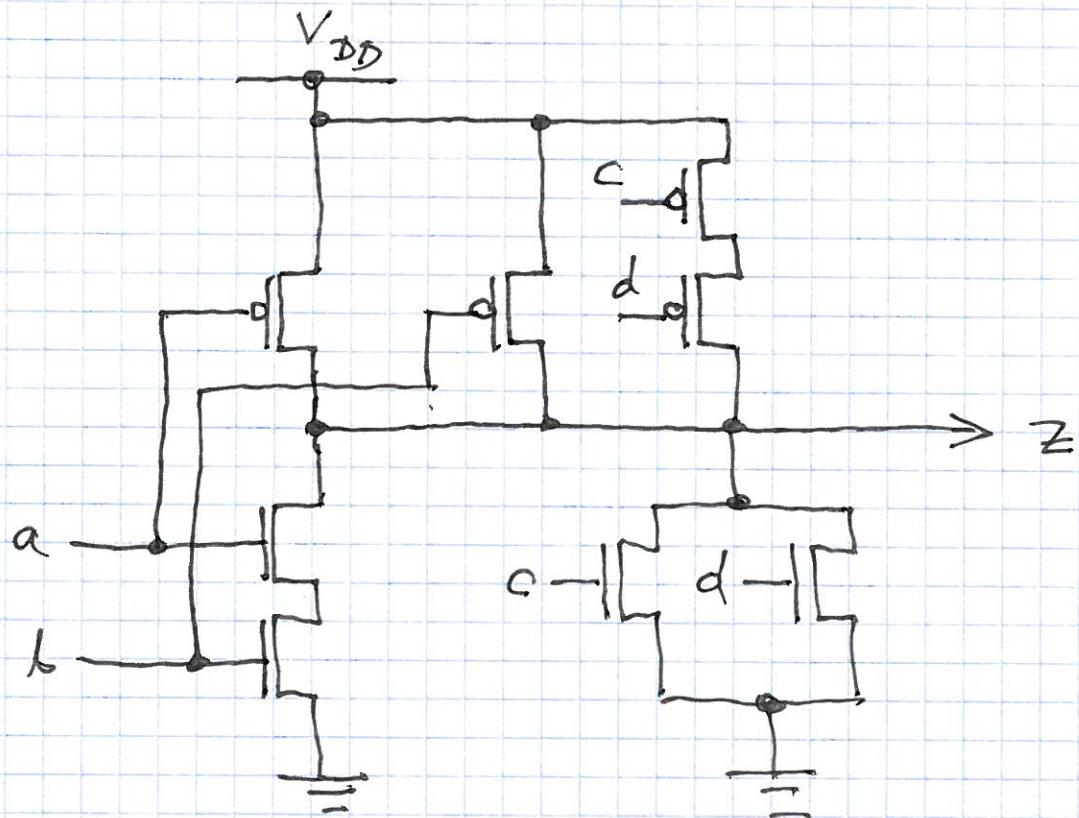
NOT

NOR

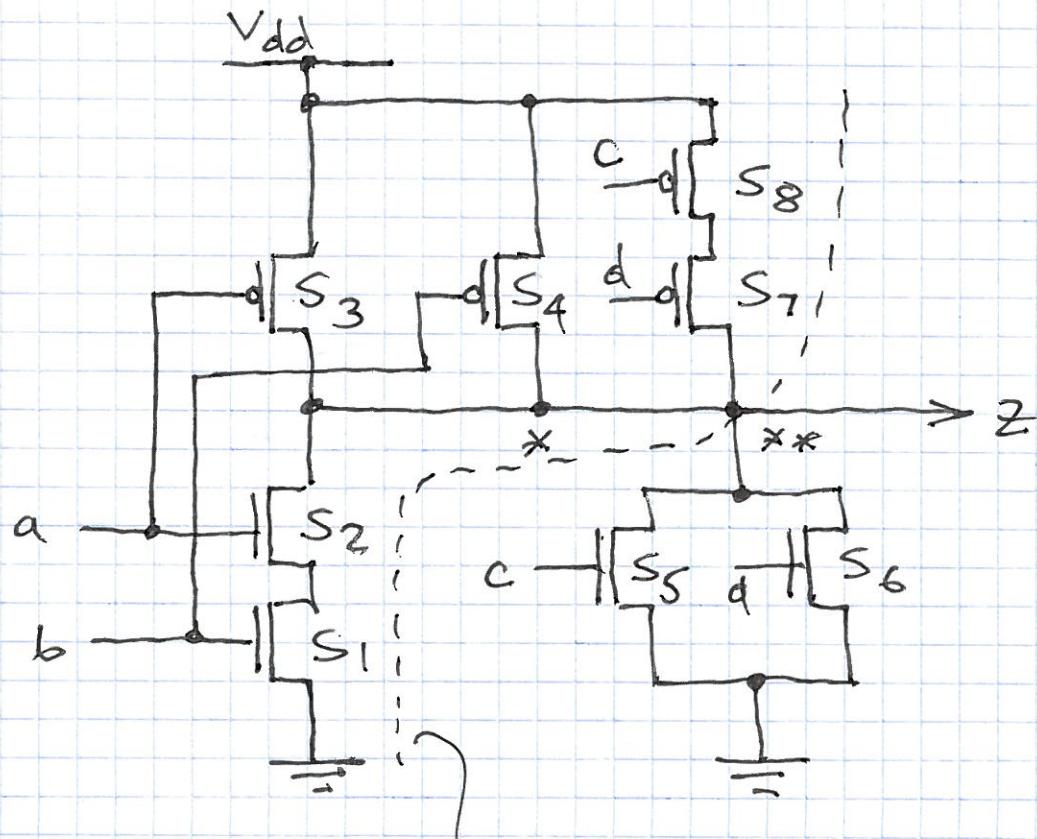


CS 551A

IS THIS CMOS NETWORK
VALID?



IS THIS CMOS NETWORK VALID?



NO,

$* \leftrightarrow (ab)'$

$** \leftrightarrow (c+d)'$

 \rightarrow 2 DIFF. FUNCTIONS —
SAME OUTPUT Z

$a = 1 \quad b = 1 \quad * = 0$

$c = 0 \quad d = 0 \quad ** = 1$

X

POTENTIAL "SHORT" BETWEEN

 V_{dd} AND GROUND $V_{dd} \rightarrow S_8 \rightarrow S_7 \rightarrow S_2 \rightarrow S_1 \rightarrow \text{GND}$

TRANSMISSION GATE

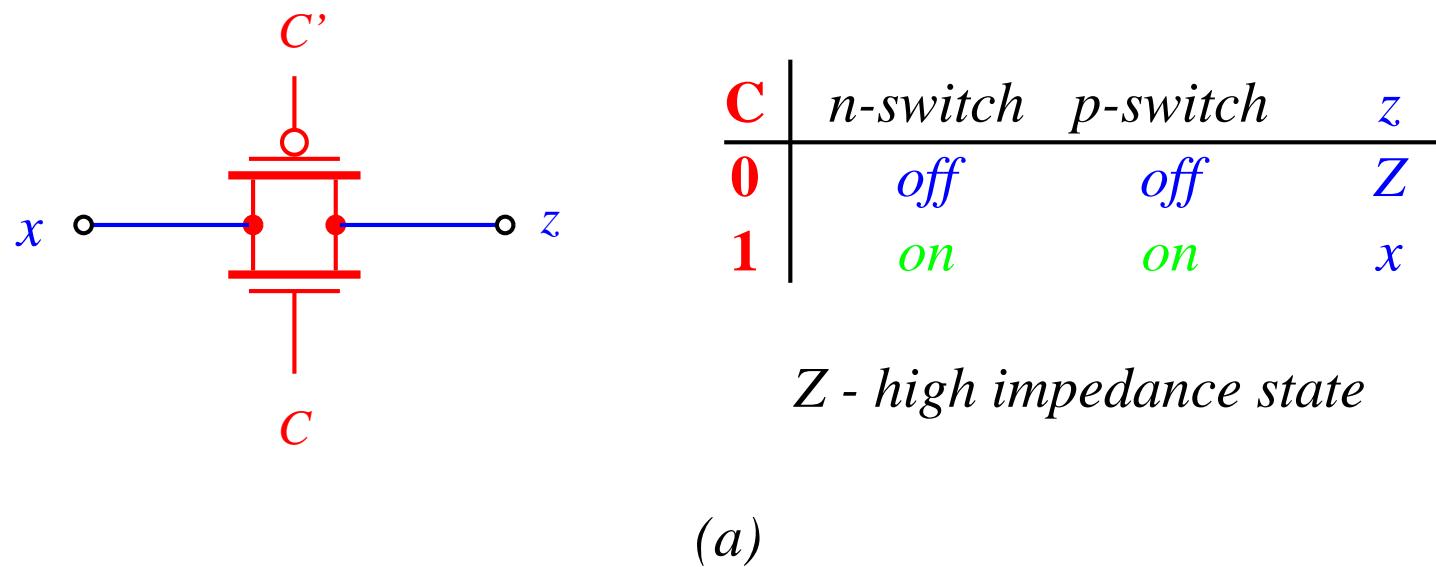


Figure 3.8: a) TRANSMISSION GATE

XOR WITH TRANSMISSION GATES

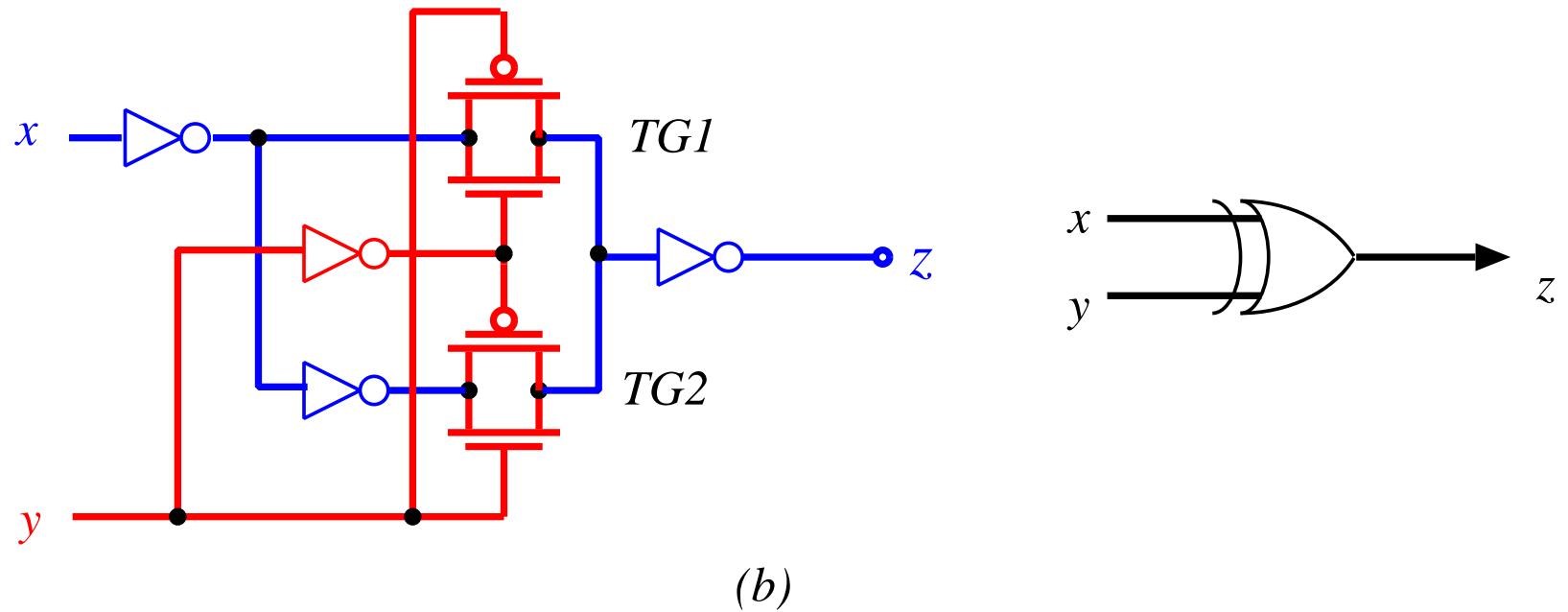


Figure 3.8: b) XOR GATE

y	$TG1$	$TG2$	z
0	ON	OFF	x
1	OFF	ON	x'

MUX WITH TRANSMISSION GATES

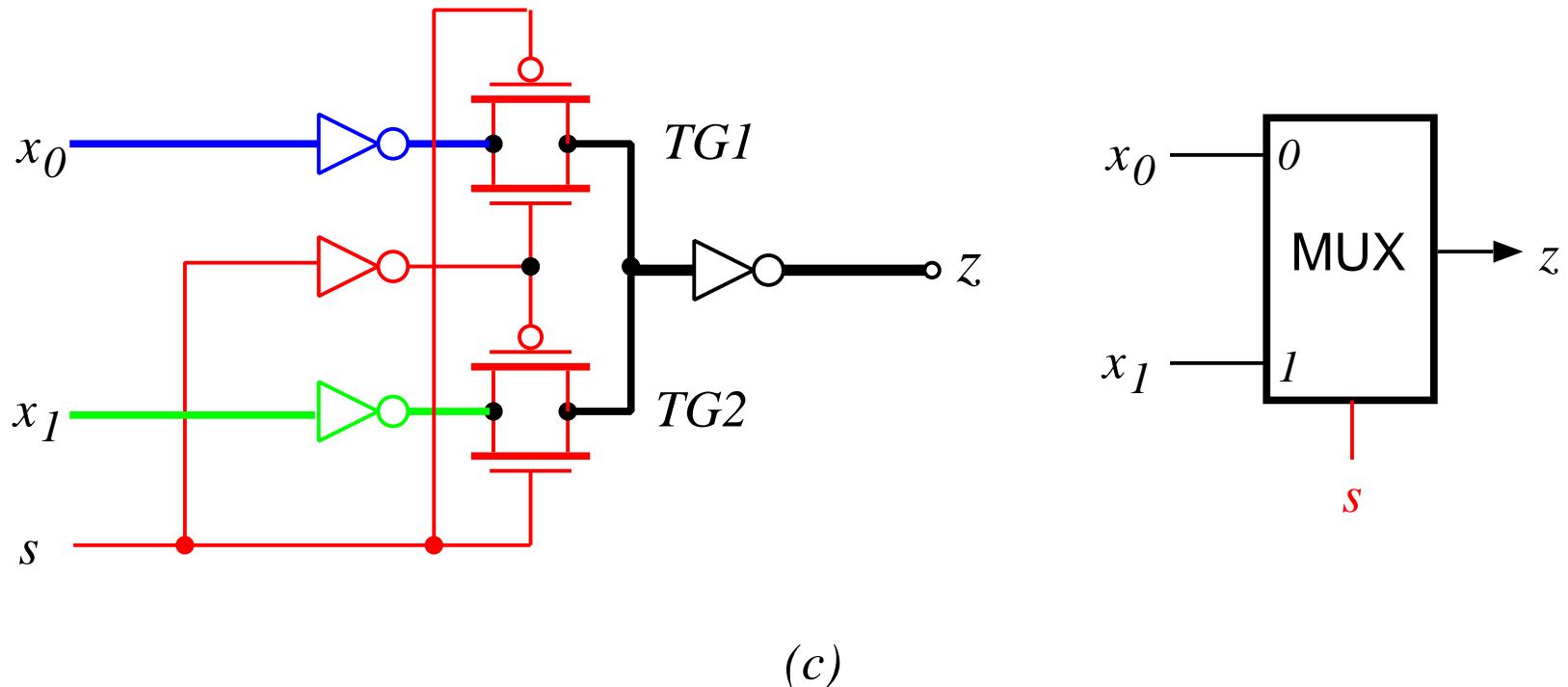


Figure 3.8: c) 2-INPUT MUX.

$$z = \text{MUX}(x_1, x_0, s) = x_1 s + x_0 s'$$

s	$TG1$	$TG2$	z
0	ON	OFF	x_0
1	OFF	ON	x_1

TIMING PARAMETERS

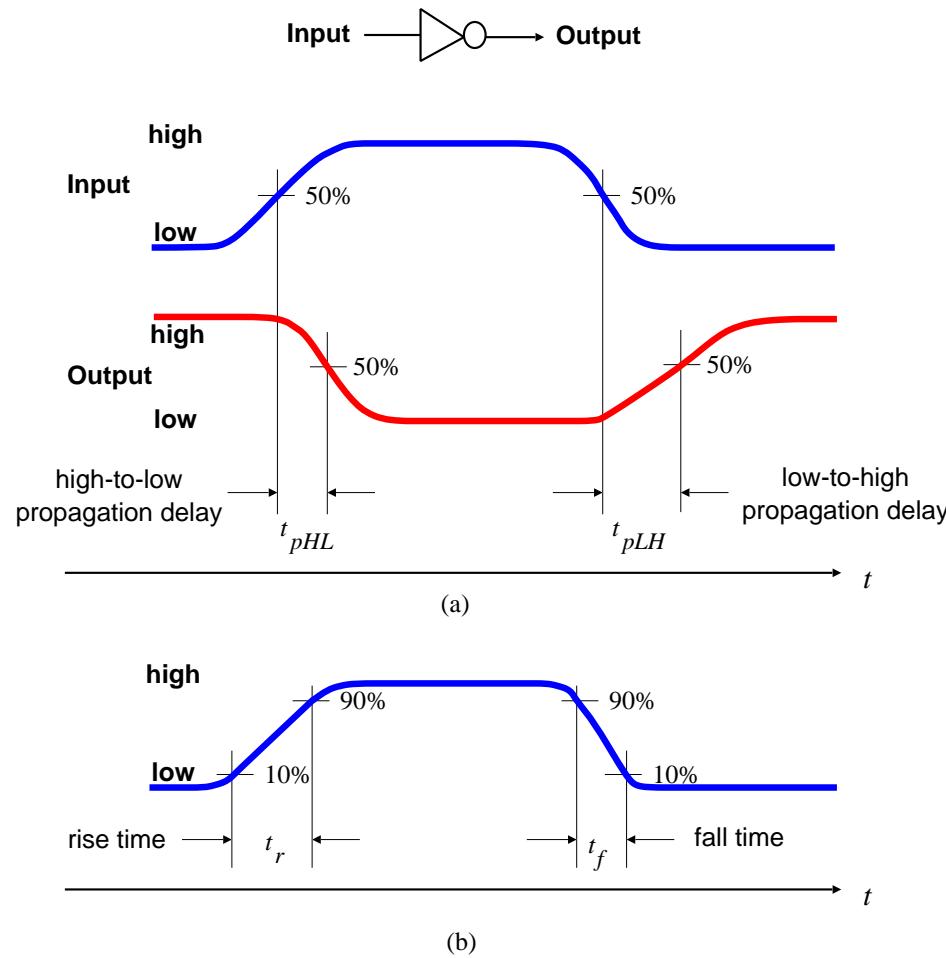


Figure 3.9: a) PROPAGATION DELAY. b) RISE AND FALL TIMES.

EFFECT OF LOAD

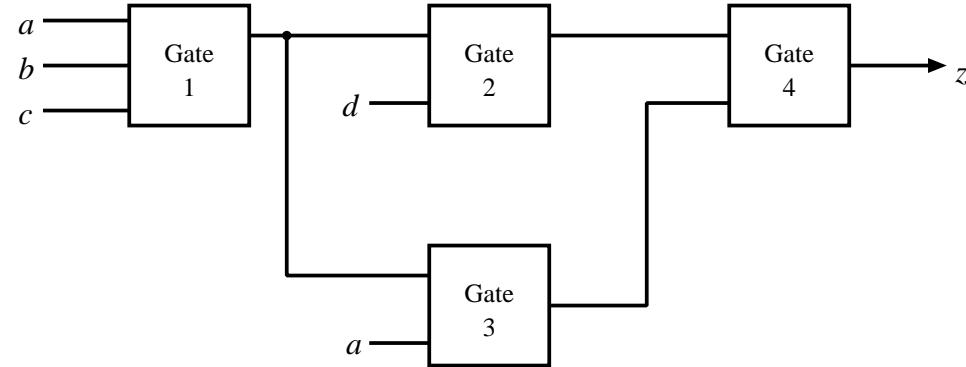


Figure 3.10: A GATE NETWORK

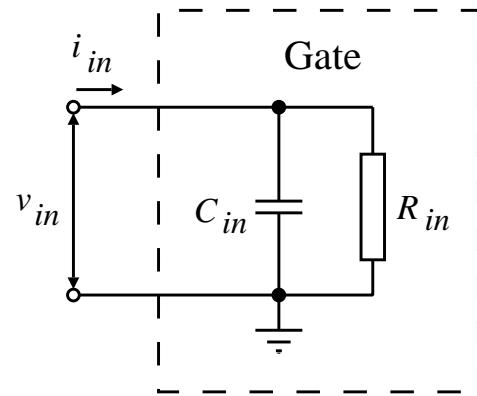


Figure 3.11: EQUIVALENT CIRCUIT FOR GATE INPUT.

EFFECT OF LOAD ON PROPAGATION DELAY

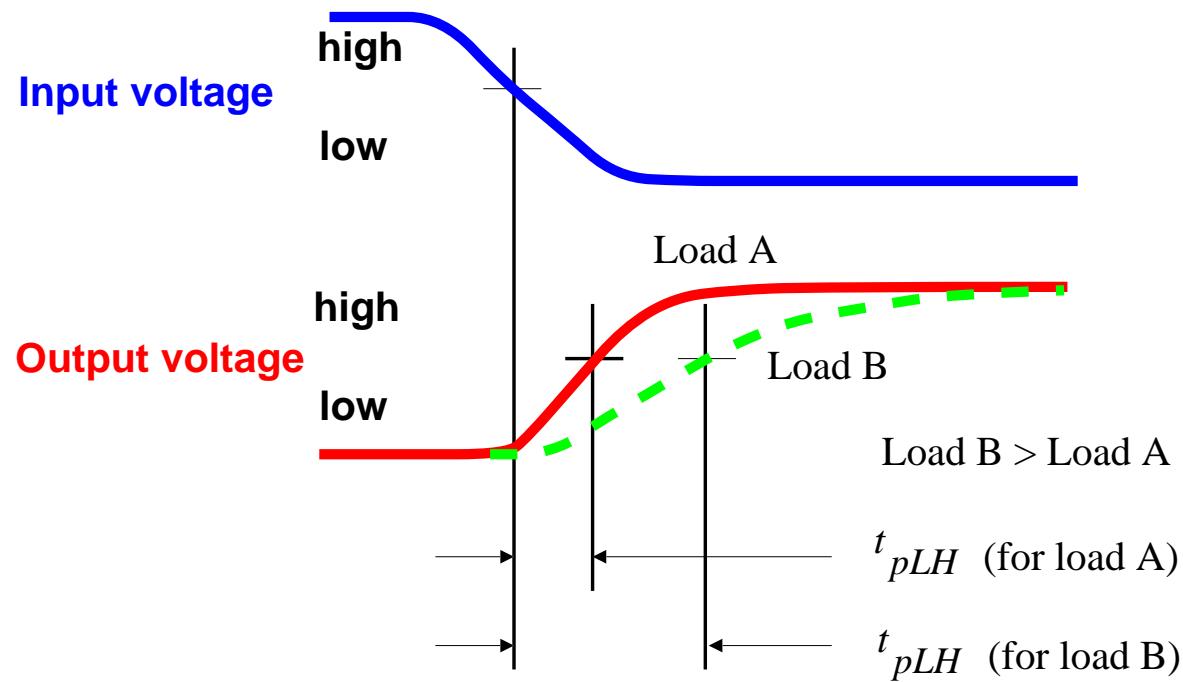


Figure 3.12: EFFECT OF LOAD ON PROPAGATION DELAY.

LOAD FACTOR AND TOTAL LOAD

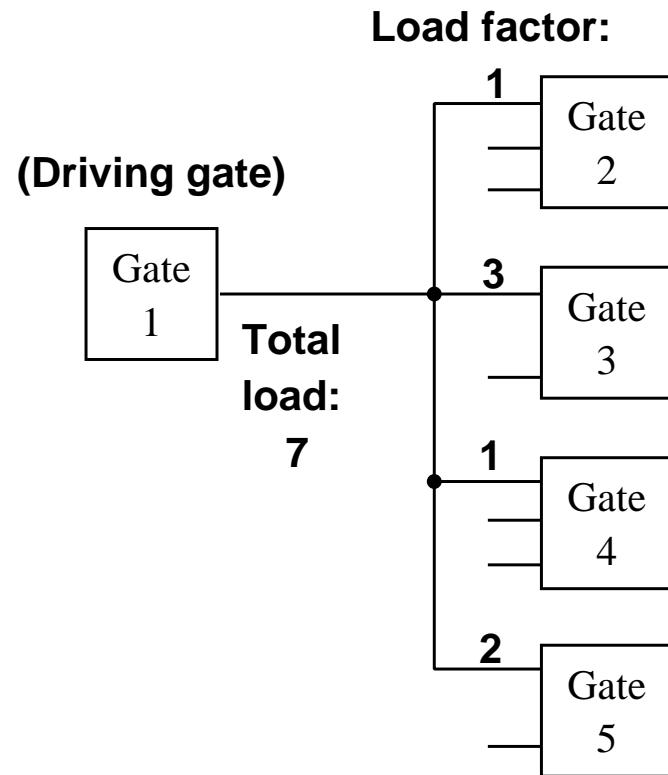
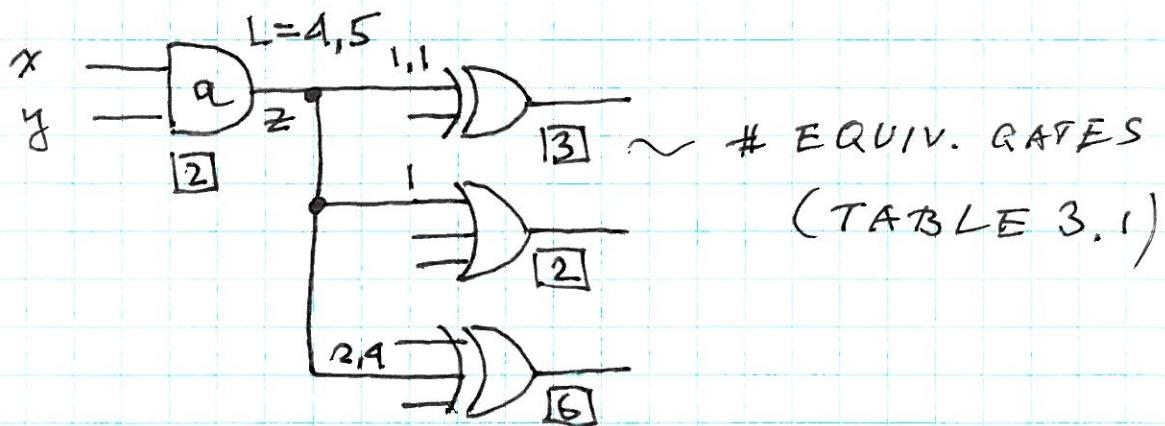


Figure 3.13: OUTPUT LOAD OF GATE 1.

Table 3.2: Characteristics of a family of CMOS gates

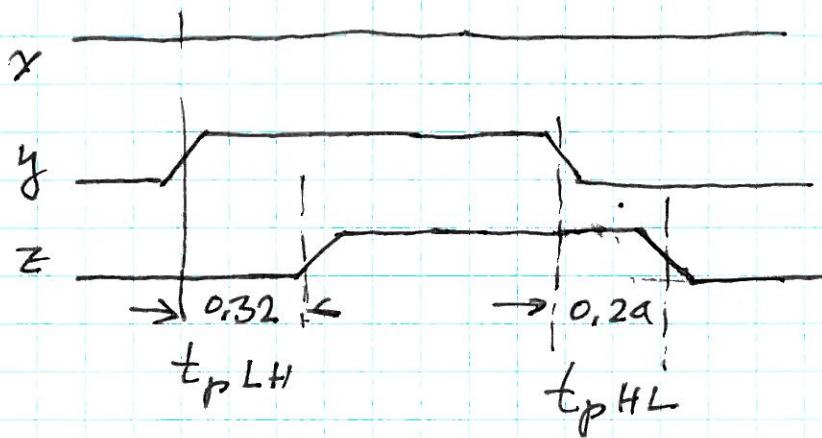
Gate type	Fan-in	Propagation delays		Load factor [standard loads]	Size [equiv. gates]
		t_{pLH} [ns]	t_{pHL} [ns]		
AND	2	$0.15 + 0.037L$	$0.16 + 0.017L$	1.0	2
AND	3	$0.20 + 0.038L$	$0.18 + 0.018L$	1.0	2
OR	2	$0.12 + 0.037L$	$0.20 + 0.019L$	1.0	2
OR	3	$0.12 + 0.038L$	$0.34 + 0.022L$	1.0	2
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$	1.0	1
NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$	1.0	1
NAND	3	$0.07 + 0.038L$	$0.09 + 0.039L$	1.0	2
NAND	8	$0.24 + 0.038L$	$0.42 + 0.019L$	1.0	6
NOR	2	$0.06 + 0.075L$	$0.07 + 0.016L$	1.0	1
NOR	3	$0.16 + 0.111L$	$0.08 + 0.017L$	1.0	2
NOR	8	$0.54 + 0.038L$	$0.23 + 0.018L$	1.0	6
XOR	2*	$0.30 + 0.036L$	$0.30 + 0.021L$	1.1	3
		$0.16 + 0.036L$	$0.15 + 0.020L$	2.0	
XOR	3*	$0.50 + 0.038L$	$0.49 + 0.027L$	1.1	6
		$0.28 + 0.039L$	$0.27 + 0.027L$	2.4	
		$0.19 + 0.036L$	$0.17 + 0.025L$	2.1	
XNOR	2*	$0.30 + 0.036L$	$0.30 + 0.021L$	1.1	3
		$0.16 + 0.036L$	$0.15 + 0.020L$	2.0	
XNOR	3*	$0.50 + 0.038L$	$0.49 + 0.027L$	1.1	6
		$0.28 + 0.039L$	$0.27 + 0.027L$	2.3	
		$0.19 + 0.036L$	$0.17 + 0.025L$	1.3	
2-OR/NAND2	4	$0.17 + 0.075L$	$0.10 + 0.028L$	1.0	2
2-AND/NOR2	4	$0.17 + 0.075L$	$0.10 + 0.028L$	1.0	2

EXAMPLE: CALCULATE DELAY OF GATE a AND COST OF THE NETWORK



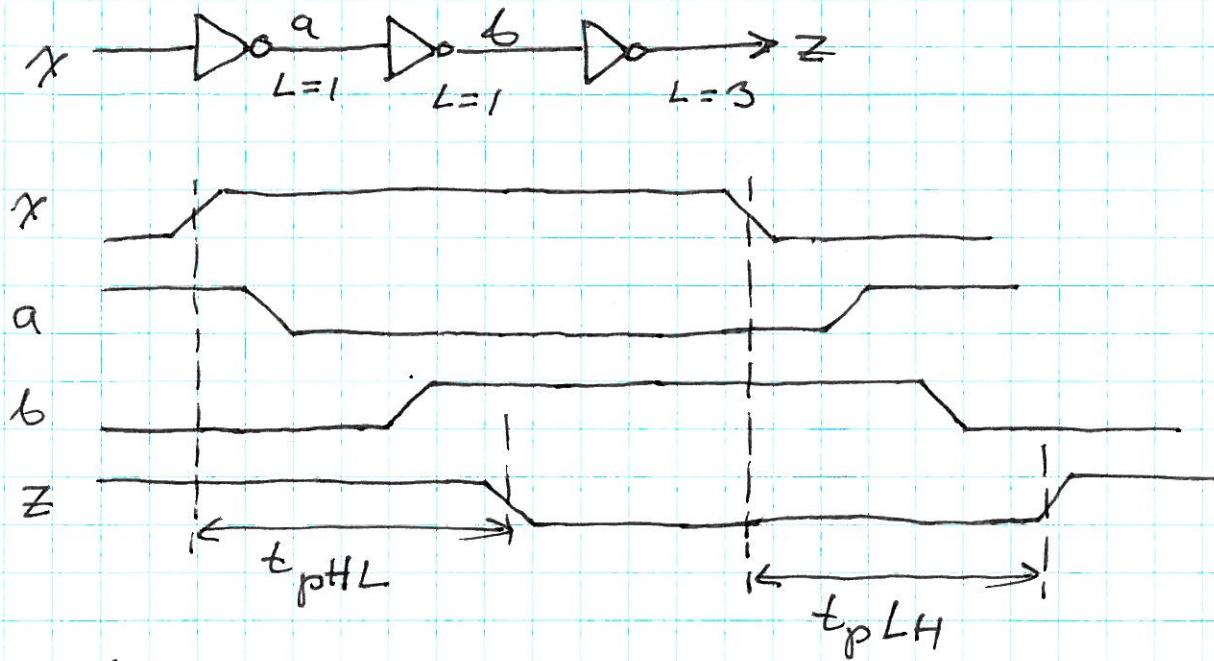
$$t_{PLH} = 0.15 + 0.037 \times 4.5 = 0.3165 \approx 0.32 \text{ us}$$

$$t_{PHL} = 0.16 + 0.017 \times 4.5 = 0.2365 \approx 0.24 \text{ us}$$



COST: $2 + 3 + 2 + 6 = 13$ EQUIVALENT GATES

EXAMPLE: CALCULATE $t_{pHL}(x, z)$ AND $t_{pLH}(x, z)$



$$t_{pHL}(x, z) = t_{pHL}(x, a) + t_{pLH}(a, b) + t_{pHL}(b, z)$$

NOT: $t_{pLH} = 0,02 + 0,038 \times L$

$$t_{pHL} = 0,05 + 0,017 \times L$$

$$\begin{aligned} t_{pHL}(x, z) &= 0,05 + 0,017 \times 1 \\ &\quad + 0,02 + 0,038 \times 1 \\ &\quad + \underbrace{0,05 + 0,017 \times 3}_{0,12 + 0,106} = 0,226 \mu s \end{aligned}$$

SIMILARLY FOR t_{pLH}

A GATE IN A NETWORK HAS A LOAD $L=70$
ITS PROP. DELAYS ARE:

$$t_{pHL} = 0.43 + 0.15L \text{ (ns)} \quad t_{pLH} = 0.35 + 0.25L \text{ (ns)}$$

a) $t_{pHL} = 0.43 + 0.15 \times 70 = 10.93 \text{ ns}$

$$t_{pLH} = 0.35 + 0.25 \times 70 = 17.85 \text{ ns}$$

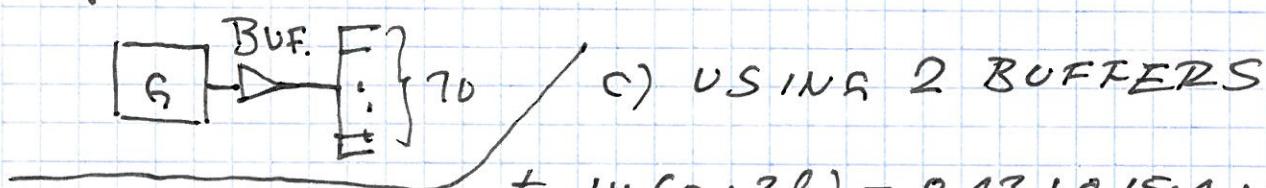


b) USING A BUFFER WITH LOAD FACTOR $I=2$ AND PROP. DELAYS

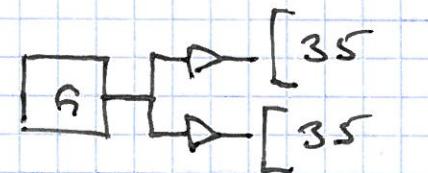
$$t_{pHL(\text{buff})} = t_{pLH(\text{buff})} = 0.6 + 0.02L \text{ (ns)}$$

$$t_{pHL(\text{gate+buff})} = 0.43 + 0.15 \times 2 + 0.6 + 0.02 \times 70 = 2.73 \text{ ns}$$

$$t_{pLH(\text{gate+buff})} = 0.35 + 0.25 \times 2 + 0.6 + 0.02 \times 70 = 2.85 \text{ ns}$$



c) USING 2 BUFFERS



$$t_{pHL(g+2b)} = 0.43 + 0.15 \times 4 + 0.6 + 0.02 \times 35 = 2.33 \text{ ns}$$

$$t_{pLH(g+2b)} = 0.35 + 0.25 \times 4 + 0.6 + 0.02 \times 35 = 2.65 \text{ ns}$$

d) DETERMINE OPTIMUM # OF BUFFERS n

$$t_{pHL(g+nb)} = 0.43 + 0.15 \times 2n + 0.6 + 0.02 \times \lceil 70/n \rceil = 1.03 + 0.3n + 0.02 \times \lceil 70/n \rceil$$

$$t_{pLH(g+nb)} = 0.35 + 0.25 \times 2n + 0.6 + 0.02 \times \lceil 70/n \rceil = 0.95 + 0.5n + 0.02 \times \lceil 70/n \rceil$$

THE FUNCTION HAS A MINIMUM. FOR $n=3$, $t_{pHL}=2.41$ $t_{pLH}=2.93 > (c)$. SO $n=2$ IS THE BEST NUMBER OF BUFFERS

VOLTAGE VARIATIONS AND NOISE MARGINS

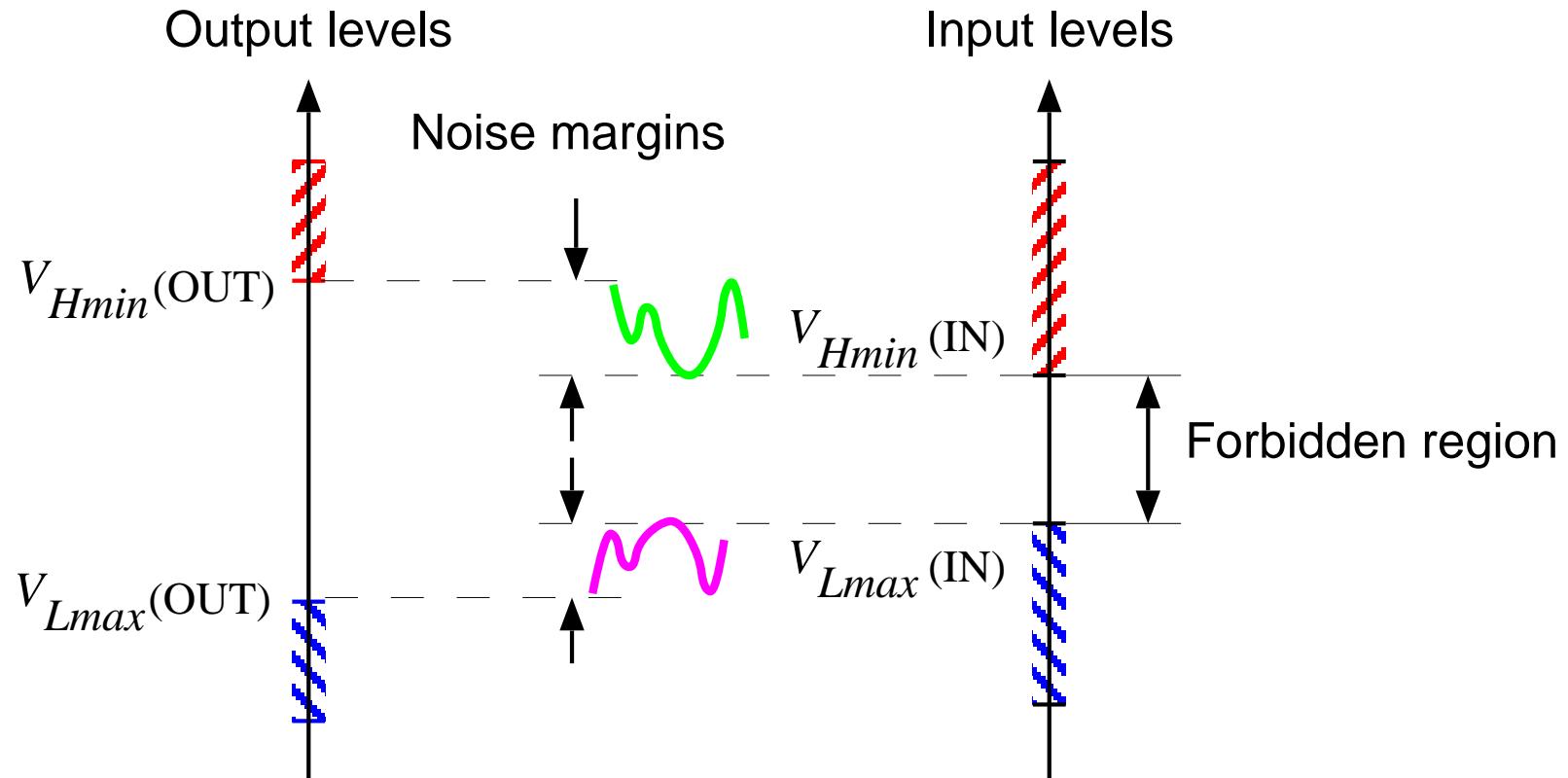


Figure 3.14: NOISE MARGINS.

NOISE MARGINS: EXAMPLE

LEVELS			NOISE MARGIN
HIGH	$V_{Hmin}(\text{OUT})$	2.4 V	0.4 V
	$V_{Hmin}(\text{IN})$	2.0 V	
LOW	$V_{Lmax}(\text{OUT})$	0.4 V	0.4 V
	$V_{Lmax}(\text{IN})$	0.8 V	

CONNECTING MODULES TO A BUS

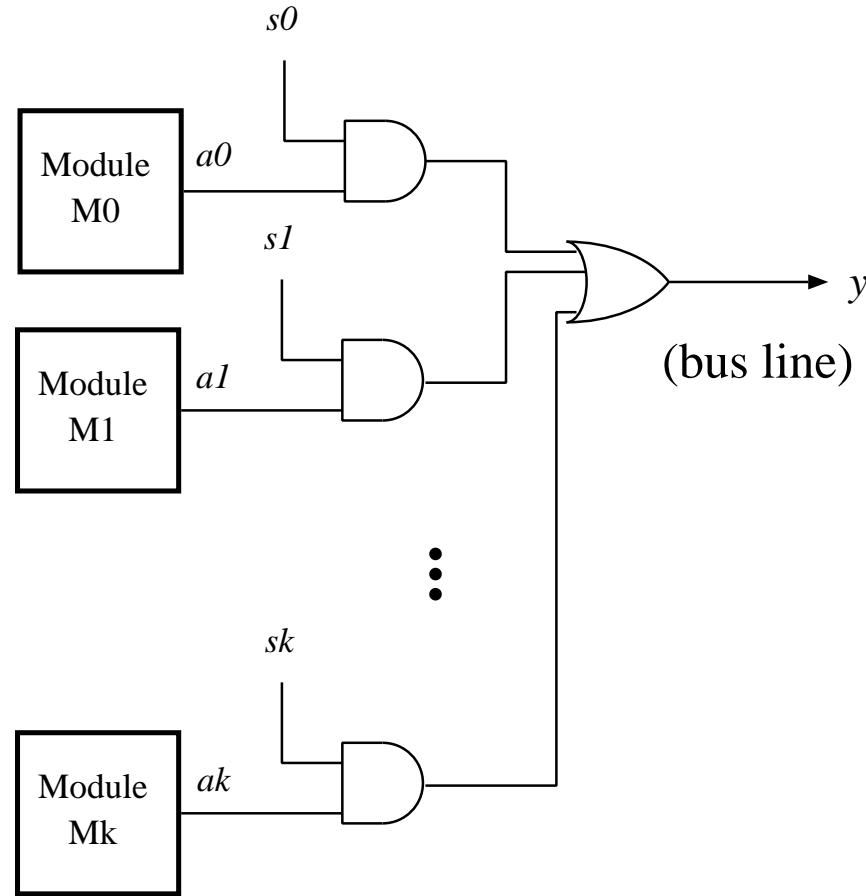
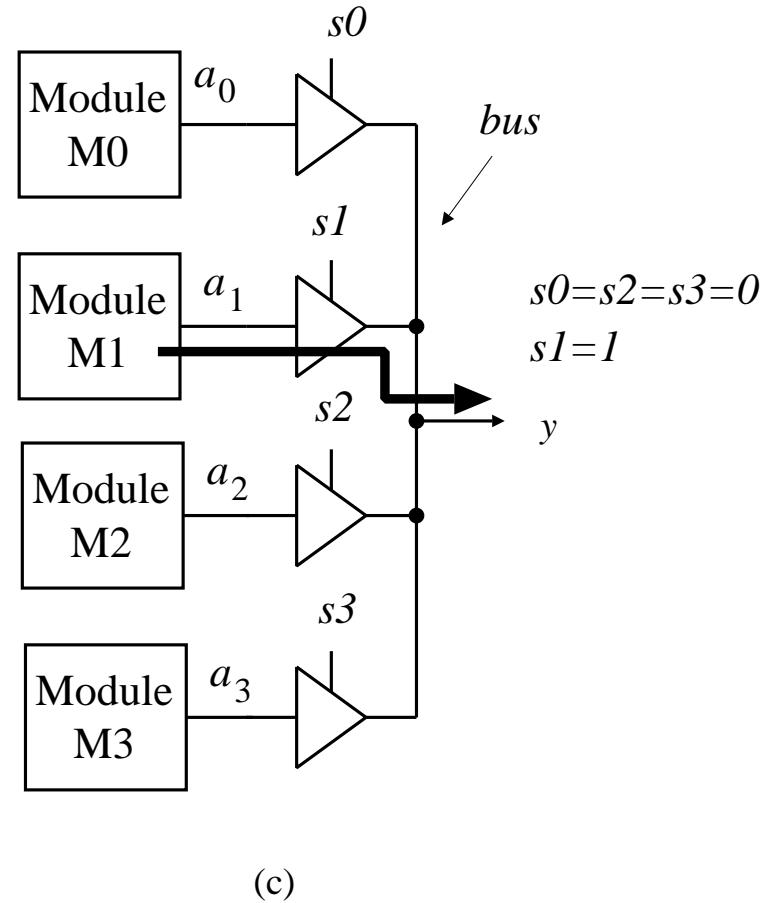


Figure 3.15: GATE NETWORK FOR SELECTING A MODULE OUTPUT.

THREE-STATE DRIVER (BUFFER)



(c)

Figure 3.16: c) EXAMPLE OF USE OF THREE-STATE DRIVERS

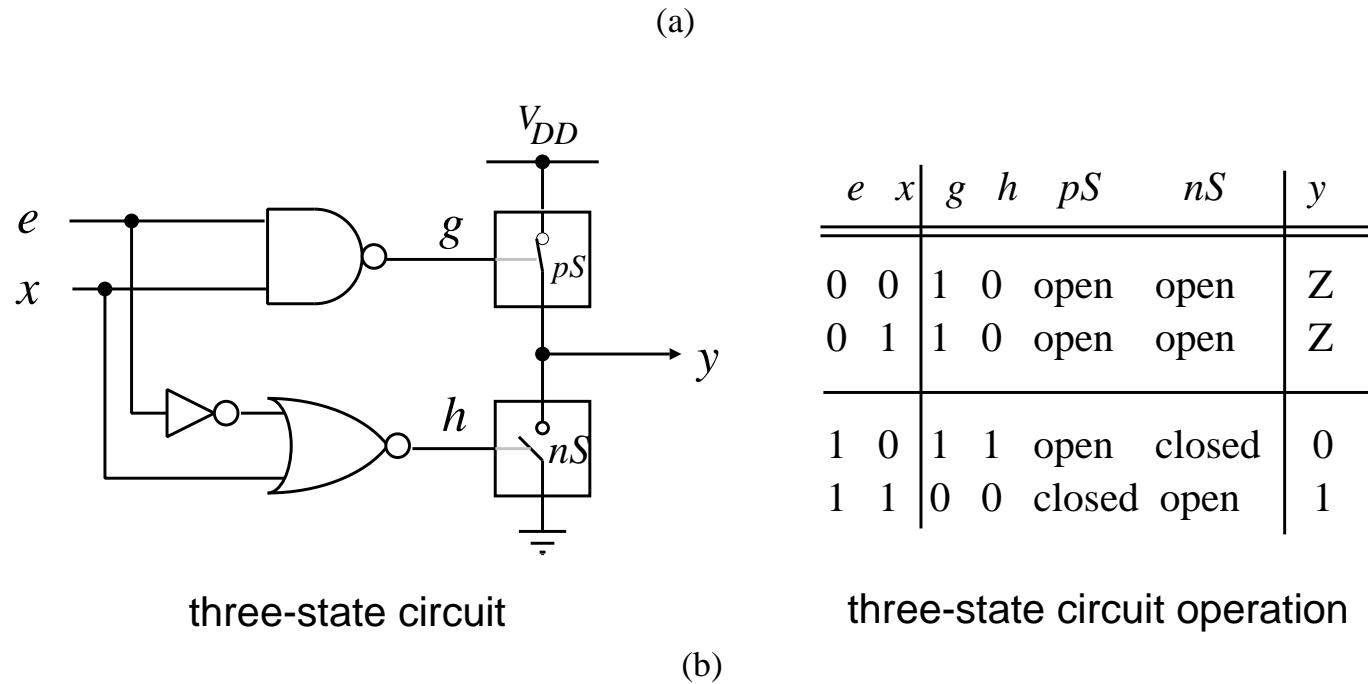
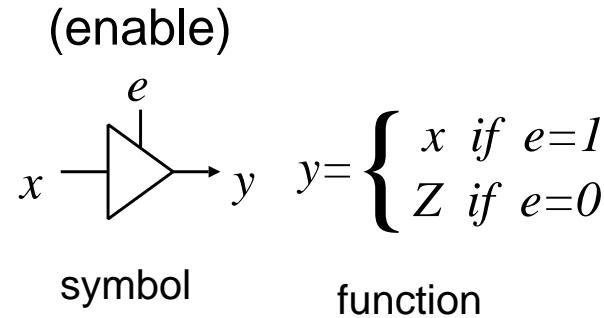


Figure 3.16: a) THREE-STATE GATE: SYMBOL AND FUNCTION. b) CIRCUIT AND OPERATION.

VLSI CIRCUIT-LEVEL DESIGN STYLES

- FULL-CUSTOM
- SEMI-CUSTOM (standard cells)
- GATE-ARRAY; FIELD-PROGRAMMABLE GATE ARRAY (FPGA)

FPGAs DISCUSSED IN CHAPTER 12

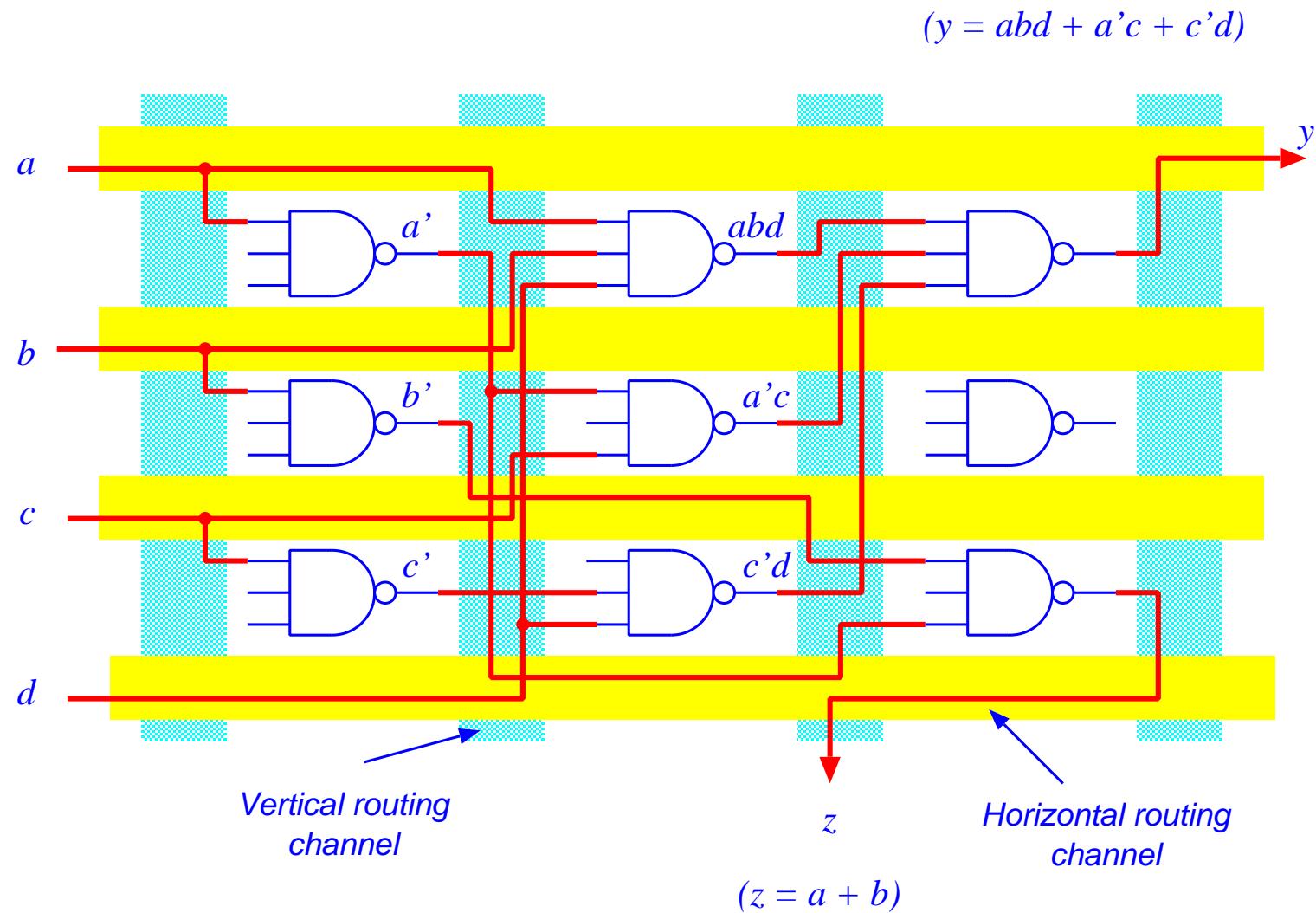


Figure 3.17: EXAMPLE OF GATE ARRAY.

PACKAGING LEVEL: CHIPS, BOARDS, AND CABINETS

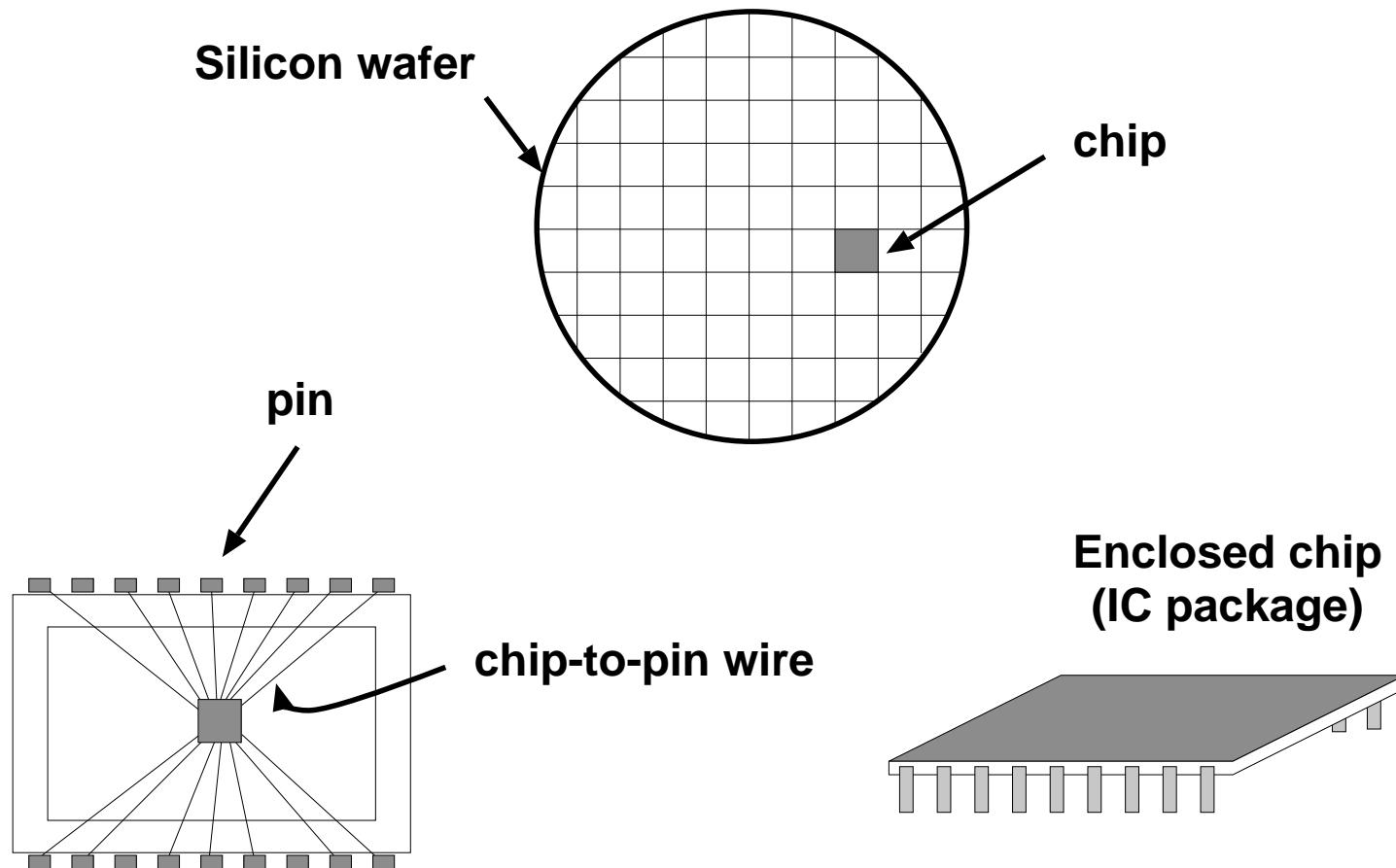


Figure 3.18: SILICON WAFER, CHIP AND INTEGRATED CIRCUIT PACKAGE

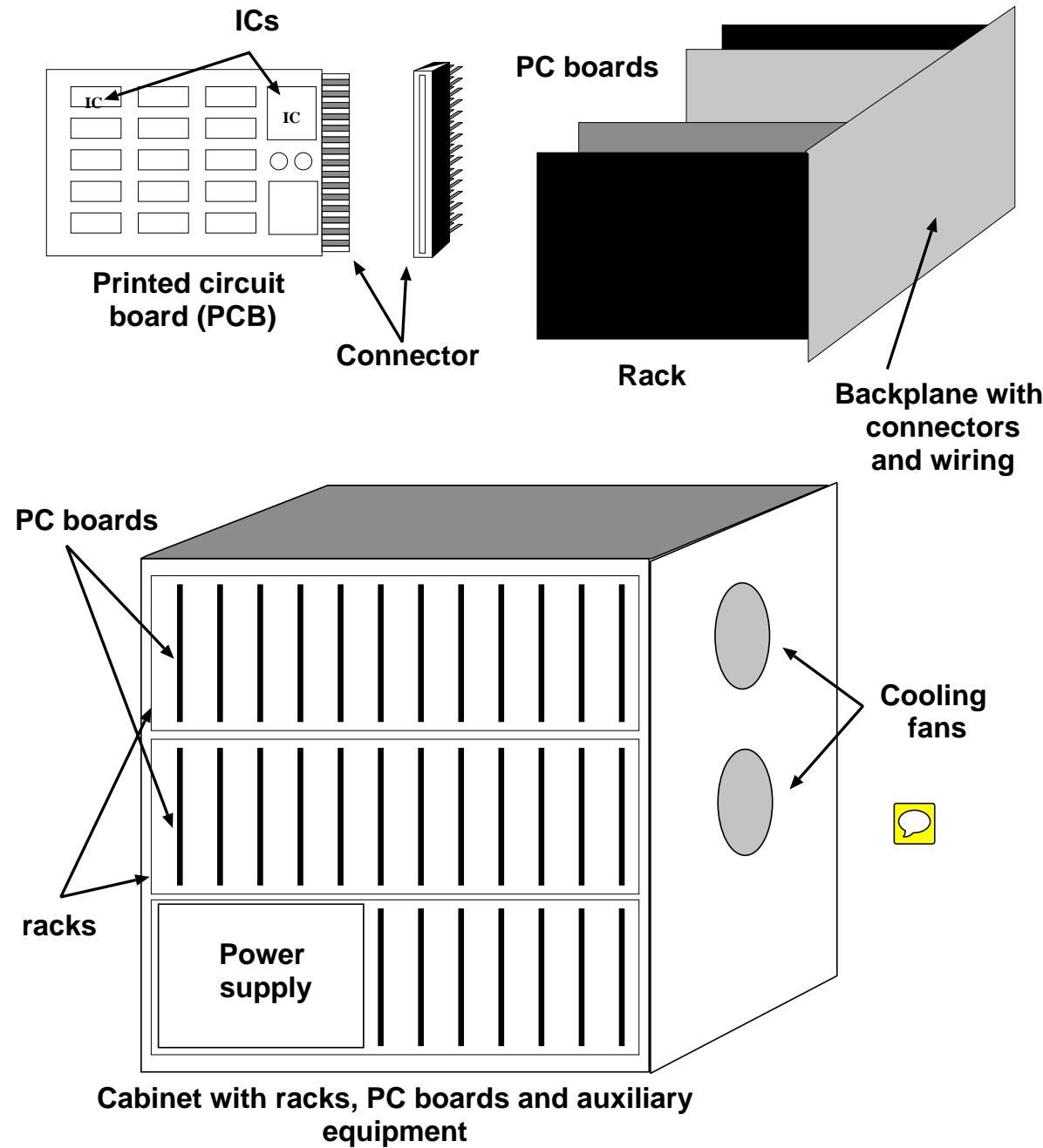


Figure 3.19: PACKAGING LEVELS

PACKAGING LEVELS: EXAMPLE



IBM 3081 central processing unit:

Level of Packaging	Number of Components	Size [mm × mm]
Module	100–133 chips	90 × 90
PC Board	6 – 9 modules	600 × 700
Subsystem (processor)	3 boards	
System (CPU)	2 subsystems	