Digital System Design

Instructor: Dr.Beitollahi

Homework 2

Topic: Intermediate VHDL (1)

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1) Answer the following questions: (10 points)

- Suggest a scenario where aliases could be beneficial in VHDL design.
- When are the assignement operators <= , := and => typically utilized in VHDL code?
- What do language defined attributes do?
- What is the difference between std_logic and std_ulogic types in VHDL?
- What is the usage of conv_std_logic_vector(p,b) and conv_signed(p.b)?

2) Design a FIFO Buffer with a capacity of 11, 8 bits data. You need to implement the following signals: (15 points)

- **clk** for clock
- **rst** to reset buffer
- **write** to enable writing new data to buffer
- **read** to enable reading data from buffer
- **full** to indicate the buffer is full
- **empty** to indicate the buffer is empty

❖ if the buffer is full and the write signal is enabled, the new data is dropped and nothing happens.
❖ if the buffer is empty and the read signal is enabled, nothing happens.

3) Design a Stack to store n, m bits data. You need to implement the following signals: (15 points)

- **clk** for clock
- **rst** to reset buffer
- **push** to enable pushing new data to stack
- **pop** to enable popping data from stack
- **full** to indicate the stack is full
- **empty** to indicate the stack is empty
- **error** to indicate the request can't be serviced

❖ **error:**
1. Stack is full and the write signal is enabled.
2. Stack is empty and the read signal is enabled.

❖ **n** and **m** must be implemented using **generics.**

4) Design a circuit for a clock with an alarm. This circuit has a signal named **clk** which determines the passage of seconds, to display the time by this circuit, we will have 8 bits for the minutes, with 4 bits for the least significant digit and 4 bits for the most significant digit. For the hours, we will need 4 bits for the least significant digit and 2 bits for the most significant digit. The signal reset will set all minute and hour values to zero. If the **set_clock** signal is high, we can input our desired time and set it. similarly, if **set_alarm** is high, we can set the alarm time by inputting our desired time. Whenever the current time reaches the specified alarm time, the **alarm_signal** will become high and will remain on until the **stop_alarm** is set. Implement this circuit using the VHDL language. (20 points)

5) Define a type for complex numbers that includes values for the real part (x) and the imaginary part (y). Then, write a program that takes two complex numbers and three signals for multiplication, addition and subtraction operators as input. It performs the desired operation on the two given numbers and output the result. (20 points)

❖ Only one of the operator signals will be equal to 1 at any given time.

6) Design a street traffic light. The initial state of this light is green, and after 15 seconds, the light color changes to yellow. After staying in this state for 5 seconds, the light color turns red. After 10 seconds in this state, the cycle repeats again. The delay for each color should be displayed in BCD format at the output. (20 points)