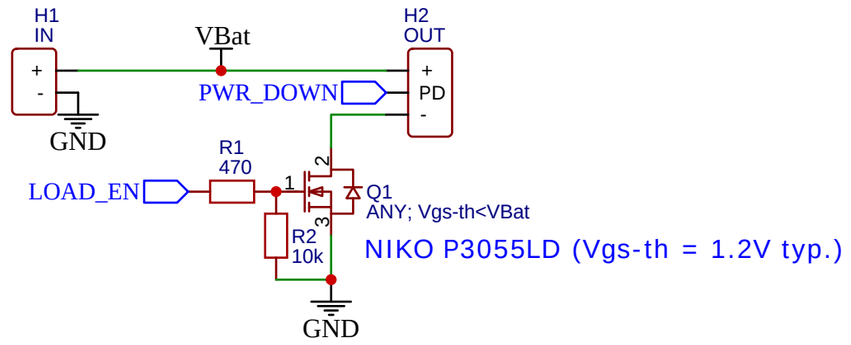
R1 should be somewhere around 100R (gate current limit)
R2 - R7 should be somewere like 1k ~ 10k (logic pull up/down)

IN is 1.8V - 5.0V supply (e.g. LiPo, 2-3x Akaline)
OUT to load (e.g. ESP)
PWR_DOWN is pulled high. Pull lowto enter low-power mode and power down the load.

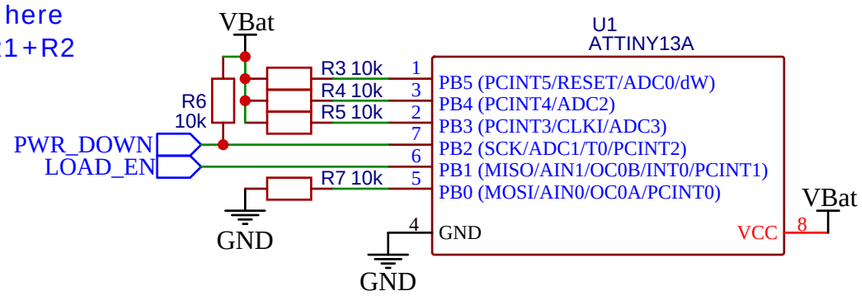


NIKO P3055LD (Vgs-th = 1.2V typ.)

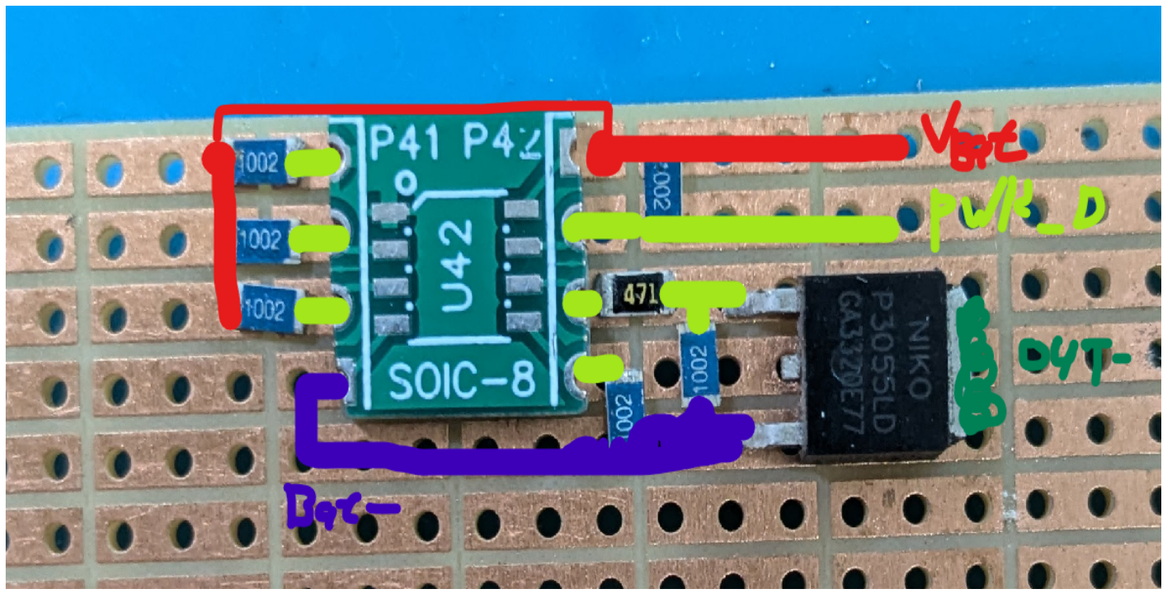
R4-R7 prevent PB4-PB1 from floating
floating inputs will increase power usage
direct GND connection not possible because ISP is needed

R3 is needed to de-assert RESET
+ ensures PB5 is not floating

PB0 does not require a pull-down here
since it's pulled to GND through R1+R2



ensure U1 is physically accessible via SOIC clip for programming



U1 code flow:
- disable ADC, internal COMP, WDT, ... (reduce power)
- set PWR_DOWN to input
- set LOAD_EN to output, set HIGH
- wait until PWR_DOWN is LOW
- set all pins to INPUT, no pullup (reduce power)
- [if any more possible, reduce power usage even further]
- wait ~ 30 minutes in idle loop
- reset

NOTE: schematic only, footprints not considered

TITLE: attiny13-sleep-mcu		REV: 1.0
	Company:	Sheet: 1/1
	Date: 2024-10-15 Drawn By:	