



Alaska[®] 88E1545/88E1543/88E1548 Datasheet

Integrated 10/100/1000 Mbps Energy
Efficient Ethernet Transceiver




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Alaska® 88E1545/88E1543/88E1548 Datasheet

Integrated 10/100/1000 Mbps Energy Efficient Ethernet Transceiver

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Overview

The latest generation Alaska® Quad family of single-chip devices contains four independent Gigabit Ethernet transceivers on a single monolithic IC. Each transceiver performs all the physical layer functions for 1000BASE-T and 100BASE-TX full or half-duplex Ethernet on CAT 5 twisted pair cable, and 10BASE-T full or half-duplex Ethernet on CAT 3, 4, and 5 cable.

The Alaska 88E1545 device supports the Quad-Serial Gigabit Media Independent Interface (QSGMII) for direct connection to a MAC/Switch port. The QSGMII combines four ports of SGMII running at 1.25 Gbps onto a single differential-pair of signals operating at 5 Gbps. QSGMII primarily decreases the number of I/O pins on the MAC interface compared to the SGMII and lowers the overall power consumption.

The Alaska 88E1543 device supports SGMII on the MAC interface in a Copper to SGMII application. In addition, the SGMII interface can also be used as media interface for Fiber/SFP applications. The device can be also configured to operate in SGMII (System) to Auto-Media Copper/Fiber mode for mixed media applications.

The Alaska 88E1548 device supports four modes of operation. Three modes use the QSGMII to support either copper, SGMII/Fiber or auto media detect to copper or SGMII/Fiber. The fourth mode supports SGMII to copper directly. The device supports IEEE 802.3az Energy Efficient Ethernet (EEE) and is IEEE 802.3az compliant.

The device integrates MDI interface termination resistors and capacitors into the PHY. This resistor integration simplifies board layout and lowers board cost by reducing the number of external components. The new Marvell® calibrated resistor scheme will achieve and exceed the accuracy requirements of the IEEE 802.3 return loss specifications. The device consumes 400 mW per port in copper applications. This reduces the overall system cost by eliminating heat-sink and reducing air-flow requirements.

The device is fully compliant with the IEEE 802.3 standard. The device includes the PMD, PMA, and PCS sub-layers. The device performs PAM5, 8B/10B, 4B/5B, MLT-3, NRZI, and Manchester encoding/decoding; digital clock/data recovery; stream cipher scrambling/descrambling; digital adaptive equalization for the receiver data path as well as digital filtering for pulse-shaping for the line transmitter; and Auto-Negotiation and management functions.

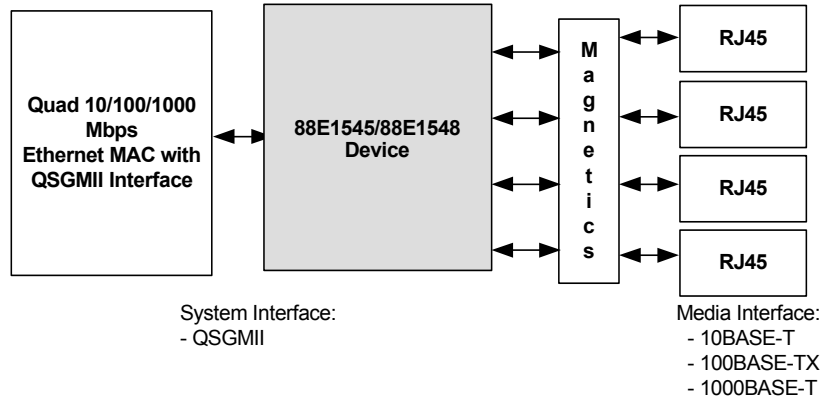
The device supports Auto-MDI/MDIX at all three speeds to enable easier installation and reduced installation costs.

The device uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a gigabit per second data rate. The device dissipates very low power while achieving robust performance in noisy environments. The device is supported with an integrated Advanced Virtual Cable Tester® (VCT™) enabling fault detection and advanced cable performance monitoring.

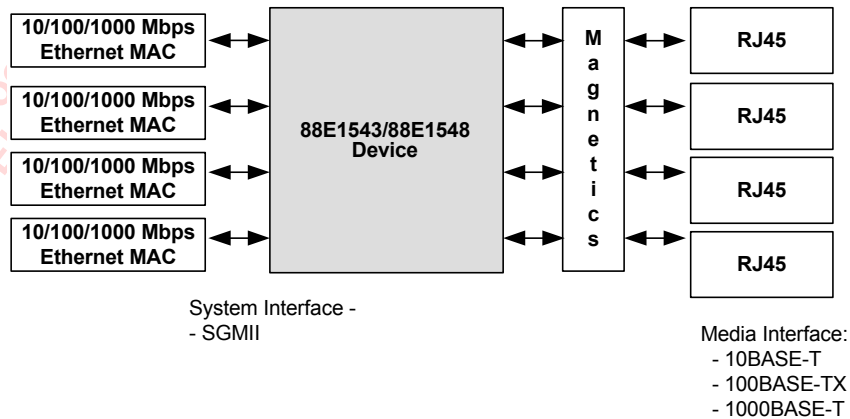
Features

- Supports Energy Efficient Ethernet (EEE) - IEEE 802.3az compliant
- 88E1545 supports one mode of operation
 - QSGMII (System) to Copper
- 88E1543 supports two modes of operation
 - SGMII (System) to Copper
 - Dual-port SGMII (system) to Copper/Fiber
- 88E1548 supports four modes of operation
 - QSGMII (System) to Copper
 - QSGMII (System) to SGMII/Fiber (Media)
 - QSGMII (System) to Copper/SGMII/Fiber Auto-Media
 - SGMII (System) to Copper
- Ultra low power consumption
- Integrated MDI interface termination resistors and capacitors
- Integrated Advanced Virtual Cable Tester® (VCT™) cable diagnostic feature
- "Downshift" mode for two-pair cable installations
- Supports up to four LEDs per port programmable to indicate link, speed, and activity functions
- Supports Advance Power Management modes for significant power savings
- Automatic MDI/MDIX crossover for all 3 speeds of operation including 100BASE-TX and 10BASE-T
- Automatic polarity correction
- 25 MHz, 125 MHz, or 156.25 MHz reference clock options
- Clock cascade up to two downstream devices
- Various loopback modes for diagnostics
- Supports IEEE 1149.1 JTAG and 1149.6 AC JTAG

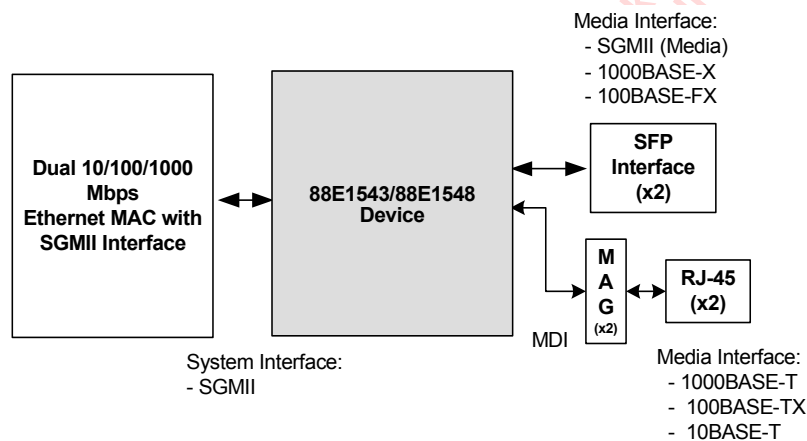
- Available in Green compliant package only
- Manufactured in a 14 x 20 mm 128-Pin LQFP with EPAD package
- 88E1545 and 88E1543 devices manufactured in a 14 x 20 mm 128-Pin LQFP with EPAD package
- 88E1548 devices manufactured in a 15 x 15 mm 196-Pin TFBGA package



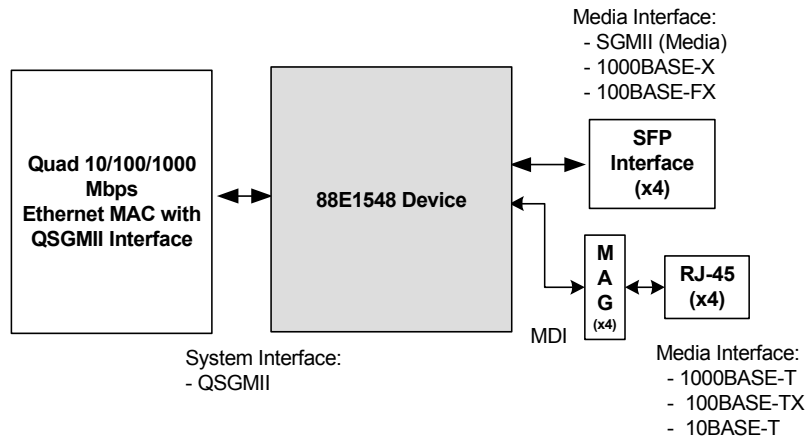
88E1545/88E1548 Device Application - QSGMII (System) to Copper



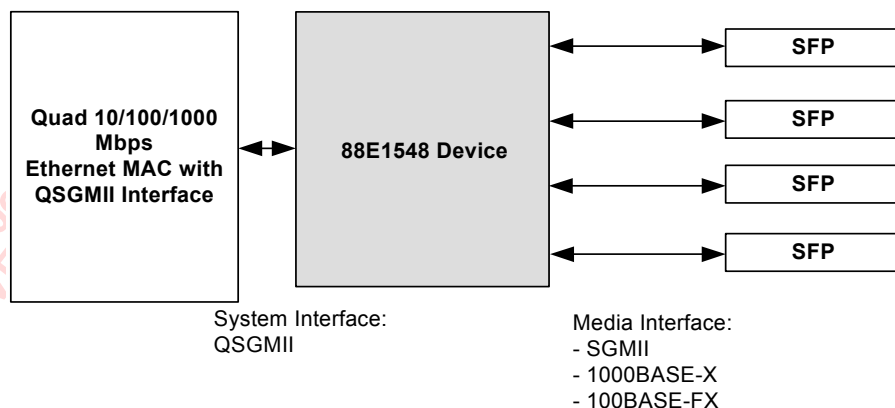
88E1543/88E1548 Device Application - SGMII (System) to Copper



88E1543/88E1548 Device Application - Dual-port SGMII (System) to Copper/SGMII/Fiber Auto Media Detect



88E1548 Device Application - QSGMII (System) to Copper/SGMII/Fiber Auto Media Detect



88E1548 Device Application - QSGMII (System) to SGMII/Fiber (Media)

Table 1: 88E1545/88E1543/88E1548 Device Features

Features	88E1545	88E1543	88E1548
Quad-port QSGMII (System) to Copper	Yes	No	Yes
Quad-port QSGMII (System) to Auto-media Copper/Fiber	No	No	Yes
Quad-port SGMII (System) to Copper	No	Yes	Yes
Dual-port SGMII (System) to Copper	No	Yes	Yes
Dual-port SGMII (System) to Fiber	No	Yes	Yes
Dual-port SGMII (System) to Auto-media Copper/Fiber	No	Yes	Yes
100BASE-FX support	No	Yes	Yes
IEEE 802.3az Energy Efficient Ethernet	Yes	Yes	Yes
Auto-Media Detect	No	Yes ¹	Yes
Package	14mm x 20mm 128-pin LQFP with EPAD		15 mm x 15 mm 196-pin TFBGA

1. 88E1543 auto-media detect is only supported in dual-port SGMII (System) to Auto-media Copper/Fiber configuration.

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1 Signal Description

1.1 Pin Description

Table 2: Pin Type Definitions

Pin Type	Definition
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

1.1.1 88E1545 128-Pin LQFP Package Pinout

Figure 1: 88E1545 Device 128-Pin LQFP Package (Top View)

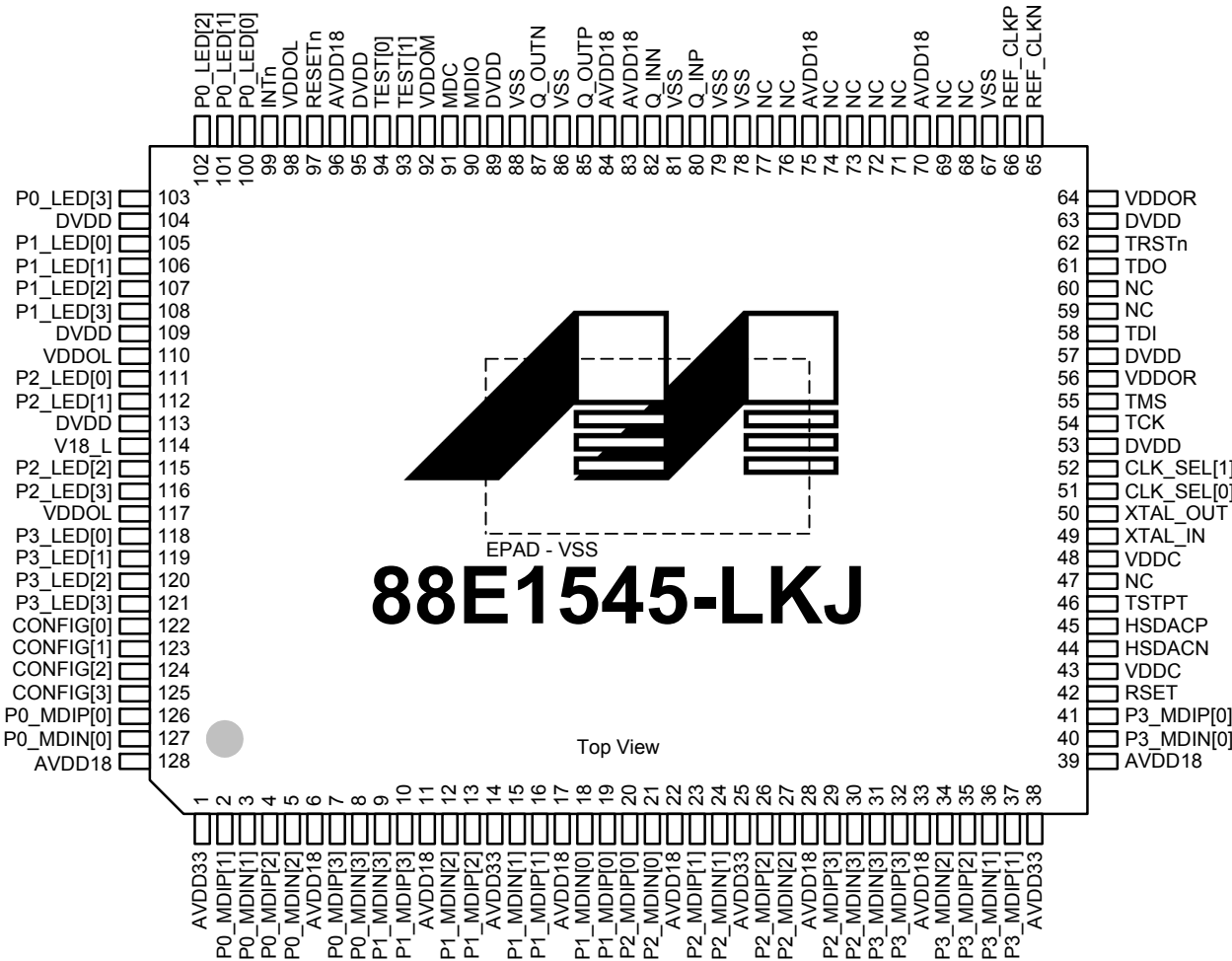


Table 3: Media Dependent Interface Port 0

88E1545 Pin #	Pin Name	Pin Type	Description
126 127	P0_MDIP[0] P0_MDIN[0]	I/O	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] correspond to BI_DA±. In MDIX configuration, MDIP/N[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. NOTE: Unused MDI pins must be left floating. The 88E1545 device contains an internal 100 ohm resistor between the MDIP/N[0] pins.
2 3	P0_MDIP[1] P0_MDIN[1]	I/O	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] correspond to BI_DB±. In MDIX configuration, MDIP/N[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. NOTE: Unused MDI pins must be left floating. The 88E1545 device contains an internal 100 ohm resistor between the MDIP/N[1] pins.
4 5	P0_MDIP[2] P0_MDIN[2]	I/O	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] correspond to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. NOTE: Unused MDI pins must be left floating. The 88E1545 device contains an internal 100 ohm resistor between the MDIP/N[2] pins.
7 8	P0_MDIP[3] P0_MDIN[3]	I/O	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] correspond to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. NOTE: Unused MDI pins must be left floating. The 88E1545 device contains an internal 100 ohm resistor between the MDIP/N[3] pins.

Table 4: Media Dependent Interface Port 1

88E1545 Pin #	Pin Name	Pin Type	Description
19 18	P1_MDIP[0] P1_MDIN[0]	I/O	Media Dependent Interface[0] for Port 1. Refer to P0_MDI[0]P/N.
16 15	P1_MDIP[1] P1_MDIN[1]	I/O	Media Dependent Interface[1] for Port 1. Refer to P0_MDI[1]P/N.
13 12	P1_MDIP[2] P1_MDIN[2]	I/O	Media Dependent Interface[2] for Port 1. Refer to P0_MDI[2]P/N.
10 9	P1_MDIP[3] P1_MDIN[3]	I/O	Media Dependent Interface[3] for Port 1. Refer to P0_MDI[3]P/N.

Table 5: Media Dependent Interface Port 2

88E1545 Pin #	Pin Name	Pin Type	Description
20 21	P2_MDIP[0] P2_MDIN[0]	I/O	Media Dependent Interface[0] for Port 2. Refer to P0_MDI[0]P/N.
23 24	P2_MDIP[1] P2_MDIN[1]	I/O	Media Dependent Interface[1] for Port 2. Refer to P0_MDI[1]P/N.
26 27	P2_MDIP[2] P2_MDIN[2]	I/O	Media Dependent Interface[2] for Port 2. Refer to P0_MDI[2]P/N.
29 30	P2_MDIP[3] P2_MDIN[3]	I/O	Media Dependent Interface[3] for Port 2. Refer to P0_MDI[3]P/N.

Table 6: Media Dependent Interface Port 3

88E1545 Pin #	Pin Name	Pin Type	Description
41 40	P3_MDIP[0] P3_MDIN[0]	I/O	Media Dependent Interface[0] for Port 3. Refer to P0_MDI[0]P/N.
37 36	P3_MDIP[1] P3_MDIN[1]	I/O	Media Dependent Interface[1] for Port 3. Refer to P0_MDI[1]P/N.
35 34	P3_MDIP[2] P3_MDIN[2]	I/O	Media Dependent Interface[2] for Port 3. Refer to P0_MDI[2]P/N.
32 31	P3_MDIP[3] P3_MDIN[3]	I/O	Media Dependent Interface[3] for Port 3. Refer to P0_MDI[3]P/N.

Table 7: QSGMII Interface

88E1545 Pin #	Pin Name	Pin Type	Description
80 82	Q_INP Q_INN	I	QSGMII Transmit Data. 5.0 GBaud input - Positive and Negative.
85 87	Q_OUTP Q_OUTN	O	QSGMII Receive Data. 5.0 GBaud output - Positive and Negative.

Table 8: Management Interface/Control

88E1545 Pin #	Pin Name	Pin Type	Description
91	MDC	I	Management Clock pin. MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 12.5 MHz.
90	MDIO	I/O	Management Data pin. MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.
99	INTn	OD	Interrupt pin. INTn functions as an active low interrupt output. The pull-up resistor used for the INTn should not be connected to voltage higher than VDDOL.

Table 9: LED/Configuration

88E1545 Pin #	Pin Name	Pin Type	Description
103 102 101 100	P0_LED[3] P0_LED[2] P0_LED[1] P0_LED[0]	O	Parallel LED Output Port 0 See Section 2.28 "LED" on page 111 for details.
108 107 106 105	P1_LED[3] P1_LED[2] P1_LED[1] P1_LED[0]	O	Parallel LED Output Port 1 See Section 2.28 "LED" on page 111 for details.
116 115 112 111	P2_LED[3] P2_LED[2] P2_LED[1] P2_LED[0]	O	Parallel LED Output Port 2 See Section 2.28 "LED" on page 111 for details.
121 120 119 118	P3_LED[3] P3_LED[2] P3_LED[1] P3_LED[0]	O	Parallel LED Output Port 3 See Section 2.28 "LED" on page 111 for details.

Table 9: LED/Configuration (Continued)

88E1545 Pin #	Pin Name	Pin Type	Description
125 124 123 122	CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	I	Global hardware configuration. See Section 2.31.1 "Hardware Configuration" on page 138 for details.
114	V18_L	I	VDDOL voltage control. Tie to VSS = VDDOL operating at 2.5V/3.3V Floating = VDDOL operating at 1.8V

Table 10: JTAG

88E1545 Pin #	Pin Name	Pin Type	Description
58	TDI	I, PU	Boundary scan test data input. TDI contains an internal 150 kohm pull-up resistor.
55	TMS	I, PU	Boundary scan test mode select input. TMS contains an internal 150 kohm pull-up resistor.
54	TCK	I, PU	Boundary scan test clock input. TCK contains an internal 150 kohm pull-up resistor.
62	TRSTn	I, PU	Boundary scan test reset input. Active low. TRSTn contains an internal 150 kohm pull-up resistor. For normal operation, TRSTn should be pulled low with a 4.7 kohm pull-down resistor.
61	TDO	O	Boundary scan test data output.

Table 11: Clock/Reset

88E1545 Pin #	Pin Name	Pin Type	Description
49	XTAL_IN	I	25 MHz Clock Input 25 MHz \pm 50 ppm tolerance crystal reference or oscillator input. XTAL_IN has internal ac-coupling. XTAL_IN must be left floating when it is not used. Refer to the 'Oscillator Level Shifting' (MV-S301630-00) application note for details on how to convert a 2.5V/3.3V clock source to 1.8V clock.
50	XTAL_OUT	O	25 MHz Crystal Output. 25 MHz \pm 50 ppm tolerance crystal reference. XTAL_OUT must be left floating when it is not used.

Table 11: Clock/Reset (Continued)

88E1545 Pin #	Pin Name	Pin Type	Description
66 65	REF_CLKP REF_CLKN	I	<p>25 MHz/125 MHz/156.25 MHz Reference Clock Input Positive and Negative ± 50 ppm tolerance differential clock inputs.</p> <p>REFCLKP/N inputs are LVDS differential inputs with a 100 ohm differential internal termination resistor and internal ac-coupling. If the REF_CLKP/N inputs are not used, the REF_CLKP/N must be left floating.</p> <p>REF_CLKP/N also supports 125 MHz single-ended clock. In this case, the unused pin must be connected with 0.1uF capacitor to ground.</p>
52 51	CLK_SEL[1] CLK_SEL[0]	I	<p>Reference Clock Selection</p> <p>CLK_SEL[1:0]</p> <p>00 = Use 156.25 MHz REF_CLKP/N</p> <p>01 = Use 125 MHz REF_CLKP/N</p> <p>10 = Use 25 MHz REF_CLKP/N</p> <p>11 = Use 25 MHz XTAL_IN/XTAL_OUT</p> <p>CLK_SEL[1:0] must be connected to VDDOR for configuration HIGH.</p>
97	RESETn	I	<p>Hardware reset. XTAL_IN must be active for a minimum of 10 clock cycles before the rising edge of RESETn. RESETn must be in inactive state for normal operation.</p> <p>The RESETn pin can accept 2.5V LVCMOS signalling when the VDDOL pin is connected to 3.3V supply.</p> <p>1 = Normal operation 0 = Reset</p>

Table 12: Test

88E1545 Pin #	Pin Name	Pin Type	Description
45 44	HSDACP HSDACN	O	<p>AC Test Points (Positive and Negative), TX_TCLK, and Clock Cascade Differential Outputs.</p> <p>The HSDACP/N outputs are used for AC Test Points, TX_TCLK, and Clock Cascade Differential Outputs. These pins must be connected to a 50 ohm termination resistor to VSS. These pins can be left floating if not used for clock cascade, IEEE testing, and debug test points are not of importance.</p> <p>When used for clock cascade purpose, these pins are differential LVDS clock outputs that must be routed differentially to the REF_CLKP/N inputs of the downstream devices. A maximum of 5 downstream devices are allowed. The clock frequency follows the clock frequency used for the REF_CLKP/N or XTAL_IN/OUT inputs.</p> <p>These pins are also used to bring out a differential TX_TCLK for IEEE testing and AC Test Points for debug purposes. When used for IEEE testing or AC Test Points, the clock cascade must be disabled.</p>

Table 12: Test (Continued)

88E1545 Pin #	Pin Name	Pin Type	Description
46	TSTPT	O	DC Test Point. The TSTPT pin should be left floating if not used.
93 94	TEST[1] TEST[0]	I, PD	Test Control. This pin should be left floating if not used.

Table 13: Reference

88E1545 Pin #	Pin Name	Pin Type	Description
42	RSET	I	Resistor Reference External 5.0 kohm 1% resistor connected to ground.

Table 14: Power & Ground

88E1545 Pin #	Pin Name	Pin Type	Description
53 57 63 89 95 104 109 113	DVDD	Power	1.0V Digital Supply
6 11 17 22 28 33 39 70 75 83 84 96 128	AVDD18	Power	1.8V Analog Supply.
1 14 25 38	AVDD33	Power	3.3V Analog Supply.
43 48	VDDC	Power	1.8V Supply ¹ .
98 110 117	VDDOL	Power	1.8V, 2.5V, or 3.3V I/O Supply ² . When V18_L is tied to VSS, VDDOL operates at 2.5V/3.3V. When V18_L is left floating, VDDOL operates at 1.8V.
92	VDDOM	Power	1.2V or 1.8V I/O Supply ³ . NOTE: For the 88E1545 device, VDDOM only supports 1.2V or 1.8V

Table 14: Power & Ground (Continued)

88E1545 Pin #	Pin Name	Pin Type	Description
56 64	VDDOR	Power	2.5V or 3.3V I/O Supply ⁴ .
67 78 79 81 86 88	VSS	Ground	Ground.
EPAD	VSS	Ground	Ground to device. The device is packaged in a 128-pin LQFP package with an EPAD (exposed die pad) on the bottom of the package. This EPAD must be soldered to VSS as it is the main VSS connection on the device. The location and dimensions of the EPAD can be found in Table 237 . See the Marvell® EPAD Layout Guidelines Application Note for EPAD layout details.

1. VDDC supplies XTAL_IN/OUT.
2. VDDOL supplies digital I/O pins for RESETn, LED, CONFIG, and INTn.
3. VDDOM supplies digital I/O pins for MDC, MDIO, and TEST.
4. VDDOR supplies digital I/O pins for TDO, TDI, TMS, TCK, TRSTn, REF_CLKP/N, and CLK_SEL[1:0].

Table 15: No Connect

88E1545 Pin #	Pin Name	Pin Type	Description
47 59 60 68 69 71 72 73 74 76 77	NC	I	No Connect. Do not connect these pins to anything. These pins must be left unconnected.

Table 16: I/O State at Various Test or Reset Modes

Pin(s)	Loopback	Software Reset	Hardware Reset	Power Down
MDI[3:0]P/N	Active	Tri-state	Tri-state	Tri-state
Q_OUTP/N	Active	Internally pulled up by terminations of 50 ohms	Internally pulled up by terminations of 50 ohms	Reg. 16.3 state 0 = Internally pulled up by terminations of 50 ohms 1 = Active
MDIO	Active	Active	Tri-state	Active
INTn	Active	Tri-state	Tri-state	Tri-state
TDO	Active	Active	Active	Active

1.1.2 88E1543 128-Pin LQFP Package Pinout

Figure 2: 88E1543 Device 128-Pin LQFP Package (Top View)

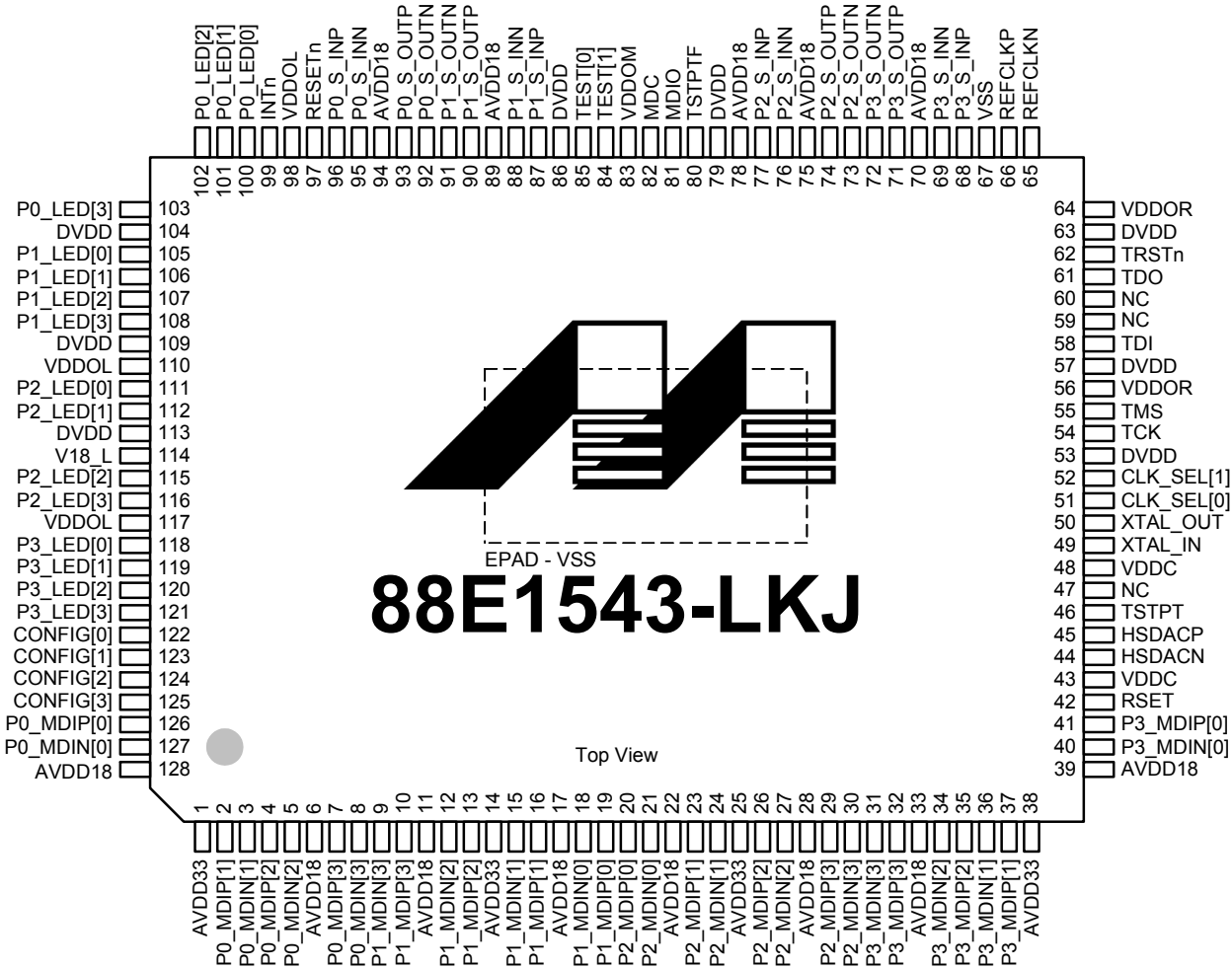


Table 17: Media Dependent Interface Port 0

88E1543 Pin #	Pin Name	Pin Type	Description
126 127	P0_MDIP[0] P0_MDIN[0]	I/O	Media Dependent Interface[0]. In 1000BASE-T mode in MDI configuration, MDIP/N[0] correspond to BI_DA±. In MDIX configuration, MDIP/N[0] correspond to BI_DB±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair. NOTE: Unused MDI pins must be left floating. The 88E1543 device contains an internal 100 ohm resistor between the MDIP/N[0] pins.
2 3	P0_MDIP[1] P0_MDIN[1]	I/O	Media Dependent Interface[1]. In 1000BASE-T mode in MDI configuration, MDIP/N[1] correspond to BI_DB±. In MDIX configuration, MDIP/N[1] correspond to BI_DA±. In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair. NOTE: Unused MDI pins must be left floating. The 88E1543 device contains an internal 100 ohm resistor between the MDIP/N[1] pins.
4 5	P0_MDIP[2] P0_MDIN[2]	I/O	Media Dependent Interface[2]. In 1000BASE-T mode in MDI configuration, MDIP/N[2] correspond to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±. In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used. NOTE: Unused MDI pins must be left floating. The 88E1543 device contains an internal 100 ohm resistor between the MDIP/N[2] pins.
7 8	P0_MDIP[3] P0_MDIN[3]	I/O	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] correspond to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. NOTE: Unused MDI pins must be left floating. The 88E1543 device contains an internal 100 ohm resistor between the MDIP/N[3] pins.

Table 18: Media Dependent Interface Port 1

88E1543 Pin #	Pin Name	Pin Type	Description
19 18	P1_MDIP[0] P1_MDIN[0]	I/O	Media Dependent Interface[0] for Port 1. Refer to P0_MDI[0]P/N.
16 15	P1_MDIP[1] P1_MDIN[1]	I/O	Media Dependent Interface[1] for Port 1. Refer to P0_MDI[1]P/N.
13 12	P1_MDIP[2] P1_MDIN[2]	I/O	Media Dependent Interface[2] for Port 1. Refer to P0_MDI[2]P/N.
10 9	P1_MDIP[3] P1_MDIN[3]	I/O	Media Dependent Interface[3] for Port 1. Refer to P0_MDI[3]P/N.

Table 19: Media Dependent Interface Port 2

88E1543 Pin #	Pin Name	Pin Type	Description
20 21	P2_MDIP[0] P2_MDIN[0]	I/O	Media Dependent Interface[0] for Port 2. Refer to P0_MDI[0]P/N.
23 24	P2_MDIP[1] P2_MDIN[1]	I/O	Media Dependent Interface[1] for Port 2. Refer to P0_MDI[1]P/N.
26 27	P2_MDIP[2] P2_MDIN[2]	I/O	Media Dependent Interface[2] for Port 2. Refer to P0_MDI[2]P/N.
29 30	P2_MDIP[3] P2_MDIN[3]	I/O	Media Dependent Interface[3] for Port 2. Refer to P0_MDI[3]P/N.

Table 20: Media Dependent Interface Port 3

88E1543 Pin #	Pin Name	Pin Type	Description
41 40	P3_MDIP[0] P3_MDIN[0]	I/O	Media Dependent Interface[0] for Port 3. Refer to P0_MDI[0]P/N.
37 36	P3_MDIP[1] P3_MDIN[1]	I/O	Media Dependent Interface[1] for Port 3. Refer to P0_MDI[1]P/N.
35 34	P3_MDIP[2] P3_MDIN[2]	I/O	Media Dependent Interface[2] for Port 3. Refer to P0_MDI[2]P/N.
32 31	P3_MDIP[3] P3_MDIN[3]	I/O	Media Dependent Interface[3] for Port 3. Refer to P0_MDI[3]P/N.

Table 21: SGMII Interface Port 0

88E1543 Pin #	Pin Name	Pin Type	Description
96 95	P0_S_INP P0_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
93 92	P0_S_OUTP P0_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

Table 22: SGMII Interface Port 1

88E1543 Pin #	Pin Name	Pin Type	Description
87 88	P1_S_INP P1_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
90 91	P1_S_OUTP P1_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

Table 23: SGMII Interface Port 2

88E1543 Pin #	Pin Name	Pin Type	Description
77 76	P2_S_INP P2_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
74 73	P2_S_OUTP P2_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

Table 24: SGMII Interface Port 3

88E1543 Pin #	Pin Name	Pin Type	Description
68 69	P3_S_INP P3_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
71 72	P3_S_OUTP P3_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

Table 25: Management Interface/Control

88E1543 Pin #	Pin Name	Pin Type	Description
82	MDC	I	Management Clock pin. MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 12.5 MHz.
81	MDIO	I/O	Management Data pin. MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.
99	INTn	OD	Interrupt pin. INTn functions as an active low interrupt output. The pull-up resistor used for the INTn should not be connected to voltage higher than VDDOL.

Table 26: LED/Configuration

88E1543 Pin #	Pin Name	Pin Type	Description
103 102 101 100	P0_LED[3] P0_LED[2] P0_LED[1] P0_LED[0]	O	Parallel LED Output Port 0 See Section 2.28, LED, on page 111 for details.
108 107 106 105	P1_LED[3] P1_LED[2] P1_LED[1] P1_LED[0]	O	Parallel LED Output Port 1 See Section 2.28, LED, on page 111 for details.
116 115 112 111	P2_LED[3] P2_LED[2] P2_LED[1] P2_LED[0]	O	Parallel LED Output Port 2 See Section 2.28, LED, on page 111 for details.
121 120 119 118	P3_LED[3] P3_LED[2] P3_LED[1] P3_LED[0]	O	Parallel LED Output Port 3 See Section 2.28, LED, on page 111 for details.
125 124 123 122	CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	I	Global hardware configuration. See Section 2.31.1, Hardware Configuration, on page 138 for details.
114	V18_L	I	VDDOL voltage control. Tie to VSS = VDDOL operating at 2.5V/3.3V Floating = VDDOL operating at 1.8V

Table 27: JTAG

88E1543 Pin #	Pin Name	Pin Type	Description
58	TDI	I, PU	Boundary scan test data input. TDI contains an internal 150 kohm pull-up resistor.
55	TMS	I, PU	Boundary scan test mode select input. TMS contains an internal 150 kohm pull-up resistor.
54	TCK	I, PU	Boundary scan test clock input. TCK contains an internal 150 kohm pull-up resistor.
62	TRSTn	I, PU	Boundary scan test reset input. Active low. TRSTn contains an internal 150 kohm pull-up resistor. For normal operation, TRSTn should be pulled low with a 4.7 kohm pull-down resistor.
61	TDO	O	Boundary scan test data output.

Table 28: Clock/Reset

88E1543 Pin #	Pin Name	Pin Type	Description
49	XTAL_IN	I	25 MHz Clock Input 25 MHz \pm 50 ppm tolerance crystal reference or oscillator input. XTAL_IN has internal ac-coupling. XTAL_IN must be left floating when it is not used. Refer to the 'Oscillator Level Shifting' (MV-S301630-00) application note for details on how to convert a 2.5V/3.3V clock source to 1.8V clock.
50	XTAL_OUT	O	25 MHz Crystal Output. 25 MHz \pm 50 ppm tolerance crystal reference. XTAL_OUT must be left floating when it is not used.
66 65	REF_CLKP REF_CLKN	I	25 MHz/125 MHz/156.25 MHz Reference Clock Input Positive and Negative \pm 50 ppm tolerance differential clock inputs. REFCLKP/N inputs are LVDS differential inputs with a 100 ohm differential internal termination resistor and internal ac-coupling. If the REF_CLKP/N inputs are not used, the REF_CLKP/N must be left floating. REF_CLKP/N also supports 125 MHz single-ended clock. In this case, the unused pin must be connected with 0.1uF capacitor to ground.

Table 28: Clock/Reset (Continued)

88E1543 Pin #	Pin Name	Pin Type	Description
52 51	CLK_SEL[1] CLK_SEL[0]	I	Reference Clock Selection CLK_SEL[1:0] 00 = Use 156.25 MHz REF_CLKP/N 01 = Use 125 MHz REF_CLKP/N 10 = Use 25 MHz REF_CLKP/N 11 = Use 25 MHz XTAL_IN/XTAL_OUT CLK_SEL[1:0] must be connected to VDDOR for configuration HIGH.
97	RESETn	I	Hardware reset. XTAL_IN must be active for a minimum of 10 clock cycles before the rising edge of RESETn. RESETn must be in inactive state for normal operation. The RESETn pin can accept 2.5V LVCMOS signalling when the VDDOL pin is connected to 3.3V supply. 1 = Normal operation 0 = Reset

Table 29: Test

88E1543 Pin #	Pin Name	Pin Type	Description
45 44	HSDACP HSDACN	O	AC Test Points (Positive and Negative), TX_TCLK, and Clock Cascade Differential Outputs. The HSDACP/N outputs are used for AC Test Points, TX_TCLK, and Clock Cascade Differential Outputs. These pins must be connected to a 50 ohm termination resistor to VSS. These pins can be left floating if not used for clock cascade, IEEE testing, and debug test points are not of importance. When used for clock cascade purpose, these pins are differential LVDS clock outputs that must be routed differentially to the REF_CLKP/N inputs of the downstream devices. A maximum of 5 downstream devices are allowed. The clock frequency follows the clock frequency used for the REF_CLKP/N or XTAL_IN/OUT inputs. These pins are also used to bring out a differential TX_TCLK for IEEE testing and AC Test Points for debug purposes. When used for IEEE testing or AC Test Points, the clock cascade must be disabled.
46	TSTPT	O	DC Test Point. The TSTPT pin should be left floating if not used.
80	TSTPTF	O	DC test point. The TSTPTF pin should be left floating if not used.
84 85	TEST[1] TEST[0]	I, PD	Test Control. This pin should be left floating if not used.

Table 30: Reference

88E1543 Pin #	Pin Name	Pin Type	Description
42	RSET	I	Resistor Reference External 5.0 kohm 1% resistor connected to ground.

Table 31: Power & Ground

88E1543 Pin #	Pin Name	Pin Type	Description
53 57 63 79 86 104 109 113	DVDD	Power	1.0V Digital Supply
6 11 17 22 28 33 39 70 75 78 89 94 128	AVDD18	Power	1.8V Analog Supply.
1 14 25 38	AVDD33	Power	3.3V Analog Supply.
43 48	VDDC	Power	1.8V Supply ¹ .
98 110 117	VDDOL	Power	1.8V, 2.5V, or 3.3V I/O Supply ² . When V18_L is tied to VSS, VDDOL operates at 2.5V/3.3V. When V18_L is left floating, VDDOL operates at 1.8V.
83	VDDOM	Power	2.5V or 3.3V I/O Supply ³ . NOTE: For the 88E1543 device, VDDOM only supports 2.5V or 3.3V
56 64	VDDOR	Power	2.5V or 3.3V I/O Supply ⁴ .
67	VSS	Ground	Ground.

Table 31: Power & Ground (Continued)

88E1543 Pin #	Pin Name	Pin Type	Description
EPAD	VSS	Ground	Ground to device. The device is packaged in a 128-pin LQFP package with an EPAD (exposed die pad) on the bottom of the package. This EPAD must be soldered to VSS as it is the main VSS connection on the device. The location and dimensions of the EPAD can be found in Table 237 . See the Marvell® EPAD Layout Guidelines Application Note for EPAD layout details.

1. VDDC supplies XTAL_IN/OUT
2. VDDOL supplies digital I/O pins for RESETn, LED, CONFIG, and INTn.
3. VDDOM supplies digital I/O pins for MDC, MDIO, and TEST.
4. VDDOR supplies digital I/O pins for TDO, TDI, TMS, TCK, TRSTn, REF_CLKP/N, and CLK_SEL[1:0].

Table 32: No Connect

88E1543 Pin #	Pin Name	Pin Type	Description
47 59 60	NC	I	No Connect. Do not connect these pins to anything. These pins must be left unconnected.

Table 33: I/O State at Various Test or Reset Modes

Pin(s)	Loopback	Software Reset	Hardware Reset	Power Down
MDI[3:0]P/N	Active	Tri-state	Tri-state	Tri-state
S_OUTP/N	Active	Internally pulled up by terminations of 50 ohms	Internally pulled up by terminations of 50 ohms	Reg. 16.3 state 0 = Internally pulled up by terminations of 50 ohms 1 = Active
MDIO	Active	Active	Tri-state	Active
INTn	Active	Tri-state	Tri-state	Tri-state
TDO	Active	Active	Active	Active

1.1.3 88E1548 196-Pin TFBGA Package Pinout

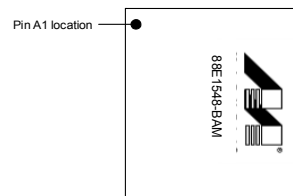
The 88E1548 device is a 10/100/1000BASE-T Gigabit Ethernet Transceiver.

Due to the large number of pins, the 196-pin TFBGA package is depicted graphically over two facing pages.

Figure 3: 88E1548 Device 196-Pin TFBGA Package (Top View)

	1	2	3	4	5	6	7	
A	P0_S_INN	P0_S_OUTN	P1_S_OUTP	P1_S_INP	TEST[1]	MDIO	VSS	A
B	P0_S_INP	P0_S_OUTP	P1_S_OUTN	P1_S_INN	TEST[0]	MDC	VSS	B
C	VSS	VSS	VSS	VSS	VSS	VSS	V12_EN	C
D	P0_LED[0]	INTn	VSS	AVDD18	AVDD18	VDDOM	VDDOM	D
E	P0_LED[2]	P0_LED[1]	RESETn	AVDD18	AVDD18	DVDD	DVDD	E
F	P1_LED[0]	P0_LED[3]	VDDOL	DVDD	VSS	VSS	VSS	F
G	P1_LED[2]	P1_LED[1]	VDDOL	DVDD	VSS	VSS	VSS	G
H	P1_LED[3]	P2_LED[0]	VDDOL	DVDD	VSS	VSS	VSS	H
J	P2_LED[1]	V18_L	VDDOL	DVDD	AVDD33	VSS	AVDD33	J
K	P2_LED[2]	P2_LED[3]	CONFIG[2]	VSS	AVDD33	VSS	AVDD33	K
L	P3_LED[0]	P3_LED[1]	CONFIG[3]	AVDD18	AVDD18	AVDD18	AVDD18	L
M	P3_LED[2]	P3_LED[3]	VSS	VSS	P0_MDIP[3]	P0_MDIN[3]	P1_MDIN[0]	M
N	CONFIG[0]	VSS	P0_MDIP[0]	P0_MDIP[1]	P0_MDIN[2]	P1_MDIP[3]	P1_MDIP[2]	N
P	CONFIG[1]	VSS	P0_MDIN[0]	P0_MDIN[1]	P0_MDIP[2]	P1_MDIN[3]	P1_MDIN[2]	P
	1	2	3	4	5	6	7	

Figure 4: 88E1548 Pin A1 Location



	8	9	10	11	12	13	14	
A	Q_OUTP	Q_INN	VSS	P2_S_INP	P2_S_OUTP	P3_S_OUTN	P3_S_INN	A
B	Q_OUTN	Q_INP	VSS	P2_S_INN	P2_S_OUTN	P3_S_OUTP	P3_S_INP	B
C	TSTPTF	VSS	VSS	VSS	VSS	VSS	VSS	C
D	AVDD18	AVDD18	AVDD18	AVDD18	TDO	REF_CLKP	REF_CLKN	D
E	DVDD	DVDD	AVDD18	AVDD18	TRSTn	V18_R	NC	E
F	VSS	VSS	VSS	DVDD	DVDD	VDDOR	NC	F
G	VSS	VSS	VSS	DVDD	TCK	TMS	TDI	G
H	VSS	VSS	VSS	VSS	VDDC	CLK_SEL[1]	CLK_SEL[0]	H
J	VSS	AVDD33	VSS	VSS	VSSC	XTAL_IN	XTAL_OUT	J
K	VSS	AVDD33	VSS	AVDD18	RSET	TSTPT	NC	K
L	AVDD18	AVDD18	AVDD18	AVDD18	VSS	HSDACN	HSDACP	L
M	P1_MDIP[0]	P2_MDIP[3]	P2_MDIN[3]	P3_MDIN[1]	P3_MDIP[1]	VSS	VSS	M
N	P1_MDIP[1]	P2_MDIN[0]	P2_MDIN[1]	P2_MDIN[2]	P3_MDIP[3]	P3_MDIP[2]	P3_MDIP[0]	N
P	P1_MDIN[1]	P2_MDIP[0]	P2_MDIP[1]	P2_MDIP[2]	P3_MDIN[3]	P3_MDIN[2]	P3_MDIN[0]	P
	8	9	10	11	12	13	14	

Table 34: Media Dependent Interface Port 0

88E1548 Pin #	Pin Name	Pin Type	Description
N3 P3	P0_MDIP[0] P0_MDIN[0]	I/O	<p>Media Dependent Interface[0].</p> <p>In 1000BASE-T mode in MDI configuration, MDIP/N[0] correspond to BI_DA±.</p> <p>In MDIX configuration, MDIP/N[0] correspond to BI_DB±.</p> <p>In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[0] are used for the transmit pair. In MDIX configuration, MDIP/N[0] are used for the receive pair.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100 ohm resistor between the MDIP/N[0] pins.</p>
N4 P4	P0_MDIP[1] P0_MDIN[1]	I/O	<p>Media Dependent Interface[1].</p> <p>In 1000BASE-T mode in MDI configuration, MDIP/N[1] correspond to BI_DB±. In MDIX configuration, MDIP/N[1] correspond to BI_DA±.</p> <p>In 100BASE-TX and 10BASE-T modes in MDI configuration, MDIP/N[1] are used for the receive pair. In MDIX configuration, MDIP/N[1] are used for the transmit pair.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100 ohm resistor between the MDIP/N[1] pins.</p>
P5 N5	P0_MDIP[2] P0_MDIN[2]	I/O	<p>Media Dependent Interface[2].</p> <p>In 1000BASE-T mode in MDI configuration, MDIP/N[2] correspond to BI_DC±. In MDIX configuration, MDIP/N[2] correspond to BI_DD±.</p> <p>In 100BASE-TX and 10BASE-T modes, MDIP/N[2] are not used.</p> <p>NOTE: Unused MDI pins must be left floating.</p> <p>The device contains an internal 100 ohm resistor between the MDIP/N[2] pins.</p>

Table 34: Media Dependent Interface Port 0 (Continued)

88E1548 Pin #	Pin Name	Pin Type	Description
M5 M6	P0_MDIP[3] P0_MDIN[3]	I/O	Media Dependent Interface[3]. In 1000BASE-T mode in MDI configuration, MDIP/N[3] correspond to BI_DD±. In MDIX configuration, MDIP/N[3] correspond to BI_DC±. In 100BASE-TX and 10BASE-T modes, MDIP/N[3] are not used. NOTE: Unused MDI pins must be left floating. The device contains an internal 100 ohm resistor between the MDIP/N[3] pins.

Table 35: Media Dependent Interface Port 1

88E1548 Pin #	Pin Name	Pin Type	Description
M8 M7	P1_MDIP[0] P1_MDIN[0]	I/O	Media Dependent Interface[0] for Port 1. Refer to P0_MDI[0]P/N.
N8 P8	P1_MDIP[1] P1_MDIN[1]	I/O	Media Dependent Interface[1] for Port 1. Refer to P0_MDI[1]P/N.
N7 P7	P1_MDIP[2] P1_MDIN[2]	I/O	Media Dependent Interface[2] for Port 1. Refer to P0_MDI[2]P/N.
N6 P6	P1_MDIP[3] P1_MDIN[3]	I/O	Media Dependent Interface[3] for Port 1. Refer to P0_MDI[3]P/N.

Table 36: Media Dependent Interface Port 2

88E1548 Pin #	Pin Name	Pin Type	Description
P9 N9	P2_MDIP[0] P2_MDIN[0]	I/O	Media Dependent Interface[0] for Port 2. Refer to P0_MDI[0]P/N.
P10 N10	P2_MDIP[1] P2_MDIN[1]	I/O	Media Dependent Interface[1] for Port 2. Refer to P0_MDI[1]P/N.
P11 N11	P2_MDIP[2] P2_MDIN[2]	I/O	Media Dependent Interface[2] for Port 2. Refer to P0_MDI[2]P/N.
M9 M10	P2_MDIP[3] P2_MDIN[3]	I/O	Media Dependent Interface[3] for Port 2. Refer to P0_MDI[3]P/N.

Table 37: Media Dependent Interface Port 3

88E1548 Pin #	Pin Name	Pin Type	Description
N14 P14	P3_MDIP[0] P3_MDIN[0]	I/O	Media Dependent Interface[0] for Port 3. Refer to P0_MDI[0]P/N.
M12 M11	P3_MDIP[1] P3_MDIN[1]	I/O	Media Dependent Interface[1] for Port 3. Refer to P0_MDI[1]P/N.
N13 P13	P3_MDIP[2] P3_MDIN[2]	I/O	Media Dependent Interface[2] for Port 3. Refer to P0_MDI[2]P/N.
N12 P12	P3_MDIP[3] P3_MDIN[3]	I/O	Media Dependent Interface[3] for Port 3. Refer to P0_MDI[3]P/N.

Table 38: SGMII Interface Port 0

88E1548 Pin #	Pin Name	Pin Type	Description
B1 A1	P0_S_INP P0_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
B2 A2	P0_S_OUTP P0_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

Table 39: SGMII Interface Port 1

88E1548 Pin #	Pin Name	Pin Type	Description
A4 B4	P1_S_INP P1_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
A3 B3	P1_S_OUTP P1_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

Table 40: SGMII Interface Port 2

88E1548 Pin #	Pin Name	Pin Type	Description
A11 B11	P2_S_INP P2_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
A12 B12	P2_S_OUTP P2_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

Table 41: SGMII Interface Port 3

88E1548 Pin #	Pin Name	Pin Type	Description
B14 A14	P3_S_INP P3_S_INN	I	SGMII Transmit Data. 1.25 GBaud input - Positive and Negative.
B13 A13	P3_S_OUTP P3_S_OUTN	O	SGMII Receive Data. 1.25 GBaud output - Positive and Negative. Output amplitude can be adjusted via register 26_1.2:0.

Table 42: QSGMII Interface

88E1548 Pin #	Pin Name	Pin Type	Description
B9 A9	Q_INP Q_INN	I	QSGMII Transmit Data. 5.0 GBaud input - Positive and Negative.
A8 B8	Q_OUTP Q_OUTN	O	QSGMII Receive Data. 5.0 GBaud output - Positive and Negative.

Table 43: Management Interface/Control

88E1548 Pin #	Pin Name	Pin Type	Description
B6	MDC	I	Management Clock pin. MDC is the management data clock reference for the serial management interface. A continuous clock stream is not expected. The maximum frequency supported is 12.5 MHz.
A6	MDIO	I/O	Management Data pin. MDIO is the management data. MDIO transfers management data in and out of the device synchronously to MDC. This pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm.
D2	INTn	OD	Interrupt pin. INTn functions as an active low interrupt output. The pull-up resistor used for the INTn should not be connected to voltage higher than VDDOL.

Table 44: LED/Configuration

88E1548 Pin #	Pin Name	Pin Type	Description
F2 E1 E2 D1	P0_LED[3] P0_LED[2] P0_LED[1] P0_LED[0]	O	Parallel LED Output Port 0 See Section 2.28, LED, on page 111 for details.
H1 G1 G2 F1	P1_LED[3] P1_LED[2] P1_LED[1] P1_LED[0]	O	Parallel LED Output Port 1 See Section 2.28, LED, on page 111 for details.
K2 K1 J1 H2	P2_LED[3] P2_LED[2] P2_LED[1] P2_LED[0]	O	Parallel LED Output Port 2 See Section 2.28, LED, on page 111 for details.
M2 M1 L2 L1	P3_LED[3] P3_LED[2] P3_LED[1] P3_LED[0]	O	Parallel LED Output Port 3 See Section 2.28, LED, on page 111 for details.
L3 K3 P1 N1	CONFIG[3] CONFIG[2] CONFIG[1] CONFIG[0]	I	Global hardware configuration. CONFIG[1] is used as PTP input data, and CONFIG[2] is used as PTP clock when the PTP_EN bit is set to 1. See Section 2.31.1, Hardware Configuration, on page 138 for details.
J2	V18_L	I	VDDOL voltage control. Tie to VSS = VDDOL operating at 2.5V/3.3V Floating = VDDOL operating at 1.8V
E13	V18_R	I	VDDOR voltage control. Tie to VSS = VDDOR operating at 2.5V/3.3V Floating = VDDOR operating at 1.8V
C7	V12_EN	I	VDDOM voltage control. Tie to VSS = VDDOM operating at 2.5V/3.3V Floating = VDDOM operating at 1.2V/1.8V

Table 45: JTAG

88E1548 Pin #	Pin Name	Pin Type	Description
G14	TDI	I, PU	Boundary scan test data input. TDI contains an internal 150 kohm pull-up resistor.
G13	TMS	I, PU	Boundary scan test mode select input. TMS contains an internal 150 kohm pull-up resistor.
G12	TCK	I, PU	Boundary scan test clock input. TCK contains an internal 150 kohm pull-up resistor.
E12	TRSTn	I, PU	Boundary scan test reset input. Active low. TRSTn contains an internal 150 kohm pull-up resistor. For normal operation, TRSTn should be pulled low with a 4.7 kohm pull-down resistor.
D12	TDO	O	Boundary scan test data output.

Table 46: Clock/Reset

88E1548 Pin #	Pin Name	Pin Type	Description
J13	XTAL_IN	I	25 MHz Clock Input 25 MHz \pm 50 ppm tolerance crystal reference or oscillator input. XTAL_IN has internal ac-coupling. XTAL_IN must be left floating when it is not used. Refer to the 'Oscillator Level Shifting' (MV-S301630-00) application note for details on how to convert a 2.5V/3.3V clock source to 1.8V clock.
J14	XTAL_OUT	O	25 MHz Crystal Output. 25 MHz \pm 50 ppm tolerance crystal reference. XTAL_OUT must be left floating when it is not used.
D13 D14	REF_CLKP REF_CLKN	I	25 MHz/125 MHz/156.25 MHz Reference Clock Input Positive and Negative \pm 50 ppm tolerance differential clock inputs. REFCLKP/N inputs are LVDS differential inputs with a 100 ohm differential internal termination resistor and internal ac-coupling. If the REF_CLKP/N inputs are not used, the REF_CLKP/N must be left floating. REF_CLKP/N also supports 125 MHz single-ended clock. In this case, the unused pin must be connected with 0.1uF capacitor to ground.

Table 46: Clock/Reset (Continued)

H13 H14	CLK_SEL[1] CLK_SEL[0]	I	<p>Reference Clock Selection CLK_SEL[1:0] 00 = Use 156.25 MHz REF_CLKP/N 01 = Use 125 MHz REF_CLKP/N 10 = Use 25 MHz REF_CLKP/N 11 = Use 25 MHz XTAL_IN/XTAL_OUT</p> <p>CLK_SEL[1:0] must be connected to VDDOR for configuration HIGH.</p>
E3	RESETn	I	<p>Hardware reset. XTAL_IN must be active for a minimum of 10 clock cycles before the rising edge of RESETn. RESETn must be in inactive state for normal operation.</p> <p>The RESETn pin can accept 2.5V LVCMOS signalling when the VDDOL pin is connected to 3.3V supply.</p> <p>1 = Normal operation 0 = Reset</p>

Table 47: Test

88E1548 Pin #	Pin Name	Pin Type	Description
L14 L13	HSDACP HSDACN	O	<p>AC Test Points (Positive and Negative), TX_TCLK, and Clock Cascade Differential Outputs.</p> <p>The HSDACP/N outputs are used for AC Test Points, TX_TCLK, and Clock Cascade Differential Outputs. These pins must be connected to a 50 ohm termination resistor to VSS. These pins can be left floating if not used for clock cascade, IEEE testing, and debug test points are not of importance.</p> <p>When used for clock cascade purpose, these pins are differential LVDS clock outputs that must be routed differentially to the REF_CLKP/N inputs of the downstream devices. A maximum of 5 downstream devices are allowed. The clock frequency follows the clock frequency used for the REF_CLKP/N or XTAL_IN/OUT inputs.</p> <p>These pins are also used to bring out a differential TX_TCLK for IEEE testing and AC Test Points for debug purposes. When used for IEEE testing or AC Test Points, the clock cascade must be disabled.</p>
K13	TSTPT	O	DC Test Point. The TSTPT pin should be left floating if not used.
C8	TSTPTF	O	DC test point. The TSTPTF pin should be left floating if not used.
A5 B5	TEST[1] TEST[0]	I, PD	Test Control. This pin should be left floating if not used.

Table 48: Reference

88E1548 Pin #	Pin Name	Pin Type	Description
K12	RSET	I	Resistor Reference External 5.0 kohm 1% resistor connected to ground.

Table 49: Power & Ground

88E1548 Pin #	Pin Name	Pin Type	Description
E6 E7 E8 E9 F4 F11 F12 G4 G11 H4 J4	DVDD	Power	1.0V Digital Supply
D4 D5 D8 D9 D10 D11 E4 E5 E10 E11 L4 L5 L7 L6 L9 L8 L10 L11 K11	AVDD18	Power	1.8V Analog Supply.
J5 K5 J7 K7 J9 K9	AVDD33	Power	3.3V Analog Supply.
H12	VDDC	Power	1.8V Supply ¹ .
D6 D7	VDDOM	Power	1.2V, 1.8V, 2.5V, or 3.3V I/O Supply ² .
F13	VDDOR	Power	1.8V, 2.5V, or 3.3V I/O Supply ³ .

Table 49: Power & Ground (Continued)

88E1548 Pin #	Pin Name	Pin Type	Description
F3 G3 H3 J3	VDDOL	Power	1.8V, 2.5V, or 3.3V I/O Supply ⁴ .
A7 A10 B7 B10 C1 C2 C3 C4 C5 C6 C9 C10 C11 C12 C13 C14 D3 F5 F6 F7 F8 F9 F10 G5 G6 G7 G8 G9 G10 H5 H6 H7 H8 H9 H10 H11 J10 J11 J6 J8 K4 K6 K8 K10 L12 M3 M4	VSS	Ground	Ground.

Table 49: Power & Ground (Continued)

88E1548 Pin #	Pin Name	Pin Type	Description
M13 M14 N2 P2	VSS (cont.)	Ground	Ground.
J12	VSSC	Ground	Ground.

1. VDDC supplies XTAL_IN/OUT
2. VDDOM supplies digital I/O pins for MDC, MDIO, and TEST.
3. VDDOR supplies digital I/O pins for TDO, TDI, TMS, TCK, TRSTn, REF_CLKP/N, and CLK_SEL[1:0].
4. VDDOL supplies digital I/O pins for RESETn, LED, CONFIG, and INTn.

Table 50: No Connect

88E1548 Pin #	Pin Name	Pin Type	Description
E14	NC	O	No Connect. Do not connect these pins to anything. These pins must be left unconnected.
F14	NC	O	No Connect. Do not connect these pins to anything. These pins must be left unconnected.
K14	NC	I	No Connect. Do not connect these pins to anything. These pins must be left unconnected.

Table 51: I/O State at Various Test or Reset Modes

Pin(s)	Loopback	Software Reset	Hardware Reset	Power Down
MDI[3:0]P/N	Active	Tri-state	Tri-state	Tri-state
S_OUTP/N	Active	Internally pulled up by terminations of 50 ohms	Internally pulled up by terminations of 50 ohms	Reg. 16.3 state 0 = Internally pulled up by terminations of 50 ohms 1 = Active
Q_OUTP/N	Active	Internally pulled up by terminations of 50 ohms	Internally pulled up by terminations of 50 ohms	Reg. 16.3 state 0 = Internally pulled up by terminations of 50 ohms 1 = Active
MDIO	Active	Active	Tri-state	Active
INTn	Active	Tri-state	Tri-state	Tri-state
TDO	Active	Active	Active	Active

1.2 Pin Assignment List

1.2.1 88E1545 128-Pin LQFP Package Pin Assignment List

Table 52: 88E1545 128-Pin LQFP List—Alphabetical by Signal Name

Pin Name	Pin Number	Pin Name	Pin Number
AVDD18	6	DVDD	53
AVDD18	11	DVDD	57
AVDD18	17	DVDD	63
AVDD18	22	DVDD	89
AVDD18	28	DVDD	95
AVDD18	33	DVDD	104
AVDD18	39	DVDD	109
AVDD18	70	DVDD	113
AVDD18	75	HSDACN	44
AVDD18	83	HSDACP	45
AVDD18	84	INTn	99
AVDD18	96	MDC	91
AVDD18	128	MDIO	90
AVDD33	1	NC	47
AVDD33	14	NC	59
AVDD33	25	NC	60
AVDD33	38	NC	68
CLK_SEL[0]	51	NC	69
CLK_SEL[1]	52	NC	71
CONFIG[0]	122	NC	72
CONFIG[1]	123	NC	73
CONFIG[2]	124	NC	74
CONFIG[3]	125	NC	76

Pin Name	Pin Number
NC	77
P0_LED[0]	100
P0_LED[1]	101
P0_LED[2]	102
P0_LED[3]	103
P0_MDIN[0]	127
P0_MDIN[1]	3
P0_MDIN[2]	5
P0_MDIN[3]	8
P0_MDIP[0]	126
P0_MDIP[1]	2
P0_MDIP[2]	4
P0_MDIP[3]	7
P1_LED[0]	105
P1_LED[1]	106
P1_LED[2]	107
P1_LED[3]	108
P1_MDIN[0]	18
P1_MDIN[1]	15
P1_MDIN[2]	12
P1_MDIN[3]	9
P1_MDIP[0]	19
P1_MDIP[1]	16
P1_MDIP[2]	13
P1_MDIP[3]	10
P2_LED[0]	111

Pin Name	Pin Number
P2_LED[1]	112
P2_LED[2]	115
P2_LED[3]	116
P2_MDIN[0]	21
P2_MDIN[1]	24
P2_MDIN[2]	27
P2_MDIN[3]	30
P2_MDIP[0]	20
P2_MDIP[1]	23
P2_MDIP[2]	26
P2_MDIP[3]	29
P3_LED[0]	118
P3_LED[1]	119
P3_LED[2]	120
P3_LED[3]	121
P3_MDIN[0]	40
P3_MDIN[1]	36
P3_MDIN[2]	34
P3_MDIN[3]	31
P3_MDIP[0]	41
P3_MDIP[1]	37
P3_MDIP[2]	35
P3_MDIP[3]	32
Q_INN	82
Q_INP	80
Q_OUTN	87

Pin Name	Pin Number
Q_OUTP	85
REF_CLKN	65
REF_CLKP	66
RESETn	97
RSET	42
TCK	54
TDI	58
TDO	61
TEST[0]	94
TEST[1]	93
TMS	55
TRSTn	62
TSTPT	46
V18_L	114
VDDC	43
VDDC	48

Pin Name	Pin Number
VDDOL	98
VDDOL	110
VDDOL	117
VDDOM	92
VDDOR	56
VDDOR	64
VSS	67
VSS	78
VSS	79
VSS	81
VSS	86
VSS	88
VSS	EPAD
XTAL_IN	49
XTAL_OUT	50

1.2.2 88E1543 128-Pin LQFP Package Pin Assignment List

Table 53: 88E1543 128-Pin LQFP List—Alphabetical by Signal Name

Pin Name	Pin Number	Pin Name	Pin Number
AVDD18	6	DVDD	79
AVDD18	11	DVDD	86
AVDD18	17	DVDD	104
AVDD18	22	DVDD	109
AVDD18	28	DVDD	113
AVDD18	33	HSDACN	44
AVDD18	39	HSDACP	45
AVDD18	70	INTn	99
AVDD18	75	MDC	82
AVDD18	78	MDIO	81
AVDD18	89	NC	47
AVDD18	94	NC	59
AVDD18	128	NC	60
AVDD33	1	P0_LED[0]	100
AVDD33	14	P0_LED[1]	101
AVDD33	25	P0_LED[2]	102
AVDD33	38	P0_LED[3]	103
CLK_SEL[0]	51	P0_MDIN[0]	127
CLK_SEL[1]	52	P0_MDIN[1]	3
CONFIG[0]	122	P0_MDIN[2]	5
CONFIG[1]	123	P0_MDIN[3]	8
CONFIG[2]	124	P0_MDIP[0]	126
CONFIG[3]	125	P0_MDIP[1]	2
DVDD	53	P0_MDIP[2]	4
DVDD	57	P0_MDIP[3]	7
DVDD	63	P0_S_INN	95
		P0_S_INP	96

Pin Name	Pin Number
P0_S_OUTN	92
P0_S_OUTP	93
P1_LED[0]	105
P1_LED[1]	106
P1_LED[2]	107
P1_LED[3]	108
P1_MDIN[0]	18
P1_MDIN[1]	15
P1_MDIN[2]	12
P1_MDIN[3]	9
P1_MDIP[0]	19
P1_MDIP[1]	16
P1_MDIP[2]	13
P1_MDIP[3]	10
P1_S_INN	88
P1_S_INP	87
P1_S_OUTN	91
P1_S_OUTP	90
P2_LED[0]	111
P2_LED[1]	112
P2_LED[2]	115
P2_LED[3]	116
P2_MDIN[0]	21
P2_MDIN[1]	24
P2_MDIN[2]	27
P2_MDIN[3]	30
P2_MDIP[0]	20
P2_MDIP[1]	23

Pin Name	Pin Number
P2_MDIP[2]	26
P2_MDIP[3]	29
P2_S_INN	76
P2_S_INP	77
P2_S_OUTN	73
P2_S_OUTP	74
P3_LED[0]	118
P3_LED[1]	119
P3_LED[2]	120
P3_LED[3]	121
P3_MDIN[0]	40
P3_MDIN[1]	36
P3_MDIN[2]	34
P3_MDIN[3]	31
P3_MDIP[0]	41
P3_MDIP[1]	37
P3_MDIP[2]	35
P3_MDIP[3]	32
P3_S_INN	69
P3_S_INP	68
P3_S_OUTN	72
P3_S_OUTP	71
REFCLKN	65
REFCLKP	66
RESETn	97
RSET	42
TCK	54
TDI	58

Pin Name	Pin Number
TDO	61
TEST[0]	85
TEST[1]	84
TMS	55
TRSTn	62
TSTPT	46
TSTPTF	80
V18_L	114
VDDC	43
VDDC	48

Pin Name	Pin Number
VDDOL	98
VDDOL	110
VDDOL	117
VDDOM	83
VDDOR	56
VDDOR	64
VSS	67
VSS	EPAD
XTAL_IN	49
XTAL_OUT	50

1.2.3 88E1548 196-Pin TFBGA Package Pin Assignment List

Table 54: 88E1548 196-Pin TFBGA List—Alphabetical by Signal Name

Pin Name	Pin Number	Pin Name	Pin Number
AVDD33	J5	CLK_SEL[1]	H13
AVDD33	K5	CONFIG[0]	N1
AVDD33	J7	CONFIG[1]	P1
AVDD33	K7	CONFIG[2]	K3
AVDD33	J9	CONFIG[3]	L3
AVDD33	K9	DVDD	E6
AVDD18	D4	DVDD	E7
AVDD18	D5	DVDD	E8
AVDD18	D8	DVDD	E9
AVDD18	D9	DVDD	F4
AVDD18	D10	DVDD	F11
AVDD18	D11	DVDD	F12
AVDD18	E4	DVDD	G4
AVDD18	E5	DVDD	G11
AVDD18	E10	DVDD	H4
AVDD18	E11	DVDD	J4
AVDD18	K11	HSDACN	L13
AVDD18	L4	HSDACP	L14
AVDD18	L5	INTn	D2
AVDD18	L6	MDC	B6
AVDD18	L7	MDIO	A6
AVDD18	L8	P0_LED[0]	D1
AVDD18	L9	P0_LED[1]	E2
AVDD18	L10	P0_LED[2]	E1
AVDD18	L11	P0_LED[3]	F2
CLK_SEL[0]	H14	P0_MDIN[0]	P3
		P0_MDIN[1]	P4

Pin Name	Pin Number
P0_MDIN[2]	N5
P0_MDIN[3]	M6
P0_MDIP[0]	N3
P0_MDIP[1]	N4
P0_MDIP[2]	P5
P0_MDIP[3]	M5
P0_S_INN	A1
P0_S_INP	B1
P0_S_OUTN	A2
P0_S_OUTP	B2
P1_LED[0]	F1
P1_LED[1]	G2
P1_LED[2]	G1
P1_LED[3]	H1
P1_MDIN[0]	M7
P1_MDIN[1]	P8
P1_MDIN[2]	P7
P1_MDIN[3]	P6
P1_MDIP[0]	M8
P1_MDIP[1]	N8
P1_MDIP[2]	N7
P1_MDIP[3]	N6
P1_S_INN	B4
P1_S_INP	A4
P1_S_OUTN	B3
P1_S_OUTP	A3
P2_LED[0]	H2
P2_LED[1]	J1

Pin Name	Pin Number
P2_LED[2]	K1
P2_LED[3]	K2
P2_MDIN[0]	N9
P2_MDIN[1]	N10
P2_MDIN[2]	N11
P2_MDIN[3]	M10
P2_MDIP[0]	P9
P2_MDIP[1]	P10
P2_MDIP[2]	P11
P2_MDIP[3]	M9
P2_S_INN	B11
P2_S_INP	A11
P2_S_OUTN	B12
P2_S_OUTP	A12
P3_LED[0]	L1
P3_LED[1]	L2
P3_LED[2]	M1
P3_LED[3]	M2
P3_MDIN[0]	P14
P3_MDIN[1]	M11
P3_MDIN[2]	P13
P3_MDIN[3]	P12
P3_MDIP[0]	N14
P3_MDIP[1]	M12
P3_MDIP[2]	N13
P3_MDIP[3]	N12
P3_S_INN	A14
P3_S_INP	B14

Pin Name	Pin Number
P3_S_OUTN	A13
P3_S_OUTP	B13
Q_INN	A9
Q_INP	B9
Q_OUTN	B8
Q_OUTP	A8
NC	E14
NC	F14
REF_CLKN	D14
REF_CLKP	D13
RESET	E3
RSET	K12
NC	K14
TCK	G12
TDI	G14
TDO	D12
TEST[0]	B5
TEST[1]	A5
TMS	G13
TRST	E12
TSTPT	K13
TSTPTF	C8
V12_EN	C7
V18_L	J2
V18_R	E13
VDDC	H12
VDDOM	D6
VDDOM	D7

Pin Name	Pin Number
VDDOL	F3
VDDOL	G3
VDDOL	H3
VDDOL	J3
VDDOR	F13
VSS	A7
VSS	A10
VSS	B7
VSS	B10
VSS	C1
VSS	C2
VSS	C3
VSS	C4
VSS	C5
VSS	C6
VSS	C9
VSS	C10
VSS	C11
VSS	C12
VSS	C13
VSS	C14
VSS	D3
VSS	F5
VSS	F6
VSS	F7
VSS	F8
VSS	F9
VSS	F10

Pin Name	Pin Number
VSS	G5
VSS	G6
VSS	G7
VSS	G8
VSS	G9
VSS	G10
VSS	H5
VSS	H6
VSS	H7
VSS	H8
VSS	H9
VSS	H10
VSS	H11
VSS	J6
VSS	J8
VSS	J10
VSS	J11
VSS	K4
VSS	K6
VSS	K8
VSS	K10
VSS	L12
VSS	M3
VSS	M4
VSS	M13
VSS	M14
VSS	N2
VSS	P2

Pin Name	Pin Number
VSSC	J12
XTAL_IN	J13
XTAL_OUT	J14

2

PHY Functional Specifications

The device is a 4-port 10/100/1000 Gigabit Ethernet transceiver. Each port of the device may operate completely independent of each other, but they are identical in performance and functionality. The functional description and electrical specifications for the device are applicable to each port. For simplicity, the functional description in this document describes the operation of a single transceiver.

Port numbers have been omitted from many diagrams and descriptive text indicating that the functionality applies to all ports. In this document, the pins for each port are specified by the port number, pin name, and signal number, respectively.

For example, LED 1 pin for Port 0 shown below:

P0_LED[1]

However, the MDIO pin supported by the device are global to the chip and do not have port numbers. Figure 5 shows the functional block diagram of the device.

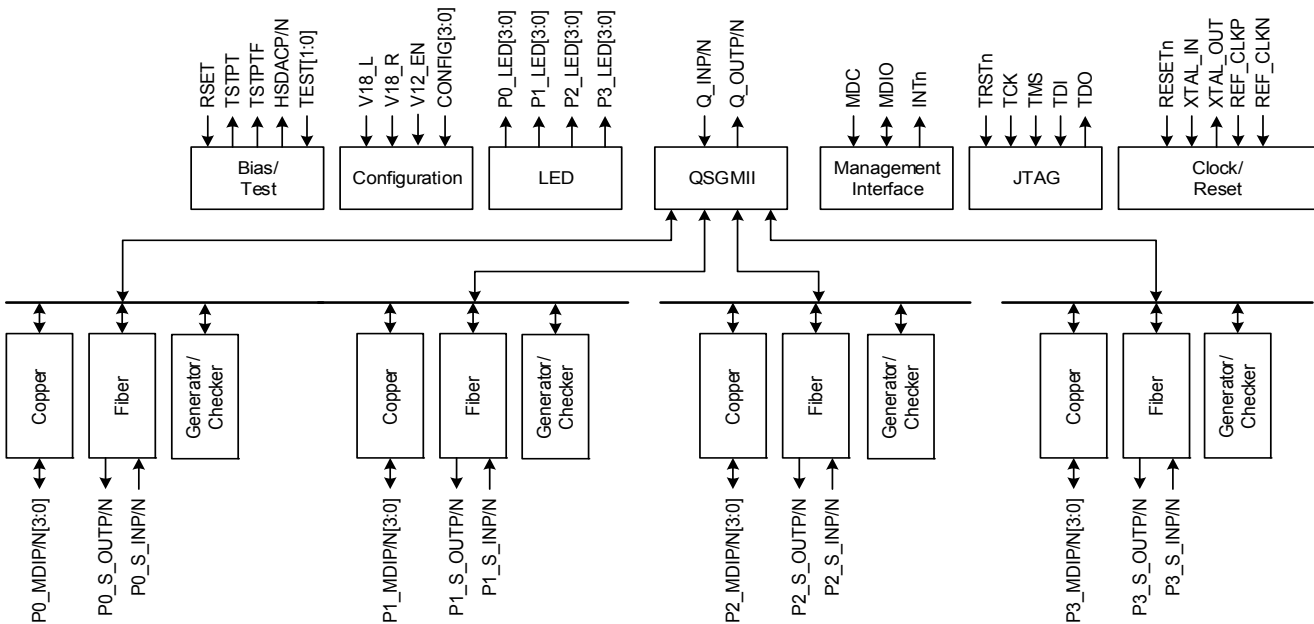


Note

For purpose of discussion, the word “device” refers to all devices.

Refer to Table 1 for a list of features supported by each device.

Figure 5: Device Functional Block Diagram



2.1 Modes of Operation and Major Interfaces

The device has three separate major electrical interfaces:

- MDI Interface to Copper Cable
- SERDES/SGMII Interface
- QSGMII Interface

The MDI Interface is always a media interface. The SGMII and QSGMII Interfaces can be on the system interface side, or on the media interface side. The QSGMII interface can be used as a Media interface only in conjunction with the QSGMII Crossover Muxing and Loopback - [Section 2.5.5, QSGMII Crossover Muxing and Loopback, on page 77](#) for details. (The system interface is also known as MAC interface. It is typically the connection between the PHY and the MAC or the system ASIC.) For example:

Figure 6: SGMII System to Copper Interface Example

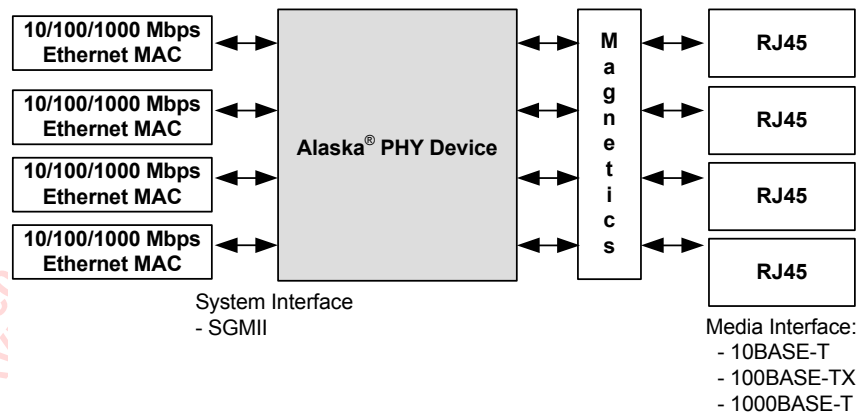


Figure 7: QSGMII System to SGMII/Fiber Media Interface Example

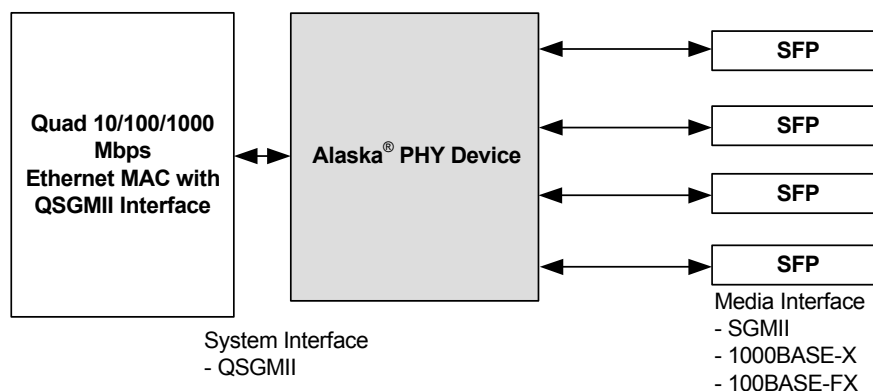
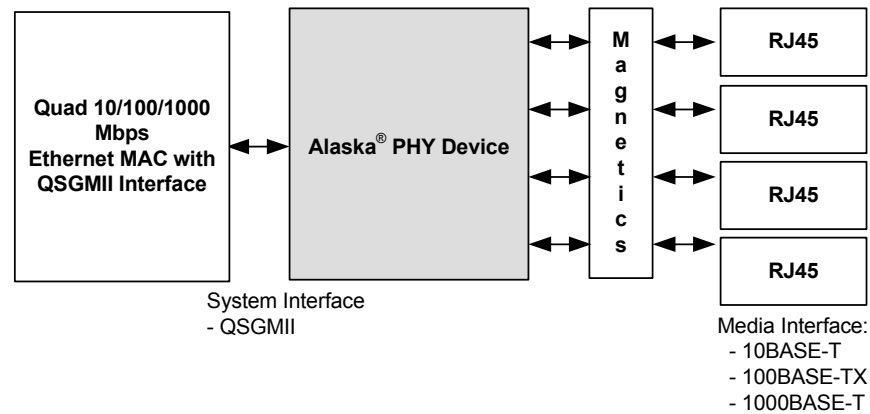


Figure 8: QSGMII System to Copper Interface Example



As can be seen from these examples, SGMII interface can act either as a system interface or a Media interface. To keep the notation simple, SGMII (System) will be used to indicate SGMII system interface and SGMII (Media) will be used to indicate SGMII media interface. It is also important to note the differences in the logical operation of the two modes. The major difference is due to the SGMII Auto-Negotiation function:

- When used as a system interface, the device implements the PHY SGMII Auto-Negotiation status (link, duplex, etc.) advertisements as specified in the Cisco SGMII specification.
- When used as a Media interface, the device implements the MAC SGMII Auto-Negotiation function, which monitors PHY status advertisements.

For details of how SGMII Auto-Negotiation operates, see [Section 2.11.3](#) as well as the Cisco SGMII specification.

The device supports 8 modes of operation as shown in [Table 55](#). For each mode of operation two or three of three interfaces as described in section 2.1, 2.2, and 2.3 are powered up. On hardware reset, all four ports are configured to operate in the same mode. However, it is possible for each port to operate in a different mode than another by programming register 20_18.2:0.

The behavior of the 1.25 GHz SERDES interface is selected by setting the MODE[2:0] register in 20_18.2:0. The SERDES can operate in 100BASE-FX, 1000BASE-X, SGMII (System), and SGMII (Media).

The behavior of the QSGMII is also selected by setting the MODE[2:0] register in 20_18.2:0. The QSGMII can operate in QSGMII (System) or QSGMII (Media).

Table 55: MODE[2:0] Select

MODE[2:0] Register 20_18.2:0	Description
000	QSGMII (System) to Copper
001	SGMII (System) to Copper
010	QSGMII (System) to 1000BASE-X
011	QSGMII (System) to 100BASE-FX or QSGMII (System) to Auto Media Detect (Copper/100BASE-FX)
100	QSGMII (System) to SGMII (Media)
101	SGMII (System) to QSGMII (Media)
110	QSGMII (System) to Auto Media Detect Copper/SGMII
111	QSGMII (System) to Auto Media Detect Copper/1000BASE-X

The device can also support SGMII to Auto-Media mode of operation as described in [Figure 22](#). In that case, one port is configured for SGMII (System) to QSGMII (Media) mode, and the other port is configured to QSGMII (System) to Auto-Media mode.

When the mode is set for auto media detect, register 20_18.5:4 specifies which media is the preferred media. See [Section 2.6 "Fiber/Copper Auto-Selection" on page 80](#) for more details.

When link is up, two of the three interfaces pass packets back and forth. The unused interface is powered down. The unused transmitter can be configured to snoop on the transmit or receive paths. Register 20_18.11:10 enables the snooping and selects which path to snoop on. See [2.7 "Snooping" on page 82](#) for more details.

There is no need to power down the unused interface via registers 0_0.11, 0_1.11, and 0_4.11. The unused interface will automatically power down when not needed.

2.2 Copper Media Interface

The copper interface consists of the MDIP/N[3:0] pins that connect to the physical media for 1000BASE-T, 100BASE-TX, and 10BASE-T modes of operation.

The device integrates MDI interface termination resistors. The IEEE 802.3 specification requires that both sides of a link have termination resistors to prevent reflections. Traditionally, these resistors and additional capacitors are placed on the board between a PHY device and the magnetics. The resistors have to be very accurate to meet the strict IEEE return loss requirements. Typically, $\pm 1\%$ accuracy resistors are used on the board. These additional components between the PHY and the magnetics complicate board layout. Integrating the resistors has many advantages including component cost savings, better ICT yield, board reliability improvements, board area savings, improved layout, and signal integrity improvements. See the Application Note: "Benefits of Integrating Termination Resistors for Ethernet Applications" for details.

2.2.1 Transmit Side Network Interface

2.2.1.1 Multi-mode TX Digital to Analog Converter

The device incorporates a multi-mode transmit DAC to generate filtered 4D PAM 5, MLT3, or Manchester coded symbols. The transmit DAC performs signal wave shaping to reduce EMI. The transmit DAC is designed for very low parasitic loading capacitances to improve the return loss requirement, which allows the use of low cost transformers.

2.2.1.2 Slew Rate Control and Waveshaping

In 1000BASE-T mode, partial response filtering and slew rate control is used to minimize high frequency EMI. In 100BASE-TX mode, slew rate control is used to minimize high frequency EMI. In 10BASE-T mode, the output waveform is pre-equalized via a digital filter.

2.2.2 Encoder

2.2.2.1 1000BASE-T

In 1000BASE-T mode, the transmit data bytes are scrambled to 9-bit symbols and encoded into 4D PAM5 symbols. Upon initialization, the initial scrambling seed is determined by the PHY address. This prevents multiple device from outputting the same sequence during idle, which helps to reduce EMI.

2.2.2.2 100BASE-TX

In 100BASE-TX mode, the transmit data stream is 4B/5B encoded, serialized, and scrambled.

2.2.2.3 10BASE-T

In 10BASE-T mode, the transmit data is serialized and converted to Manchester encoding.

2.2.3 Receive Side Network Interface

2.2.3.1 Analog to Digital Converter

The device incorporates an advanced high speed ADC on each receive channel with greater resolution than the ADC used in the reference model of the IEEE 802.3ab standard committee. Higher resolution ADC results in better SNR, and therefore, lower error rates. Patented architectures and design techniques result in high differential and integral linearity, high power supply noise rejection, and low metastability error rate. The ADC samples the input signal at 125 MHz.

2.2.3.2 Active Hybrid

The device employs a sophisticated on-chip hybrid to substantially reduce the near-end echo, which is the super-imposed transmit signal on the receive signal. The hybrid minimizes the echo to reduce the precision requirement of the digital echo canceller. The on-chip hybrid allows both the transmitter and receiver to use the same transformer for coupling to the twisted pair cable, which reduces the cost of the overall system.

2.2.3.3 Echo Canceller

Residual echo not removed by the hybrid and echo due to patch cord impedance mismatch, patch panel discontinuity, and variations in cable impedance along the twisted pair cable result in drastic SNR degradation on the receive signal. The device employs a fully developed digital echo canceller to adjust for echo impairments from more than 100 meters of cable. The echo canceller is fully adaptive to compensate for the time varying nature of channel conditions.

2.2.3.4 NEXT Canceller

The 1000BASE-T physical layer uses all 4 pairs of wires to transmit data to reduce the baud rate requirement to only 125 MHz. This results in significant high frequency crosstalk between adjacent pairs of cable in the same bundle. The device employs 3 parallel NEXT cancellers on each receive channel to cancel any high frequency crosstalk induced by the adjacent 3 transmitters. A fully adaptive digital filter is used to compensate for the time varying nature of channel conditions.

2.2.3.5 Baseline Wander Canceller

Baseline wander is more problematic in the 1000BASE-T environment than in the traditional 100BASE-TX environment due to the DC baseline shift in both the transmit and receive signals. The device employs an advanced baseline wander cancellation circuit to automatically compensate for this DC shift. It minimizes the effect of DC baseline shift on the overall error rate.

2.2.3.6 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from ADC output and uses a combination of feedforward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise (SNR) ratio.

2.2.3.7 Digital Phase Lock Loop

In 1000BASE-T mode, the slave transmitter must use the exact receive clock frequency it sees on the receive signal. Any slight long-term frequency phase jitter (frequency drift) on the receive signal must be tracked and duplicated by the slave transmitter; otherwise, the receivers of both the slave and master physical layer devices have difficulty canceling the echo and NEXT components. In the device, an advanced DPLL is used to recover and track the clock timing information from the receive signal. This DPLL has very low long-term phase jitter of its own, thereby maximizing the achievable SNR.

2.2.3.8 Link Monitor

The link monitor is responsible for determining if link is established with a link partner. In 10BASE-T mode, link monitor function is performed by detecting the presence of valid link pulses (NLPs) on the MDIP/N pins.

In 100BASE-TX and 1000BASE-T modes, link is established by scrambled idles.

If Force Link Good register 16_0.10 is set high, the link is forced to be good and the link monitor is bypassed for 100BASE-TX and 10BASE-T modes. In the 1000BASE-T mode, register 16_0.10 has no effect.

2.2.3.9 Signal Detection

In 1000BASE-T mode, signal detection is based on whether the local receiver has acquired lock to the incoming data stream.

In 100BASE-TX mode, the signal detection function is based on the receive signal energy detected on the MDIP/N pins that is continuously qualified by the squelch detect circuit, and the local receiver acquiring lock.

2.2.4 Decoder

2.2.4.1 1000BASE-T

In 1000BASE-T mode, the receive idle stream is analyzed so that the scrambler seed, the skew among the 4 pairs, the pair swap order, and the polarity of the pairs can be accounted for. Once calibrated, the 4D PAM 5 symbols are converted to 9-bit symbols that are then descrambled into 8-bit data values. If the descrambler loses lock for any reason, the link is brought down and calibration is restarted after the completion of Auto-Negotiation.

2.2.4.2 100BASE-TX

In 100BASE-TX mode, the receive data stream is recovered and converted to NRZ. The NRZ stream is descrambled and aligned to the symbol boundaries. The aligned data is then parallelized and 5B/4B decoded. The receiver does not attempt to decode the data stream unless the scrambler is locked. The descrambler “locks” to the *scrambler* state after detecting a sufficient number of consecutive idle code-groups. Once locked, the descrambler continuously monitors the data stream to make sure that it has not lost synchronization. The descrambler is always forced into the *unlocked* state when a link failure condition is detected, or when insufficient idle symbols are detected.

2.2.4.3 10BASE-T

In 10BASE-T mode, the recovered 10BASE-T signal is decoded from Manchester to NRZ, and then aligned. The alignment is necessary to insure that the start of frame delimiter (SFD) is aligned to the nibble boundary.

2.3 1.25 GHz SERDES Interface

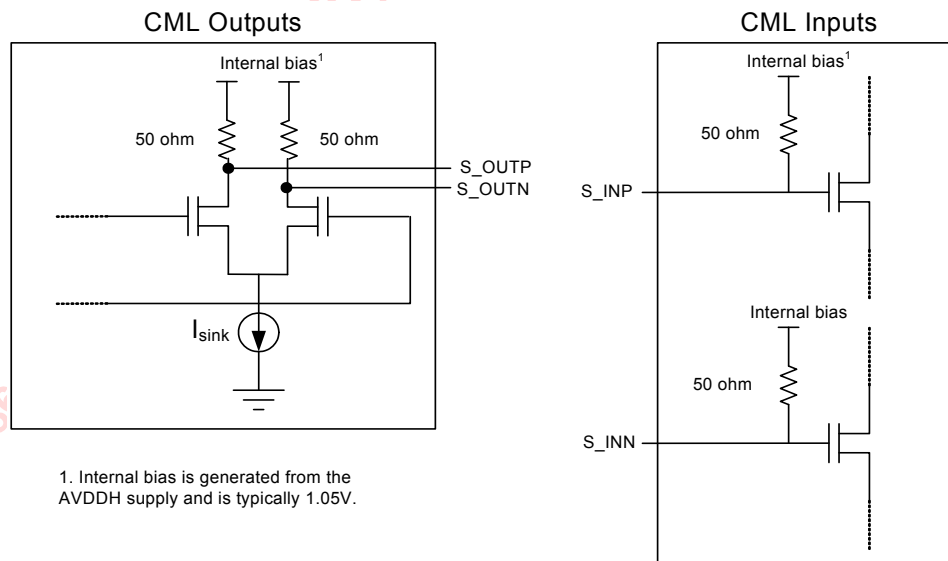
The 1.25 GHz SERDES Interface can be configured as an SGMII to be hooked up to a MAC or as a 100BASE-FX/1000BASE-X/SGMII to be hooked up to the media.

2.3.1 Electrical Interface

The input and output buffers are internally terminated to 50 ohm impedance. The output swing can be adjusted by programming register 26_1.2:0.

The input and output buffers of the 1.25 GHz SERDES interface are internally terminated by 50 ohm impedance. No external terminations are required. The 1.25 GHz SERDES I/Os are Current Mode Logic (CML) buffers. CML I/Os can be used to connect to other components with PECL or LVDS I/Os. See the "Reference Design Schematics" and "Fiber Interface" application note for details.

Figure 9: CML I/Os



2.3.2 SGMII Speed and Link

When the SGMII MAC interface is used, the media interface can be copper or QSGMII. The operational speed of the SGMII MAC interface is determined according to Table 56 media interface status and/or loopback mode.

Table 56: SGMII (MAC Interface) Operational Speed

Link Status or Media Interface Status	SGMII (MAC Interface) Speed
No Link	Determined by speed setting of 21_2.2:0
MAC Loopback	Determined by speed setting of 21_2.2:0
1000BASE-T or QSGMII (Media) at 1000 Mbps	1000 Mbps
100BASE-TX or QSGMII (Media) at 100 Mbps	100 Mbps
10BASE-T or QSGMII (Media) at 10 Mbps	10 Mbps

Two registers are available to determine whether the SGMII achieved link and sync. Register 17_1.5 indicates that the SERDES locked onto the incoming KDKDKD... sequence. Register 17_1.10 indicates whether 1000BASE-X link is established on the SERDES. If SGMII Auto-Negotiation is disabled, register 17_1.10 has the same meaning as register 17_1.5. If SGMII Auto-Negotiation is enabled, then register 17_1.10 indicates whether SGMII Auto-Negotiation successfully established link.

2.3.3 SGMII TRR Blocking

When the SGMII receives a packet with odd number of bytes, a single symbol of carrier extension will be passed on and transmitted onto 1000BASE-T. This carrier extension may cause problems with full-duplex MACs that incorrectly handle the carrier extension symbols. When register 16_1.13 is set to 1, all carrier extend and carrier extend with error symbols received by the SGMII will be converted to idle symbols when operating in full-duplex. Carrier extend and carrier extend with error symbols will not be blocked when operating in half-duplex, or if register 16_1.13 is set to 0. Note that symbol errors will continue to be propagated regardless of the setting of register 16_1.13.

This function is on by default as the SGMII rev 1.8 standard requires this function to be implemented.

2.3.4 False SERDES Link Up Prevention

The SERDES interface can operate in 1000BASE-X mode and in 100BASE-FX mode where an unconnected optical receiver will send full swing noise into the PHY. Sometimes this random noise will look like a real signal and falsely cause the 1000BASE-X or 100BASE-FX PCS to link up.

A noise filtering state machine can be enabled to reduce the probability of false link up. When the state machine is enabled it will cause a small delay in link up time.

Table 57: Fiber Noise Filtering

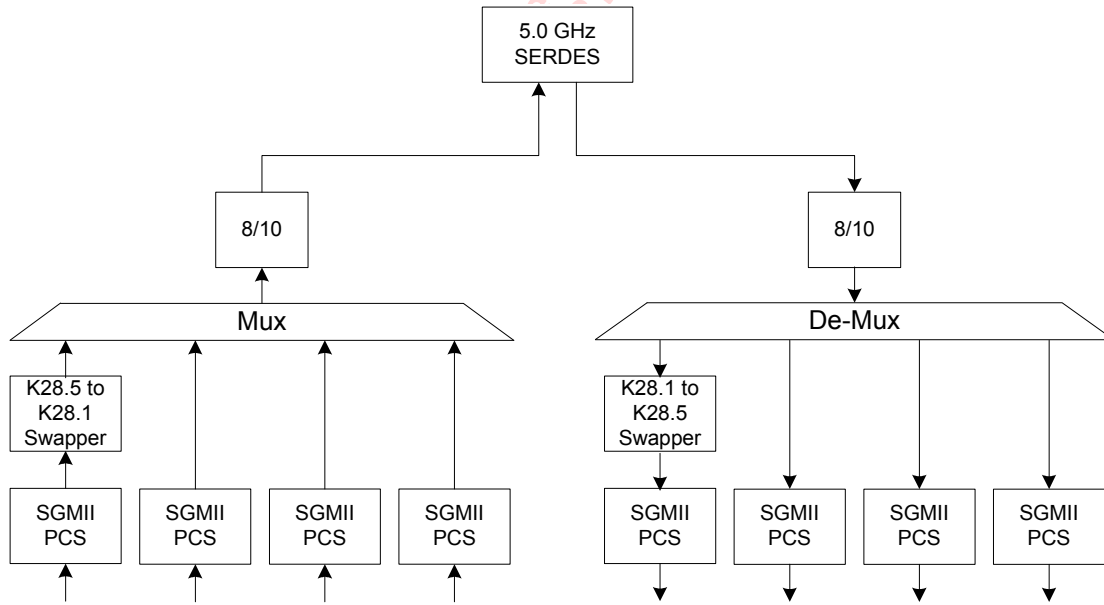
Register	Function	Setting	Mode	HW Rst	SW Rst
26_1.14	1000BASE-X Noise Filtering	1 = Enable 0 = Disable	R/W	0	Retain
26_1.13	100BASE-FX Noise Filtering	1 = Enable 0 = Disable	R/W	0	Retain

2.4 QSGMII 5.0 GHz SERDES Interface

The 5.0 GHz SERDES Interface is used as the QSGMII.

The QSGMII aggregates and de-aggregates four SGMII ports via a 5.0 GHz SERDES.

Figure 10: QSGMII



2.4.1 Electrical Interface

The input and output buffers are internally terminated to 50 ohm impedance.

The input and output buffers of the 5.0 GHz SERDES interface are internally terminated by 50 ohm impedance. No external terminations are required. The 5.0 GHz SERDES I/Os are Current Mode Logic (CML) buffers. CML I/Os can be used to connect to other components with PECL or LVDS I/Os. See the "Reference Design Schematics" and "Fiber Interface" application note for details.

The polarity of the 5.0 GHz inputs and outputs can be inverted.

Register 26_4.13 inverts the input; 0 = Invert, 1 = Normal.

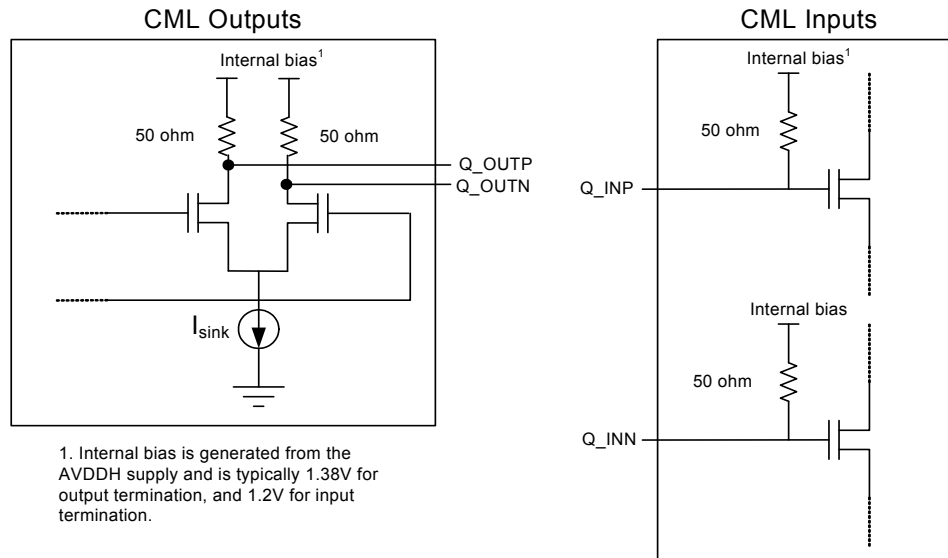
Register 26_4.12 inverts the outputs; 0 = Invert, 1 = Normal.



Note

In order to meet the QSGMII transmit and receive jitter specifications, a 125 MHz or 156.25 MHz reference clock input is required. The 25 MHz reference clock input option should not be used for applications using the QSGMII interface.

Figure 11: CML I/Os



2.4.2 QSGMII Register Addressing

QSGMII registers are accessed by setting Register 22.7:0 to 0x04. There are four copies of the QSGMII registers - one for each port. The only exception are registers 26_4 and 27_4, which are common control registers for QSGMII. These registers can be accessed via any of the four ports PHY addresses.

2.4.3 QSGMII Speed and Link

When the QSGMII MAC interface is used, the media interface can be copper or SGMII/1000BASE-X/100BASE-FX. The operational speed of the aggregated SGMII interfaces within the QSGMII MAC interface is determined according to [Table 58](#) media interface status and/or loopback mode.

Each SGMII port of the QSGMII can independently operate at different speeds.

Table 58: SGMII Port Operational Speed

Link Status	SGMII Speed
No Link	Determined by speed setting of 21_2.2:0
MAC Loopback	Determined by speed setting of 21_2.2:0
1000BASE-T, SGMII at 1000 Mbps, 1000BASE-X	1000 Mbps
100BASE-TX, SGMII at 100 Mbps, 100BASE-FX	100 Mbps
10BASE-T, SGMII at 10 Mbps	10 Mbps

Two registers are available to determine whether the QSGMII achieved link and sync. Register 17_4.5 indicates that the SERDES locked onto the incoming KDKDKD... sequence. If QSGMII Auto-Negotiation is disabled, register 17_4.10 has the same meaning as register 17_4.5. If QSGMII

Auto-Negotiation is enabled, then register 17_4.10 indicates whether QSGMII Auto-Negotiation successfully established link.

2.4.4 QSGMII TRR Blocking

When the QSGMII receives a packet with odd number of bytes, a single symbol of carrier extension will be passed on and transmitted onto 1000BASE-T. This carrier extension may cause problems with full-duplex MACs that incorrectly handle the carrier extension symbols. When register 16_4.13 is set to 1, all carrier extend and carrier extend with error symbols received by the QSGMII will be converted to idle symbols when operating in full-duplex. Carrier extend and carrier extend with error symbols will not be blocked when operating in half-duplex, or if register 16_4.13 is set to 0. Note that symbol errors will continue to be propagated regardless of the setting of register 16_4.13.

This function is on by default as the QSGMII standard requires this function to be implemented.

2.5 Loopback

The device implements various different loopback paths.

2.5.1 System Interface Loopback

The functionality, timing, and signal integrity of the System interface can be tested by placing the device in System interface loopback mode. This can be accomplished by setting register 0_0.14 = 1, 0_1.14 = 1, or 0_4.14 = 1. In loopback mode, the data received from the MAC is not transmitted out on the media interface. Instead, the data is looped back and sent to the MAC. During loopback, link will be lost and packets will not be received.

If loopback is enabled while auto-negotiating, FLP Auto-Negotiation codes will be transmitted. If loopback is enabled in forced 10BASE-T mode, 10BASE-T idle link pulses will be transmitted on the copper side. If loopback is enabled in forced 100BASE-T mode, 100BASE-T idles will be transmitted on the copper side.

The speed of the SGMII or QSGMII interface is determined by register 21_2.2:0 during loopback. 21_2.2:0 is 100 = 10 Mbps, 101 = 100 Mbps, 110 = 1000 Mbps.

Figure 12: MAC Interface Loopback Diagram - Copper Media Interface

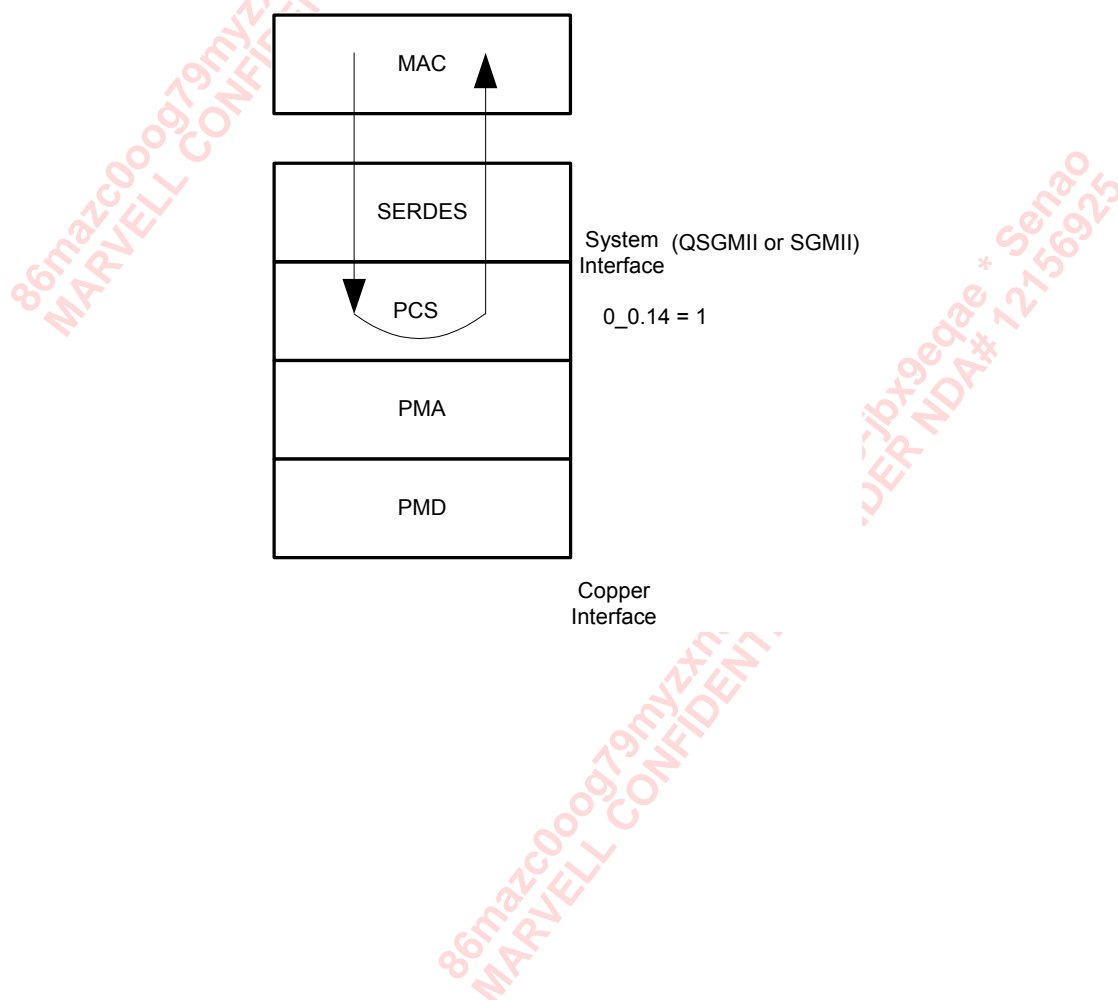


Figure 13: System Interface Loopback Diagram - Fiber Media Interface

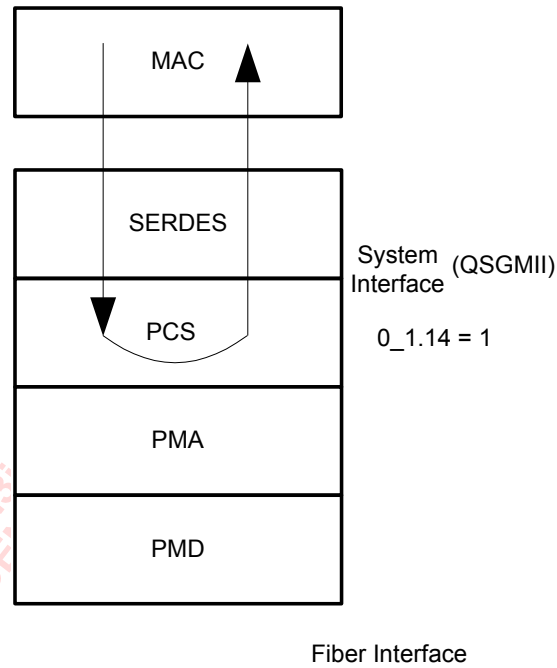
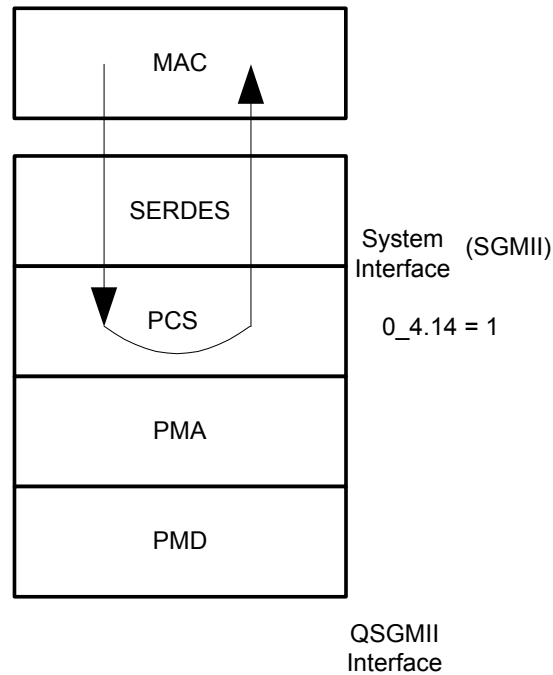


Figure 14: System Interface Loopback Diagram - QSGMII Media Interface



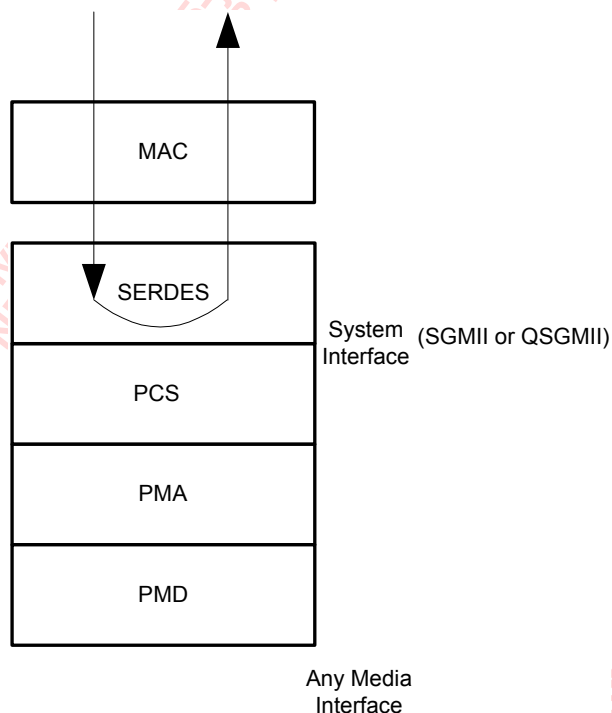
2.5.2 Synchronous SERDES Loopback

The 1.25 GHz SERDES and 5.0 GHz SERDES can loop back the raw 10 bit symbol at the receiver back to the transmitter. In this mode of operation, the received data is assumed to be frequency locked with the transmit data output by the PHY. No frequency compensation is performed when the 10 bit symbol is looped back. This mode facilitates testing using non 8/10 symbols such as PRBS.

The 1.25 GHz SERDES synchronous loopback is enabled by setting register 16_1.12 = 1 and 16_1.8 = 1.

The 5.0 GHz SERDES synchronous loopback is enabled by setting register 26_4.9 = 1.

Figure 15: Synchronous SERDES Loopback Diagram



2.5.3 Line Loopback

Line loopback allows a link partner to send frames into the device to test the transmit and receive data path. Frames from a link partner into the PHY, before reaching the MAC interface pins, are looped back and sent out on the line. They are also sent to the MAC. The packets received from the MAC are ignored during line loopback. Refer to Figure 16. This allows the link partner to receive its own frames.

Before enabling the line loopback feature, the PHY must first establish link to another PHY link partner. If Auto-Negotiation is enabled, both link partners should advertise the same speed and full-duplex. If Auto-Negotiation is disabled, both link partners need to be forced to the same speed and full-duplex. Once link is established, the line loopback mode can be enabled.

Register 21_2.14 = 1 enables the line loopback on the copper interface.

Register 16_1.12 = 1 and 16_1.8 = 0 enables the line loopback of the 1000BASE-X, SGMII interface.

Register 16_4.12 = 1 enables the line loopback of the QSGMII media interface.

Figure 16: Copper Line Loopback Data Path

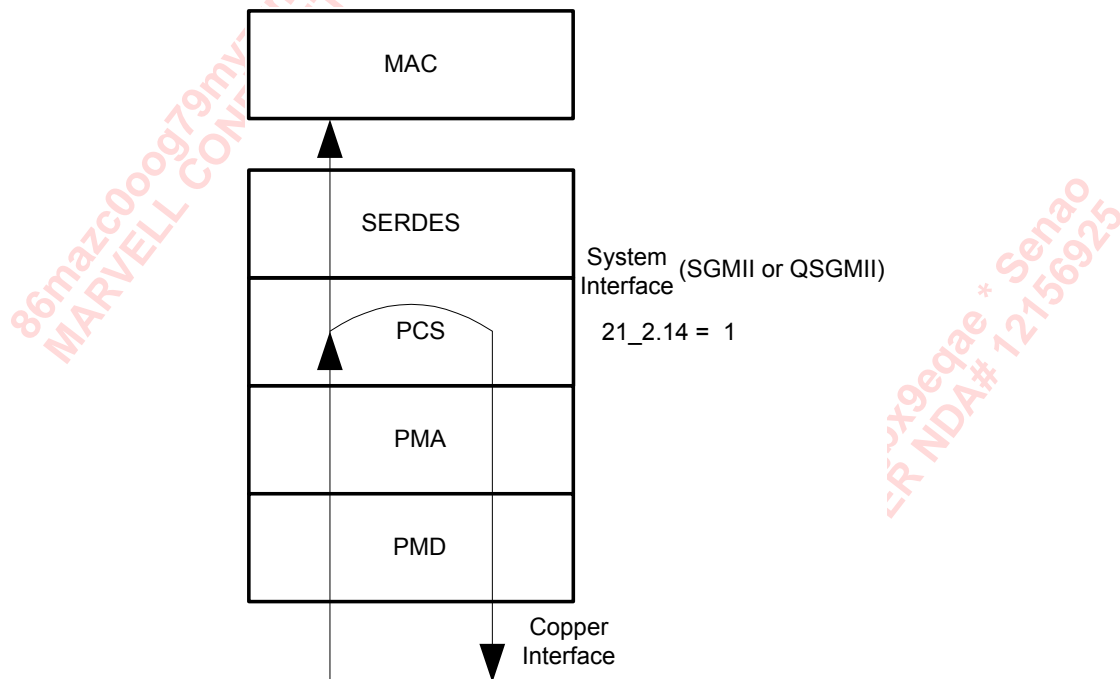


Figure 17: Fiber Line Loopback Data Path

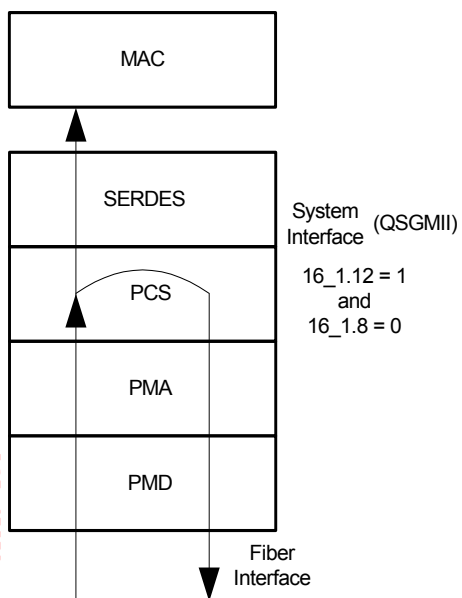
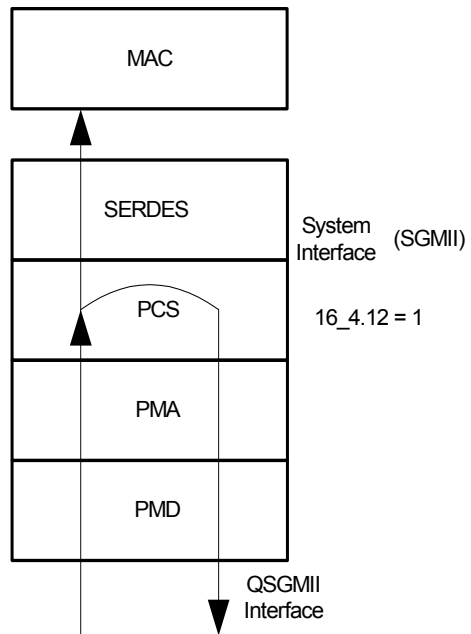


Figure 18: QSGMII Line Loopback Data Path



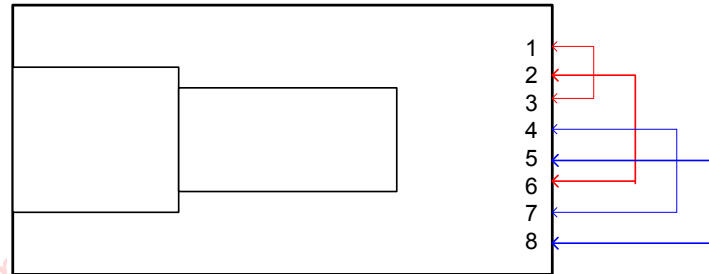
2.5.4 External Loopback

For production testing, an external loopback stub allows testing of the complete data path.

For 10BASE-T and 100BASE-TX modes, the loopback test requires no register writes. For 1000BASE-T mode, register 18_6.3 must be set to 1 to enable the external loopback. All copper modes require an external loopback stub.

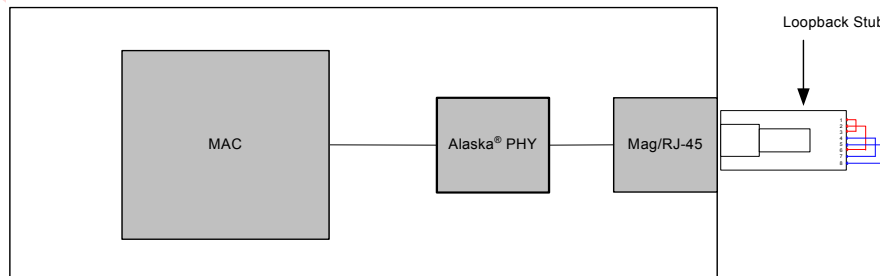
The loopback stub consists of a plastic RJ-45 header, connecting RJ-45 pair 1,2 to pair 3,6 and connecting pair 4,5 to pair 7,8, as seen in Figure 19.

Figure 19: Loopback Stub (Top View with Tab up)



The external loopback test setup requires the presence of a MAC that will originate the frames to be sent out through the PHY. Instead of a normal RJ-45 cable, the loopback stubs allows the PHY to self-link at 1000 Mbps. It also allows the actual external loopback. See Figure 20. The MAC should see the same packets it sent, looped back to it.

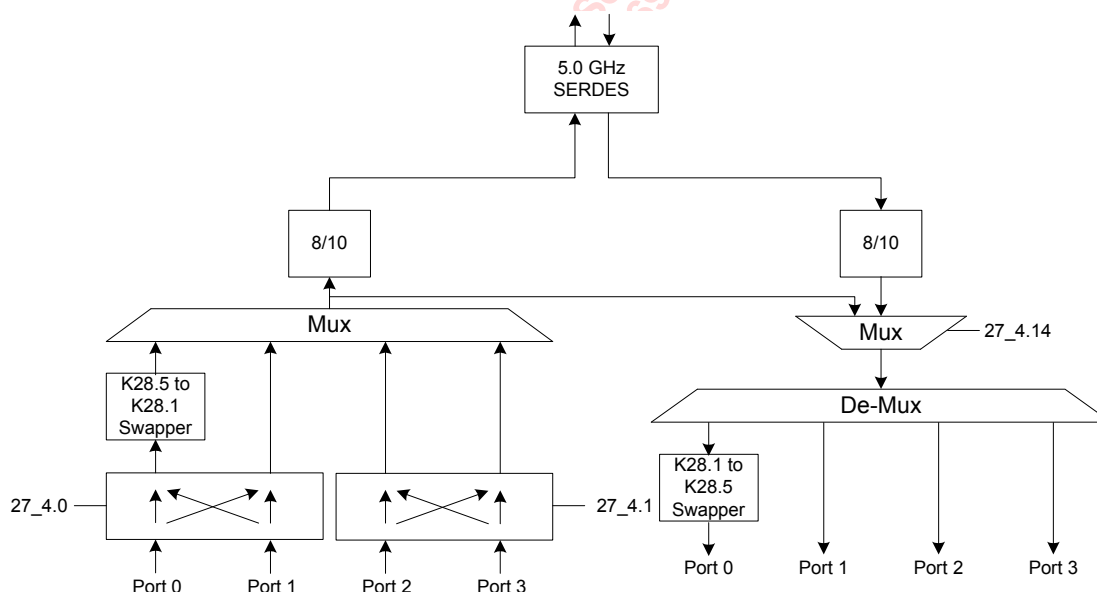
Figure 20: Test Setup for 10/100/1000 Mbps Modes using an External Loopback Stub



2.5.5 QSGMII Crossover Muxing and Loopback

Figure 22 shows 2 crossover muxes and a loopback path in QSGMII.

Figure 21: QSGMII Crossover Muxing and Loopback



Register 27_4.0 controls the crossover between Ports 0 and 1.

Register 27_4.1 controls the crossover between Ports 2 and 3.

0 = Straight

1 = Cross.

Register 27_4.14 controls the loopback at the QSGMII level. 0 = Normal, 1 = Loopback.

When this bit is set the 5.0G SERDES transmitter and receive automatically shuts down.

The crossover will swap Port 0 and 1 and also Port 2 and 3 in the transmit direction. The crossover and loopback can be done on the fly. Note that dropped packet, CRC error, lost sync (comma symbol got shifted from even to odd position), and other error conditions may occur when the crossover or loopback is switched back and forth. If the QSGMII auto-negotiation is turned on, a crossover event will force the auto-negotiation to restart since it is possible that the new port may be operating on a different speed.

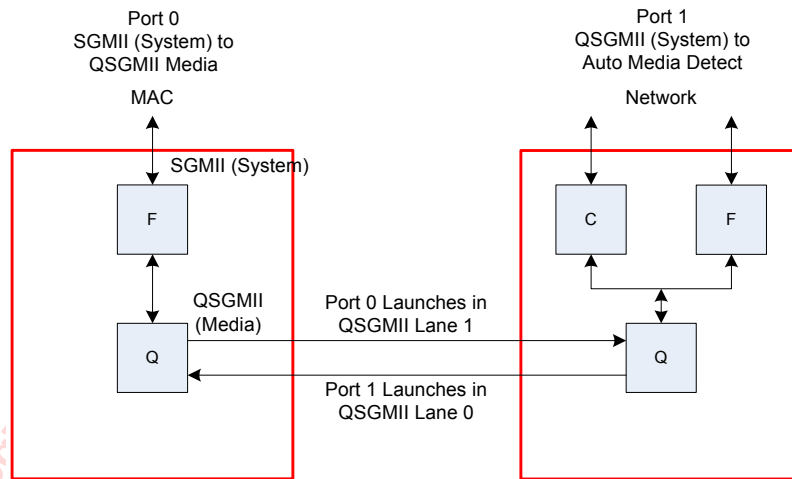
Table 59: QSGMII Global Control Register

Register	Function	Setting	Mode	HW Rst	SW Rst
27_4.1	QSGMII Output Crossover 2, 3	0 = Port 2 to QSGMII Lane 2, Port 3 to QSGMII Lane 3 1 = Port 2 to QSGMII Lane 3, Port 3 to QSGMII Lane 2	R/W	0	Retain
27_4.0	QSGMII Output Crossover 0,1	0 = Port 0 to QSGMII Lane 0, Port 1 to QSGMII Lane 1 1 = Port 0 to QSGMII Lane 1, Port 1 to QSGMII Lane 0	R/W	0	Retain

There are two primary uses for the crossover muxing and it is always used in conjunction with the QSGMII loopback.

The first use is create a two port SGMII (System) to auto media detect. Figure 22 shows how the combination of Port 0 and Port 1 with the crossover enabled and the QSGMII enabled can create such a device. Port 2 and Port 3 (not shown) can be similarly combined to form the second port.

Figure 22: SGMII (System) to Auto Media Detect



The second use is for a two port SGMII to redundant copper link. Figure 23 shows Port 1 being the active link while Port 0 is also linked but does not communicate to the MAC. Figure 24 shows the link in Port 1 is broken. Port 1 is then reconfigured into SGMII (System) to QSGMII (Media) mode to communicate with the copper link in Port 0.

Figure 23: Primary Link Active

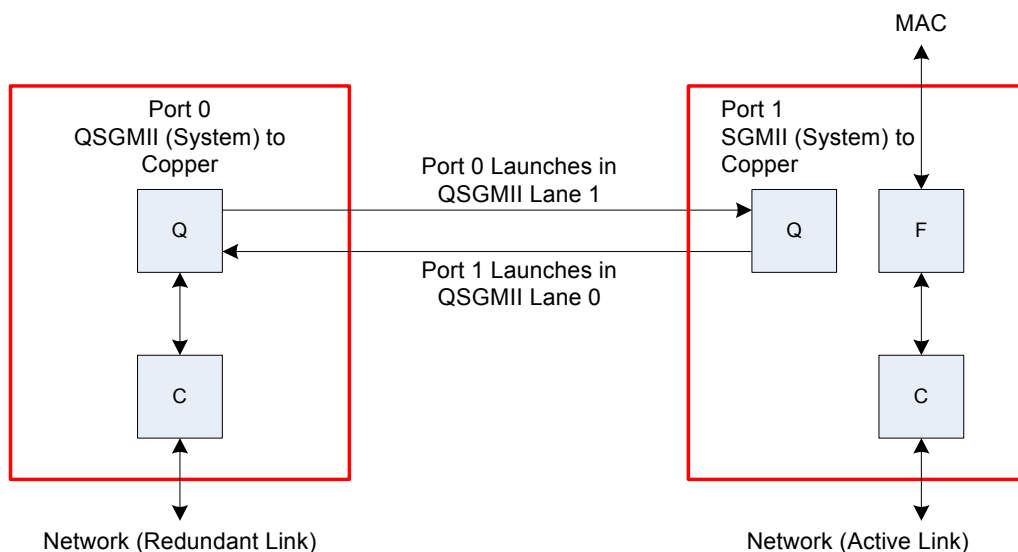
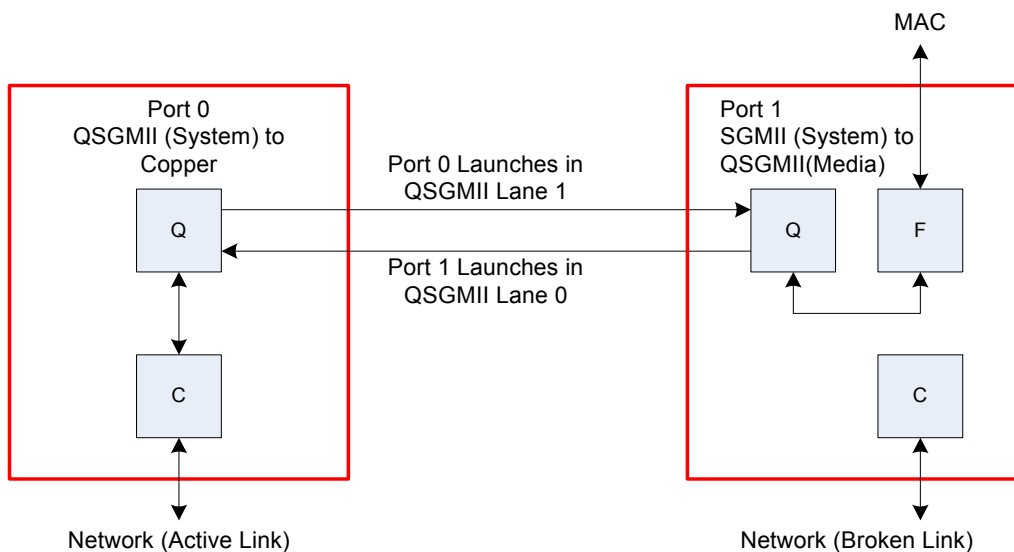


Figure 24: Redundant Link Active



2.6 Fiber/Copper Auto-Selection

The device has a patented feature to automatically detect and switch between fiber and copper cable connections. The auto-selection operates in one of three modes: Copper /1000BASE-X, Copper/100BASE-FX, and Copper/SGMII Media Interface.

Register 20_18.2:0 and register 20_18.6 select the Fiber/Copper auto media modes of operation. See Table 60 for details.

Table 60: Fiber/Copper Auto-media Modes of Operation

Reg 20_18.2:0	Reg 20_18.6	Auto-media Modes of Operation
011	0	0 = 100BASE-FX Only - no Auto-Media Detect 1 = Copper/100BASE-FX
110	X	Copper/SGMII
111	X	Copper/1000BASE-X

The device monitors the signals of the S_INP/N and the MDIP/N[3:0] lines. If a fiber optic cable is plugged in, the device will adjust itself to be in fiber mode. If an RJ-45 cable is plugged in, the device will adjust itself to be in copper mode. If both cables are connected then the first media to establish link, or the preferred media will be enabled. The media which is not enabled will turn off to save power. If the link on the first media is lost, then the inactive media will be powered up, and both media will once again start searching for link.

2.6.1 Preferred Media

The device can be programmed to give one media priority over the other. In other words if the non-preferred media establishes link first and subsequently energy is detected on the preferred media, the PHY will drop link on the non-preferred media for 4 seconds and give the preferred media a chance to establish link. Register 20_18.5:4 selects the preferred media.

- 00 = Link with the first media to establish link
- 01 = Prefer copper media
- 10 = Prefer fiber media

2.6.2 Definition of link in SGMII Media Interface in the context of auto media selection

In the conventional Copper/1000BASE-X definition of link, 1000BASE-X link is defined to be up when auto-negotiation complete if 1000BASE-X auto-negotiation is turned on, or the acquisition of comma if 1000BASE-X auto-negotiation is off. No link is defined to be when the comma is not seen for some amount of time, or when auto-negotiation restarts.

In the Copper/SGMII Media Interface definition of link, the SGMII Media Interface link is up only if bit 15 of the SGMII auto-negotiation indicates that link is up. Completing auto-negotiation is not sufficient to bring the link up. With SGMII auto-negotiation turned off or in the link down case the link definition is identical to the 1000BASE-X case.

2.6.3 Notes on Determining which Media Linked Up

Since there are two sets of IEEE registers (one for copper and the other for fiber) the software needs to be aware of register 22.7:0 so that the correct set of registers are selected. In general the sequence is as follows.

1. Set the auto-negotiation registers of the copper medium. (This step may not be necessary if the hardware defaults are acceptable.)
2. Set the auto-negotiation registers of the fiber medium. (This step may not be necessary if the hardware defaults are acceptable.)
3. Poll for link status. Go to step 4 if there is link.
4. Once there is link determine whether the link is copper or fiber medium.
5. Look at the auto-negotiation results for the medium that established link.
6. Poll for link status. If link status goes down then go back to step 3.

An example of a polling method procedure is as follows:

1. Write register 22.7:0 to 0x00 to point to the copper medium. Write the appropriate auto-negotiation registers to advertise the desired capabilities.
2. Write register 22.7:0 to 0x01 to point to the fiber medium. Write the appropriate auto-negotiation registers to advertise the desired capabilities.
3. If one medium is preferred over the other then write register 22.7:0 to 0x02 to point to the MAC registers. Set 20_18.5:4 to the preferred media.
4. Write 0_0.15 and 0_1.15 to '1' to issue software reset. This causes the auto-negotiation settings to take effect.
5. Write register 22.7:0 to 0x00 to point to the copper medium. Read the copper link status register 1_0.2. Write register 22.7:0 to 0x01 to point to the fiber medium. Read the fiber link status register 1_1.2. Keep doing this until one of the link comes up. It should be clear which link goes up. When link is up go to the next step.
6. Once the link is up set register 22.7:0 to 0x00 if the copper medium is up, or 0x01 if the fiber medium is up. Read the auto-negotiation registers for the auto-negotiation status if needed.
7. Poll register 1_0.2 or 1_1.2 depending on copper or fiber link. If link goes down go back to step 5.

2.7 Snooping

Within each mode of operation there is one unused media interface. It is possible to use the unused transmitter to snoop on the transmit or receive path. Register 20_18.11:10 enables the snooping and selects which path to snoop on as shown in Table 61. The snooping is turned off when register 20_18.11:10 is set to 00.

Register 20_18.12 determines whether the encrypted version or the unencrypted version is snooped.

0 = Non-encrypted

1 = Encrypted

Note that this bit should always be set to 0 when the snooping is turned off.

Table 61: Snooping Control

Register 20_18.2:0	Mode	Snoop Data From Network (20_18.11:10 = 10) Source	Snoop Data From MAC (20_18.11:10 = 11) Source	Transmitter Destination
000	QSGMII (System) to Copper	Copper Rx	QSGMII (System) Rx	SGMII (System)
001	SGMII (System) to Copper	Copper Rx	SGMII (System) Rx	QSGMII (System)
010	QSGMII (System) to 1000BASE-X	1000BASE-X Rx	QSGMII (System) Rx	1000BASE-T
011	QSGMII (System) to 100BASE-FX or QSGMII (System) to Auto Media Detect Copper/100BASE-FX	100BASE-FX Rx or Copper Rx	QSGMII (System) Rx	100BASE-TX or 100BASE-FX (100Mbps Only)
100	QSGMII (System) to SGMII (Media)	SGMII (Media) Rx	QSGMII (System) Rx	10/100/1000BASE-T
101	SGMII (System) to QSGMII (Media)	QSGMII (Media) Rx	SGMII (System) Rx	10/100/1000BASE-T
110	QSGMII (System) to Auto Media Detect Copper/SGMII (Media)	Copper Rx or SGMII (Media) Rx	QSGMII (System) Rx	SGMII (System) or 10/100/1000BASE-T
111	QSGMII (System) to Auto Media Detect Copper/1000BASE-X	Copper Rx or 1000BASE-X Rx	QSGMII (System) Rx	1000BASE-X or 10/100/1000BASE-T

There is no need to power down the unused interface via registers 0_0.11, 0_1.11, and 0_4.11 when snooping is turned off. The unused interface will automatically power down when not needed. Note that snooping cannot be turned on if registers 0_0.11, 0_1.11, or 0_4.11 is set to power down.

It is the responsibility of the user to insure that the PHY is configured correctly so that the interface used for snooping can link up with its link partner. Note in particular when register 20_18.2:0 is set to 111 and the copper link is up that there is no way to snoop if the copper link is operating in 10BASE-T since the interface used for snooping only operates in 1000BASE-X or 100BASE-FX and the interface is not rate matched.

2.8 Synchronizing FIFO

The device has transmit and receive synchronizing FIFOs to reconcile frequency differences between the clocks of the MAC interface and the media side. There are three FIFOs on the transmit paths of the QSGMII, copper, and fiber/SGMII as shown in Figure 25. The depth of the FIFOs can be independently programmed by programming register bits 16_1.15:14, 16_2.15:14, and 16_4.15:14. See the “Alaska Ultra FAQs” for details on how to calculate required FIFO depth and the details of the different clocks used for transmit and receive in each mode of operation.

The FIFO depths can be increased in length to support longer frames. The device can handle jumbo frame sizes up to 16 Kbytes with up to ± 100 PPM clock jitter. The deeper the FIFO depth, the higher the latency will be.

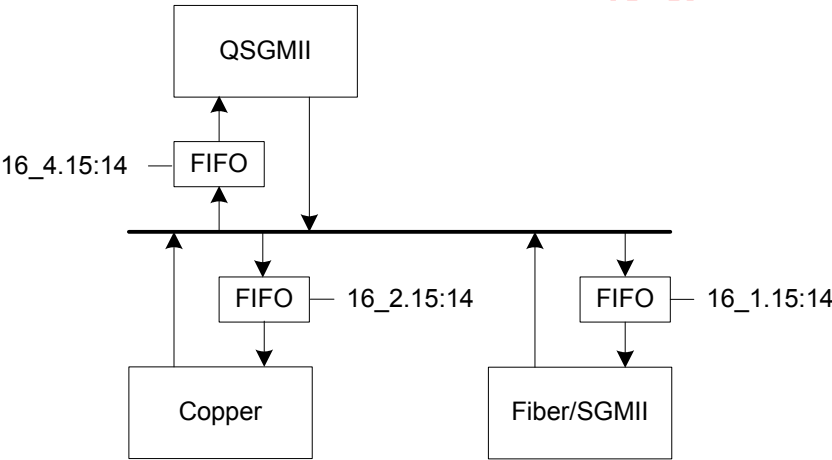
For the device, the status of the FIFO can be interrogated as in Table 62. Registers 19_2.3:2 are set depending on whether the copper transmit FIFO inserted or deleted idle symbols. Idles inserted or deleted will be flagged only if the inter packet gap is 24 bytes or less at the input of the FIFO. Inserted or deleted idles will be ignored if the inter packet gap is greater than 24 bytes.

The FIFO status bits can generate interrupts by setting the corresponding bits in register 18_1, 18_2, and 18_4.

Table 62: Device FIFO Status Bits

Register	Function	Setting
19_1.7	Fiber Transmit FIFO Over/Underflow	1 = Over/Underflow error 0 = No FIFO error
19_2.7	Copper Transmit FIFO Over/Underflow	1 = Over/Underflow error 0 = No FIFO error
19_4.7	QSGMII FIFO Over/Underflow	1 = Over/Underflow error 0 = No FIFO error
19_2.3	Copper Transmit FIFO Idle Inserted	1 = Idle inserted 0 = No idle inserted
19_2.2	Copper Transmit FIFO Idle Deleted	1 = Idle deleted 0 = No idle deleted

Figure 25: FIFO Locations



2.9 Resets

In addition to the hardware reset pin (RESETn) there are several software reset bits as summarized in [Table 63](#).

Register 27_4.15 is a software bit that emulates the hardware reset. The entire chip is reset as if the RESETn pin is asserted. Once triggered, registers are not accessible through the MDIO until the chip reset completes.

The copper, fiber, and QSGMII circuits are reset per port via register 0_0.15, 0_1.15, and 0_4.15 respectively. A reset in one circuit does not directly affect another circuit.

Register 20_18.15 resets the mode control, port power management, and generator and checkers.

Register 26_4.15 resets the QSGMII for all 4 ports including the 5.0G SERDES.

All the reset registers described are self clear.

Table 63: Reset Control Bits

Reset Register	Register Effect	Block
27_4.15	Chip Hardware Reset	Entire Chip
0_0.15	Software Reset for Bank 0, 2, 3, 5, 7	Copper - per port
0_1.15	Software Reset for Bank 1	Fiber/SGMII - per port
0_4.15	Software Reset for Bank 4	QSGMII - per port
26_4.15	Software Reset for Bank 4 - All 4 ports	QSGMII - all ports and common
20_18.15	Software Reset for Bank 6 and 18	Generator/Checker/Mode - per port

2.10 Power Management

The device supports several advanced power management modes that conserve power.

2.10.1 Manual Power Down

There are multiple power down control bits on chip and they are summarized in [Table 64](#). Each power down control independently powers down its respective circuits. In general, it is not necessary to power down an unused interface. The PHY will automatically power down any unused circuit. For example when auto-media detect is turned on, the unused interface will automatically power down.

The automatic PHY power management can be overridden by setting the power down control bits. These bits have priority over the PHY power management in that the circuit can not be powered up by the power management when its associated power down bit is set to 1. When a circuit is power back up by setting the bit to 0, a software reset is also automatically sent to the corresponding circuit.

Note that register 0_0.11 and 16_0.2 are logically ORed to form a power down control.

Table 64: Power Down Control Bits

Reset Register	Register Effect
0_0.11	Copper Power Down
16_0.2	Copper Power Down
0_1.11	Fiber/SGMII Power Down
0_4.11	QSGMII Power Down - Per port
26_4.11	Global QSGMII Power Down

2.10.2 MAC Interface Power Down

In some applications, the MAC interface must run continuously regardless of the state of the network interface. Additional power will be required to keep the MAC interface running during low power states.

If absolute minimal power consumption is required during network interface power down mode or in the Energy Detect modes, then register 16_2.3 or 16_1.3 should be set to 0 to allow the MAC interface to power down.

[Table 65](#) shows which bit controls the automatic MAC interface power down, and the MAC interface that is powered down. In general 16_2.3 is used when the network interface is copper and 16_1.3 is used when the network interface is fiber.

There is no equivalent bit when the QSGMII is used as the network interface. In MODE = 101 the power down in the QSGMII has no effect on the SGMII. Also note that there is no energy detect function in the QSGMII.

In the auto media detect modes (MODE = 110 and 111) both the fiber side and copper side has to indicate power down before the QSGMII port can be powered down.

Table 65: Automatic MAC Interface Power Down

Register 20_18.2:0	Mode	MAC Interface Power Down Control Bit	MAC Interface Powered Down
000	QSGMII (System) to Copper	16_2.3	QSGMII Port Logic
001	SGMII (System) to Copper	16_2.3	SGMII
010	QSGMII (System) to 1000BASE-X	16_1.3	QSGMII Port Logic
011	QSGMII (System) to 100BASE-FX	16_1.3	QSGMII Port Logic
100	QSGMII (System) to SGMII (Media)	16_1.3	QSGMII Port Logic
101	SGMII (System) to QSGMII (Media)	N/A	N/A
110	QSGMII (System) to Auto-Media Detect Copper/SGMII (Media)	16_2.3 for copper 16_1.3 for fiber	QSGMII Port Logic
111	QSGMII (System) to Auto-Media Detect Copper/1000BASE-X or Copper/100BASE-FX	16_2.3 for copper 16_1.3 for fiber	QSGMII Port Logic

2.10.3 Copper Energy Detect Modes

The device can be placed in energy detect power down modes by selecting either of the two energy detect modes. Both modes enable the PHY to wake up on its own by detecting activity on the CAT 5 cable. The status of the energy detect is reported in register 17_0.4 and the energy detect changes are reported in register 19_0.4.

2.10.3.1 Energy Detect (Mode 1)

Energy Detect (Mode 1) is entered by setting register 16_0.9:8 to 10.

In Mode 1, only the signal detection circuitry and serial management interface are active. If the PHY detects energy on the line, it starts to Auto-Negotiate sending FLPs for 5 seconds. If at the end of 5 seconds the Auto-Negotiation is not completed, then the PHY stops sending FLPs and goes back to monitoring receive energy. If Auto-Negotiation is completed, then the PHY goes into normal 10/100/1000 Mbps operation. If during normal operation the link is lost, the PHY will re-start Auto-Negotiation. If no energy is detected after 5 seconds, the PHY goes back to monitoring receive energy.

2.10.3.2 Energy Detect +TM (Mode 2)

Energy Detect (Mode 2) is entered by setting register 16_0.9:8 to 11.

In Mode 2, the PHY sends out a single 10 Mbps NLP (Normal Link Pulse) every one second. Except for this difference, Mode 2 is identical to Mode 1 operation. If the device is in Mode 1, it cannot wake up a connected device; therefore, the connected device must be transmitting NLPs, or either device must be woken up through register access. If the device is in Mode 2, then it can wake a connected device.

2.10.3.3 Normal 10/100/1000 Mbps Operation

Normal 10/100/1000 Mbps operation can be entered by turning off energy detect mode by setting register 16_0.9:8 to 0x.

2.10.3.4 Power State Upon Exiting Power Down

When the PHY exits power down (register 0_0.11 or 16_0.2) the active state will depend on whether the energy detect function is enabled (register 16_0.9:8 = 1x). If the energy detect function is enabled, the PHY will transition to the energy detect state first and will wake up only if there is a signal on the wire.

Table 66: Power State after Exiting Power Down

Register 0_0.11	Register 16_0.2	Register 16_0.9:8	Behavior
1	x	xx	Power down
x	1	xx	Power down
1 to 0	0	00	Transition to power up
0	1 to 0	00	Transition to power up
1 to 0	0	1x	Transition to energy detect state
0	1 to 0	1x	Transition to energy detect state

2.10.4 Low Power Modes

Three low power modes are supported in the device.

- IEEE 22.2.4.1.5 compliant power down
- Energy Detect (Mode 1)
- Energy Detect+™ (Mode 2)

IEEE 22.2.4.1.5 power down compliance allows for the PHY to be placed in a low-power consumption state by register control.

Energy Detect (Mode 1) allows the device to wake up when energy is detected on the wire.

Energy Detect+™ (Mode 2) is identical to Mode 1 with the additional capability to wake up a link partner. In Mode 2, the 10BASE-T link pulses are sent once every second while listening for energy on the line.

Details of each mode are described below.

2.10.5 Low Power Operating Modes

2.10.5.1 IEEE Power Down Mode

The standard IEEE power down mode is entered by setting register 0_0.11. In this mode, the PHY does not respond to any system interface (i.e., QSGMII/SGMII) signals except the MDC/MDIO. It also does not respond to any activity on the copper or fiber media.

In this power down mode, the PHY cannot wake up on its own by detecting activity on the media. It can only wake up by setting registers 0_0.11 and 16_0.2 = 0.

Upon deassertion of hardware reset, Register 0_0.11 and 16_0.2 are set to 1 to default the device to a power down state.

Register 0_0.11 and 16_0.2 are logically ORed to form a power down control.

2.10.5.2 Energy Detect Power Down Modes

The device can be placed in energy detect power down modes by selecting either of the two energy detect modes. Both modes enable the PHY to wake up on its own by detecting activity on the CAT 5 cable. The energy detect modes only apply to the copper media. The energy detect modes will not work while Fiber/Copper Auto Select (2.6 "Fiber/Copper Auto-Selection" on page 80) is enabled. The status of the energy detect is reported in register 17_0.4 and the energy detect changes are reported in register 19_0.4.

2.10.6 SGMII Effect on Low Power Modes

In some applications, the SGMII must run continuously regardless of the state of the PHY. Additional power will be required to keep this SGMII interface running during low power states.

If absolute minimal power consumption is required during the IEEE power down mode or the Energy Detect modes, then register 16_2.3 should be set to 0 to allow the SGMII to power down. Note that for these settings to take effect a software reset must be issued.

2.11 Auto-Negotiation

The device supports four types of Auto-Negotiation.

- 10/100/1000BASE-T Copper Auto-Negotiation. (IEEE 802.3 Clauses 28 and 40)
- 1000BASE-X Fiber Auto-Negotiation (IEEE 802.3 Clause 37)
- SGMII Auto-Negotiation (Cisco specification)
- QSGMII Auto-Negotiation (Cisco specification)

Auto-Negotiation provides a mechanism for transferring information from the local station to the link partner to establish speed, duplex, and Master/Slave preference during a link session.

Auto-Negotiation is initiated upon any of the following conditions:

- Power up reset
- Hardware reset
- Software reset (Register 0_0.15, 0_1.15, or 0_4.15)
- Restart Auto-Negotiation (Register 0_0.9, 0_1.9, 0_4.9)
- Transition from power down to power up (Register 0_0.11, 0_1.11, or 0_4.11)
- The link goes down

The following sections describe each of the Auto-Negotiation modes in detail.

2.11.1 10/100/1000BASE-T Auto-Negotiation

The 10/100/1000BASE-T Auto-Negotiation (AN) is based on Clause 28 and 40 of the IEEE 802.3 specification. It is used to negotiate speed, duplex, and flow control over CAT5 UTP cable. Once Auto-Negotiation is initiated, the device determines whether or not the remote device has Auto-Negotiation capability. If so, the device and the remote device negotiate the speed and duplex with which to operate.

If the remote device does not have Auto-Negotiation capability, the device uses the parallel detect function to determine the speed of the remote device for 100BASE-TX and 10BASE-T modes. If link is established based on the parallel detect function, then it is required to establish link at half-duplex mode only. Refer to IEEE 802.3 clauses 28 and 40 for a full description of Auto-Negotiation.

After hardware reset, 10/100/1000BASE-T Auto-Negotiation can be enabled and disabled via Register 0_0.12. Auto MDI/MDIX and Auto-Negotiation may be disabled and enabled independently. When Auto-Negotiation is disabled, the speed and duplex can be set via registers 0_0.13, 0_0.6, and 0_0.8 respectively. When Auto-Negotiation is enabled the abilities that are advertised can be changed via registers 4_0 and 9_0.

Changes to registers 0_0.12, 0_0.13, 0_0.6 and 0_0.8 do not take effect unless one of the following takes place:

- Software reset (registers 0_0.15)
- Restart Auto-Negotiation (register 0_0.9)
- Transition from power down to power up (register 0_0.11)
- The copper link goes down

To enable or disable Auto-Negotiation, Register 0_0.12 should be changed simultaneously with either register 0_0.15 or 0_0.9. For example, to disable Auto-Negotiation and force 10BASE-T half-duplex mode, register 0_0 should be written with 0x8000.

Registers 4_0 and 9_0 are internally latched once every time the Auto-Negotiation enters the Ability Detect state in the arbitration state machine. Hence, a write into Register 4_0 or 9_0 has no effect once the device begins to transmit Fast Link Pulses (FLPs). This guarantees that sequences of FLPs transmitted are consistent with one another.

Register 7_0 is treated in a similar way as registers 4_0 and 9_0 during additional next page exchanges.

If 1000BASE-T mode is advertised, then the device automatically sends the appropriate next pages to advertise the capability and negotiate master/slave mode of operation. If the user does not wish to transmit additional next pages, then the next page bit (Register 4_0.15) can be set to zero, and the user needs to take no further action.

If next pages in addition to the ones required for 1000BASE-T are needed, then the user can set register 4_0.15 to one, and send and receive additional next pages via registers 7_0 and 8_0, respectively. The device stores the previous results from register 8 in internal registers, so that new next pages can overwrite register 8_0.

Note that 1000BASE-T next page exchanges are automatically handled by the device without user intervention, regardless of whether or not additional next pages are sent.

Once the device completes Auto-Negotiation, it updates the various status in registers 1_0, 5_0, 6_0, and 10_0. Speed, duplex, page received, and Auto-Negotiation completed status are also available in registers 17_0 and 19_0.

See “PHY Register Description” on page 150.

2.11.2 1000BASE-X Auto-Negotiation

1000BASE-X Auto-Negotiation is defined in Clause 37 of the IEEE 802.3 specification. It is used to auto-negotiate duplex and flow control over fiber cable. Registers 0_1, 4_1, 5_1, 6_1, and 15_1 are used to enable AN, advertise capabilities, determine link partner's capabilities, show AN status, and show the duplex mode of operation respectively.

Register 22.7:0 must be set to one to view the fiber auto-negotiation registers.

The device supports Next Page option for 1000BASE-X Auto-Negotiation. Register 7_1 of the fiber pages is used to transmit Next Pages, and register 8_1 of the fiber pages is used to store the received Next Pages. The Next Page exchange occurs with software intervention. The user must set Register 4_1.15 to enable fiber Next Page exchange. Each Next Page received in the registers should be read before a new Next Page to be transmitted is loaded in Register 7_1.

If the PHY enables 1000BASE-X Auto-Negotiation and the link partner does not, the link cannot link up. The device implements an Auto-Negotiation bypass mode. See [Section 2.11.3.2](#) for more details.

2.11.3 SGMII Auto-Negotiation

SGMII is a de-facto standard designed by Cisco. SGMII uses 1000BASE-X coding to send data as well as Auto-Negotiation information between the PHY and the MAC. However, the contents of the SGMII Auto-Negotiation are different than the 1000BASE-X Auto-Negotiation. See the “Cisco SGMII Specification” and the “MAC Interfaces and Auto-Negotiation” application note for further details.

The device supports SGMII interface with and without Auto-Negotiation. Auto-Negotiation can be enabled or disabled by writing to Register 0_1.12 followed by a soft reset. If SGMII Auto-Negotiation is disabled, the MAC interface link, speed, and duplex status (determined by the media side) cannot be conveyed to the MAC from the PHY. The user must program the MAC with this information in some other way (e.g., by reading PHY registers for link, speed, and duplex status). However, the operational speed of the SGMII will follow the speed of the media. (See [Table 56 on page 67](#)). Regardless of whether the Auto-Negotiation is enabled or disabled.

2.11.3.1 Flow control Enhancement to SGMII Auto-Negotiation

During standard SGMII Auto-Negotiation the PHY passes the link, speed, and duplex information to the MAC. The flow control information is not communicated. Typically, the MAC will have to read the registers of the PHY to find out the flow control capability of the link partner. The device has added in-line flow control information by using some of the reserved bits of the Auto-Negotiation base page as defined by the SGMII specification. This feature is optional. The user can select the standard SGMII Auto-Negotiation or the enhanced mode as described in Table 68. Table 67 shows the bit definitions for the enhanced mode.

For Register 16_1.7:6 = 01, bit 9 corresponds to register 17_1.3 and bit 8 corresponds to register 17_1.2. For Register 16_1.7:6 = 10, bit 3 corresponds to register 17_1.3 and bit 2 corresponds to register 17_1.2.

The enhanced SGMII mode is selected through Register 16_1.7:6 (Table 67).

Table 67: Enhanced SGMII PHY Status

TX_CONFIG_REG[15:0]			
Bit Number	Reg. 16_1.7:6 = 00	Reg. 16_1.7:6 = 01 MODE 1	Reg. 16_1.7:6 = 10 MODE 2
15	1 = Link Up 0 = Link Down	1 = Link Up 0 = Link Down	1 = Link Up 0 = Link Down
14	Acknowledge	Acknowledge	Acknowledge
13	0 = Reserved	0 = Reserved	0 = Reserved
12	1 = Full-duplex 0 = Half-duplex	1 = Full-duplex 0 = Half-duplex	1 = Full-duplex 0 = Half-duplex
11:10	00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved	00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved	00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved
9	1 =EEE supported 0 = EEE not supported	1 = Transmit pause enabled 0 = Disabled	1 = EEE supported 0 = EEE not supported
8	1 = EEE clock stop supported 0 = EEE clock stop not supported	1 = Received pause enabled 0 = Disabled	1 = EEE clock stop supported 0 = EEE clock stop not supported
7	0 = Reserved	0 = 10/100/1000BASE-T 1 = 100BASE-FX/1000BASE-X	0 = Reserved
6	0 = Reserved	1 = EEE supported 0 = EEE not supported	0 = Reserved
5	0 = Reserved	1 = EEE clock stop supported 0 = EEE clock stop not supported	0 = Reserved
4	0 = Reserved	0 = Reserved	0 = Reserved
3	0 = Reserved	0 = Reserved	1 = Transmit pause enabled 0 = Disabled

Table 67: Enhanced SGMII PHY Status (Continued)

TX_CONFIG_REG[15:0]			
Bit Number	Reg. 16_1.7:6 = 00	Reg. 16_1.7:6 = 01 MODE 1	Reg. 16_1.7:6 = 10 MODE 2
2	0 = Reserved	0 = Reserved	1 = Receive pause enabled 0 = Disabled
1	0 = Reserved	0 = Reserved	0 = 10/100/1000BASE-T 1 = 100BASE-FX/1000BASE-X
0	Always 1	Always 1	Always 1

Table 68: MAC Specific Control Register 1

Register	Function	Setting	Mode	HW Rst	SW Rst
16_1.7:6	Enhanced SGMII	00 = Do not pass Flow Control through SGMII Auto-negotiation 01 = Pass Flow Control through SGMII Auto-negotiation (MODE 1 – Marvell Legacy Mode) 10 = Pass Flow Control through SGMII Auto-negotiation (MODE 2) 11 = Reserved	R/W	0	Update

2.11.3.2 Serial Interface Auto-Negotiation Bypass Mode

If the MAC or the PHY implements the Auto-Negotiation function and the other does not, two-way communication is not possible unless Auto-Negotiation is manually disabled and both sides are configured to work in the same operational modes. To solve this problem, the device implements the SGMII Interface Auto-Negotiation Bypass Mode. When entering the state "Ability_Detect", a bypass timer begins to count down from an initial value of approximately 200 ms. If the device receives idles during the 200 ms, the device will interpret that the other side is "alive" but cannot send configuration codes to perform Auto-Negotiation. After 200 ms, the state machine will move to a new state called "Bypass_Link_Up" in which the device assumes a link-up status and the operational mode is set to the value listed under the "Comments" column of [Table 69](#).

Table 69: SGMII Auto-Negotiation modes

Reg. 0_1.12	Reg. 26_1.6	Comments
0	X	No Auto-Negotiation. User responsible for determining speed, link, and duplex status by reading PHY registers.
1	0	Normal SGMII Auto-Negotiation. Speed, link, and duplex status automatically communicated to the MAC during Auto-Negotiation.
1	1	MAC Auto-Negotiation enabled. Normal operation.
		MAC Auto-Negotiation disabled. After 200 ms the PHY will disable Auto-Negotiation and link based on idles.

2.11.4 QSGMII Auto-Negotiation

The QSGMII aggregates and de-aggregates four SGMII ports with the SGMII Auto-Negotiation code word passing transparently through the QSGMII.

The SGMII Auto-Negotiation described in [Section 2.11.3](#) applies to the Auto-Negotiation used on the QSGMII. The only exception to that is that the register is accessed by setting Register 22.7:0 to 0x04 (Page 4) instead of 0x01 (Page 1), i.e., the Auto-Negotiation enable register is accessed via Register 0_4.12 instead of 0_1.12 and the enhanced SGMII mode is selected through Register 16_4.7:6 instead of 16_1.7:6.

2.12 Downshift Feature

Without the downshift feature enabled, connecting between two Gigabit link partners requires a four-pair RJ-45 cable to establish 10, 100, or 1000 Mbps link. However, there are existing cables that have only two-pairs, which are used to connect 10 Mbps and 100 Mbps Ethernet PHYs. With the availability of only pairs 1, 2 and 3,6, Gigabit link partners can Auto-Negotiate to 1000 Mbps, but fail to link. The Gigabit PHY will repeatedly go through the Auto-Negotiation but fail 1000 Mbps link and never try to link at 10 Mbps or 100 Mbps.

With the Marvell® downshift feature enabled, the device is able to Auto-Negotiate with another Gigabit link partner using cable pairs 1,2 and 3,6 to downshift and link at 10 Mbps or 100 Mbps, whichever is the next highest advertised speed common between the two Gigabit PHYs.

In the case of a three pair cable (additional pair 4,5 or 7,8 - but not both) the same downshift function for two-pair cables applies.

By default, the downshift feature is turned off. Refer to register 16_0.14:11 which describe how to enable this feature and how to control the downshift algorithm parameters.

To enable the downshift feature, the following registers must be set:

- Register 16_0.11 = 1 - enables downshift
- Register 16_0.14:12 - sets the number of link attempts before downshifting

2.13 Fast 1000BASE-T Link Down Indication

Per the IEEE 802.3 Clause 40 standard, a 1000BASE-T PHY is required to wait 750 milliseconds or more to report that link is down after detecting a problem with the link. For Metro Ethernet applications, a Fast Failover in 50 ms is specified, which cannot be met if the PHY follows the 750 ms wait time. This delay can be reduced by intentionally violating the IEEE standard by setting register 26_0.9 to 1.

The delay at which link down is to be reported can be selected by setting register 26_0.11:10. 00 = 0ms, 01 = 10 ± 2 ms, 10 = 20 ± 2ms, 11 = 40 ± 2ms.

2.14 Advanced Virtual Cable Tester®

The device Advanced Virtual Cable Tester feature uses Time Domain Reflectometry (TDR) to determine the quality of the cables, shorts, cable impedance mismatch, bad connectors, termination mismatch, and bad magnetics. The device transmits a signal of known amplitude (+1V) down each of the four pairs of an attached cable. It will conduct the cable diagnostic test on each pair, testing the MDI_0_0P/N, MDI_0_1P/N, MDI_0_2P/N, and MDI_0_3P/N pairs sequentially. The transmitted signal will continue down the cable until it reflects off of a cable imperfection.

The Advanced VCT™ has 4 modes of operation that is programmable via register 23_5.7:6. The first mode returns the peak with the maximum amplitude that is above a certain threshold. The second mode returns the first peak detected that is above a certain threshold. The third mode measures the systematic offset at the receiver. The fourth mode measures the amplitude seen at a certain specified distance.

The VCT test is initiated by setting register 23_5.15 to 1. This bit will self clear when the test is completed. Register 23_5.14 will be set to a 1 indicating that the TDR results in the registers are valid.

Each point in the VCT reflected waveform is sampled multiple times and averaged. The number of samples to take is programmable via register 23_5.10:8.

Each time the VCT test is enable, the results seen on the four receive channels are reported in registers 16_5, 17_5, 18_5, and 19_5. Register 23_5.13:11 selects which channel transmits the test pulse.

When register 23_5.13:11 is set to 000 the same channel reflection is recorded. In other words, channel 0 transmits a pulse and the reflection seen on channel 0 receiver is reported. Channel 1 transmits a pulse and the reflection seen on channel 1 receiver is reported. The same for channel 2 and channel 3.

When register 23_5.13:11 is set to 100 all 4 receive channels report the reflection seen by a pulse transmitted by channel 0.

When register 23_5.13:11 is set to 101 all 4 receive channels report the reflection seen by a pulse transmitted by channel 1.

When register 23_5.13:11 is set to 110 all 4 receive channels report the reflection seen by a pulse transmitted by channel 2.

When register 23_5.13:11 is set to 111 all 4 receive channels report the reflection seen by a pulse transmitted by channel 3.

Hence, if only the reflection seen on the same channel is desired the VCT test should be run with 23_5.13:11 = 000. If all same channel and cross channel combinations are desired then the VCT test must be run 4 times with 23_5.13:11 set to 100, 101, 110, and 111 for the 4 runs. Registers 16_5, 17_5, 18_5, and 19_5 should be read and stored between each run.

2.14.1 Maximum Peak

When register 23_5.7:6 is set to 00, the maximum peak above a certain threshold is reported. Pulses are sent out and recorded according to the setting of register 25_5.13:11.

There are 10 threshold settings for same channel reflections and are specified by registers 26_5.6:0, 26_5.14:8, 27_5.6:0, 27_5.14:8, and 28_5.6:0 for positive reflections and 26_7.6:0, 26_7.14:8, 27_7.6:0, 27_7.14:8, and 28_7.6:0 for negative reflections.

These settings correspond to the amplitude threshold the reflected signal has to exceed before it is counted. Any reflected signal below this threshold level is ignored. The threshold settings are based on cable length with the breakpoints at 10 m, 50 m, 110 m, and 140 m.

There are 4 threshold settings for cross-channel specified by registers 25_5.6:0 and 25_5.14:8 for positive reflections and 25_7.6:0 and 25_7.14:8 for negative reflections. The threshold settings are based on cable length with the breakpoints at 10 m.

The default values are targeted to 85 ohm to 115 ohms. However these threshold settings should be calibrated for the desired impedance setting on the target system.

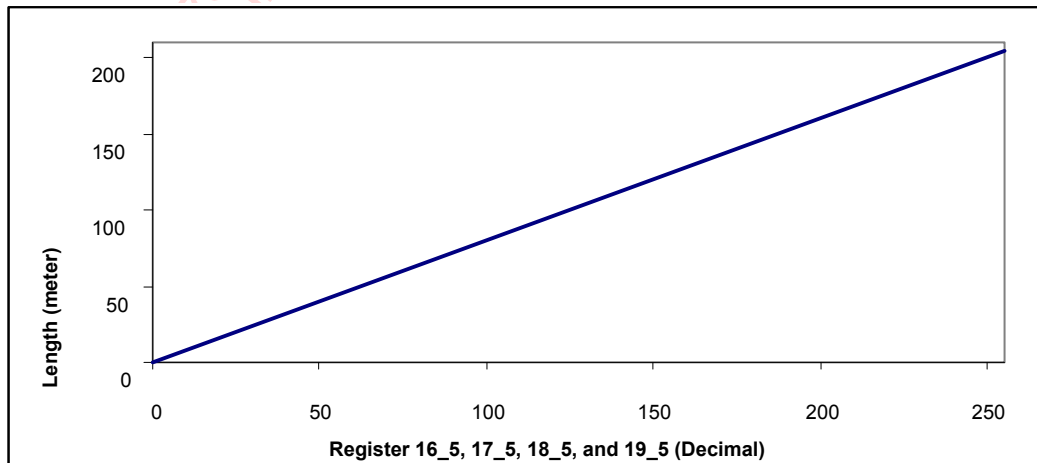
The results are stored in registers 16_5, 17_5, 18_5, and 19_5. Bits 7:0 report the distance of the peak. The distance can be converted to using the trend line in Figure 26. Bits 14:8 report the reflected amplitude. Bit 15 reports whether the reflected amplitude was positive or negative. When bits 15:8 return a value of 0x80, it means there was no peak detected above the threshold. If bits 15:8 return a value of 0x00 then the test failed.

Register 28_5.7 controls the exact distance that is reported. When set to 0 the distance where the amplitude falls to 50% of the peak amplitude is reported. When set to 1 the distance where the peak amplitude actually occurs is reported. In either case, the magnitude of the maximum amplitude is reported in bits 14:8.

In the maximum peak mode, register 24_5.7:0 is used to set the starting distance of the sweep. Normally this value should be set to 0. If this value is set to a non-zero value, any reflection below the starting distance is ignored. Note that 24_5.8 is ignored.

Note that the maximum peak only measures up to about 200 meters of cable.

Figure 26: Cable Fault Distance Trend Line



2.14.2 First Peak

When register 23_5.7:6 is set to 01, the first peak above a certain threshold is reported. The first peak operates in exactly the same way as the maximum peak except that there has to be some qualification as to what constitutes a peak since the first peak is not necessarily the maximum peak. The first peak is defined as the maximum amplitude seen before the reflected amplitude drops by some value below this peak. This hysteresis value is defined by register 23_5.5:0.

For example, in Figure 27, if Pa is greater than the hysteresis value in 23_5.5:0 and Va is above the threshold value, then Va and Da are reported since it is the first peak that is above the threshold.

If Pa is less than the hysteresis value in 23_5.5:0, then Va and Da are not reported as the first peak. Vb and Db will be reported as the first peak if Pb is greater than the hysteresis value in 23_5.5:0 and Vb is above the threshold value.

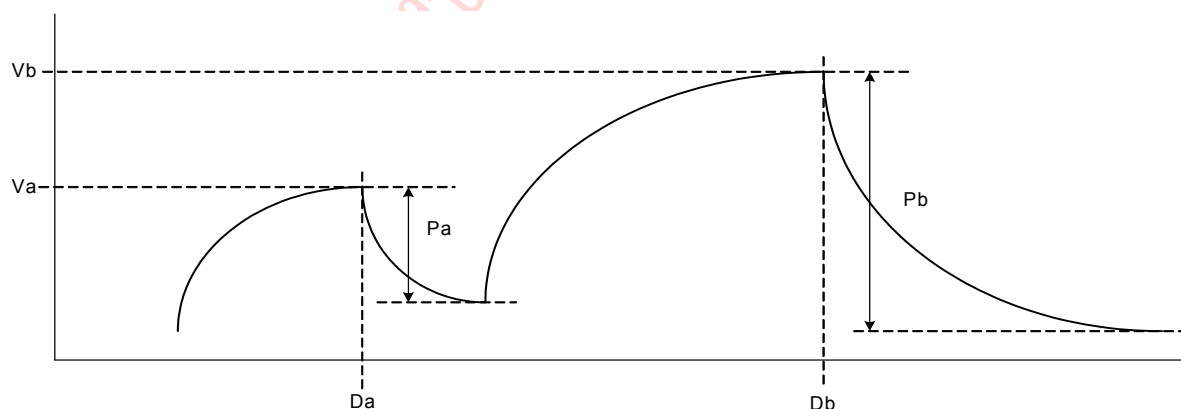
If P_a is greater than the hysteresis value in 23_5.5:0 but V_a is below the threshold value then V_a and D_a are not reported as the first peak. V_b and D_b will be reported as the first peak if P_b is greater than the hysteresis value in 23_5.5:0 and V_b is above the threshold value.

Register 28_5.7 controls the exact distance that is reported. When set to 0 the distance where the amplitude falls below the peak amplitude minus the hysteresis level as defined in register 23_5.5:0 is reported. When set to 1 the distance where the peak amplitude actually occurs is reported. In either case, the magnitude of the maximum amplitude of the first peak is reported in bits 14:8.

In the first peak mode register 24_5.7:0 is used to set the starting distance of the sweep. Normally, this value should be set to 0. If this value is set to a non-zero value, any reflection below the starting distance is ignored. This may be useful to ignore reflections at the transformer that are reported as the first peak. Note that 24_5.8 is ignored.

Note that the maximum peak only measures up to about 200 meters of cable.

Figure 27: First Peak Example



2.14.3 Offset

The offset reports the offset seen at the receiver. This is a debug mode. Bits 7:0 of registers 16_5, 17_5, 18_5, and 19_5 have no meaning. When bits 15:8 return a value of 0x80 it means there is zero offset. If bit 15:8 returns a value of 0x00 then the test failed.

Note that in the maximum peak, first peak, and sample point modes, the systematic offset is automatically subtracted from the results.

2.14.4 Sample Point

When register 20_8.7:6 is set to 11, the amplitude of the reflected pulse at a particular distance on the cable is reported. Unlike the maximum peak and first peak modes which only measures up to about 200 meters of cable, the sample point mode can measure up to 400 meters of cable.

The sample point returns the amplitude of the reflected pulse at a particular distance on the cable. The distance is set by register 24_5.8:0. The threshold registers 25_5, 26_5, 27_5, 28_5.6:0, 25_7, 26_7, 27_7, and 28_7.6:0 are ignored.

Bits 7:0 of registers 16_5, 17_5, 18_5, and 19_5 return the same value as 24_5.7:0. Note that register 24_5.8 is not returned. Bits 14:8 return the amplitude, and bit 15 the sign of the amplitude. If the test failed bits 15:8 will return 00000000 (zero amplitude will always return as 10000000).

By programming register 24_5.8:0 from 0x000 to 0x1FF and running the sample point test at each distance it is possible to reconstruct the reflected amplitude. Note that since the threshold is ignored, it is possible that some small reflections in the same channel measurements will be reported at short

cable lengths when there are none. This is because the analog hybrid does not 100% cancel out the transmitted signal.

2.14.5 Pulse Amplitude and Pulse Width

The transmitted pulse amplitude and pulse width can be adjusted via registers 28_5.9:8 and 28_5.11:10 respectively. They should normally be set to full amplitude and full pulse width.

2.14.6 Drop Link

When register 28_5.12 is set to 0 the circuit will wait 1.5 seconds to break the link before starting VCT™. When set to 1 this delay is bypassed.

2.14.7 VCT™ with Link Up

The following status requires the PHY to link up with a link partner.

- Register 20_5 reports the pair skew of each pair of wires relative to each other.
- Register 21_5.3:0 reports the polarity of each pair of wires.
- Register 21_5.6:5 reports the crossover status
- Register 20_5 and 21_5 are not valid unless register 21_5.6 is set to 1.

2.14.8 Alternate VCT Control

The registers in page 7 provides an alternate means to control VCT. When using page 7 to control the VCT, the VCT results in registers 16_5, 17_5, 18_5, and 19_5 will be altered and are not meaningful. Register 21_7.14 must be set to 0 when controlling VCT using registers in page 5.

VCT will run when any one of the following three events occur:

- Register 21_7.12 transitions from 0 to 1.
- Register 21_7.15 transitions from 0 to 1.
- Link transitions from link up to link down and register 21_7.14 = 1.

Note that if the VCT circuit is busy when any of the three events occur, the event is ignored.

If register 21_7.15 triggers VCT then the 1.5s break link prior to measurement is bypassed.

If any of the other 2 events triggers VCT then the 1.5s break link prior to measurement is not bypassed.

If register 21_7.13 = 1 then only same pair is checked using the first peak method.

If register 21_7.13 = 0 then same pair and cross pair are checked using the first peak method.

Register 21_7.11 indicates whether the cable testing is completed or not. Once completed the results are presented in registers 16_7, 17_7, 18_7, 19_7, and 20_7. It may be possible for multiple faults to occur on the same pair but only one fault can be reported. The priority in reporting in descending order is as follows.

- Test failed (busy).
- Fault at the shortest distance from the PHY (open, short, cross pair short).

- In case of a tie in distance, open and short has higher priority than cross pair short.
- Cable good

When a pair is reported as good, the value in its corresponding cable length register is invalid.

Register 21_7.10 selects how the cable length is to be presented – in meters or centimeters. Note that register 21_7.10 should not be change in the middle of a VCT test. Once the testing is complete and cable length values written into registers 16_7, 17_7, 18_7, and 19_7, the values will not change when register 21_7.10 changes. Changes to 21_7.10 will only take effect the next time VCT is started.

Table 70: Alternate VCT™ Control

Register	Function	Setting	Mode
16_7.15:0	Pair 0 Cable Length	Length to fault in meters or centimeters based on register 21_7.10.	RO
17_7.15:0	Pair 1 Cable Length	Length to fault in meters or centimeters based on register 21_7.10.	RO
18_7.15:0	Pair 2 Cable Length	Length to fault in meters or centimeters based on register 21_7.10.	RO
19_7.15:0	Pair 3 Cable Length	Length to fault in meters or centimeters based on register 21_7.10.	RO
20_7.15:12	Pair 3 Fault Code	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved	RO
20_7.11:8	Pair 2 Fault Code	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved	RO
20_7.7:4	Pair 1 Fault Code	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved	RO
20_7.3:0	Pair 0 Fault Code	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy else = Reserved	RO
21_7.15	Run Immediately	0 = No Action 1 = Run VCT Now	R/W, SC

Table 70: Alternate VCT™ Control (Continued)

Register	Function	Setting	Mode
21_7.14	Run at each Auto-Negotiation Cycle	0 = Do No Run At Auto-Negotiation Cycle 1 = Run At Auto-Negotiation Cycle	R/W
21_7.13	Disable Cross Pair Check	0 = Enable Cross Pair Check 1 = Disable Cross Pair Check	R/W
21_7.12	Run After Break Link	0 = No Action 1 = Run VCT After Breaking Link	R/W, SC
21_7.11	Cable Diagnostics Status	0 = Complete 1 = In Progress	RO
21_7.10	Cable Length Unit	0 = Centimeters 1 = Meters	R/W

2.15 Data Terminal Equipment (DTE) Detect

The device supports the Data Terminal Equipment (DTE) power function. The DTE power function is used to detect if a link partner requires power supplied by the POE PSE device.

The DTE power function can be enabled by writing to register 26_0.8. When DTE is enabled, the device will first monitor for any activity transmitted by the link partner. If the link partner is active, then the link partner has power and power from the POE PSE device is not required. If there is no activity coming from the link partner, DTE power engages, and special pulses are sent to detect if the link partner requires DTE power. If the link partner has a low pass filter (or similar fixture) installed, the link partner will be detected as requiring DTE power.

The DTE power status register (Register 17_0.2) immediately comes up as soon as link partner is detected as a device requiring DTE power. Register 19_0.2 is a stray bit that reports the DTE power status has changed states.

If a link partner that requires DTE power is unplugged, the DTE power status (register 17_0.2) will drop after a user controlled delay (default is 20 seconds - Register 26_0.7:4) to avoid DTE power status register drop during the link partner powering up (for most applications), since the low pass filter (or similar fixture) is removed during power up. If DTE power status drop is desired to be reported immediately, write register 26_0.7:4 to 4'b0000.

A detailed description of the register bits used for DTE power detection for the device are shown in [Table 71](#).

Table 71: Registers for DTE Power

Register	Description
26_0.8 - Enable power over Ethernet detection	1 = Enable DTE detect 0 = Disable DTE detect A soft reset is required to enable this feature HW reset: 0 SW reset: Update
17_0.2 - Power over Ethernet detection status	1 = Need power 0 = Do not need power HW reset: 0 SW reset: 0
19_0.2 - Power over Ethernet detection state changed	1 = Changed 0 = No change HW reset: 0 SW reset: 0
26_0.7:4 - DTE detect status drop	Once the PHY no longer detects that the link partner filter, the PHY will wait a period of time before clearing the power over Ethernet detection status bit (17_0.2). The wait time is 5 seconds multiplied by the value of these bits. Example: (5 * 0x4 = 20 seconds) Default at HW reset: 0x4 At SW reset: retain

2.16 Energy Efficient Ethernet (EEE)

The device implements Energy Efficient Ethernet (EEE) functions based on IEEE 802.3az. The device supports EEE on the following System and Media Interfaces:

- 10BASE-T_e
- 100BASE-TX EEE
- 1000BASE-T EEE
- 1000BASE-X/SGMII EEE
- QSGMII EEE

The EEE registers are defined in Clause 22 Page 18 registers and Clause 45 XMDIO space. Refer to “PHY XMDIO Register Description” on page 226 for details.

2.16.1 Energy Efficient Ethernet Low Power Modes

There are two EEE modes supported: master (legacy) and slave (EEE-aware).



Note

The slave and the Master mode EEE operation must not be confused with the Master and Slave mode operation of 1000BASE-T.

2.16.2 Master (Legacy) mode

The EEE Master (Legacy) mode is enabled by setting Reg 0_18.0 to '1'. In this mode, the phy assumes that the system and the external MAC are not aware of EEE. The MAC and the system are completely transparent to the EEE operation. In this mode, the EEE buffer is enabled and used to store data from the MAC when the PHY media interface is preparing to leave from the Low Power Idle (LPI) mode. The buffer basically ensures that none of the packets are lost by the PHY during the transition from a low power state to normal operation. Once the media interface exits the LPI mode, the data in the buffer is sent out through the media transmit side. The phy decides when to go to Low Power Idle (LPI) mode based on the buffer level. The phy does not expect to see the LPI Idle (LPI) code-groups on the system interface. If the external MAC sends the LPI Idle code-group, it will be ignored.

The EEE buffer has enter timer and exit timer defined. The enter timer and exit timer settings are available in Reg 1_18 and 2_18. When the buffer is empty, the enter timer will be started. If there is any packet received before the enter timer expires, the timer will be restarted. When the buffer remains empty until the enter timer expires, it will enter the LPI mode and transmits the LPI signals. While it is in LPI mode, it will stay in LPI mode until the buffer is not. As soon as the buffer is not empty, the exit timer is started and the phy initiates a wake signal to the link partner to indicate that the data will be transmitted shortly. The phy can also wake from LPI mode if it receives the wake signal from the link partner. When the exit timer expires, it will exit the LPI mode and resume normal transmission.

2.16.3 Slave mode

By default the phy is configured in EEE Slave mode (Reg 0_18.0 = 0). In the EEE Slave mode, the external MAC connected to the system interface must be EEE-capable and meets the IEEE 802.3az clause 78 requirements. In this mode, the EEE buffering is disabled and EEE enter/exit timers settings are ignored. The MAC is expected to buffer the packets while the phy transitions from the LPI mode to normal mode. The MAC is also responsible to initiate the low power mode by sending the LPI idles (to initiate LPI mode) or normal idles (to exit the LPI mode). The phy will pass through the LPI idles from the system interface to the media interface and vice versa.

2.16.4 Energy Efficient Ethernet (EEE) Auto-Negotiation

In order for the EEE to work, both the local PHY and its link partner needs to support EEE. The 100/1000BASE-T EEE capabilities are exchanged through standard 10/100/1000BASE-T auto-negotiation (IEEE 802.3 clauses 28 and 40). These capabilities are exchanged through the Next Page exchanges. The auto-negotiation process is used only for the exchange of speed and duplex information and not any timer information with regards to the sleep, refresh, and wake cycles.

10BASE-Te capability is not part of 10/100/1000BASE-T Auto-Negotiation. 10BASE-Te can be enabled by writing Reg 0_20.7 = '1'. When the 10BASE-Te is enabled, the copper media transmit amplitude is reduced to save some power consumption.

The 1000BASE-X, SGMII, and QSGMII PCS are modified to support low power idle code groups /LI1/ and /LI2/ ordered sets. The SGMII auto-negotiation tx_config_reg contains additional two bits to communicate EEE statuses through in-band SGMII auto-negotiation (See Table 67 Enhanced SGMII PHY Status).

2.17 CRC Error Counter and Frame Counter

The CRC counter and frame counters, normally found in MACs, are available in the device. The error counter and frame counter features are enabled through register writes and each counter is stored in eight register bits.

Register 18_18.2:0 controls which path the CRC checker and packet counter is counting.

If register 18_18.2:0 is set to 010 then the Copper receive path is checked.

If register 18_18.2:0 is set to 100 then the SGMII/Fiber input path is checked.

If register 18_18.2:0 is set to 110 then the QSGMII input path is checked.

2.17.1 Enabling The CRC Error Counter and Frame Counter

To enable the counters to count, set register 18_18.2:0 to a non-zero value. If the counters are enabled while receiving any packets, the packet may be counted as an error packet. It is recommended to clear the counters after the counters are enabled.

To disable the counters, set register 18_18.2:0 to 000.

To read the CRC counter and frame counter, read register 17_18.

17_18.15:8 (Frame count is stored in these bits)

17_18.7:0 (CRC error count is stored in these bits)

The CRC counter and frame counter do not clear on a read command.

To clear the counters, write Register 18_18.4 = 1. The register 18_18.4 is a self-clear bit. Disabling the counters by writing register 18_18.2:0 to 000 will also reset the counters.

2.18 Packet Generator

The device contains a very simple packet generator. Table 222 lists the device Packet Generator register details.

The packet generator is enabled when:

Register 16_18.7:5 controls which path the packet generator is connected to.

If register 16_18.7:5 is set to 010 then the input into the SGMII/Fiber or the QSGMII is ignored and the packet is generated onto the copper transmit path.

If register 16_18.7:5 is set to 100 then the copper receiver or the QSGMII is ignored and the packet is generated onto the SGMII/Fiber output path.

If register 16_18.7:5 is set to 110 then the copper receiver or the SGMII/Fiber is ignored and the packet is generated onto the QSGMII output path.

Once enabled, a fixed length packet of 64 or 1518 byte frame (including CRC) will be transmitted separated by 12 bytes of IPG the inter-packet-gap (IPG). The length of the IPG between the packets can be programmed (by default the IPG is set to 12 bytes). The preamble length will be 8 bytes. The payload of the frame is either a fixed 5A, A5, 5A, A5 pattern or a pseudo random pattern. A correct IEEE CRC is appended to the end of the frame. An error packet can also be generated.

The registers are as follows:

16_18.7:5 Packet generator enable. 000 = Normal operation. Else = Enable internal packet generator

16_18.4 Packet generator trigger/status. 0 = Packet Generator is transmitting packets. 1 = Transmission is done. Writing '0' when this bit is '1' will retrigger the packet generator to send another burst of packets.

16_18.3 Packet generator self clear control. 0 = Resume normal operation after all packets are sent. 1 = Stay in packet generator mode after all packets are sent.

16_18.2 Payload type. 0 = Pseudo random. 1 = Fixed 5A, A5, 5A, A5,...

16_18.1 Packet length. 0 = 64 bytes. 1 = 1518 bytes

16_18.0 Error packet. 0 = Good CRC. 1 = Symbol error and corrupt CRC.

16_18.15:8 Packet Burst Size. 0x00 = Continuous. 0x01 to 0xFF = Burst 1 to 255 packets.

19_18.7:0 IPG Length + 1 (in bytes). Default is 12 bytes.

If register 16_18.15:8 is set to a non-zero value (to send burst packets), the register 16_18.7:5 packet generator behavior is controlled by register 16_18.4:3. If register 16_18.3 is set to '0', register 16_18.7:5 will self clear once the required numbers of packets are generated. Note that if register 16_18.7:5 is manually set to 0 while packets are still bursting, the bursting will cease immediately once the current active packet finishes transmitting. The value in register 16_18.15:8 should not be changed while register 16_18.7:5 is set to a non-zero value. If register 16_18.3 is set to '1', register 16_18.7:5 will retain the value and the packet generator will stay active. Normal packets that sent towards the direction of the packet generator are transmitting will be blocked until the packet generator control is released. As an example, if the copper packet generator is enabled, any packets sent from the SGMII/QSGMII interface to the copper interface will be blocked. Register 16_18.4 indicates the status of the packet generator transmission. When register 16_18.4 is '1', writing '0' will trigger the packet generator to send another burst packets.

2.19 RX_ER Byte Capture

Whenever there is an RX_ER in the internal GMII interface the PHY will capture 4 bytes before the RX_ER is asserted. Once the bytes preceding the RX_ER assertion are captured into the registers, they will not be over written by new errors and they will only be cleared after the registers are read.

There are two sets of RX_ER capture registers. One captures the receive path of the copper/fiber path. The other captures the receive path of the QSGMII. These capture registers are always running.

The one in the copper/fiber path is accessed via register 26_18. The one in the QSGMII is accessed via register 20_4. The description below applies to both the copper/fiber path and the QSGMII path but we will refer to register 26_18 only. Register 20_4 should be used when accessing the QSGMII path.

Once an error event is captured register 26_18.15 is set to 1 indicating that the capture data is valid. No further errors are captured until all captured registers are read. Register 26_18.13:12 is set to 00. Register 26_18.9:0 outputs the byte that is the earliest received. Once register 26_18 is read register 26_18.13:12 increments and register 26_18.9:0 is updated with the next earliest byte. The register is incremented and byte updated until the fourth read occurs. After the fourth read to register 26_18 is completed, register 26_18.15 is set to 0 and the error capturing resumes four RX_CLK cycles after the final read is completed. The 4 RX_CLK cycle delay is required to insure that the register has 4 valid bytes loaded prior to being frozen. Note that a side effect of doing this is the RX_ER may be high in the captured bytes.

Table 72: Error Byte Capture

Register	Function	Setting
26_18.15	Capture Data Valid	1 = Bits 14:0 Valid 0 = Bits 14:0 Invalid
26_18.13:12	Byte Number	00 = 4 bytes before RX_ER asserted 01 = 3 bytes before RX_ER asserted 10 = 2 bytes before RX_ER asserted 11 = 1 byte before RX_ER asserted The byte number increments after every read when register 26_18.15 is set to 1.
26_18.9	RX_ER	RX Error. Normally this bit will be low since the capture is triggered by RX_ER being high. However, it is possible to see an RX_ER high when the capture is re-enabled after reading the fourth byte and there happens to be a long sequence of RX_ER when the capture restarts.
26_18.8	RX_DV	RX Data Valid
26_18.7:0	RXD[7:0]	RX Data

2.20 QSGMII PRBS Generator and Checker

A PRBS generator and checker are available for use on the QSGMII. PRBS7, PRBS23, and PRBS31 are supported.

An alternating 101010.... pattern generator is also available. When set to this mode the checker function is not supported.

A 32-bit checker is implemented. Note that the reads are atomic. A read to the LSB will update the MSB register. The counters only clear when register 23_4.4 is set to 1. This bit self clears.

The checker and generator polarity can be inverted by setting registers 23_4.7 and 23_4.6 respectively.

Register 23_4.5 controls whether the checker has to lock before counting commences.

Table 73: QSGMII PRBS Registers

Register	Function	Setting
23_4.7	Invert Checker Polarity	0 = Invert 1 = Normal
23_4.6	Invert Generator Polarity	0 = Invert 1 = Normal
23_4.5	PRBS Lock	0 = Counter Free Runs 1 = Do not start counting until PRBS locks first
23_4.4	Clear Counter	0 = Normal 1 = Clear Counter
23_4.3:2	Pattern Select	00 = PRBS 7, $x^7 + x^6 + 1 = 0$ 01 = PRBS 23, $x^{23} + x^{18} + 1 = 0$ 10 = PRBS 31, $x^{31} + x^{28} + 1 = 0$ 11 = Generate 1010101010... pattern
23_4.1	PRBS Checker Enable	0 = Disable 1 = Enable
23_4.0	PRBS Generator Enable	0 = Disable 1 = Enable
24_4.15:0	PRBS Error Count LSB	A read to this register freezes register 25_4. Cleared only when register 23_4.4 is set to 1.
25_4.15:0	PRBS Error Count MSB	This register does not update unless register 24_4 is read first. Cleared only when register 23_4.4 is set to 1.

2.21 1.25G PRBS Generator and Checker

A PRBS generator and checker are available for use on the 1.25G SERDES. PRBS7 is supported.

A 32-bit checker is implemented. Note that the reads are atomic. A read to the LSB will update the MSB register. The counters only clear when register 23_1.4 is set to 1. This bit self clears.

The checker and generator polarity can be inverted by setting registers 23_1.7 and 23_1.6 respectively.

Register 23_1.5 controls whether the checker has to lock before counting commences.

Table 74: 1.25 GHz SERDES PRBS Registers

Register	Function	Setting
23_1.7	Invert Checker Polarity	0 = Normal 1 = Invert
23_1.6	Invert Generator Polarity	0 = Normal 1 = Invert
23_1.5	PRBS Lock	0 = Counter Free Runs 1 = Do not start counting until PRBS locks first
23_1.4	Clear Counter	0 = Normal 1 = Clear Counter
23_1.3:2	Pattern Select	00 = PRBS 7, $x^7 + x^6 + 1 = 0$ 01 = PRBS 23, $x^{23} + x^{18} + 1 = 0$ 10 = PRBS 31, $x^{31} + x^{28} + 1 = 0$ 11 = Generate 1010101010... pattern
23_1.1	PRBS Checker Enable	0 = Disable 1 = Enable
23_1.0	PRBS Generator Enable	0 = Disable 1 = Enable
24_1.15:0	PRBS Error Count LSB	A read to this register freezes register 25_1. Cleared only when register 23_1.4 is set to 1.
25_1.15:0	PRBS Error Count MSB	This register does not update unless register 24_1 is read first. Cleared only when register 23_1.4 is set to 1.

2.22 MDI/MDIX Crossover

The device automatically determines whether or not it needs to cross over between pairs as shown in Table 75 so that an external crossover cable is not required. If the device interoperates with a device that cannot automatically correct for crossover, the device makes the necessary adjustment prior to commencing Auto-Negotiation. If the device interoperates with a device that implements MDI/MDIX crossover, a random algorithm as described in IEEE 802.3 clause 40.4.4 determines which device performs the crossover.

When the device interoperates with legacy 10BASE-T devices that do not implement Auto-Negotiation, the device follows the same algorithm as described above since link pulses are present. However, when interoperating with legacy 100BASE-TX devices that do not implement Auto-Negotiation (i.e. link pulses are not present), the device uses signal detect to determine whether or not to crossover.

The auto MDI/MDIX crossover function can be disabled via register 16_0.6.5.

The pin mapping in MDI and MDIX modes is shown in Table 75.

Table 75: Media Dependent Interface Pin Mapping

Pin	MDI			MDIX		
	1000BASE-T	100BASE-TX	10BASE-T	1000BASE-T	100BASE-TX	10BASE-T
MDIP/N[0]	BI_DA±	TX±	TX±	BI_DB±	RX±	RX±
MDIP/N[1]	BI_DB±	RX±	RX±	BI_DA±	TX±	TX±
MDIP/N[2]	BI_DC±	unused	unused	BI_DD±	unused	unused
MDIP/N[3]	BI_DD±	unused	unused	BI_DC±	unused	unused

Note: Table 75 assumes no crossover on PCB.

The MDI/MDIX status is indicated by Register 17_0.6. This bit indicates whether the receive pairs (3,6) and (1,2) are crossed over. In 1000BASE-T operation, the device can correct for crossover between pairs (4,5) and (7,8) as shown in Table 75. However, this is not indicated by Register 17_0.6.

If 1000BASE-T link is established, pairs (1,2) and (3,6) crossover is reported in register 21_5.4, and pairs (4,5) and (7,8) crossover is reported in register 21_5.5.

2.23 Unidirectional Transmit

IEEE 802.3ah requires OAM support with unidirectional transmit capability. Unidirectional transmit allows a PHY to transmit data when the PHY does not have link due to potential issues on the receive path. IEEE 802.3ah formally requires two bits for this capability. Register 0.5 enables this capability, and 1.7 advertises this ability. This ability only applies to 100BASE-TX or 1000BASE-X. It doesn't apply to 1000BASE-T since 1000BASE-T requires MASTER/SLAVE relationship and training with both link partners participating, which requires that link exists for any data transmit.

The device can support transmit of packets when there is no link by using register bit 16_0.10 = 1 (Force Copper Link Good) and 16_1.10 = 1 (Force Fiber Link Good). This is not the official bit specified by the IEEE 802.3ah but serves the same function.

2.24 Polarity Correction

The device automatically corrects polarity errors on the receive pairs in 1000BASE-T and 10BASE-T modes. In 100BASE-TX mode, the polarity does not matter.

In 1000BASE-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the descrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10BASE-T mode, polarity errors are corrected based on the detection of validly spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10BASE-T link is up. The polarity becomes unlocked when link is down.

The polarity correction status is indicated by Register 17_0.1. This bit indicates whether the receive pair (3,6) is polarity reversed in MDI mode of operation. In MDIX mode of operation, the receive pair is (1,2) and Register 17_0.1 indicates whether this pair is polarity reversed. Although all pairs are corrected for receive polarity reversal, Register 17_0.1 only indicates polarity reversal on the pairs described above.

If 1000BASE-T link is established register 21_5.3:0 reports the polarity on all 4 pairs.

Polarity correction can be disabled by register write 16_0.1 = 1. Polarity will then be forced in normal 10BASE-T mode.

2.25 FLP Exchange Complete with No Link

Sometimes when link does not come up, it is difficult to determine whether the failure is due to the auto-negotiation Fast Link Pulse (FLP) not completing or from the 10/100/1000BASE-T link not being able to come up.

Register 19_0.3 is a sticky bit that gets set to 1 whenever the FLP exchange is completed but the link cannot be established for some reason. Once the bit is set, it can be cleared only by reading the register.

This bit will not be set if the FLP exchange is not completed, or if link is established.

2.26 Duplex Mismatch Indicator

When operating in half-duplex mode collisions should occur within the first 512 bit time. Collisions that are detected after this point can indicate an incorrect environment (too many repeaters in the system, too long cable) or it can indicate that the link partner thinks the link is a full-duplex link.

Registers 23_6.7:0, 23_6.15:8, 24_6.7:0, and 24_6.15:8 are 8 bit counters that count late collisions.

They will increment only when the PHY is in half-duplex mode and only applies to the copper interface.

Each counter increments when a late collision is detected in a certain window as shown in Table 76. The four late collision counters will increment based on when the late collision starts. The counters clear on read. If the counter reaches FF it will not roll over.

Table 76: Late Collision Registers

Register	Function	Setting	Mode
23_6.15:8	Late Collision 97-128 bytes	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 96th to 128th bytes of the packet are transmitted.	RO, SC
		The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.	
23_6.7:0	Late Collision 65-96 bytes	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 65th to 96th bytes of the packet are transmitted.	RO, SC
		The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.	
24_6.15:8	Late Collision >192 bytes	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received after 192 bytes of the packet are transmitted.	RO, SC
		The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.	
24_6.7:0	Late Collision 129-192 bytes	This counter increments by 1 when the PHY is in half-duplex and a start of packet is received while the 129th to 192nd bytes of the packet are transmitted.	RO, SC
		The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.	
25_6.12:8	Late Collision Window Adjust	Number of bytes to advance in late collision window. 0 = start at 64th byte, 1 = start at 63rd byte, etc.	R/W

The real point of measurement for late collision should be done at the MAC and not at the PHY. In order to compensate for additional latency between the PHY and the MAC register 25_6.12:8 is used to move the window earlier. For example, if register 25_6.12:8 is set to 2 then the first window is 63 to 94 bytes, the second window is 95 to 129 bytes, etc. It is up to the user to program this register correctly since it is system dependent.

2.27 Link Disconnect Counter

The link disconnect counter increments every time the link transitions from up to down. This applies regardless of whether the link is a copper link or fiber link. Note that this counter will not increment if the link is QSGMII (MODE[2:0] = 101).

Register 25_18.7:0 is used as the counter. It clears on read and will not roll over when it reaches 0xFF.

2.28 LED

The LED[3:0] pins can be used to drive LED pins. Registers 16_3, 17_3, 18_3, and 19_3 controls the operation of the LED pins. LED[3:0] are used to configure the PHY per [Section 2.31.1, Hardware Configuration, on page 138](#). After the configuration is completed, LED[3:0] will operate per this section.

The LED[2] pin outputs either the LED[2] function or the LED[4] function. Register 19_3.14 controls the selection.

The LED[3] pin outputs either the LED[3] function or the LED[5] function. Register 19_3.15 controls the selection.

The LED[4] and LED[5] pins do not exist.

In general, 19_3.7:4 controls the LED[5] function, 19_3.3:0 controls the LED[4] function, 16_3.15:12 controls the LED[3] function, 16_3.11:8 controls the LED[2] function, 16_3.7:4 controls the LED[1] function, and 16_3.3:0 controls the LED[0] function. These are referred to as single LED modes.

However, there are some LED modes where LED[5:4] function operates as a unit, LED[3:2] function operates as a unit and LED[1:0] operate as a unit. These are entered when 19_3.3:2 is set to 11, 16_3.11:10 is set to 11, or 16_3.3:2 is set to 11 respectively. These are referred to as dual LED modes. In dual LED modes, register 19_3.7:4 have no meaning when 19_3.3:2 is set to 11, 16_3.15:12 have no meaning when 16_3.11:10 is set to 11, and 16_3.7:4 have no meaning when 16_3.3:2 is set to 11.

The LED reports the status of the active media interface i.e., copper or fiber.

[Figure 28](#) shows the general chaining of function for the LEDs. The various functions are described in the following sections.

Figure 28: LED Chain

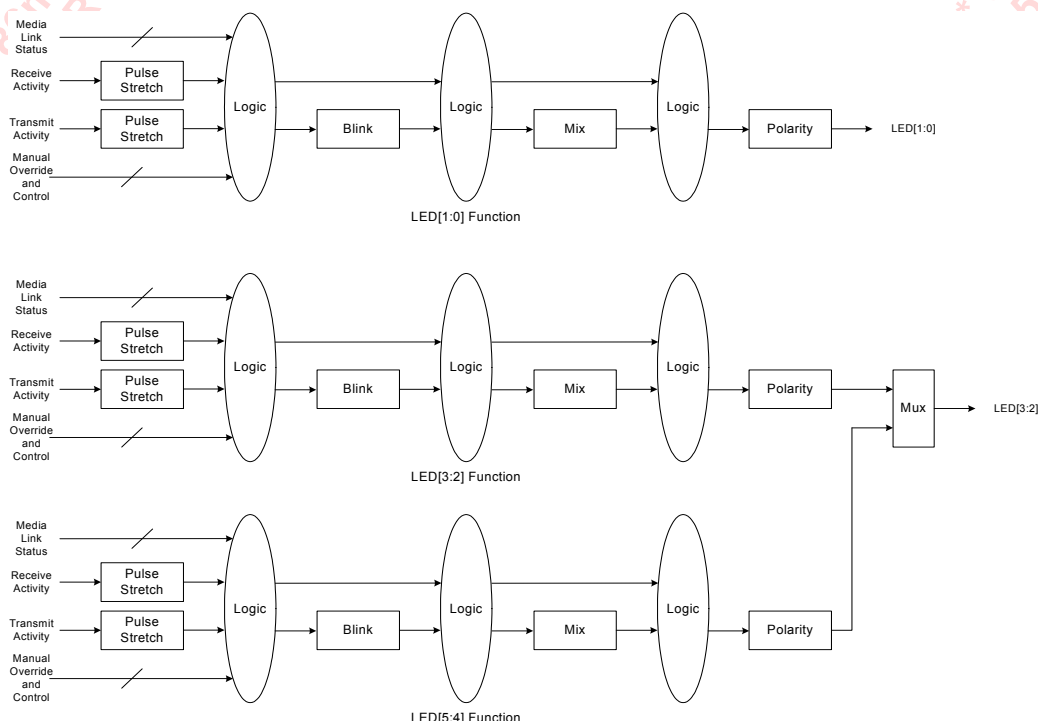


Table 77: LED[3:2] Functional Pin Mapping

Register	LED Pin	Definition
19_3.15	LED[3]	0 = Output LED[3] function to LED[3] pin 1 = Output LED[5] function to LED[3] pin
19_3.14	LED[2]	0 = Output LED[2] function to LED[2] pin 1 = Output LED[4] function to LED[2] pin

2.28.1 LED Polarity

There are a variety of ways to hook up the LEDs. Some examples are shown in Figure 29. In order to make things more flexible registers 19_3.11:10, 19_3.9:8, 17_3.7:6, 17_3.5:4, 17_3.3:2, and 17_3.1:0 specify the output polarity for the LED[5:0] function. The lower bit of each pair specifies the on (active) state of the LED, either high or low. The upper bit of each pair specifies whether the off state of the LED should be driven to the opposite level of the on state or Hi-Z. The Hi-Z state is useful in cases such the LOS and INIT function where the inactive state is Hi-Z.

Figure 29: Various LED Hookup Configurations

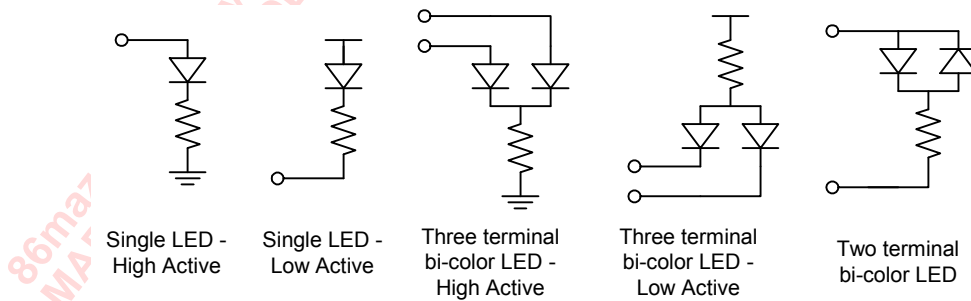


Table 78: LED Polarity

Register	LED Function	Definition
19_3.11:10	LED[5]	00 = On - drive LED[5] low, Off - drive LED[5] high 01 = On - drive LED[5] high, Off - drive LED[5] low 10 = On - drive LED[5] low, Off - tristate LED[5] 11 = On - drive LED[5] high, Off - tristate LED[5]
19_3.9:8	LED[4]	00 = On - drive LED[4] low, Off - drive LED[4] high 01 = On - drive LED[4] high, Off - drive LED[4] low 10 = On - drive LED[4] low, Off - tristate LED[4] 11 = On - drive LED[4] high, Off - tristate LED[4]
17_3.7:6	LED[3]	00 = On - drive LED[3] low, Off - drive LED[3] high 01 = On - drive LED[3] high, Off - drive LED[3] low 10 = On - drive LED[3] low, Off - tristate LED[3] 11 = On - drive LED[3] high, Off - tristate LED[3]
17_3.5:4	LED[2]	00 = On - drive LED[2] low, Off - drive LED[2] high 01 = On - drive LED[2] high, Off - drive LED[2] low 10 = On - drive LED[2] low, Off - tristate LED[2] 11 = On - drive LED[2] high, Off - tristate LED[2]

Table 78: LED Polarity

Register	LED Function	Definition
17_3.3:2	LED[1]	00 = On - drive LED[1] low, Off - drive LED[1] high 01 = On - drive LED[1] high, Off - drive LED[1] low 10 = On - drive LED[1] low, Off - tristate LED[1] 11 = On - drive LED[1] high, Off - tristate LED[1]
17_3.1:0	LED[0]	00 = On - drive LED[0] low, Off - drive LED[0] high 01 = On - drive LED[0] high, Off - drive LED[0] low 10 = On - drive LED[0] low, Off - tristate LED[0] 11 = On - drive LED[0] high, Off - tristate LED[0]

2.28.2 Pulse Stretching and Blinking

Register 18_3.14:12 specifies the pulse stretching duration of a particular activity. Only the transmit activity, receive activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

Some status will require blinking instead of a solid on. Register 18_3.10:8 specifies the blink rate. Note that the pulse stretching is applied first and the blinking will reflect the duration of the stretched pulse.

The stretched/blinked output will then be mixed if needed ([Section 2.28.3](#)) and then inverted/Hi-Z according to the polarity described in section ([Section 2.28.1](#))

Table 79: Pulse Stretching and Blinking

Register	LED Function	Definition
18_3.14:12	Pulse stretch duration	000 = No pulse stretching 001 = 21 ms to 42 ms 010 = 42 ms to 84 ms 011 = 84 ms to 170 ms 100 = 170 ms to 340 ms 101 = 340 ms to 670 ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
18_3.10:8	Blink Rate	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved

2.28.3 Bi-Color LED Mixing

In the dual LED modes the mixing function allows the 2 colors of the LED to be mixed to form a third color. This is useful since the PHY is tri speed and the three colors each represent one of the speeds. Register 17_3.15:12 control the amount to mix in the LED[5], LED[3], and LED[1] pins. Register 17_3.11:8 control the amount to mix in the LED[4], LED[2], and LED[0] pins. The mixing is determined by the percentage of time the LED is on during the active state. The percentage is selectable in 12.5% increments.

Note that there are two types of bi-color LEDs: three terminal type, and two terminal type. For example, the third and fourth LED block from the left in Figure 29 illustrates three terminal types, and the one on the far right is the two terminal type. In the three terminal type both of the LEDs can be turned on at the same time. Hence the sum of the percentage specified by 17_3.15:12 and 17_3.11:8 can exceed 100%. However, in the two terminal type the sum should never exceed 100% since only one LED can be turned on at any given time.

The mixing only applies when register 19_3.3:0, 16_3.11:8 or 16_3.3:0 are set to 11xx. There is no mixing in single LED modes.

Table 80: Bi-Color LED Mixing

Register	LED Function	Definition
17_3.15:12	LED[5], LED[3], LED[1] mix percentage	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5% . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
17_3.11:8	LED[4], LED[2], LED[0] mix percentage	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0% 0001 = 12.5%, . . . 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved

2.28.4 Modes of Operation

The LED pins relay some modes of the PHY so that these modes can be displayed by the LEDs. Most of the single LED modes are self-explanatory from the register map of register 16_3. We will cover the non-obvious ones in this section.

Table 81: Modes of Operation

Register	LED Function	Definition
19_3.7:4	LED[5] Control	<p>If 19_3.3:2 is set to 11 then 19_3.7:4 has no effect</p> <p>0000 = On - Receive, Off - No Receive</p> <p>0001 = On - Link, Blink - Activity, Off - No Link</p> <p>0010 = On - Link, Blink - Receive, Off - No Link</p> <p>0011 = On - Activity, Off - No Activity</p> <p>0100 = Blink - Activity, Off - No Activity</p> <p>0101 = On - Transmit, Off - No Transmit</p> <p>0110 = On - Full-duplex, Off - Half-duplex</p> <p>0111 = On - Full-duplex, Blink - Collision Off - Half-duplex</p> <p>1000 = Force Off</p> <p>1001 = Force On</p> <p>1010 = Force Hi-Z</p> <p>1011 = Force Blink</p> <p>11xx = Reserved</p>
19_3.3:0	LED[4] Control	<p>0000 = On - Receive, Off - No Receive</p> <p>0001 = On - Link, Blink - Activity, Off - No Link</p> <p>0010 = On - Link, Blink - Receive, Off - No Link</p> <p>0011 = On - Activity, Off - No Activity</p> <p>0100 = Blink - Activity, Off - No Activity</p> <p>0101 = On - Transmit, Off - No Transmit</p> <p>0110 = On - Full-duplex, Off - Half-duplex</p> <p>0111 = On - Full-duplex, Blink - Collision Off - Half-duplex</p> <p>1000 = Force Off</p> <p>1001 = Force On</p> <p>1010 = Force Hi-Z</p> <p>1011 = Force Blink</p> <p>1100 = MODE 1 (Dual LED mode)</p> <p>1101 = MODE 2 (Dual LED mode)</p> <p>1110 = MODE 3 (Dual LED mode)</p> <p>1111 = MODE 4 (Dual LED mode)</p>
16_3.15:12	LED[3] Control	<p>If 16_3.11:10 is set to 11 then 16_3.15:12 has no effect</p> <p>0000 = On - Fiber Link, Off - Else</p> <p>0001 = On - Link, Blink - Activity, Off - No Link</p> <p>0010 = On - Link, Blink - Receive, Off - No Link</p> <p>0011 = On - Activity, Off - No Activity</p> <p>0100 = Blink - Activity, Off - No Activity</p> <p>0101 = Reserved</p> <p>0110 = On - 10 Mbps or 1000 Mbps Master, Off - Else</p> <p>0111 = On - Full-duplex, Off - Half-duplex</p> <p>1000 = Force Off</p> <p>1001 = Force On</p> <p>1010 = Force Hi-Z</p> <p>1011 = Force Blink</p> <p>11xx = Reserved</p>

Table 81: Modes of Operation (Continued)

Register	LED Function	Definition
16_3.11:8	LED[2] Control	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = Reserved 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - 10/1000 Mbps Link, Off - Else 0111 = On - 10 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)
16_3.7:4	LED[1] Control	If 16_3.3:2 is set to 11 then 16_3.7:4 has no effect 0000 = On - Copper Link, Off - Else 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - 100 Mbps, Link or Fiber Link, Off - Else 0110 = On - 100/1000 Mbps Link, Off - Else 0111 = On - 100 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
16_3.3:0	LED[0] Control	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000 Mbps 2 blinks - 100 Mbps 1 blink - 10 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)

2.28.4.1 Compound LED Modes

Compound LED modes are defined in [Table 82](#).

Table 82: Compound LED Status

Compound Mode	Description
Activity	Transmit Activity OR Receive Activity
Copper Link	10BASE-T link OR 100BASE-TX Link OR 1000BASE-T Link
Link	Copper Link or Fiber Link

2.28.4.2 Speed Blink

When 16_3.3:0 is set to 0010 the LED[0] pin takes on the following behavior.

LED[0] outputs the sequence shown in [Table 83](#) depending on the status of the link. The sequence consists of 8 segments. If a 1000 Mbps link is established the LED[0] outputs 3 pulses, 100 Mbps 2 pulses, 10 Mbps 1 pulse, and no link 0 pulses. The sequence repeats over and over again indefinitely.

The odd numbered segment pulse duration is specified in 18_3.1:0. The even numbered pulse duration is specified in 18_3.3:2.

Table 83: Speed Blinking Sequence

Segment	10 Mbps	100 Mbps	1000 Mbps	No Link	Duration
1	On	On	On	Off	18_3.1:0
2	Off	Off	Off	Off	18_3.3:2
3	Off	On	On	Off	18_3.1:0
4	Off	Off	Off	Off	18_3.3:2
5	Off	Off	On	Off	18_3.1:0
6	Off	Off	Off	Off	18_3.3:2
7	Off	Off	Off	Off	18_3.1:0
8	Off	Off	Off	Off	18_3.3:2

Table 84: Speed Blink

Register	LED Function	Definition
18_3.3:2	Pulse Period for even segments	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
18_3.1:0	Pulse Period for odd segments	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

2.28.4.3 Manual Override

When 19_3.7:6, 19_3.3:2, 16_3.15:14, 16_3.11:10, 16_3.7:6, and 16_3.3:2 are set to 10 the LED[5:0] are manually forced. Registers 19_3.5:4, 19_3.1:0, 16_3.13:12, 16_3.9:8, 16_3.5:4, and 16_3.1:0 then select whether the LEDs are to be on, off, Hi-Z, or blink.

If bi-color LEDs are used, the manual override will select only one of the two colors. In order to get the third color by mixing, MODE 1 and MODE 2 should be used (Section 2.28.4.4).

2.28.4.4 MODE 1, MODE 2, MODE 3, MODE 4

MODE 1 to 4 are dual LED modes. These are used to mix a third color using bi-color LEDs.

When 19_3.3:0, 16_3.11:8 or 16_3.3:0 is set to 11xx then one of the 4 modes are enabled.

MODE 1 – Solid mixed color. The mixing is discussed in Section 2.28.3.

MODE 2 – Blinking mixed color. The mixing is discussed in Section 2.28.3. The blinking is discussed in section 2.28.2.

MODE 3 – Behavior according to Table 85.

MODE 4 – Behavior according to Table 86.

Note that MODE 4 is the same as MODE 3 except the 10 Mbps and 100 Mbps are reversed.

Table 85: MODE 3 Behavior

Status	LED[5] LED[3] LED[1]	LED[4] LED[2] LED[0]
1000 Mbps Link - No Activity	Off	Solid On
1000 Mbps Link - Activity	Off	Blink
100 Mbps Link - No Activity	Solid Mix	Solid Mix
100 Mbps Link - Activity	Blink Mix	Blink Mix
10 Mbps Link - No Activity	Solid On	Off
10 Mbps Link - Activity	Blink	Off
No link	Off	Off

Table 86: MODE 4 Behavior

Status	LED[5] LED[3] LED[1]	LED[4] LED[2] LED[0]
1000 Mbps Link - No Activity	Off	Solid On
1000 Mbps Link - Activity	Off	Blink
100 Mbps Link - No Activity	Solid On	Off
100 Mbps Link - Activity	Blink	Off
10 Mbps Link - No Activity	Solid Mix	Solid Mix
10 Mbps Link - Activity	Blink Mix	Blink Mix
No link	Off	Off

2.28.5 Behavior in Various Low Power States

When the PHY is in software reset, powered down, or the energy detect state, the LEDs are set to the inactive state in order to save power unless overridden by the user.

If the LED[x] control (Registers 16_3.11:8, 16_3.7:4, and 16_3.3:0 is set to 10xx (forced mode) then the LEDs will be forced regardless of the power state. This allows the user to have direct control over the LEDs. Note that the LED will not BLINK when the PHY is in low power state.

If the LED[x] control is not set to 10xx, then the LEDs will be forced off when the PHY is in the software reset, power down state or in the energy detect state. The off value for LED[x] is defined by the setting in registers 17_3.7:6, 17_3.5:4, 17_3.3:2, 17_3.1:0, 19_3.11:10, and 19_3.9:8.

When the PHY is in the powered up state and not in the energy detect state, the LED[x] will operate normally.

2.28.6 Random Blinking

Some status will require blinking instead of a solid on. When a multi-port device (or multiple parts) is used in a system, there is a phenomena where all the LED may be turned on and off at the same time. This is because all ports are getting the same reset and same configuration. The random LED blinking feature enables the LED blinking in a random fashion from port to port.

There are two parameters to control the LED blinking randomness; these two parameters would produce different visual LED blinking effects: the "Random Scale" and "Trigger Time Interval". These parameters are controlled by Register 28_3. The "Random Scale" can be programmed to 6.25%, 12.5%, 25%, and 50%. The higher random scale range would result in stronger randomness effects on LED blinking between ports. Each port generates a random number in certain period of time. The circuit only advances to the next random number when a timer expired. Within this period of time, each port's LED is turned on and off based on its random number. The "Trigger Time Interval" controls how often a random number get updated for each port. The "Trigger Time Interval" is blended with "Random Scale" setting to achieve another level of randomness. Even though all the ports are programmed to the same "Trigger Time interval" setting, the actual time period of advancing to the next random number will be different from port to port, that the port-to-port difference is controlled by "Random Scale" setting.

The random number is generated by a 15-TAP LFSR. The LFSR polynomial is automatically calculated by circuit upon reset. Advance users could overwrite the default calculated value with their polynomial by setting the register 29_3.

2.29 IEEE 1149.1 and 1149.6 Controller

The IEEE 1149.1 standard defines a test access port and boundary-scan architecture for digital integrated circuits and for the digital portions of mixed analog/digital integrated circuits. The IEEE 1149.6 standard defines a test access port and boundary-scan architecture for AC coupled signals.

This standard provides a solution for testing assembled printed circuit boards and other products based on highly complex digital integrated circuits and high-density surface-mounting assembly techniques.

The device implements the instructions shown in Table 87. Upon reset, ID_CODE instruction is selected. The PROG_HYST is a proprietary command used to adjust the test receiver hysteresis threshold. The instruction opcodes are shown in Table 87.

Table 87: TAP Controller Opcodes

Instruction	OpCode
EXTEST	00000000
SAMPLE/PRELOAD	00000001
CLAMP	00000010
HIGH-Z	00000011
ID_CODE	00000100
EXTEST_PULSE	00000101
EXTEST_TRAIN	00000110
PROG_HYST	00001000
BYPASS	11111111

The device reserves 5 pins called the Test Access Port (TAP) to provide test access: Test Mode Select Input (TMS), Test Clock Input (TCK), Test Data Input (TDI), and Test Data Output (TDO), and Test Reset Input (TRSTn). To ensure race-free operation all input and output data is synchronous with the test clock (TCK). TAP input signals (TMS and TDI) are clocked into the test logic on the rising edge of TCK, while output signal (TDO) is clocked on the falling edge. For additional details refer to the IEEE 1149.1 Boundary Scan Architecture document.

2.29.1 BYPASS Instruction

The BYPASS instruction uses the bypass register. This register contains a single shift-register stage and is used to provide a minimum length serial path between the TDI and TDO pins of the device when test operation is not required. This arrangement allows rapid movement of test data to and from other testable devices in the system.

2.29.2 SAMPLE/PRELOAD Instruction

The SAMPLE/PRELOAD instruction enables scanning of the boundary-scan register without causing interference to the normal operation of the device. Two functions are performed when this instruction is selected: sample and preload.

Sample allows a snapshot to be taken of the data flowing from the system pins to the on-chip test logic or vice versa, without interfering with normal operation. The snapshot is taken on the rising edge of TCK in the Capture-DR controller state, and the data can be viewed by shifting through the component's TDO output.

While sampling and shifting data out through TDO for observation, preload enables an initial data pattern to be shifted in through TDI and to be placed at the latched parallel output of the boundary-scan register cells that are connected to system output pins. This step ensures that known data is driven through the system output pins upon entering the extest instruction. Without preload,

indeterminate data would be driven until the first scan sequence is complete. The shifting of data for the sample and preload phases can occur simultaneously. While data capture is being shifted out, the preload data can be shifted in.

2.29.3 EXTEST Instruction

The EXTEST instruction enables circuitry external to the device (typically the board interconnections) to be tested. Prior to executing the EXTEST instruction, the first test stimulus to be applied is shifted into the boundary-scan registers using the sample/preload instruction. Thus, when the change to the extest instruction takes place, known data is driven immediately from the to its external connections. Note that the S_OUTP/N and Q_OUTP/N pins will be driven to static levels. The positive and negative legs of the S_OUTP/N and Q_OUTP/N pins are controlled via a single boundary scan cell. The positive leg outputs the level specified by the boundary scan cell while the negative leg outputs the opposite level.

2.29.4 The CLAMP Instruction

The CLAMP instruction enables the state of the signals driven from component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the component pins do not change while the clamp instruction is selected.

2.29.5 The HIGH-Z Instruction

The HIGH-Z instruction places all of the digital component system logic outputs in an inactive high-impedance drive state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

2.29.6 ID CODE Instruction

The ID CODE contains the manufacturer identity, part and version.

Table 88: ID CODE Instruction

Version	Part Number	Manufacturer Identity	
Bit 31 to 28	Bit 27 to 12	Bit 11 to 1	0
0000	0000000000101011	00111101001	1

2.29.7 EXTEST_PULSE Instruction

The AC or DC JTAG test modes can be selected for each port individually by scanning in the desired bit value into AC/DC select scan registers shown in the scan chain (Table 92 and Table 94). When the AC/DC select is set to DC the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_PULSE instruction has the same behavior as the EXTEST instruction except for the behavior of the S_OUTP/N and Q_OUTP/N pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction the S_OUTP and Q_OUTP pins output the level specified by the test stimulus and S_OUTN and S_CLKN pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state the S_OUTN and Q_OUTN pins output the level specified by the test stimulus and S_OUTP and Q_OUTP pins output the opposite level.

When the TAP controller exits the Run-Test/Idle state, the S_OUTP and Q_OUTP pins again output the level specified by the test stimulus and S_OUTN and Q_OUTN pins output the opposite level.

2.29.8 EXTEST_TRAIN Instruction

When the AC/DC select is set to DC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction.

When the AC/DC select is set to AC, the EXTEST_TRAIN instruction has the same behavior as the EXTEST instruction except for the behavior of the S_OUTP/N and Q_OUTP/N pins.

As in the EXTEST instruction, the test stimulus must first be shifted into the boundary-scan registers. Upon the execution of the EXTEST_PULSE instruction the S_OUTP and Q_OUTP pins output the level specified by the test stimulus and S_OUTN and Q_OUTN pins output the opposite level.

However, if the TAP controller enters into the Run-Test/Idle state the S_OUTP/N and Q_OUTP/N will toggle between inverted and non-inverted levels on the falling edge of TCK. This toggling will continue for as long as the TAP controller remains in the Run-Test/Idle state.

When the TAP controller exits the Run-Test/Idle state, the S_OUTP and Q_OUTP pins again output the level specified by the test stimulus and S_OUTN and Q_OUTN pins output the opposite level.

2.29.9 PROG_HYST Instruction

The test receivers connected to the S_INP/N and Q_INP/N pins requires the hysteresis level to be set according to the application that the SERDES is used in. The amount of hysteresis required is a function of the expected voltage swing on the input. The proprietary command PROG_HYST will program three registers in the tap controller which will set the value of the hysteresis.

When the PROG_HYST opcode is in the instruction register, the following actions occur in the following TAP controller states.

Capture-DR state: Load the value in HYST[2:0] into SR_HYST[2:0].

Shift-DR state: Shift TDI into SR_HYST[0], SR_HYST[1:0] into SR_HYST[2:1], and SR_HYST[2] to TDO. Three bits should be loaded to set the new test receiver hysteresis value.

Update-DR state: Load the value in SR_HYST[2:0] into HYST[2:0].

HYST[2:0] is the register that sets the hysteresis in the test receiver.

SR_HYST[2:0] is the 3 bit shift register used to shift the values in and out.

The hysteresis mapping is shown in Table 89. 70 mV is the default setting. When the TAP controller is in the Test-Logic-Reset state or when TRSTn is forced low, the HYST[2:0] is reset to the default state.

Table 89: Test Receiver Hysteresis Setting

HYST[2:0]	Hysteresis
000	12 mV
001	25 mV
010	50 mV
011	70 mV
100	90 mV
101	105 mV
110	135 mV
111	150 mV

2.29.10 AC-JTAG Fault Detection

The fault detection across AC coupled connections can be detected with a combination of (DC) EXTEST and any one of the AC JTAG commands. The AC coupled connection is shown in Figure 30. The fault signature is shown in Table 90. Column 1 lists the fault type.

Columns 2 to 5 lists the behavior when both the transmitter and receiver are running the EXTEST_TRAIN and EXTEST_PULSE commands. Column 2 shows the expected value captured by the boundary scan cell that is connected to the test receiver, which is connected to the positive input when a negative differential pulse is transmitted. Column 3 is the same as column 2 except for the negative input. Columns 4 and 5 are similar to columns 2 and 3 except a positive differential pulse is transmitted.

Columns 6 to 9 is similar to columns 2 to 5 except both the transmitter and receiver are running the (DC) EXTEST command.

While it is not possible to identify precisely which fault is occurring based on the fault signature, the signature to the no fault condition is unique when the (DC) EXTEST command is run with at least one of the EXTEST_TRAIN, or EXTEST_PULSE commands. Note that running only AC JTAG commands is not sufficient since the no fault condition signature is not distinguishable from the TX to RX short (see shaded cells in Table 90).

Figure 30: AC Coupled Connection

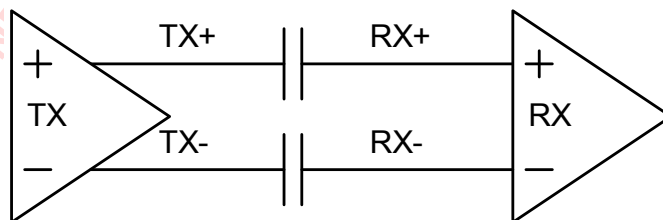


Table 90: AC Coupled Connection Fault Signature

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
TX+ Open	0	X	0	X	1	X	1	X
TX- Open	X	0	X	0	X	1	X	1
RX+ Open	0	X	0	X	1	X	1	X
RX- Open	X	0	X	0	X	1	X	1
TX+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
TX- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
RX+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
RX- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
TX+ short to ground	0	X	0	X	1	X	1	X
TX- short to ground	X	0	X	0	X	1	X	1
RX+ short to ground	0	X	0	X	0	X	0	X
RX- short to ground	X	0	X	0	X	0	X	0
TX+ short to TX-	Note 1	Note 1	Note 1	Note 1	1	1	1	1
RX+ short to RX-	Note 1	Note 1	Note 1	Note 1	1	1	1	1
TX+ short to RX-	X	0	X	1	X	0	X	1
TX- short to RX+	1	X	0	X	1	X	0	X
TX+ short to RX+	0	X	1	X	0	X	1	X
TX- short to RX-	X	1	X	0	X	1	X	0
No Fault	0	1	1	0	1	1	1	1
Note 1	Short on positive and negative leg can have several behavior on the test receiver. If both drivers cancel each other out then output on both legs is 0. If one driver dominates the other then both legs are either both 1 or both 0. In any case, the result is that both legs will have same value.							
Note 2	A solid short to power is assumed. If the short has high inductance then a pulse may still be sent at the receiver and will be mistaken as a good connection.							

The fault detection across DC coupled connections can be detected with any one of the AC JTAG or (DC) EXTEST commands. The DC coupled connection is shown in Figure 31. The fault signature is shown in Table 91.

Figure 31: DC Coupled Connection

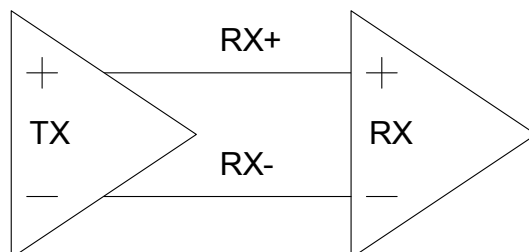


Table 91: DC Coupled Connection Fault Signature

DC Coupled Fault	AC Testing Sample 0		AC Testing Sample 1		(DC) EXTEST Sample 0		(DC) EXTEST Sample 1	
	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg	Positive Leg	Negative Leg
RX+ Open	0	X	0	X	1	X	1	X
RX- Open	X	0	X	0	X	1	X	1
RX+ short to power	0/Note 2	X	0/Note 2	X	1	X	1	X
RX- short to power	X	0/Note 2	X	0/Note 2	X	1	X	1
RX+ short to ground	0	X	0	X	0	X	0	X
RX- short to ground	X	0	X	0	X	0	X	0
RX+ short to RX-	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1	Note 1
No Fault	0	1	1	0	0	1	1	0
Note 1	Short on positive and negative leg can have several behaviors on the test receiver. If both drivers cancel each other out then output on both legs is 0. If one driver dominates the other then both legs are either both 1 or both 0. In any case, the result is that both legs will have same value.							
Note 2	A solid short to power is assumed. If the short has high inductance then a pulse may still be sent at the receiver and will be mistaken as a good connection.							

Table 92: 88E1545 Boundary Scan Chain Order

Pin	I/O
P3_LED[3]	Output
P3_LED[2]	Output
P3_LED[1]	Output
P3_LED[0]	Output
P3_LED[3]	Output Enable
P3_LED[2]	Output Enable
P3_LED[1]	Output Enable
P3_LED[0]	Output Enable
P2_LED[3]	Output
P2_LED[2]	Output
P2_LED[1]	Output
P2_LED[0]	Output
P2_LED[3]	Output Enable
P2_LED[2]	Output Enable
P2_LED[1]	Output Enable
P2_LED[0]	Output Enable
P1_LED[3]	Output
P1_LED[2]	Output
P1_LED[1]	Output
P1_LED[0]	Output
P1_LED[3]	Output Enable
P1_LED[2]	Output Enable
P1_LED[1]	Output Enable
P1_LED[0]	Output Enable
P0_LED[3]	Output
P0_LED[2]	Output
P0_LED[1]	Output
P0_LED[0]	Output
P0_LED[3]	Output Enable
P0_LED[2]	Output Enable
P0_LED[1]	Output Enable
P0_LED[0]	Output Enable
CONFIG[3]	Input
CONFIG[2]	Input
CONFIG[1]	Input
CONFIG[0]	Input

Table 92: 88E1545 Boundary Scan Chain Order (Continued)

Pin	I/O
MDC	Input
MDIO	Input
MDIO	Output
MDIO	Output Enable
RESETn	Input
CLK_SEL[1]	Input
CLK_SEL[0]	Input
RSVD (Reserved)	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
INTn	Output
INTn	Output Enable
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
Q_OUTN/Q_OUTP	Output Enable
Q_OUTN/Q_OUTP	Output
QSGMII AC/DC Select	AC/DC Select
Q_INP	Input
Q_INN	Input
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal

Table 92: 88E1545 Boundary Scan Chain Order (Continued)

Pin	I/O
RSVD	Internal
RSVD	Internal

Table 93: 88E1545 Boundary Scan Exclusion List

Pin	I/O
P0_MDIN_0	Analog
P0_MDIN_1	Analog
P0_MDIN_2	Analog
P0_MDIN_3	Analog
P0_MDIP_0	Analog
P0_MDIP_1	Analog
P0_MDIP_2	Analog
P0_MDIP_3	Analog
P1_MDIN_0	Analog
P1_MDIN_1	Analog
P1_MDIN_2	Analog
P1_MDIN_3	Analog
P1_MDIP_0	Analog
P1_MDIP_1	Analog
P1_MDIP_2	Analog
P1_MDIP_3	Analog
P2_MDIN_0	Analog
P2_MDIN_1	Analog
P2_MDIN_2	Analog
P2_MDIN_3	Analog
P2_MDIP_0	Analog
P2_MDIP_1	Analog
P2_MDIP_2	Analog
P2_MDIP_3	Analog
P3_MDIN_0	Analog
P3_MDIN_1	Analog
P3_MDIN_2	Analog
P3_MDIN_3	Analog
P3_MDIP_0	Analog
P3_MDIP_1	Analog
P3_MDIP_2	Analog

Table 93: 88E1545 Boundary Scan Exclusion List (Continued)

Pin	I/O
P3_MDIP_3	Analog
REF_CLKN	Analog
REF_CLKP	Analog
RSET	Analog
TEST_0	Analog
TEST_1	Analog
TSTPT	Analog
TSTPTF	Analog
V18_L	Analog
XTAL_IN	Analog
XTAL_OUT	Analog
HSDACN	Analog
HSDACP	Analog

Table 94: 88E1543 Boundary Scan Chain Order

Pin	I/O
P3_LED[3]	Output
P3_LED[2]	Output
P3_LED[1]	Output
P3_LED[0]	Output
P3_LED[3]	Output Enable
P3_LED[2]	Output Enable
P3_LED[1]	Output Enable
P3_LED[0]	Output Enable
P2_LED[3]	Output
P2_LED[2]	Output
P2_LED[1]	Output
P2_LED[0]	Output
P2_LED[3]	Output Enable
P2_LED[2]	Output Enable
P2_LED[1]	Output Enable
P2_LED[0]	Output Enable
P1_LED[3]	Output
P1_LED[2]	Output
P1_LED[1]	Output
P1_LED[0]	Output

Table 94: 88E1543 Boundary Scan Chain Order (Continued)

Pin	I/O
P1_LED[3]	Output Enable
P1_LED[2]	Output Enable
P1_LED[1]	Output Enable
P1_LED[0]	Output Enable
P0_LED[3]	Output
P0_LED[2]	Output
P0_LED[1]	Output
P0_LED[0]	Output
P0_LED[3]	Output Enable
P0_LED[2]	Output Enable
P0_LED[1]	Output Enable
P0_LED[0]	Output Enable
CONFIG[3]	Input
CONFIG[2]	Input
CONFIG[1]	Input
CONFIG[0]	Input
MDC	Input
MDIO	Input
MDIO	Output
MDIO	Output Enable
RESETn	Input
CLK_SEL[1]	Input
CLK_SEL[0]	Input
RSVD (Reserved)	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
INTn	Output
INTn	Output Enable
P3_S_OUTP/P3_S_OUTN	Output Enable
P3_S_OUTP/P3_S_OUTN	Output
P3_S_OUTN/P3_S_OUTN AC/DC Select	AC/DC Select
P3_S_INN	Input
P3_S_INP	Input
P2_S_OUTP/P2_S_OUTN	Output Enable
P2_S_OUTP/P2_S_OUTN	Output
P2_S_OUTN/P2_S_OUTN AC/DC Select	AC/DC Select

Table 94: 88E1543 Boundary Scan Chain Order (Continued)

Pin	I/O
P2_S_INN	Input
P2_S_INP	Input
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
P1_S_OUTP/P1_S_OUTN	Output Enable
P1_S_OUTP/P1_S_OUTN	Output
P1_S_OUTN/P1_S_OUTN AC/DC Select	AC/DC Select
P1_S_INN	Input
P1_S_INP	Input
P0_S_OUTP/P0_S_OUTN	Output Enable
P0_S_OUTP/P0_S_OUTN	Output
P0_S_OUTN/P0_S_OUTN AC/DC Select	AC/DC Select
P0_S_INN	Input
P0_S_INP	Input

Table 95: 88E1543 Boundary Scan Exclusion List

Pin	I/O
P0_MDIN_0	Analog
P0_MDIN_1	Analog
P0_MDIN_2	Analog
P0_MDIN_3	Analog
P0_MDIP_0	Analog
P0_MDIP_1	Analog
P0_MDIP_2	Analog
P0_MDIP_3	Analog
P1_MDIN_0	Analog
P1_MDIN_1	Analog
P1_MDIN_2	Analog
P1_MDIN_3	Analog
P1_MDIP_0	Analog
P1_MDIP_1	Analog
P1_MDIP_2	Analog
P1_MDIP_3	Analog

Table 95: 88E1543 Boundary Scan Exclusion List (Continued)

Pin	I/O
P2_MDIN_0	Analog
P2_MDIN_1	Analog
P2_MDIN_2	Analog
P2_MDIN_3	Analog
P2_MDIP_0	Analog
P2_MDIP_1	Analog
P2_MDIP_2	Analog
P2_MDIP_3	Analog
P3_MDIN_0	Analog
P3_MDIN_1	Analog
P3_MDIN_2	Analog
P3_MDIN_3	Analog
P3_MDIP_0	Analog
P3_MDIP_1	Analog
P3_MDIP_2	Analog
P3_MDIP_3	Analog
REF_CLKN	Analog
REF_CLKP	Analog
RSET	Analog
TEST_0	Analog
TEST_1	Analog
TSTPT	Analog
TSTPTF	Analog
V18_L	Analog
XTAL_IN	Analog
XTAL_OUT	Analog
HSDACN	Analog
HSDACP	Analog

Table 96: 88E1548 Boundary Scan Chain Order

Pin	I/O
P3_LED[3]	Output
P3_LED[2]	Output
P3_LED[1]	Output
P3_LED[0]	Output
P3_LED[3]	Output Enable
P3_LED[2]	Output Enable
P3_LED[1]	Output Enable
P3_LED[0]	Output Enable
P2_LED[3]	Output
P2_LED[2]	Output
P2_LED[1]	Output
P2_LED[0]	Output
P2_LED[3]	Output Enable
P2_LED[2]	Output Enable
P2_LED[1]	Output Enable
P2_LED[0]	Output Enable
P1_LED[3]	Output
P1_LED[2]	Output
P1_LED[1]	Output
P1_LED[0]	Output
P1_LED[3]	Output Enable
P1_LED[2]	Output Enable
P1_LED[1]	Output Enable
P1_LED[0]	Output Enable
P0_LED[3]	Output
P0_LED[2]	Output
P0_LED[1]	Output
P0_LED[0]	Output
P0_LED[3]	Output Enable
P0_LED[2]	Output Enable
P0_LED[1]	Output Enable
P0_LED[0]	Output Enable
CONFIG[3]	Input
CONFIG[2]	Input
CONFIG[1]	Input

Table 96: 88E1548 Boundary Scan Chain Order (Continued)

Pin	I/O
CONFIG[0]	Input
MDC	Input
MDIO	Input
MDIO	Output
MDIO	Output Enable
RESETn	Input
CLK_SEL[1]	Input
CLK_SEL[0]	Input
RSVD (Reserved)	Internal
RSVD	Internal
RSVD	Internal
RSVD	Internal
INTn	Output
INTn	Output Enable
P3_S_OUTP/P3_S_OUTN	Output Enable
P3_S_OUTP/P3_S_OUTN	Output
P3_S_OUTN/P3_S_OUTN AC/DC Select	AC/DC Select
P3_S_INN	Input
P3_S_INP	Input
P2_S_OUTP/P2_S_OUTN	Output Enable
P2_S_OUTP/P2_S_OUTN	Output
P2_S_OUTN/P2_S_OUTN AC/DC Select	AC/DC Select
P2_S_INN	Input
P2_S_INP	Input
Q_OUTN/Q_OUTP	Output Enable
Q_OUTN/Q_OUTP	Output
QSGMII AC/DC Select	AC/DC Select
Q_INP	Input
Q_INN	Input
P1_S_OUTP/P1_S_OUTN	Output Enable
P1_S_OUTP/P1_S_OUTN	Output
P1_S_OUTN/P1_S_OUTN AC/DC Select	AC/DC Select
P1_S_INN	Input
P1_S_INP	Input
P0_S_OUTP/P0_S_OUTN	Output Enable
P0_S_OUTP/P0_S_OUTN	Output
P0_S_OUTN/P0_S_OUTN AC/DC Select	AC/DC Select

Table 96: 88E1548 Boundary Scan Chain Order (Continued)

Pin	I/O
P0_S_INN	Input
P0_S_INP	Input

Table 97: 88E1548 Boundary Scan Exclusion List

Pin	I/O
P0_MDIN_0	Analog
P0_MDIN_1	Analog
P0_MDIN_2	Analog
P0_MDIN_3	Analog
P0_MDIP_0	Analog
P0_MDIP_1	Analog
P0_MDIP_2	Analog
P0_MDIP_3	Analog
P1_MDIN_0	Analog
P1_MDIN_1	Analog
P1_MDIN_2	Analog
P1_MDIN_3	Analog
P1_MDIP_0	Analog
P1_MDIP_1	Analog
P1_MDIP_2	Analog
P1_MDIP_3	Analog
P2_MDIN_0	Analog
P2_MDIN_1	Analog
P2_MDIN_2	Analog
P2_MDIN_3	Analog
P2_MDIP_0	Analog
P2_MDIP_1	Analog
P2_MDIP_2	Analog
P2_MDIP_3	Analog
P3_MDIN_0	Analog
P3_MDIN_1	Analog
P3_MDIN_2	Analog
P3_MDIN_3	Analog
P3_MDIP_0	Analog
P3_MDIP_1	Analog

Table 97: 88E1548 Boundary Scan Exclusion List (Continued)

Pin	I/O
P3_MDIP_2	Analog
P3_MDIP_3	Analog
REF_CLKN	Analog
REF_CLKP	Analog
RSET	Analog
TEST_0	Analog
TEST_1	Analog
TSTPT	Analog
TSTPTF	Analog
V18_L	Analog
XTAL_IN	Analog
XTAL_OUT	Analog
HSDACN	Analog
HSDACP	Analog

2.30 Interrupt

The INTn pin supports the interrupt function. INTn is active low.

Registers 18_0, 18_1, 18_2, 18_4, and 26_6.7 are the Interrupt Enable registers.

Registers 19_0, 19_1, 19_2, 19_4, and 26_6.6 are the Interrupt Status registers.

Registers 23_0 is the Interrupt Status summary registers. Register 23_0 lists the ports that have active interrupts. Register 23_0 provides a quick way to isolate the interrupt so that the MAC or switch does not have to poll register 19 for all ports. Reading register 23_0 does not de-assert the INTn pin. Note that register 23_0 can be accessed by reading register 23_0 using the PHY address of any of the four ports.

The various pages of register 18 and 26_6.7 are used to select the interrupt events that can activate the interrupt pin. The interrupt pin will be activated if any of the selected events on any page of register 18 or 26_6.7 occurs.

If a certain interrupt event is not enabled for the INTn pin, it will still be indicated by the corresponding Interrupt status bits if the interrupt event occurs. The unselected events will not cause the INTn pin to be activated.

2.31 Configuring the Device

The device can be configured two ways:

- Hardware configuration strap options (unmanaged applications)
- MDC/MDIO register writes (managed applications)

All hardware configuration options can be overwritten by software except PHYADR[4:2] and PHY_ORDER.

2.31.1 Hardware Configuration

After the deassertion of RESETn the device will be hardware configured.

The device is configured through the CONFIG[3:0] pins and CLK_SEL[1:0].

CLK_SEL[1:0] are used to select the reference clock input option. See [Section 2.33, Reference Clock, on page 146](#) for details.

Each CONFIG[3:0] pin is used to configure 4 bits. The 4-bit value is set depending on what is connected to the CONFIG pins soon after the deassertion of hardware reset. The 4-bit mapping is shown in [Table 98](#).

Table 98: Four Bit Mapping

Pin	Bit 3, 2, 1, 0
VSS	0000
P0_LED[1]	0001
P0_LED[2]	0010
P0_LED[3]	0011
P1_LED[0]	0100
P1_LED[1]	0101
P1_LED[2]	0110
P1_LED[3]	0111
P2_LED[0]	1000
P2_LED[1]	1001
P2_LED[2]	1010
P2_LED[3]	1011
P3_LED[0]	1100
P3_LED[1]	1101
P3_LED[2]	1110
VDDO	1111
P0_LED[0]	Reserved
P3_LED[3]	Reserved

The 4 bits for each CONFIG pin is mapped as shown in [Table 99](#).

Table 99: Configuration Mapping

Pin	Bit3	Bit 2	Bit1	Bit 0
CONFIG[0]	PHY_ORDER	PHYAD[4]	PHYAD[3]	PHYAD[2]
CONFIG[1]	SEL_MS	ENA_PAUSE	C_ANEG[1]	C_ANEG[0]
CONFIG[2]	S_ANEG, Q_ANEG	ENA_XC	DIS_SLEEP	PDOWN
CONFIG[3]	Reserved (Set to 0)	MODE[2]	MODE[1]	MODE[0]

Each bit in the configuration is defined as shown in [Table 100](#).

Table 100: Device Configuration Definition

Bits	Definition	Register Affected
PHYAD[4:2]	PHY Address Bits 4:2	None
PHY_ORDER	0 = PHYAD[1:0] is set as follows: Port 0 - 00, Port 1 - 01, Port 2 - 10, Port 3 - 11 1 = PHYAD[1:0] is set as follows: Port 0 - 11, Port 1 - 10, Port 2 - 01, Port 3 - 00	None
C_ANEG[1:0]	00 = Advertise 1000BASE-T/1000BASE-X Full-Duplex Only	4_0.8:5 = 0000, 9_0.8 = 0, 4_1.6:5 = 01
	01 = Advertise 1000BASE-T/1000BASE-X Full and Half-Duplex Only	4_0.8:5 = 0000, 9_0.8 = 1, 4_1.6:5 = 11
	10 = Advertise All Capabilities Except 1000BASE-T/1000BASE-X Half-Duplex	4_0.8:5 = 1111, 9_0.8 = 0, 4_1.6:5 = 01
	11 = Advertise All Capabilities	4_0.8:5 = 1111, 9_0.8 = 1, 4_1.6:5 = 11
ENA_PAUSE	0 = Do Not Advertise Pause and Asymmetric Pause	4_0.11:10 = 00, 4_1.8:7 = 00
	1 = Advertise Pause and Asymmetric Pause	4_0.11:10 = 11, 4_1.8:7 = 11
PDOWN	0 = Default Power Up Port	See Table 101
	1 = Default Power Down Port	See Table 101
DIS_SLEEP	0 = Default Energy Detect On	16_0.9:8 = 11
	1 = Default Energy Detect Off	16_0.9:8 = 00
ENA_XC	0 = Default Disable Auto-Crossover	16_0.6 = 0
	1 = Default Enable Auto-Crossover	16_0.6 = 1
SEL_MS	0 = Prefer Slave	9_0.11:10 = 00
	1 = Prefer Master	9_0.11:10 = 11

Table 100: Device Configuration Definition (Continued)

Bits	Definition	Register Affected
MODE[2:0]	000 = QSGMII (System) to Copper	20_18.2:0 = 000
	001 = SGMII (System) to Copper	20_18.2:0 = 001
	010 = QSGMII (System) to 1000BASE-X	20_18.2:0 = 010
	011 = If Register 20_18.6 = 0 QSGMII (System) to 100BASE-FX If Register 20_18.6 = 1 QSGMII (System) to Auto Media Detect (Copper/100BASE-FX)	20_18.2:0 = 011
	100 = QSGMII (System) to SGMII (Media)	20_18.2:0 = 100
	101 = SGMII (System) to QSGMII (Media)	20_18.2:0 = 101
	110 = QSGMII (System) to Auto Media Detect (Copper/SGMII (Media))	20_18.2:0 = 110
	111 = QSGMII (System) to Auto Media Detect (Copper/1000BASE-X)	20_18.2:0 = 111
S_ANEG	0 = SGMII/1000BASE-X Auto-Negotiations Off	0_1.12 = 0
	1 = SGMII/1000BASE-X Auto-Negotiations On	0_1.12 = 1
Q_ANEG	0 = SGMII Auto-Negotiations on QSGMII Off	0_4.12 = 0
	1 = SGMII Auto-Negotiations on QSGMII On	0_4.12 = 1

Table 101: PDOWN Register setting as a function of MODE[2:0]

MODE[2:0]	PDOWN	0_0.11	0_1.11	0_4.11
xxx	0	0	0	0
000	1	1	0	0
001	1	1	0	0
010	1	0	1	0
011	1	0	1	0
100	1	0	1	0
101	1	0	0	1
110	1	1	1	0
111	1	1	1	0

2.31.2 Software Configuration - Management Interface

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3 Clause 22 and Clause 45 MDIO protocol. MDC is the management data clock input and, it can run from DC to a maximum rate of 12.5 MHz. At high MDIO fanouts the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bi-directional signal that runs synchronously to MDC.

The MDIO pin requires a pull-up resistor in a range from 1.5 kohm to 10 kohm that pulls the MDIO high during the idle and turnaround.

PHY address is configured during the hardware reset sequence. Refer to [Section 2.31.1, Hardware Configuration, on page 138](#) for more information on how to configure PHY addresses.

All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in the Register Description.

2.31.2.1 Clause 22 MDC/MDIO Management Interface

Typical read and write operations on the management interface are shown in [Figure 32](#) and [Figure 33](#).

Figure 32: Typical MDC/MDIO Read Operation

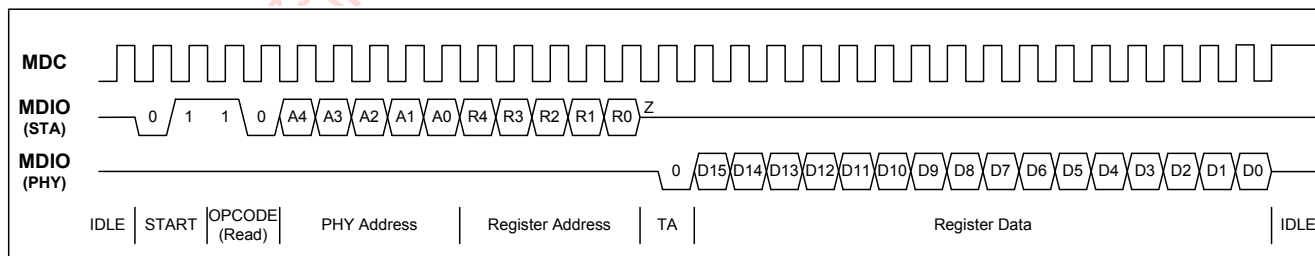
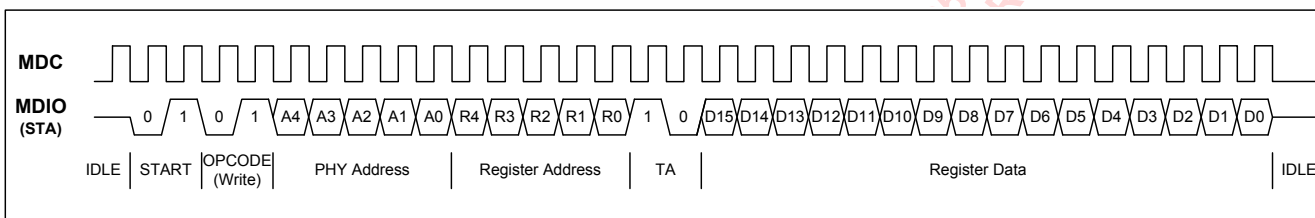


Figure 33: Typical MDC/MDIO Write Operation



[Table 102](#) is an example of a read operation.

Table 102: Serial Management Interface Protocol

32-Bit Preamble	Start of Frame	OpCode Read = 10 Write = 01	5-Bit PHY Device Address	5-Bit PHY Register Address (MSB)	2-Bit Turn around Read = z0 Write = 10	16-Bit Data Field	Idle
11111111	01	10	01100	00000	z0	0001001100000000	11111111

2.31.2.2 Extended Register Access

The IEEE defines only 32 registers address space for the PHY. In order to extend the number of registers address space available a paging mechanism is used. Register 22 bits 7 to 0 are used to specify the page. There is no paging for registers 22.

In this document, the short hand used to specify the registers take the form register_page.bit:bit, register_page.bit, register.bit:bit, or register.bit.

For example:

Register 16 page 2 bits 5 to 2 is specified as 16_2.5:2.

Register 16 page 2 bits 5 is specified as 16_2.5.

It takes four MDIO write commands to write the same register to the same value on all 4 ports. Register 22.15:14 can be used to selectively ignore PHYAD[4:2] and PHYAD[1:0] as shown in Table 103 so that the same register address can be written to all four ports in one MDIO write command. PHYAD[4:0] will still be decoded for read commands.

Care must be taken to setup multiple port write. To enable the concurrent write access write register 22 four times in a row with bit 14 set to 1 – once to each PHYAD[4:0]. The values written on all 16 bits must be the same otherwise unpredictable behavior will occur.

Once the four write commands to register 22 are issued, all subsequent writes will be concurrent to all ports including writes to register 22.

Concurrent write access will continue as long as every write to register 22 sets 22.14 to 1.

To disable concurrent write access simply write register 22.14 to 0.

Table 103: Page Address

Register	Function	Setting	Mode	HW Rst	SW Rst
22.15	Ignore PHYAD[4:2]	0 = Use PHYAD[4:2] to decode write commands 1 = Ignore PHYAD[4:2] to decode write commands	R/W	0	Retain
22.14	Ignore PHYAD[1:0]	0 = Use PHYAD[1:0] to decode write commands 1 = Ignore PHYAD[1:0] to decode write commands	R/W	0	Retain
22.13:8	Reserved	00000000	RO	0	0
22.7:0	Page select for registers 0 to 21, 23 to 28	Page Number	R/W	00	Retain

2.31.2.3 Clause 45 MDC/MDIO Management Interface (XMDIO)

Clause 45 provides extension of Clause 22 MDC/MDIO management interface to access more device registers while retaining its logical compatibility of the frame format. Clause 22 uses frame format with “Start of Frame” code of ‘01’ while Clause 45 uses frame format with “Start of Frame” code of ‘00’. The extensions for Clause 45 MDIO indirect register accesses are specified in Table 104.

Table 104: Extensions for Management Frame Format for Indirect Access

Frame	32-bit Preamble	Start of Frame	Opcode	5-bit PHY Address (MSB)	Device Address	2-bit Turnaround	16-bit ADDRESS/DATA Field	Idle
Address	1..1	00	00	PPPPP	DDDDD	10	AAAAAAAAAAAAAAAA	Z
Write	1..1	00	01	PPPPP	DDDDD	10	DDDDDDDDDDDDDDDD	Z
Read	1..1	00	11	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z
Read Increment	1..1	00	10	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z

Clause 45 MDIO implements a 16-bit address register that stores the address of the register to be accessed. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, post-read increment-address cycles, the field contains the data for the register. At power up and reset, the contents of the register are undefined. Write, read, and post-read-increment-address frames access the address register, though write and read frames do not modify the contents of the address register.

2.31.2.4 Clause 22 Access to Clause 45 MDIO Manageable Device (MMD)

Clause 22 provides access to registers in a clause 45 MDIO MMD space using Register 13 and 14. Register 22.7:0 must be set to 0 to 7. If Register 22.7:0 is 8 to 255, the MMD registers are not accessible.

The MMD Access Control Register and Address/Data Register definitions are shown in [Table 105](#) and [Table 106](#).

Table 105: MMD Access Control Register
Page 0, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Function	R/W	0x0	0x0	15:14 00 = Address 01 = Data, no post increment 10 = Data, post increment on reads and writes 11 = Data, post increment on writes only
13:5	Reserved	RO	0x000	0x000	Reserved
4:0	DEVAD	RO	0x00	0x00	Device address

Table 106: MMD Access Address/Data Register
Page 0, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Address Data	R/W	0x0000	0x0000	If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register.

Write Operation

To write to the MMD register access:

1. To Register 13, write the Function field to 00 (address) and DEVAD field with the device address value;
2. To Register 14, write the MMD's register address value;
3. To Register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value (as step #1);
4. To Register 14, write the content to be written to the selected MMD's register

Step 1 and 2 can be skipped if the MMD's address register was previously configured.

Read Operation

To read from the MMD register access:

1. To Register 13, write the Function field to 00 (address) and DEVAD field with the device address value;
2. To Register 14, write the MMD's register address value;
3. To Register 13, write the Function field to 01 (Data, no post increment) and DEVAD field to the same device address value (as step #1);
4. From Register 14, read the content from the selected MMD's register.

Step 1 and 2 can be skipped if the MMD's address register was previously configured.

Write/Read Operation with Post Increment Function

Function '10' can be used to increment the address after each read and write access. Function '11' can be used to increment the address after write operation only. Function '11' enables a read-modify-write capability for successive addressed registers within the MMD.

2.31.2.5 Clause 45 Access to Clause 22 Registers

Clause 22 registers space can also be access through the Clause 45 MDIO protocol. All of the Clause 22 registers are mapped into Clause 45 Device Address (DEVAD) 3 vendor specific register space (0x8000 – 0x9FFF). The Clause 22 registers are mapped as the following:

$C45_REGAD[15:0] = \{3b'100, P22[7:0], C22_REGAD[4:0]\}$

Where:

$P22[7:0]$ – Clause 22 register 22 paging

$C22_REGAD[4:0]$ – Clause 22 REGAD[4:0]

$C45_REGAD[15:0]$ – Clause 45 REGAD[15:0]

Table 107: Clause 45 Access to Clause 22 Registers Example

Clause 22 Registers		Clause 45 Registers	
Page	Register Address	Device Address	Register Address
0x0	0x4	0x3	0x8004 (3b'100, 8b'0000 0000, 5b'00100)
0x1	0x11 (Register 17)	0x3	0x8031 (3b'100, 8b'0000 0000, 5b'10001)
0x12	0x14 (Register 20)	0x3	0x8254 (3b'100, 8b'0001 0010, 5b'10100)

2.31.2.6 Preamble Suppression

The device is permanently programmed for preamble suppression. A minimum of one idle bit is required between operations.

2.32 Jumbo Packet Support

The device supports jumbo packets up to 16Kbytes on all data paths.

2.33 Reference Clock

The device can use a 25 MHz crystal, 25 MHz oscillator, 125 MHz single-ended clock, 25/125/156.25MHz differential clock as reference clock. REF_CLKP/N are LVDS differential inputs with an internal 100 ohm differential termination resistor and internal ac-coupling. The connection to the reference clock pins are shown in Table 108. The reference frequency used must be indicated by the CLK_SEL[1:0] pins.

Table 108: Reference Clock Pin Connections

Reference Source	CLK_SEL[1:0]	XTAL_IN	XTAL_OUT	REF_CLKP	REF_CLKN
25 MHz Crystal	11	Connect to Crystal	Connect to Crystal	Leave Floating	Leave Floating
25 MHz Oscillator	11	Connect to Driver	Leave Floating	Leave Floating	Leave Floating
25 MHz Differential	10	Leave Floating	Leave Floating	Connect to Driver	Connect to Driver
125 MHz Differential	01	Leave Floating	Leave Floating	Connect to Driver	Connect to Driver
125 MHz Single-ended	01	Leave Floating	Leave Floating	Connect to Driver	0.1 μ f cap to ground
156.25 MHz Differential	00	Leave Floating	Leave Floating	Connect to Driver	Connect to Driver

When using a 25/125/156.25 MHz diff clock, the REF_CLKP/N inputs are used instead of XTAL_IN/XTAL_OUT.



Note

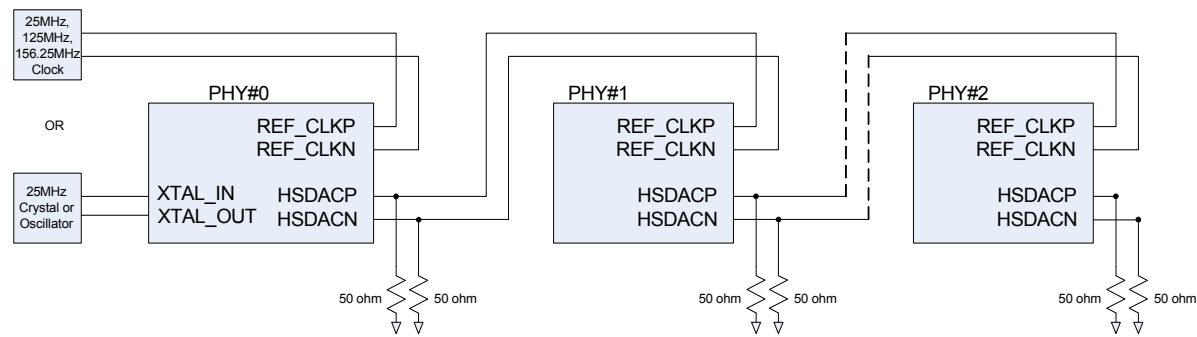
In order to meet the QSGMII transmit and receive jitter specifications, a 125 MHz or 156.25 MHz reference clock input is required. The 25 MHz reference clock input option should not be used for applications using the QSGMII interface.

2.33.1 Clock Cascade

The device supports clock cascade to lower the system cost by reducing the number of clock source required. For this purpose, the HSDACP/N are used as differential LVDS clock outputs that must be routed differentially to the REF_CLKP/N inputs of the downstream devices. A maximum of 2 downstream devices are allowed. The clock frequency follows the clock frequency used for the REF_CLKP/N or XTAL_IN/OUT inputs.

The clock cascade is by default enabled upon powering up the device. This allows the clock to be running to the entire downstream devices before the hardware reset signal is deasserted. Figure X shows the clock cascade example.

Figure 34: Clock Cascade Usage Block Diagram



If the clock cascade feature is not used, it can be disabled to save some power by writing to Reg 27_4.8 to '0' (See Table 109). When the HSDACP/N used for IEEE testing or debug purpose, the clock cascade feature must be disabled.

Table 109: QSGMII Global Control Register 2 (Page 4, Register 27)

Register	Function	Setting	Mode	HW Rst	SW Rst
27_4.8	Clock Cascade Enable	Clock Cascade Enable 1 = Enable 0 = Disable	R/W	0x1	Retain

2.34 Temperature Sensor

The device contains an internal temperature sensor. Register 26_6.4:0 reports the die temperature and is updated approximately once per second. The result can be read back on any port as long as the port is not disabled (i.e. register 0.11 = 1).

An interrupt can be generated when the temperature exceeds a certain threshold.

Register 26_6.6 is set high whenever the temperature is greater than or equal to the value programmed in register 26_6.12:8. Register 26_6.6 remains high until read.

Register 26_6.7 controls whether the interrupt pin is asserted when register 26_6.6 is high.

The interrupt should be enabled on only one port since there is only 1 temperature sensor for the entire chip.

Table 110: Temperature Sensor Register

Register	Function	Setting	Mode	HW Rst	SW Rst
26_6.12:8	Temperature Threshold	Temperature in C = 5 x 26_6.4:0 - 25 i.e., for 100C the value is 11001	R/W	11001	Retain
26_6.7	Temperature Sensor Interrupt Enable	1 = Interrupt Enable 0 = Interrupt Enable	R/W	0	Retain
26_6.6	Temperature Sensor Interrupt	1 = Temperature Reached Threshold 0 = Temperature Below Threshold	RO, LH	0	0
26_6.4:0	Temperature Sensor (5-bit)	Temperature in C = 5 x 26_6.4:0 - 25 i.e., for 100C the value is 11001	RO	xxxxx	xxxxx

2.35 Power Supplies

The device requires three power supplies: 1.0V, 1.8V, and 3.3V. If 2.5V I/Os are required (e.g., JTAG or MDC/MDIO pins), then a fourth supply of 2.5V will be required. The VDDOM can operate at 1.2V. If VDDO is 2.5V, then I/Os are not 3.3V tolerant. For I/Os to be 3.3V tolerant, VDDO must be 3.3V.

2.35.1 AVDD33

AVDD33 is used as 3.3V analog supply.

2.35.2 AVDD18

AVDD18 is used as the 1.8V analog supply.

2.35.3 VDDC

VDDC is used as the 1.8V XTAL_IN/OUT supply. The XTAL_IN/OUT pins are not 3.3V or 2.5V tolerant.

Refer to the 'Oscillator Level Shifting' (MV-S301630-00) application note for details on how to convert a 2.5V/3.3V clock source to 1.8V clock.

2.35.4 DVDD

DVDD is used for the digital logic. DVDD is the 1.0V digital supply.

2.35.5 VDDOL

VDDOL supplies the digital I/O pins for RESETn¹, LED, CONFIG, and INTn.

V18_L should be tied to VSS if the VDDOL voltage is set to 2.5V or 3.3V.

V18_L should be floating if the VDDOL voltage is set to 1.8V.

2.35.6 VDDOR

VDDOR supplies the digital I/O pins for TDO, TDI, TMS, TCK, TRST, REF_CLKP/N, or CLK_SEL[1:0].

V18_R should be tied to VSS if the VDDOR voltage is set to 2.5V or 3.3V.

V18_R should be floating if the VDDOR voltage is set to 1.8V.

For the 88E1543 LKJ device, VDDOR is 2.5V or 3.3V.

For the 88E1545 LKJ device, VDDOR is 2.5V or 3.3V.

2.35.7 VDDOM

VDDOM supplies the digital I/O pins for MDC, MDIO, and TEST.

V12_EN should be tied to VSS if the VDDOM voltage is set to 2.5V or 3.3V.

V12_EN should be floating if the VDDOM voltage is set to 1.2V or 1.8V.

For the 88E1543 LKJ device, VDDOM is 2.5V or 3.3V.

For the 88E1545 LKJ device, VDDOM is 1.2V or 1.8V.

2.35.8 Power Supply Sequencing

On power-up, no special power supply sequencing is required.

1. When VDDOL = 3.3V, the RESETn pin can operate at 2.5V level. See [Section 4.5.3, RESETn Pin, on page 238](#) for details.

3

PHY Register Description

The device supports both Clause 22 MDIO register access protocol and Clause 45 XMDIO register access protocol. The device also supports Clause 22 MDIO access to registers in Clause 45 XMDIO space using Page 0 register 13 and 14.

Table 111 below defines the register types used in the register map.

Table 111: Register Types

Type	Description
C	Clear after read.
LH	Register field with latching high function. If status is high, then the register is set to one and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If status is low, then the register is cleared to zero and remains zero until a read operation is performed through the management interface or a reset occurs.
Retain	The register value is retained after software reset is executed.
RES	Reserved for future use. All reserved bits are read as zero unless otherwise noted.
RO	Read only.
ROS	Read only, Set high after read.
ROC	Read only clear. After read, register field is cleared.
RW	This bit or these bits must be read and left unchanged when performing a write.
RWR	Read/Write clear on read. All field bits are readable and writable. After reset, register field is cleared to 0.
RWS	Read/Write set. All field bits are readable and writable. After reset, register field is set to a non-zero value specified in the text.
SC	Self-Clear. Writing a one to this register causes the desired function to be immediately executed, then the register field is automatically cleared to zero when the function is complete.
Update	Value written to the register field doesn't take effect until soft reset is executed.
WO	Write only. Reads to this type of register field return undefined data.

For all binary equations appearing in the register map, the symbol | is equal to a binary OR operation.

3.1 PHY MDIO Register Description

The IEEE defines only 32 registers address space for the PHY. In order to extend the number of registers address space available a paging mechanism is used. Register 22 bits 7 to 0 are used to specify the page. There is no paging for register 22.

In this document, the short hand used to specify the registers take the form register_page.bit:bit, register_page.bit, register.bit:bit, or register.bit.

For example:

Register 16 page 2 bits 5 to 2 is specified as 16_2.5:2.

Register 16 page 2 bits 5 is specified as 16_2.5.

Register 2 bit 3 to 0 is specified as 2.3:0.

Note that in this context the setting of the page register (register 22) has no effect.

Register 2 bit 3 is specified as 2.3.

Table 112: Device Register Map Summary - Page 0 - Page 7

Register Address	Page Address							
	0	1	2	3	4	5	6	7
	Copper Adv	SGMII	MAC Ctrl/Status	LED	QSGMII	Advanced VCT	Packet Gen/Chk	Cable Diagnostics
0	Copper Control Register	Fiber Control Register			QSGMII Control Register			
1	Copper Status Register	Fiber Status Register			QSGMII Status Register			
2	PHY Identifier 1	PHY Identifier 1						
3	PHY Identifier 2	PHY Identifier 2						
4	Copper Auto-Negotiation Advertisement Register	Fiber Auto-Negotiation Advertisement Register			QSGMII Auto-Negotiation Advertisement Register			
5	Copper Link Partner Ability Register - Base Page	Fiber Link Partner Ability Register			QSGMII Link Partner Ability Register			
6	Copper Auto-Negotiation Expansion Register	Fiber Auto-Negotiation Expansion Register			QSGMII Auto-Negotiation Expansion Register			
7	Copper Next Page Transmit Register	Fiber Next Page Transmit Register						
8	Copper Link Partner Next Page Register	Fiber Link Partner Next Page Register						
9	1000BASE-T Control Register							
10	1000BASE-T Status Register							
11								
12								
13	MMD access control register							
14	MMD access Address/Data register							
15	Extended Status Register	Extended Status Register						
16	Copper Specific Control Register 1	Fiber Specific Control Register 1	MAC Specific Control Register 1	LED[3:0] Function Control Register	QSGMII Specific Control Register	Advanced VCT TX to MDI[0] Rx Coupling	Packet Generation	PHY Cable Diagnostics Pair 0 Length
17	Copper Specific Status Register 1	Fiber Specific Status Register		LED[3:0] Polarity Control Register	QSGMII Specific Status Register	Advanced VCT TX to MDI[1] Rx Coupling	CRC Counters	PHY Cable Diagnostics Pair 1 Length
18	Copper Specific Interrupt Enable Register	Fiber Specific Interrupt Enable Register	MAC Specific Interrupt Enable Register	LED Timer Control Register	QSGMII Specific Interrupt Enable Register	Advanced VCT TX to MDI[2] Rx Coupling	Checker Control	PHY Cable Diagnostics Pair 2 Length
19	Copper Interrupt Status Register	Fiber Interrupt Status Register	MAC Specific Status Register	LED[5:4] Function Control and Polarity Register	QSGMII Interrupt Status Register	Advanced VCT TX to MDI[3] Rx Coupling	Copper Port Packet Generator IPG Control	PHY Cable Diagnostics Pair 3 Length
20	Copper Specific Control Register 2				QSGMII RX_ER Byte Capture	1000BASE-T Pair Skew Register	General Control Register	PHY Cable Diagnostics Results
21	Copper Specific Receive Error Counter	Fiber Specific Receive Error Counter	MAC Specific Control Register 2		QSGMII Specific Receive Error Counter	1000BASE-T Pair Swap and Polarity		PHY Cable Diagnostics Control
22	Page Address							
23	Global Interrupt Status	PRBS Control			PRBS Control	Advance VCT Control	Late Collision Counters 1 & 2	
24		PRBS Error Counter LSB			PRBS Error Counter LSB	Advanced VCT Sample Point Distance	Late Collision Counters 3 & 4	
25		PRBS Error Counter MSB			PRBS Error Counter MSB	Advanced VCT Cross Pair Positive Threshold	Late Collision Window Adjust	Advanced VCT Cross Pair Negative Threshold
26	Copper Specific Control Register 3	Fiber Specific Control Register 2			QSGMII Global Control Register 1	Advanced VCT Same Pair Impedance Positive Threshold 0 and 1	Misc Test	Advanced VCT Same Pair Impedance Negative Threshold 0 and 1
27					QSGMII Global Control Register 2	Advanced VCT Same Pair Impedance Positive Threshold 2 and 3	Temperature Sensor	Advanced VCT Same Pair Impedance Negative Threshold 2 and 3
28				LED Random Blinking Control 1		Advanced VCT Same Pair Impedance Positive Threshold 4 and Transmit Pulse Control		Advanced VCT Same Pair Impedance Negative Threshold 4
29				LED Random Blinking Control 2				
30								
31								

Table 113: Device Register Map Summary - Page 8 - Page 255

		Page Address													
		8	9	10,11	12	13	14	15	16	17	18	19	20	21 to 254	255
											Common				
Register Address	0										EEE Control Register 1				Factory Test Modes
	1										EEE Control Register 2				Factory Test Modes
	2										EEE Control Register 3				Factory Test Modes
	3														Factory Test Modes
	4														Factory Test Modes
	5														Factory Test Modes
	6														Factory Test Modes
	7														Factory Test Modes
	8														Factory Test Modes
	9														Factory Test Modes
	10														Factory Test Modes
	11														Factory Test Modes
	12														Factory Test Modes
	13														Factory Test Modes
	14														Factory Test Modes
	15														Factory Test Modes
	16										Packet Generation				Factory Test Modes
	17										CRC Counters				Factory Test Modes
	18														Factory Test Modes
	19										Packet Generator IPG Control				Factory Test Modes
	20										General Control Register 1				Factory Test Modes
	21														Factory Test Modes
	22	Page Address													
	23														Factory Test Modes
	24														Factory Test Modes
	25										Link Disconnect Count				Factory Test Modes
	26										RX_ER byte capture				Factory Test Modes
	27														Factory Test Modes
	28														Factory Test Modes
	29														
	30														
	31														Factory Test Modes

Table 114: Register Map

Register Name	Register Address	Table and Page
Copper Control Register	Page 0, Register 0	Table 115, p. 158
Copper Status Register	Page 0, Register 1	Table 116, p. 160
PHY Identifier 1	Page 0, Register 2	Table 117, p. 161
PHY Identifier 2	Page 0, Register 3	Table 118, p. 161
Copper Auto-Negotiation Advertisement Register	Page 0, Register 4	Table 119, p. 162
Copper Link Partner Ability Register - Base Page	Page 0, Register 5	Table 120, p. 165
Copper Auto-Negotiation Expansion Register	Page 0, Register 6	Table 121, p. 166
Copper Next Page Transmit Register	Page 0, Register 7	Table 122, p. 166
Copper Link Partner Next Page Register	Page 0, Register 8	Table 123, p. 167
1000BASE-T Control Register	Page 0, Register 9	Table 124, p. 167
1000BASE-T Status Register	Page 0, Register 10	Table 125, p. 168
MMD Access Control Register	Page 0, Register 13	Table 126, p. 169
MMD Access Address/Data Register	Page 0, Register 14	Table 127, p. 169
Extended Status Register	Page 0, Register 15	Table 128, p. 170
Copper Specific Control Register 1	Page 0, Register 16	Table 129, p. 170
Copper Specific Status Register 1	Page 0, Register 17	Table 130, p. 171
Copper Specific Interrupt Enable Register	Page 0, Register 18	Table 131, p. 173
Copper Interrupt Status Register	Page 0, Register 19	Table 132, p. 174
Copper Specific Control Register 2	Page 0, Register 20	Table 133, p. 175
Copper Specific Receive Error Counter Register	Page 0, Register 21	Table 134, p. 175
Page Address	Page Any, Register 22	Table 135, p. 175
Global Interrupt Status	Page 0, Register 23	Table 136, p. 176
Copper Specific Control Register 3	Page 0, Register 26	Table 137, p. 176
Fiber Control Register	Page 1, Register 0	Table 138, p. 177
Fiber Status Register	Page 1, Register 1	Table 139, p. 179
PHY Identifier	Page 1, Register 2	Table 140, p. 180
PHY Identifier	Page 1, Register 3	Table 141, p. 180
Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)	Page 1, Register 4	Table 142, p. 180
Fiber Auto-Negotiation Advertisement Register - SGMII (System mode) (Register 16_1.1:0 = 10)	Page 1, Register 4	Table 143, p. 182
Fiber Auto-Negotiation Advertisement Register - SGMII (Media mode) (Register 16_1.1:0 = 11)	Page 1, Register 4	Table 144, p. 182
Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)	Page 1, Register 5	Table 145, p. 182
Fiber Link Partner Ability Register - SGMII (System mode) (Register 16_1.1:0 = 10)	Page 1, Register 5	Table 146, p. 183
Fiber Link Partner Ability Register - SGMII (Media mode) (Register 16_1.1:0 = 11)	Page 1, Register 5	Table 147, p. 184
Fiber Auto-Negotiation Expansion Register	Page 1, Register 6	Table 148, p. 185

Table 114: Register Map (Continued)

Register Name	Register Address	Table and Page
Fiber Next Page Transmit Register	Page 1, Register 7	Table 149, p. 185
Fiber Link Partner Next Page Register	Page 1, Register 8	Table 150, p. 186
Extended Status Register	Page 1, Register 15	Table 151, p. 186
Fiber Specific Control Register 1	Page 1, Register 16	Table 152, p. 186
Fiber Specific Status Register	Page 1, Register 17	Table 153, p. 188
Fiber Interrupt Enable Register	Page 1, Register 18	Table 154, p. 189
Fiber Interrupt Status Register	Page 1, Register 19	Table 155, p. 189
Fiber Receive Error Counter Register	Page 1, Register 21	Table 156, p. 190
PRBS Control	Page 1, Register 23	Table 157, p. 190
PRBS Error Counter LSB	Page 1, Register 24	Table 158, p. 191
PRBS Error Counter MSB	Page 1, Register 25	Table 159, p. 191
Fiber Specific Control Register 2	Page 1, Register 26	Table 160, p. 191
MAC Specific Control Register 1	Page 2, Register 16	Table 161, p. 192
MAC Specific Interrupt Enable Register	Page 2, Register 18	Table 162, p. 192
MAC Specific Status Register	Page 2, Register 19	Table 163, p. 193
MAC Specific Control Register 2	Page 2, Register 21	Table 164, p. 193
LED[3:0] Function Control Register	Page 3, Register 16	Table 165, p. 194
LED[3:0] Polarity Control Register	Page 3, Register 17	Table 166, p. 195
LED Timer Control Register	Page 3, Register 18	Table 167, p. 196
LED[5:4] Function Control and Polarity Register	Page 3, Register 19	Table 168, p. 196
LED Random Blinking Control 1 Register	Page 3, Register 28	Table 169, p. 197
LED Random Blinking Control 2 Register	Page 3, Register 29	Table 170, p. 198
QSGMII Control Register	Page 4, Register 0	Table 171, p. 198
QSGMII Status Register	Page 4, Register 1	Table 172, p. 199
QSGMII Auto-Negotiation Advertisement Register - SGMII (System mode) (Register 16_4.0 = 0)	Page 4, Register 4	Table 173, p. 199
QSGMII Auto-Negotiation Advertisement Register - SGMII (Media mode) (Register 16_4.0 = 1)	Page 4, Register 4	Table 174, p. 200
QSGMII Link Partner Ability Register - SGMII (System mode) Mode (Register 16_4.0 = 0)	Page 4, Register 5	Table 175, p. 200
QSGMII Link Partner Ability Register - SGMII (Media mode) Mode (Register 16_4.0 = 1)	Page 4, Register 5	Table 176, p. 201
QSGMII Auto-Negotiation Expansion Register	Page 4, Register 6	Table 177, p. 201
QSGMII Specific Control Register 1	Page 4, Register 16	Table 178, p. 202
QSGMII Specific Status Register	Page 4, Register 17	Table 179, p. 203
QSGMII Interrupt Enable Register	Page 4, Register 18	Table 180, p. 204
QSGMII Interrupt Status Register	Page 4, Register 19	Table 181, p. 204
QSGMII RX_ER Byte Capture	Page 4, Register 20	Table 182, p. 205
QSGMII Receive Error Counter Register	Page 4, Register 21	Table 183, p. 205
PRBS Control	Page 4, Register 23	Table 184, p. 206
PRBS Error Counter LSB	Page 4, Register 24	Table 185, p. 206

Table 114: Register Map (Continued)

Register Name	Register Address	Table and Page
PRBS Error Counter MSB	Page 4, Register 25	Table 186, p. 206
QSGMII Global Control Register 1	Page 4, Register 26	Table 187, p. 206
QSGMII Global Control Register 2	Page 4, Register 27	Table 188, p. 207
Advanced VCT™ TX to MDI[0] Rx Coupling	Page 5, Register 16	Table 189, p. 208
Advanced VCT™ TX to MDI[1] Rx Coupling	Page 5, Register 17	Table 190, p. 209
Advanced VCT™ TX to MDI[2] Rx Coupling	Page 5, Register 18	Table 191, p. 210
Advanced VCT™ TX to MDI[3] Rx Coupling	Page 5, Register 19	Table 192, p. 211
1000BASE-T Pair Skew Register	Page 5, Register 20	Table 193, p. 212
1000BASE-T Pair Swap and Polarity	Page 5, Register 21	Table 194, p. 212
Advanced VCT™ Control	Page 5, Register 23	Table 195, p. 213
Advanced VCT™ Sample Point Distance	Page 5, Register 24	Table 196, p. 213
Advanced VCT Cross Pair Positive Threshold	Page 5, Register 25	Table 197, p. 214
Advanced VCT Same Pair Impedance Positive Threshold 0 and 1	Page 5, Register 26	Table 198, p. 214
Advanced VCT™ Same Pair Impedance Positive Threshold 2 and 3	Page 5, Register 27	Table 199, p. 214
Advanced VCT Same Pair Impedance Positive Threshold 4 and Transmit Pulse Control	Page 5, Register 28	Table 200, p. 214
Copper Port Packet Generation	Page 6, Register 16	Table 201, p. 215
Copper Port CRC Counters	Page 6, Register 17	Table 202, p. 216
Checker Control	Page 6, Register 18	Table 203, p. 216
Copper Port Packet Generator IPG Control	Page 6, Register 19	Table 204, p. 217
Late Collision Counters 1 & 2	Page 6, Register 23	Table 205, p. 217
Late Collision Counters 3 & 4	Page 6, Register 24	Table 206, p. 217
Late Collision Window Adjust/Link Disconnect	Page 6, Register 25	Table 207, p. 217
Misc Test	Page 6, Register 26	Table 208, p. 218
PHY Cable Diagnostics Pair 0 Length	Page 7, Register 16	Table 209, p. 218
PHY Cable Diagnostics Pair 1 Length	Page 7, Register 17	Table 210, p. 218
PHY Cable Diagnostics Pair 2 Length	Page 7, Register 18	Table 211, p. 218
PHY Cable Diagnostics Pair 3 Length	Page 7, Register 19	Table 212, p. 219
PHY Cable Diagnostics Results	Page 7, Register 20	Table 213, p. 219
PHY Cable Diagnostics Control	Page 7, Register 21	Table 214, p. 219
Advanced VCT™ Cross Pair Negative Threshold	Page 7, Register 25	Table 215, p. 220
Advanced VCT Same Pair Impedance Negative Threshold 0 and 1	Page 7, Register 26	Table 216, p. 220
Advanced VCT Same Pair Impedance Negative Threshold 2 and 3	Page 7, Register 27	Table 217, p. 220
Advanced VCT Same Pair Impedance Negative Threshold 4	Page 7, Register 28	Table 218, p. 221
EEE Control Register 1	Page 18, Register 0	Table 219, p. 221
EEE Control Register 2	Page 18, Register 1	Table 220, p. 221

Table 114: Register Map (Continued)

Register Name	Register Address	Table and Page
EEE Control Register 3	Page 18, Register 2	Table 221, p. 221
Packet Generation	Page 18, Register 16	Table 222, p. 222
CRC Counters	Page 18, Register 17	Table 223, p. 223
Checker Control	Page 18, Register 18	Table 224, p. 223
Packet Generator IPG Control	Page 18, Register 19	Table 225, p. 223
General Control Register 1	Page 18, Register 20	Table 226, p. 224
Link Disconnect Count	Page 18, Register 25	Table 227, p. 224
Copper/SERDES RX_ER Byte Capture	Page 18, Register 26	Table 228, p. 225

Table 115: Copper Control Register
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Reset	R/W, SC	0x0	SC	Copper Software Reset. Affects pages 0, 2, 3, 5, and 7. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD is looped back to RXD internally. Link is broken when loopback is enabled. Loopback speed is determined by Registers 21_2.2:0. 1 = Enable Loopback 0 = Disable Loopback
13	Speed Select (LSB)	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
12	Auto-Negotiation Enable	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation If Register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 is set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T. 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process

Table 115: Copper Control Register (Continued)
Page 0, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Power Down	R/W	See Descr	Retain	Power down is controlled via register 0_0.11 and 16_0.2. Both bits must be set to 0 before the PHY will transition from power down to normal operation. When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_0.15) and Restart Auto-Negotiation (0_0.9) are not set by the user. Upon hardware reset this bit takes on the value of PDOWN and (MODE[2:0] = 00x or 11x) 1 = Power down 0 = Normal operation
10	Isolate	RO	0x0	0x0	This bit has no effect.
9	Restart Copper Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware or software reset regardless of whether or not the restart bit (0_0.9) is set. 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Copper Duplex Mode	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation 1 = Full-duplex 0 = Half-duplex
7	Collision Test	RO	0x0	0x0	This bit has no effect.
6	Speed Selection (MSB)	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation bit 6, 13 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
5:0	Reserved	RO	Always 000000	Always 000000	Reserved

Table 116: Copper Status Register
Page 0, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	Always 0	Always 0	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	Always 1	Always 1	1 = PHY able to perform full-duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	Always 1	Always 1	1 = PHY able to perform half-duplex 100BASE-X
12	10 Mbps Full-Duplex	RO	Always 1	Always 1	1 = PHY able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	Always 1	Always 1	1 = PHY able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform half-duplex
8	Extended Status	RO	Always 1	Always 1	1 = Extended status information in Register 15
7	Reserved	RO	Always 0	Always 0	Reserved
6	MF Preamble Suppression	RO	Always 1	Always 1	1 = PHY accepts management frames with preamble suppressed
5	Copper Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete
4	Copper Remote Fault	RO,LH	0x0	0x0	1 = Remote fault condition detected 0 = Remote fault condition not detected
3	Auto-Negotiation Ability	RO	Always 1	Always 1	1 = PHY able to perform Auto-Negotiation
2	Copper Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_0.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Jabber Detect	RO,LH	0x0	0x0	1 = Jabber condition detected 0 = Jabber condition not detected
0	Extended Capability	RO	Always 1	Always 1	1 = Extended register capabilities

Table 117: PHY Identifier 1
Page 0, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	<p>Marvell® OUI is 0x005043</p> <p>0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24</p> <p>Register 2.[15:0] show bits 3 to 18 of the OUI.</p> <p>0000000101000001 ^ ^ bit 3.....bit18</p>

Table 118: PHY Identifier 2
Page 0, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 000011	Always 000011	<p>Organizationally Unique Identifier bits 19:24</p> <p>00 0011 ^.....^ bit 19...bit24</p>
9:4	Model Number	RO	Always 101010	Always 101010	Model Number 101010
3:0	Revision Number	RO	See Descr	See Descr	Rev Number See relevant product Release Notes for details.

Table 119: Copper Auto-Negotiation Advertisement Register
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. If 1000BASE-T is advertised then the required next pages are automatically transmitted. Register 4.15 should be set to 0 if no additional next pages are needed. 1 = Advertise 0 = Not advertised
14	Ack	RO	Always 0	Always 0	Must be 0.
13	Remote Fault	R/W	0x0	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Set Remote Fault bit 0 = Do not set Remote Fault bit
12	Reserved	R/W	0x0	Update	Reserved
11	Asymmetric Pause	R/W	See Descr.	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Upon hardware reset this bit takes on the value of ENA_PAUSE. 1 = Asymmetric Pause 0 = No asymmetric Pause
10	Pause	R/W	See Descr.	Update	A write to this register bit does not take effect until any one of the following occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Upon hardware reset this bit takes on the value of ENA_PAUSE. 1 = MAC PAUSE implemented 0 = MAC PAUSE not implemented
9	100BASE-T4	R/W	0x0	Retain	0 = Not capable of 100BASE-T4

Table 119: Copper Auto-Negotiation Advertisement Register (Continued)
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
8	100BASE-TX Full-Duplex	R/W	See Descr.	Update	<p>A write to this register bit does not take effect until any one of the following occurs:</p> <ul style="list-style-type: none"> Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. <p>If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T.</p> <p>Upon hardware reset this bit takes on the value of C_ANEG[1].</p> <p>1 = Advertise 0 = Not advertised</p>
7	100BASE-TX Half-Duplex	R/W	See Descr.	Update	<p>A write to this register bit does not take effect until any one of the following occurs:</p> <ul style="list-style-type: none"> Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. <p>If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0.13 and 0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0.8 set to 0. Registers 4.8:5 and 9.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T.</p> <p>Upon hardware reset this bit takes on the value of C_ANEG[1].</p> <p>1 = Advertise 0 = Not advertised</p>

Table 119: Copper Auto-Negotiation Advertisement Register (Continued)
Page 0, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
6	10BASE-TX Full-Duplex	R/W	See Descr.	Update	<p>A write to this register bit does not take effect until any one of the following occurs:</p> <ul style="list-style-type: none"> Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. <p>If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T.</p> <p>Upon hardware reset this bit takes on the value of C_ANEG[1].</p> <p>1 = Advertise 0 = Not advertised</p>
5	10BASE-TX Half-Duplex	R/W	See Descr.	Update	<p>A write to this register bit does not take effect until any one of the following occurs:</p> <ul style="list-style-type: none"> Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. <p>If register 0_0.12 is set to 0 and speed is manually forced to 1000 Mbps in Registers 0_0.13 and 0_0.6, then Auto-Negotiation will still be enabled and only 1000BASE-T full-duplex is advertised if register 0_0.8 is set to 1, and 1000BASE-T half-duplex is advertised if 0_0.8 set to 0. Registers 4_0.8:5 and 9_0.9:8 are ignored. Auto-Negotiation is mandatory per IEEE for proper operation in 1000BASE-T.</p> <p>Upon hardware reset this bit takes on the value of C_ANEG[1].</p> <p>1 = Advertise 0 = Not advertised</p>
4:0	Selector Field	R/W	0x01	Retain	<p>Selector Field mode</p> <p>00001 = 802.3</p>

Table 120: Copper Link Partner Ability Register - Base Page
Page 0, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page
14	Acknowledge	RO	0x0	0x0	Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner does not have Next Page ability
13	Remote Fault	RO	0x0	0x0	Remote Fault Received Code Word Bit 13 1 = Link partner detected remote fault 0 = Link partner has not detected remote fault
12	Technology Ability Field	RO	0x0	0x0	Received Code Word Bit 12
11	Asymmetric Pause	RO	0x0	0x0	Received Code Word Bit 11 1 = Link partner requests asymmetric pause 0 = Link partner does not request asymmetric pause
10	Pause Capable	RO	0x0	0x0	Received Code Word Bit 10 1 = Link partner is capable of pause operation 0 = Link partner is not capable of pause operation
9	100BASE-T4 Capability	RO	0x0	0x0	Received Code Word Bit 9 1 = Link partner is 100BASE-T4 capable 0 = Link partner is not 100BASE-T4 capable
8	100BASE-TX Full-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 8 1 = Link partner is 100BASE-TX full-duplex capable 0 = Link partner is not 100BASE-TX full-duplex capable
7	100BASE-TX Half-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 7 1 = Link partner is 100BASE-TX half-duplex capable 0 = Link partner is not 100BASE-TX half-duplex capable
6	10BASE-T Full-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 6 1 = Link partner is 10BASE-T full-duplex capable 0 = Link partner is not 10BASE-T full-duplex capable
5	10BASE-T Half-Duplex Capability	RO	0x0	0x0	Received Code Word Bit 5 1 = Link partner is 10BASE-T half-duplex capable 0 = Link partner is not 10BASE-T half-duplex capable
4:0	Selector Field	RO	0x00	0x00	Selector Field Received Code Word Bit 4:0

Table 121: Copper Auto-Negotiation Expansion Register
Page 0, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x000	0x000	Reserved.
4	Parallel Detection Fault	RO, LH	0x0	0x0	Register 6_0.4 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = A fault has been detected via the Parallel Detection function 0 = A fault has not been detected via the Parallel Detection function
3	Link Partner Next page Able	RO	0x0	0x0	Register 6_0.3 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	0x1	0x1	Register 6_0.2 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Local Device is Next Page able 0 = Local Device is not Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 6_0.1 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	Register 6_0.0 is not valid until the Auto-Negotiation complete bit (Reg 1_0.5) indicates completed. 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 122: Copper Next Page Transmit Register
Page 0, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7_0 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Link fail will clear Reg 7_0. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Reserved
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Table 123: Copper Link Partner Next Page Register
Page 0, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Table 124: 1000BASE-T Control Register
Page 0, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Test Mode	R/W	0x0	Retain	TX_CLK comes from the RX_CLK pin for jitter testing in test modes 2 and 3. After exiting the test mode, hardware reset or software reset (Register 0_0.15) should be issued to ensure normal operation. A restart of Auto-Negotiation will clear these bits. 000 = Normal Mode 001 = Test Mode 1 - Transmit Waveform Test 010 = Test Mode 2 - Transmit Jitter Test (MASTER mode) 011 = Test Mode 3 - Transmit Jitter Test (SLAVE mode) 100 = Test Mode 4 - Transmit Distortion Test 101, 110, 111 = Reserved
12	MASTER/SLAVE Manual Configuration Enable	R/W	0x0	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. 1 = Manual MASTER/SLAVE configuration 0 = Automatic MASTER/SLAVE configuration
11	MASTER/SLAVE Configuration Value	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Upon hardware reset this bit takes on the value of SEL_MS. 1 = Manual configure as MASTER 0 = Manual configure as SLAVE

Table 124: 1000BASE-T Control Register (Continued)

Page 0, Register 9

Bits	Field	Mode	HW Rst	SW Rst	Description
10	Port Type	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Register 9_0.10 is ignored if Register 9_0.12 is equal to 1. Upon hardware reset this bit takes on the value of SEL_MS. 1 = Prefer multi-port device (MASTER) 0 = Prefer single port device (SLAVE)
9	1000BASE-T Full-Duplex	R/W	0x1	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
8	1000BASE-T Half-Duplex	R/W	See Descr.	Update	A write to this register bit does not take effect until any of the following also occurs: Software reset is asserted (Register 0_0.15) Restart Auto-Negotiation is asserted (Register 0_0.9) Power down (Register 0_0.11, 16_0.2) transitions from power down to normal operation Copper link goes down. Upon hardware reset this bit takes on the value of C_ANEG[0]. 1 = Advertise 0 = Not advertised
7:0	Reserved	R/W	0x00	Retain	Reserved

Table 125: 1000BASE-T Status Register

Page 0, Register 10

Bits	Field	Mode	HW Rst	SW Rst	Description
15	MASTER/SLAVE Configuration Fault	RO, LH	0x0	0x0	This register bit will clear on read. 1 = MASTER/SLAVE configuration fault detected 0 = No MASTER/SLAVE configuration fault detected
14	MASTER/SLAVE Configuration Resolution	RO	0x0	0x0	1 = Local PHY configuration resolved to MASTER 0 = Local PHY configuration resolved to SLAVE
13	Local Receiver Status	RO	0x0	0x0	1 = Local Receiver OK 0 = Local Receiver is Not OK
12	Remote Receiver Status	RO	0x0	0x0	1 = Remote Receiver OK 0 = Remote Receiver Not OK

Table 125: 1000BASE-T Status Register (Continued)

Page 0, Register 10

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Link Partner 1000BASE-T Full-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T full-duplex 0 = Link Partner is not capable of 1000BASE-T full-duplex
10	Link Partner 1000BASE-T Half-Duplex Capability	RO	0x0	0x0	1 = Link Partner is capable of 1000BASE-T half-duplex 0 = Link Partner is not capable of 1000BASE-T half-duplex
9:8	Reserved	RO	0x0	0x0	Reserved
7:0	Idle Error Count	RO, SC	0x00	0x00	MSB of Idle Error Counter These register bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.

Table 126: MMD Access Control Register

Page 0, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Function	R/W	0x0	0x0	15:14 00= address 01= data, no post increment 10= data, post increment on reads and writes 11= data, post increment on writes only
13:5	Reserved	RO	0x000	0x000	Reserved
4:0	DEVAD	RO	0x00	0x00	Device address

Table 127: MMD Access Address/Data Register

Page 0, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Address Data	R/W	0x0000	0x0000	If 13.15:14 = 00, MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register

Table 128: Extended Status Register
Page 0, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	Always 0	Always 0	0 = not 1000BASE-X full-duplex capable
14	1000BASE-X Half-Duplex	RO	Always 0	Always 0	0 = not 1000BASE-X half-duplex capable
13	1000BASE-T Full-Duplex	RO	Always 1	Always 1	1 = 1000BASE-T full-duplex capable
12	1000BASE-T Half-Duplex	RO	Always 1	Always 1	1 = 1000BASE-T half-duplex capable
11:0	Reserved	RO	0x000	0x000	Reserved

Table 129: Copper Specific Control Register 1
Page 0, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Disable Link Pulses	R/W	0x0	0x0	1 = Disable Link Pulse 0 = Enable Link Pulse
14:12	Downshift counter	R/W	0x3	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1x, 2x,...8x is the number of times the PHY attempts to establish Gigabit link before the PHY downshifts to the next highest speed. 000 = 1x 100 = 5x 001 = 2x 101 = 6x 010 = 3x 110 = 7x 011 = 4x 111 = 8x
11	Downshift Enable	R/W	0x0	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. 1 = Enable downshift. 0 = Disable downshift.
10	Force Copper Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. In 1000BASE-T mode this has no effect. 1 = Force link good 0 = Normal operation
9:8	Energy Detect	R/W	See Descr.	Update	Upon hardware reset both bits takes on the inverted value of DIS_SLEEP. 0x = Off 10 = Sense only on Receive (Energy Detect) 11 = Sense and periodically transmit NLP (Energy Detect+TM)
7	Enable Extended Distance	R/W	0x0	Retain	When using cable exceeding 100m, the 10BASE-T receive threshold must be lowered in order to detect incoming signals. 1 = Lower 10BASE-T receive threshold 0 = Normal 10BASE-T receive threshold

Table 129: Copper Specific Control Register 1 (Continued)
Page 0, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
6:5	MDI Crossover Mode	R/W	See Descr.	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. Upon hardware reset bits defaults as follows: ENA_XC Bits 6:5 0 01 1 11 00 = Manual MDI configuration 01 = Manual MDIX configuration 10 = Reserved 11 = Enable automatic crossover for all modes
4	Reserved	R/W	0x0	Retain	Reserved
3	Copper Transmitter Disable	R/W	0x0	Retain	1 = Transmitter Disable 0 = Transmitter Enable
2	Power Down	R/W	0x0	Retain	Power down is controlled via register 0_0.11 and 16_0.2. Both bits must be set to 0 before the PHY will transition from power down to normal operation. When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_0.15) and Restart Auto-Negotiation (0_0.9) are not set by the user. 1 = Power down 0 = Normal operation
1	Polarity Reversal Disable	R/W	0x0	Retain	If polarity is disabled, then the polarity is forced to be normal in 10BASE-T. 1 = Polarity Reversal Disabled 0 = Polarity Reversal Enabled The detected polarity status is shown in Register 17_0.1, or in 1000BASE-T mode, 21_5.3:0.
0	Disable Jabber	R/W	0x0	Retain	Jabber has effect only in 10BASE-T half-duplex mode. 1 = Disable jabber function 0 = Enable jabber function

Table 130: Copper Specific Status Register 1
Page 0, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x2	Retain	These status bits are valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex

Table 130: Copper Specific Status Register 1 (Continued)
Page 0, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled 17_0.11 = 1. 1 = Resolved 0 = Not resolved
10	Copper Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
9	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause enabled 0 = Transmit pause disable
8	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause enabled 0 = Receive pause disabled
7	Reserved	RO	0x0	0x0	Reserved
6	MDI Crossover Status	RO	0x1	Retain	This status bit is valid only after resolved bit 17_0.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. This bit is 0 or 1 depending on what is written to 16.6:5 in manual configuration mode. Register 16.6:5 are updated with software reset. 1 = MDIX 0 = MDI
5	Downshift Status	RO	0x0	0x0	1 = Downshift 0 = No Downshift
4	Copper Energy Detect Status	RO	0x0	0x0	1 = Sleep 0 = Active
3	Global Link Status	RO	0x0	0x0	1 = Copper link is up 0 = Copper link is down
2	DTE power status	RO	0x0	0x0	1 = Link partner needs DTE power 0 = Link partner does not need DTE power
1	Polarity (real time)	RO	0x0	0x0	1 = Reversed 0 = Normal Polarity reversal can be disabled by writing to Register 16_0.1. In 1000BASE-T mode, polarity of all pairs are shown in Register 21_5.3:0.
0	Jabber (real time)	RO	0x0	0x0	1 = Jabber 0 = No jabber

Table 131: Copper Specific Interrupt Enable Register
Page 0, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Auto-Negotiation Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	Reserved	R/W	0x0	Retain	Reserved
6	MDI Crossover Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
5	Downshift Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
4	Copper Energy Detect Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
3	FLP Exchange Complete but no Link Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
2	DTE power detection status changed interrupt enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1	Polarity Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
0	Jabber Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 132: Copper Interrupt Status Register
Page 0, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Copper Auto-Negotiation Error	RO,LH	0x0	0x0	An error is said to occur if MASTER/SLAVE does not resolve, parallel detect fault, no common HCD, or link does not come up after negotiation is completed. 1 = Auto-Negotiation Error 0 = No Auto-Negotiation Error
14	Copper Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Copper Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed
12	Copper Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Copper Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Copper Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Copper Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	Copper False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
7	Reserved	RO	Always 0	Always 0	Reserved
6	MDI Crossover Changed	RO,LH	0x0	0x0	1 = Crossover changed 0 = Crossover not changed
5	Downshift Interrupt	RO,LH	0x0	0x0	1 = Downshift detected 0 = No down shift
4	Copper Energy Detect Changed	RO,LH	0x0	0x0	1 = Energy Detect state changed 0 = No Energy Detect state change detected
3	FLP Exchange Complete but no Link	RO,LH	0x0	0x0	1 = FLP Exchange Completed but Link Not Established 0 = No Event Detected
2	DTE power detection status changed interrupt	RO,LH	0x0	0x0	1 = DTE power detection status changed 0 = No DTE power detection status change detected
1	Polarity Changed	RO,LH	0x0	0x0	1 = Polarity Changed 0 = Polarity not changed
0	Jabber	RO,LH	0x0	0x0	1 = Jabber 0 = No jabber

Table 133: Copper Specific Control Register 2
Page 0, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x000	Retain	Reserved
7	10BASE-Teee Enable	R/W	0x0	Retain	1 = 10BASE-Teee Enabled 0 = 10BASE-Teee Disabled
6	Break Link On Insufficient IPG	R/W	0x0	Retain	0 = Break link on insufficient IPGs in 10BASE-T and 100BASE-TX. 1 = Do not break link on insufficient IPGs in 10BASE-T and 100BASE-TX.
5	100 BASE-T Transmitter Clock Source	R/W	0x1	Update	1 = Local Clock 0 = Recovered Clock
4	Accelerate 100BASE-T Link Up	R/W	0x0	Retain	0 = No Acceleration 1 = Accelerate
3	Reverse MDIP/N[3] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity, 1 = Reverse Transmit Polarity
2	Reverse MDIP/N[2] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity, 1 = Reverse Transmit Polarity
1	Reverse MDIP/N[1] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity, 1 = Reverse Transmit Polarity
0	Reverse MDIP/N[0] Transmit Polarity	R/W	0x0	Retain	0 = Normal Transmit Polarity, 1 = Reverse Transmit Polarity

Table 134: Copper Specific Receive Error Counter Register
Page 0, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported.

Table 135: Page Address
Page Any, Register 22

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Ignore PHYAD[4:2]	R/W	0x0	Retain	0 = Use PHYAD[4:2] to decode write commands 1 = Ignore PHYAD[4:2] to decode write commands
14	Ignore PHYAD[1:0]	R/W	0x0	Retain	0 = Use PHYAD[1:0] to decode write commands 1 = Ignore PHYAD[1:0] to decode write commands
13:8	Reserved	RO	0x00	0x00	Reserved
7:0	Page select for registers 0 to 28	R/W	0x00	Retain	Page Number

Table 136: Global Interrupt Status
Page 0, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	Reserved
3:0	Port X Interrupt	RO	0x0	0x0	1 = Interrupt active on port X 0 = No interrupt active on port X

Table 137: Copper Specific Control Register 3
Page 0, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	Reserved
14	Reserved	R/W	0x0	Retain	Reserved
13	Reserved	R/W	0x0	Retain	Reserved
12	Reserved	R/W	0x0	Retain	Reserved
11:10	Gigabit Link Down Delay	R/W	0x0	Retain	This register only have effect if register 26_0.9 is set to 1. 00 = 0ms 01 = 10 ± 2ms 10 = 20 ± 2ms 11 = 40 ± 2ms
9	Speed Up Gigabit Link Down Time	R/W	0x0	Retain	1 = Enable faster gigabit link down 0 = Use IEEE gigabit link down
8	DTE detect enable	R/W	0x0	Update	1 = Enable DTE detection 0 = Disable DTE detection
7:4	DTE detect status drop hysteresis	R/W	0x4	Retain	0000: report immediately 0001: report 5s after DTE power status drop ... 1111: report 75s after DTE power status drop
3:2	100 MB test select	R/W	0x0	Retain	0x = Normal Operation 10 = Select 112 ns sequence 11 = Select 16 ns sequence
1	10 BT polarity force	R/W	0x0	Retain	1 = Force negative polarity for Receive only 0 = Normal Operation
0	Reserved	R/W	0x0	Retain	Reserved

Table 138: Fiber Control Register
Page 1, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Fiber Reset	R/W	0x0	SC	Fiber Software Reset. Affects page 1. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD of the internal bus is looped back to RXD of the internal bus. Link is broken when loopback is enabled. Loopback speed is determined by the mode the device is in. 1000BASE-X - loopback is always in 1000Mbps. 100BASE-FX - loopback is always in 100Mbps. 1 = Enable Loopback 0 = Disable Loopback
13	Speed Select (LSB)	RO, R/W	0x0	Retain	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is always 1. If register 16_1.1:0 (MODE[1:0]) = 01 then this bit is always 0. If register 16_1.1:0 (MODE[1:0]) = 10 then this bit is 1 when the PHY is at 100 Mbps, else it is 0. If register 16_1.1:0 (MODE[1:0]) = 11 then this bit is R/W. bit 6,13 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
12	Auto-Negotiation Enable	R/W	See Descr	Retain	If the value of this bit is changed, the link will be broken and Auto-Negotiation Restarted This bit has no effect when in 100BASE-FX mode When this bit gets set/reset, Auto-negotiation is restarted (bit 0_1.9 is set to 1). On hardware reset this bit takes on the value of S_ANEG 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	Power Down	R/W	See Descr	0x0	When the port is switched from power down to normal operation, software reset and restart Auto-Negotiation are performed even when bits Reset (0_1.15) and Restart Auto-Negotiation (0_1.9) are not set by the user. On hardware reset, bit 0_1.11 takes on the value of PDOWN and (MODE[2:0] = 01x or 11x or 100) 1 = Power down 0 = Normal operation
10	Isolate	RO	0x0	0x0	This function is not supported

Table 138: Fiber Control Register (Continued)
Page 1, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
9	Restart Fiber Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware, software reset (0_1.15) or change in auto-negotiation enable (0_1.12) regardless of whether or not the restart bit (0_1.9) is set. The bit is set when Auto-negotiation is Enabled or Disabled in 0_1.12 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Duplex Mode	R/W	0x1	Retain	Writing this bit has no effect unless one of the following events occur: Software reset is asserted (Register 0_1.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Auto-Negotiation Enable changes (Register 0_1.12) Power down (Register 0_1.11) transitions from power down to normal operation 1 = Full-duplex 0 = Half-duplex
7	Collision Test	RO	0x0	0x0	This bit has no effect.
6	Speed Selection (MSB)	RO, R/W	0x1	Retain	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is always 0. If register 16_1.1:0 (MODE[1:0]) = 01 then this bit is always 1. If register 16_1.1:0 (MODE[1:0]) = 10 then this bit is 1 when the PHY is at 1000 Mbps, else it is 0. If register 16_1.1:0 (MODE[1:0]) = 11 then this bit is R/W. bit 6,13 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
5:0	Reserved	RO	Always 000000	Always 000000	Reserved

Table 139: Fiber Status Register
Page 1, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	Always 0	Always 0	100BASE-T4. This protocol is not available. 0 = PHY not able to perform 100BASE-T4
14	100BASE-X Full-Duplex	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 1, else this bit is 0. bit 6,13 1 = PHY able to perform full duplex 100BASE-X 0 = PHY not able to perform full duplex 100BASE-X
13	100BASE-X Half-Duplex	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 1, else this bit is 0. bit 6,13 1 = PHY able to perform half-duplex 100BASE-X 0 = PHY not able to perform half-duplex 100BASE-X
12	10 Mbps Full Duplex	RO	Always 0	Always 0	0 = PHY not able to perform full-duplex 10BASE-T
11	10 Mbps Half-Duplex	RO	Always 0	Always 0	0 = PHY not able to perform half-duplex 10BASE-T
10	100BASE-T2 Full-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform full-duplex
9	100BASE-T2 Half-Duplex	RO	Always 0	Always 0	This protocol is not available. 0 = PHY not able to perform half-duplex
8	Extended Status	RO	Always 1	Always 1	1 = Extended status information in Register 15
7	Reserved	RO	Always 0	Always 0	Reserved
6	MF Preamble Suppression	RO	Always 1	Always 1	1 = PHY accepts management frames with preamble suppressed
5	Fiber Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete Bit is not set when link is up due of Fiber Auto-negotiation Bypass or if Auto-negotiation is disabled.
4	Fiber Remote Fault	RO,LH	0x0	0x0	1 = Remote fault condition detected 0 = Remote fault condition not detected This bit is always 0 in SGMII modes.
3	Auto-Negotiation Ability	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 0, else this bit is 1. bit 6,13 1 = PHY able to perform Auto-Negotiation 0 = PHY not able to perform Auto-Negotiation
2	Fiber Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_1.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Reserved	RO,LH	Always 0	Always 0	Reserved
0	Extended Capability	RO	Always 1	Always 1	1 = Extended register capabilities

Table 140: PHY Identifier
Page 1, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x0141	0x0141	<p>Marvell® OUI is 0x005043</p> <p>0000 0000 0101 0000 0100 0011 ^ ^ bit 1.....bit 24</p> <p>Register 2.[15:0] show bits 3 to 18 of the OUI.</p> <p>0000000101000001 ^ ^ bit 3.....bit18</p>

Table 141: PHY Identifier
Page 1, Register 3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	OUI LSb	RO	Always 000011	Always 000011	<p>Organizationally Unique Identifier bits 19:24</p> <p>000011 ^.....^ bit 19...bit24</p>
9:4	Model Number	RO	Always 101010	Always 101010	Model Number 101010
3:0	Revision Number	RO	See Descr	See Descr	Rev Number See relevant product Release Notes for details.

Table 142: Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	<p>A write to this register bit does not take effect until any one of the following occurs:</p> <p>Software reset is asserted (Register 0_1.15) Restart Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised</p>
14	Reserved	RO	Always 0	Always 0	Reserved

Table 142: Fiber Auto-Negotiation Advertisement Register - 1000BASE-X Mode (Register 16_1.1:0 = 01) (Continued)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
13:12	Remote Fault 2/ RemoteFault 1	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down Device has no ability to detect remote fault. 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	Always 000	Always 000	Reserved
8:7	Pause	R/W	See Descr.	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down Upon hardware reset both bits takes on the value of ENA_PAUSE. 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half-Duplex	R/W	See Descr.	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down Upon hardware reset this bit takes on the value of C_ANEG[0]. 1 = Advertise 0 = Not advertised
5	1000BASE-X Full-Duplex	R/W	0x1	Retain	A write to this register bit does not take effect until any one of the following also occurs: Software reset is asserted (Register 0_1.15) Re-start Auto-Negotiation is asserted (Register 0_1.9) Power down (Register 0_1.11) transitions from power down to normal operation Link goes down 1 = Advertise 0 = Not advertised
4:0	Reserved	R/W	0x00	0x00	Reserved

Table 143: Fiber Auto-Negotiation Advertisement Register - SGMII (System mode) (Register 16_1.1:0 = 10)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link Status	RO	0x0	0x0	0 = Link is Not up on the Copper Interface 1 = Link is up on the Copper Interface
14	Reserved	RO	Always 0	Always 0	Reserved
13	Reserved	RO	Always 0	Always 0	Reserved
12	Duplex Status	RO	0x0	0x0	0 = Interface Resolved to Half-duplex 1 = Interface Resolved to Full-duplex
11:10	Speed[1:0]	RO	0x0	0x0	00 = Interface speed is 10 Mbps 01 = Interface speed is 100 Mbps 10 = Interface speed is 1000 Mbps 11 = Reserved
9	Transmit Pause	RO	0x0	0x0	Note that if register 16_1.7 is set to 0 then this bit is always forced to 0. 0 = Disabled, 1 = Enabled
8	Receive Pause	RO	0x0	0x0	Note that if register 16_1.7 is set to 0 then this bit is always forced to 0. 0 = Disabled, 1 = Enabled
7	Fiber/Copper	RO	0x0	0x0	Note that if register 16_1.7 is set to 0 then this bit is always forced to 0. 0 = Copper media, 1 = Fiber media
6:0	Reserved	RO	Always 0000001	Always 0000001	Reserved

Table 144: Fiber Auto-Negotiation Advertisement Register - SGMII (Media mode) (Register 16_1.1:0 = 11)
Page 1, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RO	Always 0x0001	Always 0x0001	Reserved

Table 145: Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Link partner capable of next page 0 = Link partner not capable of next page

**Table 145: Fiber Link Partner Ability Register - 1000BASE-X Mode (Register 16_1.1:0 = 01)
(Continued)**

Bits	Field	Mode	HW Rst	SW Rst	Description
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:12	Remote Fault 2/ Remote Fault 1	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 13:12 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	0x0	0x0	Reserved
8:7	Asymmetric Pause	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 8:7 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 6 1 = Link partner capable of 1000BASE-X half-duplex. 0 = Link partner not capable of 1000BASE-X half-duplex.
5	1000BASE-X Full-Duplex	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word bit 5 1 = Link partner capable of 1000BASE-X full-duplex. 0 = Link partner not capable of 1000BASE-X full-duplex.
4:0	Reserved	RO	0x00	0x00	Reserved

**Table 146: Fiber Link Partner Ability Register - SGMII (System mode) (Register 16_1.1:0 = 10)
Page 1, Register 5**

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Reserved
14	Acknowledge	RO	0x0	0x0	Acknowledge Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:0	Reserved	RO	0x0000	0x0000	Reserved

Table 147: Fiber Link Partner Ability Register - SGMII (Media mode) (Register 16_1.1:0 = 11)
Page 1, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Copper Link is up on the link partner 0 = Copper Link is not up on the link partner
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13	Reserved	RO	0x0	0x0	Reserved
12	Duplex Status	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 12 1 = Copper Interface on the link Partner is capable of Full-duplex 0 = Copper Interface on the link partner is capable of Half-duplex
11:10	Speed Status	RO	0x0	0x0	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:10 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved
9	Transmit Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 9 0 = Disabled, 1 = Enabled
8	Receive Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 8 0 = Disabled, 1 = Enabled
7	Fiber/Copper Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 7 0 = Copper media, 1 = Fiber media
6:0	Reserved	RO	0x00	0x00	Reserved

Table 148: Fiber Auto-Negotiation Expansion Register
Page 1, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	Reserved
3	Link Partner Next page Able	RO	0x0	0x0	SGMII and 100BASE-FX modes this bit is always 0. In 1000BASE-X mode register 6_1.3 is set when a base page is received and the received link control word has bit 15 set to 1. The bit is cleared when link goes down. 1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able
2	Local Next Page Able	RO	Always 1	Always 1	1 = Local Device is Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 6_1.1 is set when a valid page is received. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	This bit is set when there is sync status, the fiber receiver has received 3 non-zero matching valid configuration code groups and Auto-negotiation is enabled in register 0_1.12 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 149: Fiber Next Page Transmit Register
Page 1, Register 7

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to register 7_1 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. Register 7_1 only has effect in the 1000BASE-X mode. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11. This bit is internally set to the opposite value each time a page is received
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Table 150: Fiber Link Partner Next Page Register
Page 1, Register 8

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Register 8_1 only has effect in the 1000BASE-X mode. The register is loaded only when a next page is received from the link partner. It is cleared each time the link goes down. Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/ Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Table 151: Extended Status Register
Page 1, Register 15

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full-Duplex	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 0, else this bit is 1. 1 = 1000BASE-X full duplex capable 0 = not 1000BASE-X full duplex capable
14	1000BASE-X Half-Duplex	RO	See Descr	See Descr	If register 16_1.1:0 (MODE[1:0]) = 00 then this bit is 0, else this bit is 1. 1 = 1000BASE-X half duplex capable 0 = not 1000BASE-X half duplex capable
13	1000BASE-T Full-Duplex	RO	0x0	0x0	0 = not 1000BASE-T full duplex capable
12	1000BASE-T Half-Duplex	RO	0x0	0x0	0 = not 1000BASE-T half duplex capable
11:0	Reserved	RO	0x000	0x000	Reserved

Table 152: Fiber Specific Control Register 1
Page 1, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Fiber Transmit FIFO Depth	R/W	0x1	Retain	00 = ± 16 Bits 01 = ± 24 Bits 10 = ± 32 Bits 11 = ± 40 Bits
13	Block Carrier Extension Bit	R/W	0x0	Retain	Carrier extension and carrier extension with error are converted to idle symbols on the RXD only during full duplex mode. 1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension

Table 152: Fiber Specific Control Register 1
Page 1, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
12	SERDES Loop-back	R/W	0x0	0x0	Register 16_1.8 selects the line loopback path. 1 = Enable loopback from SERDES input to SERDES output 0 = Normal Operation
11	Assert CRS on Transmit	R/W	0x0	Retain	This bit has no effect in full-duplex. 1 = Assert on transmit 0 = Never assert on transmit
10	Force Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. 1 = Force link good 0 = Normal operation
9	Reserved	R/W	0x0	Retain	Reserved
8	SERDES Loop-back Type	R/W	0x0	Retain	0 = Loopback Through PCS (Tx and Rx can be asynchronous) 1 = Loopback raw 10 bit data (Tx and Rx must be synchronous)
7:6	Enhanced SGMII	R/W	0x1	Update	00 = Do not pass Flow Control through SGMII Auto-negotiation 01 = Pass Flow Control through SGMII Auto-negotiation (MODE 1 – Marvell Legacy Mode) 10 = Pass Flow Control through SGMII Auto-negotiation (MODE 2) 11 = Reserved
5:4	Reserved	R/W	0x0	Retain	Reserved
3	MAC Interface Power Down	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. This bit determines whether MAC interface powers down when Register 0_1.11 is used to power down the device or when the PHY enters the energy detect state. 1 = Always power up 0 = Can power down
2	Reserved	R/W	0x1	Retain	Must set to 1
1:0	MODE[1:0]	RO	See Desc.	See Desc.	These bits reflect the mode as programmed in register of 20_18.2:0 00 = 100BASE-FX 01 = 1000BASE-X 10 = SGMII System mode 11 = SGMII Media mode

Table 153: Fiber Specific Status Register
Page 1, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x0	Retain	These status bits are valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit is always 01. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit follows register 0_1.8. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	In 100BASE-FX mode this bit is always 0. 1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled or in 100BASE-FX mode this bit is always 1. 1 = Resolved 0 = Not resolved If bit 26_1.5 is 1, then this bit will be 0.
10	Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
9:6	Reserved	RO	Always 00000	Always 00000	Reserved
5	Sync status	RO	0x0	0x0	1 = Sync 0 = No Sync
4	Fiber Energy Detect Status	RO	0x1	0x1	1 = No energy detected 0 = Energy Detected
3	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit is always 0. 1 = Transmit pause enabled 0 = Transmit pause disable
2	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_1.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit is always 0. 1 = Receive pause enabled 0 = Receive pause disabled

Table 153: Fiber Specific Status Register (Continued)

Page 1, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
1:0	Reserved	RO	Always 00	Always 00	Reserved

Table 154: Fiber Interrupt Enable Register

Page 1, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Reserved
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	FIFO Over/Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6:5	Reserved	RO	Always 00	Always 00	Reserved
4	Fiber Energy Detect Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
3:0	Reserved	RO	Always 0000	Always 0000	Reserved

Table 155: Fiber Interrupt Status Register

Page 1, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0	Always 0	Reserved
14	Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed

Table 155: Fiber Interrupt Status Register (Continued)

Page 1, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
7	FIFO Over/Underflow	RO,LH	0x0	0x0	1 = Over/Underflow Error 0 = No FIFO Error
6:5	Reserved	RO	Always 00	Always 00	Reserved
4	Fiber Energy Detect Changed	RO,LH	0x0	0x0	1 = Energy Detect state changed 0 = No Energy Detect state change detected
3:0	Reserved	RO	Always 00000	Always 00000	Reserved

Table 156: Fiber Receive Error Counter Register

Page 1, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported.

Table 157: PRBS Control

Page 1, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Reserved
7	Invert Checker Polarity	R/W	0x0	Retain	0 = Normal 1 = Invert
6	Invert Generator Polarity	R/W	0x0	Retain	0 = Normal 1 = Invert
5	PRBS Lock	R/W	0x0	Retain	0 = Counter Free Runs 1 = Do not start counting until PRBS locks first
4	Clear Counter	R/W, SC	0x0	0x0	0 = Normal 1 = Clear Counter
3:2	Pattern Select	R/W	0x0	Retain	00 = PRBS 7, $x^7 + x^6 + 1 = 0$ 01 = PRBS 23, $x^{23} + x^{18} + 1 = 0$ 10 = PRBS 31, $x^{31} + x^{28} + 1 = 0$ 11 = Generate 10101010... pattern
1	PRBS Checker Enable	R/W	0x0	0x0	0 = Disable 1 = Enable

Table 157: PRBS Control
Page 1, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
0	PRBS Generator Enable	R/W	0x0	0x0	0 = Disable 1 = Enable

Table 158: PRBS Error Counter LSB
Page 1, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count LSB	RO	0x0000	Retain	A read to this register freezes register 25_1. Cleared only when register 23_1.4 is set to 1.

Table 159: PRBS Error Counter MSB
Page 1, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count MSB	RO	0x0000	Retain	This register does not update unless register 24_1 is read first. Cleared only when register 23_1.4 is set to 1.

Table 160: Fiber Specific Control Register 2
Page 1, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	Reserved
14	1000BASE-X Noise Filtering	R/W	0x0	Retain	1 = Enable 0 = Disable
13	100BASE-FX Noise Filtering	R/W	0x0	Retain	1 = Enable 0 = Disable
12:10	Reserved	R/W	0x0	Update	Reserved
9	FEFI Enable	R/W	0x0	Retain	100BASE-FX FEFI 1 = Enable 0 = Disable
8	Reserved	R/W	0x0	Retain	Reserved
7	Reserved	R/W	0x0	Update	Reserved
6	Serial Interface Auto-Negotiation bypass enable	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. 1 = Bypass Allowed 0 = No Bypass Allowed
5	Serial Interface Auto-Negotiation bypass status	RO	0x0	0x0	1 = Serial interface link came up because bypass mode timer timed out and fiber Auto-Negotiation was bypassed. 0 = Serial interface link came up because regular fiber Auto-Negotiation completed. If this bit is 1, then bit 17_1.11 will be 0.
4	Reserved	R/W	0x0	Update	Reserved

Table 160: Fiber Specific Control Register 2 (Continued)

Page 1, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
3	Fiber Transmitter Disable	R/W	0x0	Retain	1 = Transmitter Disable 0 = Transmitter Enable
2:0	SGMII/Fiber Output Amplitude	R/W	0x2	Retain	Differential voltage peak measured. See AC/DC section for valid VOD values. 000 = 14mV 001 = 112mV 010 = 210 mV 011 = 308mV 100 = 406mV 101 = 504mV 110 = 602mV 111 = 700mV

Table 161: MAC Specific Control Register 1

Page 2, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Copper Transmit FIFO Depth	R/W	0x1	Retain	00 = ± 16 Bits 01 = ± 24 Bits 10 = ± 32 Bits 11 = ± 40 Bits
13:4	Reserved	R/W	0x200	Retain	Reserved
3	MAC Interface Power Down	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. This bit determines whether the MAC Interface powers down when Register 0_0.11, 16_0.2 are used to power down the device or when the PHY enters the energy detect state. 1 = Always power up 0 = Can power down
2:0	Reserved	R/W	0x0	Retain	Reserved

Table 162: MAC Specific Interrupt Enable Register

Page 2, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	00000000
7	FIFO Over/Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6:4	Reserved	R/W	0x0	Retain	000
3	FIFO Idle Inserted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable

Table 162: MAC Specific Interrupt Enable Register
Page 2, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
2	FIFO Idle Deleted Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
1:0	Reserved	R/W	0x0	Retain	00

Table 163: MAC Specific Status Register
Page 2, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	Always 00	Always 00	Reserved
7	Copper FIFO Over/Underflow	RO,LH	0x0	0x0	1 = Over/Underflow Error 0 = No FIFO Error
6:4	Reserved	RO	Always 0	Always 0	Reserved
3	Copper FIFO Idle Inserted	RO,LH	0x0	0x0	1 = Idle Inserted 0 = No Idle Inserted
2	Copper FIFO Idle Deleted	RO,LH	0x0	0x0	1 = Idle Deleted 0 = Idle not Deleted
1:0	Reserved	RO	Always 0	Always 0	Reserved

Table 164: MAC Specific Control Register 2
Page 2, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	0x0	Reserved
14	Copper Line Loopback	R/W	0x0	0x0	1 = Enable Loopback of MDI to MDI 0 = Normal Operation
13:12	Reserved	R/W	0x1	Update	Reserved
11:7	Reserved	R/W	0x00	0x00	Reserved
6	Reserved	R/W	0x1	Update	Reserved
5:4	Reserved	R/W	0x0	Retain	Reserved
3	Block Carrier Extension Bit	R/W	0x0	Retain	1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension
2:0	Default MAC interface speed	R/W	0x6	Update	Changes to these bits are disruptive to the normal operation; therefore, any changes to these registers must be followed by software reset to take effect. MAC Interface Speed during Link down while Auto-Negotiation is enabled. Bit Speed 0XX = Reserved 100 = 10 Mbps 101 = 100 Mbps 110 = 1000 Mbps 111 = Reserved

Table 165: LED[3:0] Function Control Register
Page 3, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	LED[3] Control	R/W	0x1	Retain	<p>If 16_3.11:10 is set to 11 then 16_3.15:12 has no effect</p> <p>0000 = On - Fiber Link, Off - Else</p> <p>0001 = On - Link, Blink - Activity, Off - No Link</p> <p>0010 = On - Link, Blink - Receive, Off - No Link</p> <p>0011 = On - Activity, Off - No Activity</p> <p>0100 = Blink - Activity, Off - No Activity</p> <p>0101 = Reserved</p> <p>0110 = On - 10 Mbps or 1000 Mbps Master, Off - Else</p> <p>0111 = On - Full-duplex, Off - Half-duplex</p> <p>1000 = Force Off</p> <p>1001 = Force On</p> <p>1010 = Force Hi-Z</p> <p>1011 = Force Blink</p> <p>11xx = Reserved</p>
11:8	LED[2] Control	R/W	0x7	Retain	<p>0000 = On - Link, Off - No Link</p> <p>0001 = On - Link, Blink - Activity, Off - No Link</p> <p>0010 = Reserved</p> <p>0011 = On - Activity, Off - No Activity</p> <p>0100 = Blink - Activity, Off - No Activity</p> <p>0101 = On - Transmit, Off - No Transmit</p> <p>0110 = On - 10/1000 Mbps Link, Off - Else</p> <p>0111 = On - 10 Mbps Link, Off - Else</p> <p>1000 = Force Off</p> <p>1001 = Force On</p> <p>1010 = Force Hi-Z</p> <p>1011 = Force Blink</p> <p>1100 = MODE 1 (Dual LED mode)</p> <p>1101 = MODE 2 (Dual LED mode)</p> <p>1110 = MODE 3 (Dual LED mode)</p> <p>1111 = MODE 4 (Dual LED mode)</p>
7:4	LED[1] Control	R/W	0x7	Retain	<p>If 16_3.3:2 is set to 11 then 16_3.7:4 has no effect</p> <p>0000 = On - Copper Link, Off - Else</p> <p>0001 = On - Link, Blink - Activity, Off - No Link</p> <p>0010 = On - Link, Blink - Receive, Off - No Link</p> <p>0011 = On - Activity, Off - No Activity</p> <p>0100 = Blink - Activity, Off - No Activity</p> <p>0101 = On - 100 Mbps Link or Fiber Link, Off - Else</p> <p>0110 = On - 100/1000 Mbps Link, Off - Else</p> <p>0111 = On - 100 Mbps Link, Off - Else</p> <p>1000 = Force Off</p> <p>1001 = Force On</p> <p>1010 = Force Hi-Z</p> <p>1011 = Force Blink</p> <p>11xx = Reserved</p>

Table 165: LED[3:0] Function Control Register (Continued)

Page 3, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	LED[0] Control	R/W	0x7	Retain	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000 Mbps 2 blinks - 100 Mbps 1 blink - 10 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)

Table 166: LED[3:0] Polarity Control Register

Page 3, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	LED[5], LED[3], LED[1] mix percentage	R/W	0x8	Retain	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0%, 0001 = 12.5%,..., 0111 = 87.5%, 1000 = 100% 1001 to 1111 = Reserved
11:8	LED[4], LED[2], LED[0] mix percentage	R/W	0x8	Retain	When using 2 terminal bi-color LEDs the mixing percentage should not be set greater than 50%. 0000 = 0%, 0001 = 12.5%,..., 0111 = 87.5%, 1000 = 100% 1001 to 1111 = Reserved
7:6	LED[3] Polarity	R/W	0x0	Retain	00 = On - drive LED[3] low, Off - drive LED[3] high 01 = On - drive LED[3] high, Off - drive LED[3] low 10 = On - drive LED[3] low, Off - tristate LED[3] 11 = On - drive LED[3] high, Off - tristate LED[3]
5:4	LED[2] Polarity	R/W	0x0	Retain	00 = On - drive LED[2] low, Off - drive LED[2] high 01 = On - drive LED[2] high, Off - drive LED[2] low 10 = On - drive LED[2] low, Off - tristate LED[2] 11 = On - drive LED[2] high, Off - tristate LED[2]
3:2	LED[1] Polarity	R/W	0x0	Retain	00 = On - drive LED[1] low, Off - drive LED[1] high 01 = On - drive LED[1] high, Off - drive LED[1] low 10 = On - drive LED[1] low, Off - tristate LED[1] 11 = On - drive LED[1] high, Off - tristate LED[1]
1:0	LED[0] Polarity	R/W	0x0	Retain	00 = On - drive LED[0] low, Off - drive LED[0] high 01 = On - drive LED[0] high, Off - drive LED[0] low 10 = On - drive LED[0] low, Off - tristate LED[0] 11 = On - drive LED[0] high, Off - tristate LED[0]

Table 167: LED Timer Control Register
Page 3, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force INT	R/W	0x0	Retain	1 = Interrupt pin forced to be asserted 0 = Normal Operation
14:12	Pulse stretch duration	R/W	0x4	Retain	000 = no pulse stretching 001 = 21 ms to 42ms 010 = 42 ms to 84ms 011 = 84 ms to 170ms 100 = 170 ms to 340ms 101 = 340 ms to 670ms 110 = 670 ms to 1.3s 111 = 1.3s to 2.7s
11	Reserved	R/W	0x1	Retain	Reserved
10:8	Blink Rate	R/W	0x3	Retain	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
7:4	Reserved	R/W	0x0	Retain	0000
3:2	Speed Off Pulse Period	R/W	0x1	Retain	00 = 84ms, 01 = 170ms, 10 = 340ms, 11 = 670ms
1:0	Speed On Pulse Period	R/W	0x1	Retain	00 = 84ms, 01 = 170ms, 10 = 340ms, 11 = 670ms

Table 168: LED[5:4] Function Control and Polarity Register
Page 3, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LED[3] function pin mapping	R/W	0x0	Retain	0 = Map LED[3] function to LED[3] pin 1 = Map LED[5] function to LED[3] pin
14	LED[2] function pin mapping	R/W	0x0	Retain	0 = Map LED[2] function to LED[2] pin 1 = Map LED[4] function to LED[2] pin
13:12	Reserved	R/W	0x0	Retain	Reserved
11:10	LED[5] Polarity	R/W	0x0	Retain	00 = On - drive LED[5] low, Off - drive LED[5] high 01 = On - drive LED[5] high, Off - drive LED[5] low 10 = On - drive LED[5] low, Off - tristate LED[5] 11 = On - drive LED[5] high, Off - tristate LED[5]
9:8	LED[4] Polarity	R/W	0x0	Retain	00 = On - drive LED[4] low, Off - drive LED[4] high 01 = On - drive LED[4] high, Off - drive LED[4] low 10 = On - drive LED[4] low, Off - tristate LED[4] 11 = On - drive LED[4] high, Off - tristate LED[4]

Table 168: LED[5:4] Function Control and Polarity Register (Continued)
Page 3, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
7:4	LED[5] Control	R/W	0x7	Retain	If 19_3.3:2 is set to 11 then 19_3.7:4 has no effect 0000 = On - Receive, Off - No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Full-duplex, Off - Half-duplex 0111 = On - Full-duplex, Blink - Collision Off - Half-duplex 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved
3:0	LED[4] Control	R/W	0x3	Retain	0000 = On - Receive, Off - No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Full-duplex, Off - Half-duplex 0111 = On - Full-duplex, Blink - Collision Off - Half-duplex 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)

Table 169: LED Random Blinking Control 1 Register
Page 3, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Random Re-seed	R/W, SC	0x0	Retain	Re-seed random LED blinking circuit
14:6	Reserved	RO	0x0	0	Reserved
5:4	Trigger Time Interval	R/W	0x0	Retain	Trigger time interval.
3	Random LED Blinking Enable	R/W	0x0	Retain	0 = Disable Random LED Blinking 1 = Enable Random LED Blinking
2	Reserved	RO	0x0	0	Reserved
1:0	Random Scale Selection	R/W	0x3	Retain	Randomized led blinking timer scale select (the blinking cycle is within the following range) 00 = $\pm 3.125\%$ 01 = $\pm 6.250\%$ 10 = $\pm 12.50\%$ 11 = $\pm 25.00\%$

Table 170: LED Random Blinking Control 2 Register
Page 3, Register 29

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Polynomial Enable	R/W	0x0	Retain	0 = Disable user defined LFSR polynomial 1 = Enable user defined LFSR polynomial
14	Reserved	RO	0x0	0	Reserved
13:0	Polynomial	R/W	0x0	Retain	User defined LSFR polynomial

Table 171: QSGMII Control Register
Page 4, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x0	0x0	QSGMII Port Software Reset. Affects bank 4. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD of the internal bus is looped back to RXD of the internal bus. Link is broken when loopback is enabled. 1 = Enable Loopback 0 = Disable Loopback
13	Speed Select (LSB)	RO, R/W	0x0	See Descr/ Retain	If register 16_4.0 = 0 then this bit follows the network speed. If register 16_4.0 = 1 then this bit is R/W. bit 6,13 10 = 1000 Mbps 01 = 100Mbps
12	Auto-Negotiation Enable	R/W	See Descr	Retain	If the value of this bit is changed, the link will be broken and Auto-Negotiation Restarted When this bit gets set/reset, Auto-negotiation is restarted (bit 0_4.9 is set to 1). On hardware reset this bit takes on the value of S_ANEG 1 = Enable Auto-Negotiation Process 0 = Disable Auto-Negotiation Process
11	Power Down	R/W	See Descr	Retain	On hardware reset this register takes on the value of 1 if PDOWN = 1 and MODE[2:0] is 101 else takes on a value of 0. 1 = Power down 0 = Normal operation
10	Reserved	R/W	0x0	Retain	Reserved

Table 171: QSGMII Control Register (Continued)
Page 4, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
9	Restart Fiber Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware, software reset (0_4.15) or change in auto-negotiation enable (0_4.12) regardless of whether or not the restart bit (0_4.9) is set. The bit is set when Auto-negotiation is Enabled or Disabled in 0_4.12 1 = Restart Auto-Negotiation Process 0 = Normal operation
8	Reserved	RO	0x1	0x1	Reserved
7	Reserved	RO	0x0	0x0	Reserved
6	Speed Selection (MSB)	RO, R/W	0x1	See Descr/ Retain	If register 16_4.0 = 0 then this bit follows the network speed. If register 16_4.0 = 1 then this bit is R/W. bit 6,13 10 = 1000 Mbps 01 = 100Mbps
5:0	Reserved	RO	0x00	0x00	Reserved

Table 172: QSGMII Status Register
Page 4, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0x000	0x000	Reserved
5	Fiber Auto-Negotiation Complete	RO	0x0	0x0	1 = Auto-Negotiation process complete 0 = Auto-Negotiation process not complete Bit is not set when link is up due of Fiber Auto-negotiation Bypass or if Auto-negotiation is disabled.
4	Reserved	RO	0x0	0x0	Reserved
3	Reserved	RO	0x0	0x0	Reserved
2	Fiber Link Status	RO,LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read Register 17_4.10 Link Real Time. 1 = Link is up 0 = Link is down
1	Reserved	RO	0x0	0x0	Reserved
0	Reserved	RO	0x0	0x0	Reserved

Table 173: QSGMII Auto-Negotiation Advertisement Register - SGMII (System mode) (Register 16_4.0 = 0)
Page 4, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link Status	RO	0x0	0x0	0 = Link is Not up on the Copper Interface 1 = Link is up on the Copper Interface
14	Reserved	RO	0x0	0x0	Reserved
13	Reserved	RO	0x0	0x0	Reserved

Table 173: QSGMII Auto-Negotiation Advertisement Register - SGMII (System mode) (Register 16_4.0 = 0) (Continued)
Page 4, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Duplex Status	RO	0x0	0x0	0 = Interface Resolved to Half-duplex 1 = Interface Resolved to Full-duplex
11:10	Speed[1:0]	RO	0x0	0x0	00 = Interface speed is 10 Mbps 01 = Interface speed is 100 Mbps 10 = Interface speed is 1000 Mbps 11 = Reserved
9	Transmit Pause	RO	0x0	0x0	Note that if register 16_4.7 is set to 0 then this bit is always forced to 0. 0 = Disabled, 1 = Enabled
8	Receive Pause	RO	0x0	0x0	Note that if register 16_4.7 is set to 0 then this bit is always forced to 0. 0 = Disabled, 1 = Enabled
7	Fiber/Copper	RO	0x0	0x0	Note that if register 16_4.7 is set to 0 then this bit is always forced to 0. 0 = Copper media, 1 = Fiber media
6:0	Reserved	RO	Always 0000001	Always 0000001	Reserved

Table 174: QSGMII Auto-Negotiation Advertisement Register - SGMII (Media mode) (Register 16_4.0 = 1)
Page 4, Register 4

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Reserved	RO	Always 0x0001	Always 0x0001	Reserved

Table 175: QSGMII Link Partner Ability Register - SGMII (System mode) Mode (Register 16_4.0 = 0)
Page 4, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Reserved
14	Acknowledge	RO	0x0	0x0	Acknowledge Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13:0	Reserved	RO	0x0000	0x0000	Reserved

Table 176: QSGMII Link Partner Ability Register - SGMII (Media mode) Mode (Register 16_4.0 = 1)
Page 4, Register 5

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Link	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 15 1 = Copper Link is up on the link partner 0 = Copper Link is not up on the link partner
14	Acknowledge	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Acknowledge Received Code Word Bit 14 1 = Link partner received link code word 0 = Link partner has not received link code word
13	Reserved	RO	0x0	0x0	Reserved
12	Duplex Status	RO	0x0	0x0	Register bit is cleared when link goes down and loaded when a base page is received Received Code Word Bit 12 1 = Copper Interface on the link Partner is capable of Full-duplex 0 = Copper Interface on the link partner is capable of Half-duplex
11:10	Speed Status	RO	0x0	0x0	Register bits are cleared when link goes down and loaded when a base page is received Received Code Word Bit 11:10 00 = 10 Mbps 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved
9	Transmit Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 9 0 = Disabled, 1 = Enabled
8	Receive Pause Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 8 0 = Disabled, 1 = Enabled
7	Fiber/Copper Status	RO	0x0	0x0	This bit is non-zero only if the link partner supports enhanced SGMII auto negotiation. Received Code Word Bit 7 0 = Copper media, 1 = Fiber media
6:0	Reserved	RO	0x00	0x00	Reserved

Table 177: QSGMII Auto-Negotiation Expansion Register
Page 4, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	Reserved
3	Link Partner Next page Able	RO	0x0	0x0	1 = Link Partner is Next Page able 0 = Link Partner is not Next Page able

Table 177: QSGMII Auto-Negotiation Expansion Register
Page 4, Register 6

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Local Next Page Able	RO	0x0	0x0	1 = Local Device is Next Page able
1	Page Received	RO, LH	0x0	0x0	Register 6_4.1 is set when a valid page is received. 1 = A New Page has been received 0 = A New Page has not been received
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	This bit is set when there is sync status, the fiber receiver has received 3 non-zero matching valid configuration code groups and Auto-negotiation is enabled in register 0_4.12 1 = Link Partner is Auto-Negotiation able 0 = Link Partner is not Auto-Negotiation able

Table 178: QSGMII Specific Control Register 1
Page 4, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Transmit FIFO Depth	R/W	0x1	Retain	00 = ± 16 Bits 01 = ± 24 Bits 10 = ± 32 Bits 11 = ± 40 Bits
13	Block Carrier Extension Bit	R/W	0x1	Retain	Carrier extension and carrier extension with error are converted to idle symbols on the RXD only during full duplex mode. 1 = Enable Block Carrier Extension 0 = Disable Block Carrier Extension
12	QSGMII Loop-back	R/W	0x0	0x0	1 = Enable loopback from QSGMII input to QSGMII output 0 = Normal operation
11	Reserved	R/W	0x0	Retain	Reserved
10	Force Link Good	R/W	0x0	Retain	If link is forced to be good, the link state machine is bypassed and the link is always up. 1 = Force link good 0 = Normal operation
9	Serial Interface Auto-Negotiation bypass enable	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; hence, any changes to these registers must be followed by software reset to take effect. 1 = Bypass Allowed 0 = No Bypass Allowed
8	Reserved	R/W	0x0	Retain	Reserved
7:6	Enhanced SGMII	R/W	0x1	Update	00 = Do not pass Flow Control through SGMII Auto-negotiation 01 = Pass Flow Control through SGMII Auto-negotiation (MODE 1 – Marvell Legacy Mode) 10 = Pass Flow Control through SGMII Auto-negotiation (MODE 2) 11 = Reserved
5:2	Reserved	R/W	0x1	Retain	Reserved
1	Power Down on Static K Symbol	R/W	0x0	Retain	1 = Automatically power down device when static K28.5 or K28.1 is received on the QSGMII. 0 = Do not automatically power down.

Table 178: QSGMII Specific Control Register 1 (Continued)

Page 4, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
0	Mode	R/W	See Desc.	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. On hardware reset the register default to 1 if MODE[2:0] is 101, else the register defaults to 0. 0 = SGMII System mode 1 = SGMII Media mode

Table 179: QSGMII Specific Status Register

Page 4, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x0	Retain	These status bits are valid only after resolved bit 17_4.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = 10 Mbps
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 17_4.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full-duplex 0 = Half-duplex
12	Page Received	RO, LH	0x0	0x0	1 = Page received 0 = Page not received
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled this bit is always 1. 1 = Resolved 0 = Not resolved
10	Link (real time)	RO	0x0	0x0	1 = Link up 0 = Link down
9	Serial Interface Auto-Negotiation bypass status	RO	0x0	0x0	1 = Serial interface link came up because bypass mode timer timed out and fiber Auto-Negotiation was bypassed. 0 = Serial interface link came up because regular fiber Auto-Negotiation completed. If this bit is 1, then bit 17_4.11 will be 0.
8:6	Reserved	RO	0x0	0x0	Reserved
5	Sync status	RO	0x0	0x0	1 = Sync 0 = No Sync
4	Reserved	RO	0x0	0x0	Reserved
3	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_4.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit is always 0. 1 = Transmit pause enabled 0 = Transmit pause disable

Table 179: QSGMII Specific Status Register (Continued)
Page 4, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
2	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 17_4.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. In 100BASE-FX mode this bit is always 0. 1 = Receive pause enabled 0 = Receive pause disabled
1:0	Reserved	RO	0x0	0x0	Reserved

Table 180: QSGMII Interrupt Enable Register
Page 4, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	Reserved
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
7	FIFO Over/Underflow Interrupt Enable	R/W	0x0	Retain	1 = Interrupt enable 0 = Interrupt disable
6:0	Reserved	R/W	0x00	Retain	Reserved

Table 181: QSGMII Interrupt Status Register
Page 4, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Reserved
14	Speed Changed	RO,LH	0x0	0x0	1 = Speed changed 0 = Speed not changed
13	Duplex Changed	RO,LH	0x0	0x0	1 = Duplex changed 0 = Duplex not changed

Table 181: QSGMII Interrupt Status Register
Page 4, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Page Received	RO,LH	0x0	0x0	1 = Page received 0 = Page not received
11	Auto-Negotiation Completed	RO,LH	0x0	0x0	1 = Auto-Negotiation completed 0 = Auto-Negotiation not completed
10	Link Status Changed	RO,LH	0x0	0x0	1 = Link status changed 0 = Link status not changed
9	Symbol Error	RO,LH	0x0	0x0	1 = Symbol error 0 = No symbol error
8	False Carrier	RO,LH	0x0	0x0	1 = False carrier 0 = No false carrier
7	FIFO Over/Underflow	RO,LH	0x0	0x0	1 = Over/Underflow Error 0 = No FIFO Error
6:0	Reserved	RO	0x00	0x00	Reserved

Table 182: QSGMII RX_ER Byte Capture
Page 4, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Capture Data Valid	RO	0x0	0x0	1 = Bits 14:0 Valid 0 = Bits 14:0 Invalid
14	Reserved	RO	0x0	0x0	Reserved
13:12	Byte Number	RO	0x0	0x0	00 = 4 bytes before RX_ER asserted 01 = 3 bytes before RX_ER asserted 10 = 2 bytes before RX_ER asserted 11 = 1 byte before RX_ER asserted The byte number increments after every read when register 20_4.15 is set to 1.
11:10	Reserved	RO	0x0	0x0	Reserved
9	RX_ER	RO	0x0	0x0	RX Error. Normally this bit will be low since the capture is triggered by RX_ER being high. However it is possible to see an RX_ER high when the capture is re-enabled after reading the fourth byte and there happens to be a long sequence of RX_ER when the capture restarts.
8	RX_DV	RO	0x0	0x0	RX Data Valid
7:0	RXD[7:0]	RO	0x00	0x00	RX Data

Table 183: QSGMII Receive Error Counter Register
Page 4, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	Counter will peg at 0xFFFF and will not roll over. Both False carrier and symbol errors are reported.

Table 184: PRBS Control
Page 4, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Reserved
7	Invert Checker Polarity	R/W	0x0	Retain	0 = Invert 1 = Normal
6	Invert Generator Polarity	R/W	0x0	Retain	0 = Invert 1 = Normal
5	PRBS Lock	R/W	0x0	Retain	0 = Counter Free Runs 1 = Do not start counting until PRBS locks first
4	Clear Counter	R/W, SC	0x0	0x0	0 = Normal 1 = Clear Counter
3:2	Pattern Select	R/W	0x0	Retain	00 = PRBS 7, $x^7 + x^6 + 1 = 0$ 01 = PRBS 23, $x^{23} + x^{18} + 1 = 0$ 10 = PRBS 31, $x^{31} + x^{28} + 1 = 0$ 11 = Generate 1010101010... pattern
1	PRBS Checker Enable	R/W	0x0	0x0	0 = Disable 1 = Enable
0	PRBS Generator Enable	R/W	0x0	0x0	0 = Disable 1 = Enable

Table 185: PRBS Error Counter LSB
Page 4, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count LSB	RO	0x0000	Retain	A read to this register freezes register 25_4. Cleared only when register 23_4.4 is set to 1.

Table 186: PRBS Error Counter MSB
Page 4, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count MSB	RO	0x0000	Retain	This register does not update unless register 24_4 is read first. Cleared only when register 23_4.4 is set to 1.

Table 187: QSGMII Global Control Register 1
Page 4, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	QSGMII Global Reset	R/W, SC	0x0	SC	QSGMII Global Software Reset. Writing a 1 to this bit cause all four ports as well as the common circuit to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation

Table 187: QSGMII Global Control Register 1 (Continued)

Page 4, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
14	QSGMII Reference Clock Source Select	R/W	0x0	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. 1 = Reserved 0 = Use XTAL_IN/REF_CLKP/N as source
13	Invert Q_INP/N Polarity	R/W	0x1	Retain	0 = Invert, 1 = Normal
12	Invert Q_OUTP/N Polarity	R/W	0x1	Retain	0 = Invert, 1 = Normal
11	QSGMII Global Power down	R/W	See Desc.	Retain	1 = Power down all four ports as well as the common circuit 0 = Power up common circuit. Per port power state is a function of register 0_4.11. On hardware reset this register takes on the value of 1 if MODE[2:0] is 001 else takes on a value of 0.
10	Reserved	R/W	0x0	Update	Reserved
9	Raw 10-bit Line Loopback	R/W	0x0	0x0	0 = Normal 1 = Loopback raw 10 bit data from QSGMII input to QSGMII output (Tx and Rx must be synchronous)
8	Reserved	R/W	0x0	Retain	Reserved
7	Reserved	R/W	0x0	Retain	Reserved
6:5	Reserved	R/W	0x0	Retain	Reserved
4	Reserved	R/W	0x0	Retain	Reserved
3	Enable Running Disparity Checking	R/W	0x0	Retain	1 = Output error symbol if running disparity is incorrect. 0 = Ignore running disparity when determining whether symbol error occurred.
2:0	Reserved	R/W	0x2	Retain	Reserved

Table 188: QSGMII Global Control Register 2

Page 4, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Chip Hardware Reset	R/W, SC	0x0	0x0	Writing a 1 to this bit cause the entire chip to hard reset 1 = PHY reset 0 = Normal operation
14	Internal QSGMII Loopback	R/W	0x0	Retain	0 = Pass data through 5.0G SERDES 1 = Loopback QSGMII data on internal bus and power down 5.0G SERDES
13:9	Reserved	R/W	0x3F	Retain	Reserved
8	Clock Cascade Enable	R/W	0x1	Retain	Clock Cascade Enable / Disable 1 = Enable 0 = Disable
7	Reserved	R/W	0x1	Retain	Reserved
6:2	Reserved	R/W	0x00	Retain	Reserved

Table 188: QSGMII Global Control Register 2
Page 4, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
1	QSGMII Output Crossover 2, 3	R/W	0x0	Retain	0 = Port 2 to QSGMII Lane 2, Port 3 to QSGMII Lane 3 1 = Port 2 to QSGMII Lane 3, Port 3 to QSGMII Lane 2
0	QSGMII Output Crossover 0, 1	R/W	0x0	Retain	0 = Port 0 to QSGMII Lane 0, Port 1 to QSGMII Lane 1 1 = Port 0 to QSGMII Lane 1, Port 1 to QSGMII Lane 0

Table 189: Advanced VCT™ TX to MDI[0] Rx Coupling
Page 5, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection, 0 = negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 100 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 100 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.



Note

This register reports the reflection see based on the setting of register 23_5.13:11
000 = MDI[0] Tx to MDI[0] Rx
100 = MDI[0] Tx to MDI[0] Rx
101 = MDI[1] Tx to MDI[0] Rx
110 = MDI[2] Tx to MDI[0] Rx
111 = MDI[3] Tx to MDI[0] Rx

Table 190: Advanced VCT™ TX to MDI[1] Rx Coupling
Page 5, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection, 0 = negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 101 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 101 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.

**Note**

This register reports the reflection see based on the setting of register 23_5.13:11

000 = MDI[1] Tx to MDI[1] Rx

100 = MDI[0] Tx to MDI[1] Rx

101 = MDI[1] Tx to MDI[1] Rx

110 = MDI[2] Tx to MDI[1] Rx

111 = MDI[3] Tx to MDI[1] Rx

Table 191: Advanced VCT™ TX to MDI[2] Rx Coupling
Page 5, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection, 0 = negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	0000000 = No reflection (0 mV) each bit above increases 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 110 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 110 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.
7:0	Distance	RO	xx	Retain	Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.



Note

This register reports the reflection see based on the setting of register 23_5.13:11
000 = MDI[2] Tx to MDI[2] Rx
100 = MDI[0] Tx to MDI[2] Rx
101 = MDI[1] Tx to MDI[2] Rx
110 = MDI[2] Tx to MDI[2] Rx
111 = MDI[3] Tx to MDI[2] Rx

Table 192: Advanced VCT™ TX to MDI[3] Rx Coupling
Page 5, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reflected Polarity	RO	xx	Retain	1 = Positive Reflection, 0 = negative reflection
14:8	Reflected Amplitude	RO	xx	Retain	<p>0000000 = No reflection (0 mV) each bit above increases 7.8125mV. When 23_5.7 = 0 and 23_5.13:11 = 000 or 111 the reflected amplitude between the thresholds specified in registers 26_5, 27_5, 28_5.6:0, 26_7, 27_7, and 28_7.6:0 are reported as 0 mV. When 23_5.7 = 0 and 23_5.13:11 is not 000 or 111 the reflected amplitude between the thresholds specified in register 25_5 and 25_7 are reported as 0 mV. When 23_5.7 = 1 the actual offset or reflected amplitude is reported and the threshold specified in registers 25_5, 26_5, 27_5, 28_5, 25_7, 26_7, 27_7, and 28_7 are ignored. The amplitude value is valid only When 23_5.14 = 1. If bit 15:8 = 0x00 indicates that the test failed.</p>
7:0	Distance	RO	xx	Retain	<p>Distance of reflection. The distance value is valid only when 23_5.7 = 0 and 23_5.14 = 1.</p>

**Note**

This register reports the reflection see based on the setting of register 23_5.13:11

000 = MDI[3] Tx to MDI[3] Rx

100 = MDI[0] Tx to MDI[3] Rx

101 = MDI[1] Tx to MDI[3] Rx

110 = MDI[2] Tx to MDI[3] Rx

111 = MDI[3] Tx to MDI[3] Rx

Table 193: 1000BASE-T Pair Skew Register
Page 5, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Pair 7,8 (MDI[3]±)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within ± 8ns. The contents of 20_5.15:0 are valid only if Register 21_5.6 = 1
11:8	Pair 4,5 (MDI[2]±)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within ± 8ns.
7:4	Pair 3,6 (MDI[1]±)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within ± 8ns.
3:0	Pair 1,2 (MDI[0]±)	RO	0x0	0x0	Skew = bit value x 8ns. Value is correct to within ± 8ns.

Table 194: 1000BASE-T Pair Swap and Polarity
Page 5, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	Reserved
6	Register 20_5 and 21_5 valid	RO	0x0	0x0	The contents of 21_5.5:0 and 20_5.15:0 are valid only if Register 21_5.6 = 1 1 = Valid 0 = Invalid
5	C, D Crossover	RO	0x0	0x0	1 = Channel C received on MDI[2]± Channel D received on MDI[3]± 0 = Channel D received on MDI[2]± Channel C received on MDI[3]±
4	A, B Crossover	RO	0x0	0x0	1 = Channel A received on MDI[0]± Channel B received on MDI[1]± 0 = Channel B received on MDI[0]± Channel A received on MDI[1]±
3	Pair 7,8 (MDI[3]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
2	Pair 4,5 (MDI[2]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
1	Pair 3,6 (MDI[1]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive
0	Pair 1,2 (MDI[0]±) Polarity	RO	0x0	0x0	1 = Negative 0 = Positive

Table 195: Advanced VCT™ Control
Page 5, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Enable Test	R/W, SC	0x0	0x0	0 = disable test, 1 = enable test This bit will self clear when the test is completed
14	Test status	RO	0x0	0x0	0 = Test not started/in progress, 1 = test completed
13:11	Transmitter Channel Select	R/W	0x0	0x0	000 - Tx 0 => Rx 0, Tx 1 => Rx 1, Tx 2 => Rx 2, Tx 3 => Rx 3. 100 - Tx 0 => Rx 0, Tx 0 => Rx 1, Tx 0 => Rx 2, Tx 0 => Rx 3. 101 - Tx 1 => Rx 0, Tx 1 => Rx 1, Tx 1 => Rx 2, Tx 1 => Rx 3. 110 - Tx 2 => Rx 0, Tx 2 => Rx 1, Tx 2 => Rx 2, Tx 2 => Rx 3. 111 - Tx 3 => Rx 0, Tx 3 => Rx 1, Tx 3 => Rx 2, Tx 3 => Rx 3. 01x - Reserved 0x1 - Reserved
10:8	Number of Sample Averaged	R/W	0x6	Retain	0 = 2 samples 1 = 4 samples 2 = 8 samples 3 = 16 samples 4 = 32 samples 5 = 64 samples 6 = 128 samples 7 = 256 samples
7:6	Mode	R/W	0x0	Retain	00 = Maximum peak above threshold 01 = First or last peak above threshold. See register 28_5.13. 10 = Offset 11 = Sample point at distance set by 24_5.7:0
5:0	Peak Detection Hysteresis	R/W	0x03	Retain	0x00 = 0 mV, 0x01 = 7.81 mV, ..., 0x3F = ± 492 mv

Table 196: Advanced VCT™ Sample Point Distance
Page 5, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	0x00	Reserved
9:0	Distance to measure/ Distance to start	R/W	0x000	Retain	When 23_5.7:6 = 11 the measurement is taken at this distance. (00 to 3FF) When 23_5.7:6 = 0x any distance below this distance is not considered (00 to FF). Bit 9:8 is ignored.

Table 197: Advanced VCT Cross Pair Positive Threshold
Page 5, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Reserved
14:8	Cross Pair Positive Threshold > 30m	R/W	0x01	Retain	0x00 = 0 mV, 0x01 = 7.81 mV,..., 0x7F = 992 mV
7	Reserved	RO	0x0	0x0	Reserved
6:0	Cross Pair Positive Threshold < 30m	R/W	0x04	Retain	0x00 = 0 mV, 0x01 = 7.81 mV, ..., 0x7F = 992 mV

Table 198: Advanced VCT Same Pair Impedance Positive Threshold 0 and 1
Page 5, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Reserved
14:8	Same-Pair Positive Threshold 10m - 50m	R/W	0x0F	Retain	0x00 = 0 mV, 0x01 = 7.81 mV, ..., 0x7F = 992 mV
7	Reserved	RO	0x0	0x0	Reserved
6:0	Same-Pair Positive Threshold < 10m	R/W	0x12	Retain	0x00 = 0 mV, 0x01 = 7.81 mV, ..., 0x7F = 992 mV

Table 199: Advanced VCT™ Same Pair Impedance Positive Threshold 2 and 3
Page 5, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Reserved
14:8	Same-Pair Positive Threshold 110m - 140m	R/W	0x0A	Retain	0x00 = 0 mV, 0x01 = 7.81 mV, ..., 0x7F = 992 mV
7	Reserved	RO	0x0	0x0	Reserved
6:0	Same-Pair Positive Threshold 50m - 110m	R/W	0x0C	Retain	0x00 = 0 mV, 0x01 = 7.81 mV, ..., 0x7F = 992 mV

Table 200: Advanced VCT Same Pair Impedance Positive Threshold 4 and Transmit Pulse Control
Page 5, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RO	0x0	0x0	Reserved
13	First Peak/Last Peak Select	R/W	0x0	Retain	This register takes effect only if register 23_5.7:6 = 01. 0 = First Peak 1 = Last Peak

Table 200: Advanced VCT Same Pair Impedance Positive Threshold 4 and Transmit Pulse Control (Continued)

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Break Link Prior to Measurement	R/W	0x0	Retain	1 = Do not wait 1.5s to break link before starting VCT 0 = Wait 1.5s to break link before starting VCT
11:10	Transmit Pulse Width	R/W	0x0	Retain	00 = full pulse (128ns) 01 = 3/4 pulse 10 = 1/2 pulse 11 = 1/4 pulse
9:8	Transmit Amplitude	R/W	0x0	Retain	00 = full amplitude 01 = 3/4 amplitude 10 = 1/2 amplitude 11 = 1/4 amplitude
7	Distance Measurement Point	R/W	0x0	Retain	If 23_5.7:6 = 00 then 0 = Measure distance when amplitude drops to 50% of peak amplitude 1 = Measure distance at actual maximum amplitude If 23_5.7:6 = 01 then 0 = Measure distance when amplitude drops below hysteresis 1 = Measure distance at actual maximum amplitude If 23_5.7:6 = 1X then this bit is ignored.
6:0	Same-Pair Positive Threshold > 140m	R/W	0x06	Retain	0x00 = 0 mV, 0x01 = 7.81 mV, ..., 0x7F = 992 mv

Table 201: Copper Port Packet Generation
Page 6, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Burst	R/W	0x00	Retain	0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets
7	Packet Generator Transmit Trigger/Status	R/W	0x0	Retain	This bit is used to trigger the packet generator to send another burst packets and also indicates the status of the packet generator in burst mode. This bit is valid only when Reg 16_6.6 = '1', Reg 16_6.3 = '1', and Reg 16_6.15:8 is not equal to zero Read: 1 = Packet generator is done transmitting data 0 = Packet generator is transmitting data Write: When this bit is 1, writing '0' will trigger the packet generator to send another burst of packets. When this bit is 0, Writing '0' or '1' will have no effect.

Table 201: Copper Port Packet Generation
Page 6, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
6	Packet Generator Self Clear Control	R/W	0x0	Retain	This bit controls the behavior of Reg 16_6.3 (Enable Packet Generator Bit) to stay in the packet generator mode or resume normal operation after all packets are sent. This bit is valid only in burst mode and ignored in continuous mode. 1 = Reg 16_6.3 stays in packet generator mode after all packets are sent 0 = Reg 16_6.3 self clears after all packets are sent
5	Reserved	R/W	0x0	Retain	Reserved
4	Enable CRC checker	R/W	0x0	Retain	1 = Enable 0 = Enable
3	Enable packet generator	R/W	0x0	Retain	1 = Enable 0 = Enable
2	Payload of packet to transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = 5A,A5,5A,A5,...
1	Length of packet to transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored packet	R/W	0x0	Retain	1 = Tx packets with CRC errors & Symbol Error 0 = No error

Table 202: Copper Port CRC Counters
Page 6, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Count	RO	0x00	Retain	0x00 = no packets received 0xFF = 256 packets received (max count). Bit 16_6.4 must be set to 1 in order for register to be valid.
7:0	CRC Error Count	RO	0x00	Retain	0x00=noCRCerrorsdetectedinthe packetsreceived. 0xFF = 256 CRC errors detected in the packets received (max count). Bit 16_6.4 must be set to 1 in order for register to be valid.

Table 203: Checker Control
Page 6, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0x000	Retain	Reserved
4	CRC Counters Reset	R/W, SC	0x0	0x0	Writing '1' to this bit clears the Packet/CRC Counters Register (Reg 17_6). After writing '1', this bit self-clears to '0' 1 = Resets/Clears the Packet/CRC Counters Register
3	Enable Stub Test	R/W	0x0	Retain	1 = Enable stub test 0 = Normal Operation
2:0	Reserved	R/W	0x0	Retain	Reserved

Table 204: Copper Port Packet Generator IPG Control
Page 6, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Reserved
7:0	IPG Length	R/W	0xB	Retain	These bits define the length of inter-packet-gap (IPG) between packets sent by the packet generator. The IPG length is the programmed value + 1. Unit is in number of bytes.

Table 205: Late Collision Counters 1 & 2
Page 6, Register 23

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Late Collision 97-128 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half duplex and a start of packet is received while the 97th to 128th bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.
7:0	Late Collision 65-96 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half duplex and a start of packet is received while the 65th to 96th bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.

Table 206: Late Collision Counters 3 & 4
Page 6, Register 24

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Late Collision >192 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half duplex and a start of packet is received after 192 bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.
7:0	Late Collision 129-192 bytes	RO, SC	0x00	Retain	This counter increments by 1 when the PHY is in half duplex and a start of packet is received while the 129th to 192nd bytes of the packet are transmitted. The measurement is done at the internal GMII interface. The counter will not roll over and will clear on read.

Table 207: Late Collision Window Adjust/Link Disconnect
Page 6, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	R/W	0x0	Retain	Reserved
12:8	Late Collision Window Adjust	R/W	0x00	Retain	Number of bytes to advance in late collision window. 0 = start at 64th byte, 1 = start at 63rd byte, etc.
7:0	Reserved	R/W	0x00	Retain	Reserved

Table 208: Misc Test
Page 6, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TX_TCLK Enable	R/W	0x0	0x0	The highest numbered enabled port will drive the transmit clock to the HSDACP/N pin. Reg 27_4.8 must be set to '0' when TX_TCLK is set to '1' 1 = Enable 0 = Disable
14:13	Reserved	R/W	0x0	Retain	Reserved
12:8	Temperature Threshold	R/W	0x19	Retain	Temperature in C = 5 x 26_6.4:0 - 25 i.e. for 100C the value is 11001
7	Temperature Sensor Interrupt Enable	R/W	0x0	Retain	1 = Interrupt Enable 0 = Interrupt Disable
6	Temperature Sensor Interrupt	RO, LH	0x0	0x0	1 = Temperature Reached Threshold 0 = Temperature Below Threshold
5	Reserved	R/W	0x0	Retain	Reserved
4:0	Temperature Sensor (5-bit)	RO	xxxxx	xxxxx	Temperature in C = 5 x 26_6.4:0 - 25 i.e. for 100C the value is 11001

Table 209: PHY Cable Diagnostics Pair 0 Length
Page 7, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Pair 0 Cable Length	RO	0x0000	Retain	Length to fault in meters or centimeters based on register 21_7.10.

Table 210: PHY Cable Diagnostics Pair 1 Length
Page 7, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Pair 1 Cable Length	RO	0x0000	Retain	Length to fault in meters or centimeters based on register 21_7.10.

Table 211: PHY Cable Diagnostics Pair 2 Length
Page 7, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Pair 2 Cable Length	RO	0x0000	Retain	Length to fault in meters or centimeters based on register 21_7.10.

Table 212: PHY Cable Diagnostics Pair 3 Length
Page 7, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Pair 3 Cable Length	RO	0x0000	Retain	Length to fault in meters or centimeters based on register 21_7.10.

Table 213: PHY Cable Diagnostics Results
Page 7, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Pair 3 Fault Code	RO	0x0	Retain	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy Else = Reserved
11:8	Pair 2 Fault Code	RO	0x0	Retain	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy Else = Reserved
7:4	Pair 1 Fault Code	RO	0x0	Retain	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy Else = Reserved
3:0	Pair 0 Fault Code	RO	0x0	Retain	0000 = Invalid 0001 = Pair Ok 0010 = Pair Open 0011 = Same Pair Short 0100 = Cross Pair Short 1001 = Pair Busy Else = Reserved

Table 214: PHY Cable Diagnostics Control
Page 7, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Run Immediately	R/W, SC	0x0	0x0	0 = No Action 1 = Run VCT™ Now
14	Run At Each Auto-Negotiation Cycle	R/W	0x1	Retain	0 = Do No Run At Auto-Negotiation Cycle 1 = Run At Auto-Negotiation Cycle
13	Disable Cross Pair Check	R/W	0x0	Retain	0 = Enable Cross Pair Check 1 = Disable Cross Pair Check

Table 214: PHY Cable Diagnostics Control
Page 7, Register 21

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Run After Break Link	R/W, SC	0x0	0x0	0 = No Action 1 = Run VCT After Breaking Link
11	Cable Diagnostics Status	RO	0x0	Retain	0 = Complete 1 = In Progress
10	Cable Length Unit	R/W	0x0	Retain	0 = Centimeters 1 = Meters
9:0	Reserved	RO	0x000	0x000	Reserved

Table 215: Advanced VCT™ Cross Pair Negative Threshold
Page 7, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Reserved
14:8	Cross Pair Negative Threshold > 30m	R/W	0x01	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV, ..., 0x7F = - 992 mV
7	Reserved	RO	0x0	0x0	Reserved
6:0	Cross Pair Negative Threshold < 30m	R/W	0x04	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV, ..., 0x7F = - 992 mV

Table 216: Advanced VCT Same Pair Impedance Negative Threshold 0 and 1
Page 7, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Reserved
14:8	Same-Pair Negative Threshold 10m - 50m	R/W	0x0F	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV, ..., 0x7F = - 992 mV
7	Reserved	RO	0x0	0x0	Reserved
6:0	Same-Pair Negative Threshold < 10m	R/W	0x12	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV, ..., 0x7F = - 992 mV

Table 217: Advanced VCT Same Pair Impedance Negative Threshold 2 and 3
Page 7, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Reserved
14:8	Same-Pair Negative Threshold 110m - 140m	R/W	0x0A	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV, ..., 0x7F = - 992 mV
7	Reserved	RO	0x0	0x0	Reserved

Table 217: Advanced VCT Same Pair Impedance Negative Threshold 2 and 3
Page 7, Register 27

Bits	Field	Mode	HW Rst	SW Rst	Description
6:0	Same-Pair Negative Threshold 50m - 110m	R/W	0x0C	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV, ..., 0x7F = - 992 mV

Table 218: Advanced VCT Same Pair Impedance Negative Threshold 4
Page 7, Register 28

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	Reserved
6:0	Same-Pair Negative Threshold > 140m	R/W	0x06	Retain	0x00 = 0 mV, 0x01 = - 7.81 mV, ..., 0x7F = - 992 mV

Table 219: EEE Control Register 1
Page 18, Register 0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x6	Retain	Reserved
7:1	Reserved	R/W	0x0	Retain	Reserved
0	EEE Master/Slave Mode	R/W	0	Retain	EEE Master/Slave Mode. When the EEE is configured to be Master mode (Legacy Mode), the EEE buffer is enabled and the LPI Idle will be initiated by the PHY. In Slave mode, the external MAC is responsible for the EEE buffering and assertion/deassertion of the LPI signals. 1 = EEE Master Mode (Legacy Mode) 0 = EEE Slave Mode

Table 220: EEE Control Register 2
Page 18, Register 1

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	fast_exit_time	R/W	0x11	Retain	LPI Exit Timer when port speed is 1000 Mbps. Unit is in microseconds. Default is 17 μ s
7:0	slow_exit_time	R/W	0x1E	Retain	LPI Exit Timer when port speed is 100 Mbps. Unit is in microseconds. Default is 30 μ s

Table 221: EEE Control Register 3
Page 18, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	fast_enter_time	R/W	0x11	Retain	LPI Enter Timer when port speed is 1000 Mbps. Unit is in microseconds. Default is 17 μ s

Table 221: EEE Control Register 3
Page 18, Register 2

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	slow_enter_time	R/W	0x1E	Retain	LPI Enter Timer when port speed is 100 Mbps. Unit is in microseconds. Default is 30 μ s

Table 222: Packet Generation
Page 18, Register 16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Burst	R/W	0x00	Retain	0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets
7:5	Enable Packet Generator	R/W, SC	0x0	Retain	000 = Normal Operation 010 = Generate Packets on Copper Interface 100 = Generate Packets on SGMII Interface 110 = Generate Packets on QSGMII Interface else = Reserved
4	Packet Generator Transmit Trigger/Status	R/W	0x0	Retain	This bit is used to trigger the packet generator to send another burst packets and also indicates the status of the packet generator in burst mode. This bit is valid only when Reg 16_18.3 = '1' and Reg 16_18.15:8 is not equal to zero Read: 1 = Packet generator is done transmitting data 0 = Packet generator is transmitting data Write: When this bit is 1, writing '0' will trigger the packet generator to send another burst of packets. When this bit is 0, Writing '0' or '1' will have no effect.
3	Packet Generator Self Clear Control	R/W	0x0	Retain	This bit controls the behavior of Reg 16_18.7:5 (Enable Packet Generator Bits) to stay in the packet generator mode or resume normal operation after all packets are sent. This bit is valid only in burst mode and ignored in continuous mode. 1 = Reg 16_18.7:5 stays in packet generator mode after all packets are sent 0 = Reg 16_18.7:5 self clears after all packets are sent
2	Payload of packet to transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = 5A,A5,5A,A5,...
1	Length of packet to transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored packet	R/W	0x0	Retain	1 = Tx packets with CRC errors & Symbol Error 0 = No error

Table 223: CRC Counters
Page 18, Register 17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Count	RO	0x00	Retain	0x00 = no packets received 0xFF = 256 packets received (max count). Bit 16_18.4 must be set to enable the counter in order for register to be valid.
7:0	CRC Error Count	RO	0x00	Retain	0x00=noCRCerrorsdetectedinthepacketsreceived. 0xFF = 256 CRC errors detected in the packets received (max count). Bit 16_18.4 must be set to enable the counter in order for register to be valid.

Table 224: Checker Control
Page 18, Register 18

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0x0	Retain	Reserved
4	CRC Counters Reset	R/W, SC	0x0	Retain	Writing '1' to this bit clears the Packet/CRC Counters Register (Reg 17_18). After writing '1', this bit self-clears to '0' 1 = Resets/Clears the Packet/CRC Counters Register
3	Reserved	R/W	0x0	Retain	Reserved
2:0	Enable CRC Checker	R/W	0x00	Retain	000 = Disable/reset CRC Checker 010 = Check data from Copper interface 100 = Check data from SGMII interface 110 = Check data from QSGMII interface else = Reserved

Table 225: Packet Generator IPG Control
Page 18, Register 19

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Reserved
7:0	IPG Length	R/W	0xB	Retain	These bits define the length of inter-packet-gap (IPG) between packets sent by the packet generator. The IPG length is the programmed value + 1. Unit is in number of bytes.

Table 226: General Control Register 1
Page 18, Register 20

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x0	0x0	Mode Software Reset. Affects page 6 and 18. Writing a 1 to this bit causes the PHY state machines to be reset. When the reset operation is done, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14:7	Reserved	R/W	0x4	Retain	Reserved
6	Auto-Media Detect Copper/100BASE-FX	R/W	0x0	Retain	This bit modify the MODE[2:0] = '011' definition as the following: 1 = AMD between copper and 100BASE-FX 0 = 100BASE-FX Only. No AMD.
5:4	Auto Media Detect Preferred Media	R/W	0x0	Retain	00 = Link on first media 01 = Copper Preferred 10 = Fiber Preferred 11 = Reserved
3	Reserved	R/W	0x0	Retain	Reserved
2:0	MODE[2:0]	R/W	See Descr.	Update	Changes to this bit are disruptive to the normal operation; therefore, any changes to these registers must be followed by a software reset to take effect. On hardware reset these bits take on the value of MODE[2:0].
			0x0	0x0	000 = QSGMII (System mode) to Copper 001 = SGMII (System mode) to Copper 010 = QSGMII (System mode) to 1000BASE-X 011 = QSGMII (System mode) to 100BASE-FX (Reg 20_18.6 = '0') QSGMII (System mode) to Auto Media Detect Copper/100BASE-FX (Reg 20_18.6 = '1') 100 = QSGMII (System mode) to SGMII (Media mode) 101 = SGMII (System mode) to QSGMII (Media mode) 110 = QSGMII (System mode) to Auto Media Detect Copper/SGMII (Media mode) 111 = QSGMII (System mode) to Auto Media Detect Copper/1000BASE-X

Table 227: Link Disconnect Count
Page 18, Register 25

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Reserved
7:0	Link Disconnect	RO, SC	0x00	Retain	This counter counts the number of times link status changed from up to down. The counter will not roll over and will clear on read.

Table 228: Copper/SERDES RX_ER Byte Capture
Page 18, Register 26

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Capture Data Valid	RO	0x0	0x0	1 = Bits 14:0 Valid 0 = Bits 14:0 Invalid
14	Reserved	RO	0x0	0x0	Reserved
13:12	Byte Number	RO	0x0	0x0	00 = 4 bytes before RX_ER asserted 01 = 3 bytes before RX_ER asserted 10 = 2 bytes before RX_ER asserted 11 = 1 byte before RX_ER asserted The byte number increments after every read when register 26_18.15 is set to 1.
11:10	Reserved	RO	0x0	0x0	Reserved
9	RX_ER	RO	0x0	0x0	RX Error. Normally this bit will be low since the capture is triggered by RX_ER being high. However it is possible to see an RX_ER high when the capture is re-enabled after reading the fourth byte and there happens to be a long sequence of RX_ER when the capture restarts.
8	RX_DV	RO	0x0	0x0	RX Data Valid
7:0	RXD[7:0]	RO	0x00	0x00	RX Data

3.2 PHY XMDIO Register Description

Table 229: Register Map

Register Name	Register Address	Table and Page
PCS control 1 register	Device 3, Register 0x0	Table 230, p. 226
PCS status 1 register	Device 3, Register 0x1	Table 231, p. 226
PCS EEE capability register	Device 3, Register 0x14	Table 232, p. 227
PCS EEE wake error counter	Device 3, Register 0x16	Table 233, p. 227
EEE advertisement register	Device 7, Register 0x3C	Table 234, p. 227
EEE Link partner advertisement register	Device 7, Register 0x3D	Table 235, p. 228

Table 230: PCS control 1 register
Device 3, Register 0x0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	RO	0x00	Retain	Reserved
10	Clock Stoppable	R/W	0x0	Retain	1 = Clock stoppable during LPI 0 = Clock not stoppable
9:0	Reserved	RO	0x000	Retain	Reserved

Table 231: PCS status 1 register
Device 3, Register 0x1

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	Retain	Reserved
11	Tx LP idle received	RO/LH	0x0	Retain	1 = Tx PCS has received LP idle 0 = LP Idle not received
10	Rx LP idle received	RO/LH	0x0	Retain	1 = Rx PCS has received LP idle 0 = LP Idle not received
9	Tx LP idle indication	RO	0x0	Retain	1 = Tx PCS is currently receiving LP idle 0 = PCS is not currently receiving LP idle
8	Rx LP idle indication	RO	0x0	Retain	1 = Rx PCS is currently receiving LP idle 0 = PCS is not currently receiving LP idle
7:3	Reserved	RO	0x00	Retain	Reserved
2	PCS receive link status	RO	0x0	Retain	1 = PCS receive link up 0 = PCS receive link down
1	Low-power ability	RO	0x0	Retain	1 = PCS supports low-power mode 0 = PCS does not support low-power mode
0	Reserved	RO	0x0	Retain	Reserved

Table 232: PCS EEE capability register
Device 3, Register 0x14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	Retain	Reserved
6	10GBASE-KR EEE	RO	0x0	Retain	1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR
5	10GBASE-KX4 EEE	RO	0x0	Retain	1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 1000BASE-KX RO
4	1000BASE-KX	RO	0x0	Retain	1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX RO
3	10GBASE-T EEE	RO	0x0	Retain	1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T
2	1000BASE-T EEE	RO	0x0	Retain	1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T
1	100BASE-TX EEE	RO	0x0	Retain	1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX
0	Reserved	RO	0x0	Retain	Reserved

Table 233: PCS EEE wake error counter
Device 3, Register 0x16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	EEE wake error counter	RO,NR	0x0000	Retain	This counter is incremented for each transition of lpi_wake_timer_done from FALSE to TRUE

Table 234: EEE advertisement register
Device 7, Register 0x3C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	Retain	Reserved
6	10GBASE-KR EEE	RO	0x0	Retain	1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR
5	10GBASE-KX4 EEE	RO	0x0	Retain	1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 1000BASE-KX RO
4	1000BASE-KX	RO	0x0	Retain	1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX RO
3	10GBASE-T EEE	RO	0x0	Retain	1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T
2	1000BASE-T EEE	R/W	0x0	Retain	1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T
1	100BASE-TX EEE	R/W	0x0	Retain	1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX
0	Reserved	RO	0x0	Retain	Reserved

Table 235: EEE Link partner advertisement register
Device 7, Register 0x3D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	Retain	Reserved
6	LP 10GBASE-KR EEE	RO	0x0	Retain	1 = EEE is supported for 10GBASE-KR 0 = EEE is not supported for 10GBASE-KR
5	LP 10GBASE-KX4 EEE	RO	0x0	Retain	1 = EEE is supported for 10GBASE-KX4 0 = EEE is not supported for 1000BASE-KX RO
4	LP 1000BASE-KX	RO	0x0	Retain	1 = EEE is supported for 1000BASE-KX 0 = EEE is not supported for 1000BASE-KX RO
3	LP 10GBASE-T EEE	RO	0x0	Retain	1 = EEE is supported for 10GBASE-T 0 = EEE is not supported for 10GBASE-T
2	LP 1000BASE-T EEE	RO	0x0	Retain	1 = EEE is supported for 1000BASE-T 0 = EEE is not supported for 1000BASE-T
1	LP 100BASE-TX EEE	RO	0x0	Retain	1 = EEE is supported for 100BASE-TX 0 = EEE is not supported for 100BASE-TX
0	Reserved	RO	0x0	Retain	Reserved

4 Electrical Specifications

4.1 Absolute Maximum Ratings¹

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Units
V _{DDA18}	Power Supply Voltage on AVDD18 with respect to VSS	-0.5		2.5	V
V _{DD}	Power Supply Voltage on DVDD with respect to VSS	-0.5		1.5	V
V _{DDA33}	Power Supply Voltage on AVDD33 with respect to VSS	-0.5		3.6	V
V _{DDOL}	Power Supply Voltage on VDDOL with respect to VSS	-0.5		3.6	V
V _{DDOR}	Power Supply Voltage on VDDOR with respect to VSS	-0.5		3.6	V
V _{DDOM}	Power Supply Voltage on VDDOM with respect to VSS	-0.5		3.6	V
V _{DDC}	Power Supply Voltage on VDDC with respect to VSS	-0.5		2.5	V
V _{PIN}	Voltage applied to any digital input pin	-0.5		5.0 or V _{DDO} + 0.7, whichever is less	V
T _{STORAGE}	Storage temperature	-55		+125 ²	°C

1. On power-up, no special power supply sequencing is required.
2. 125 °C is only used as bake temperature for not more than 24 hours. Long term storage (e.g weeks or longer) should be kept at 85 °C or lower.

4.2 Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Units
V _{DDA18} ¹	AVDD18 supply	For AVDD18	1.71	1.8	1.89	V
V _{DDC} ¹	VDDC supply	For VDDC	1.71	1.8	1.89	V
V _{DDA33}	AVDD33 supply	For AVDD33	3.13	3.3	3.47	V
V _{DD} ¹	DVDD supply	For DVDD at 1.0V	0.95	1.0	1.05	V
V _{DDOL} ¹	VDDOL supply	For VDDOL at 1.8V	1.71	1.8	1.89	V
		For VDDOL at 2.5V	2.38	2.5	2.63	V
		For VDDOL at 3.3V	3.13	3.3	3.47	V
V _{DDOR} ¹	VDDOR supply	For VDDOR at 1.8V	1.71	1.8	1.89	V
		For VDDOR at 2.5V	2.38	2.5	2.63	V
		For VDDOR at 3.3V	3.13	3.3	3.47	V
V _{DDOM} ¹	VDDOM supply	For VDDOM at 1.2V	1.14	1.2	1.26	V
		For VDDOM at 1.8V	1.71	1.8	1.89	V
		For VDDOM at 2.5V	2.38	2.5	2.63	V
		For VDDOM at 3.3V	3.13	3.3	3.47	V
RSET	Internal bias reference	Resistor connected to V _{SS}		5000 ± 1% Tolerance		Ω
T _A	Commercial Ambient operating temperature		0		70 ²	°C
T _J	Maximum junction temperature				125 ³	°C

1. Maximum noise allowed on supplies is 50 mV peak-peak.
2. Commercial operating temperatures are typically below 70 °C, e.g. 45 °C ~55 °C. The 70 °C max is Marvell® specification limit
3. Refer to white paper on TJ Thermal Calculations for more information.

4.3 Package Thermal Information

4.3.1 Thermal Conditions for 128-pin LQFP Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance ¹ - junction to ambient for the 128-Pin, LQFP package $\theta_{JA} = (T_J - T_A) / P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		24.9		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		21.8		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		20.9		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		20.3		°C/W
ψ_{JT}	Thermal characteristic parameter ^a - junction to top center of the 128-Pin, LQFP package $\psi_{JT} = (T_J - T_{top}) / P$ P = Total power dissipation, T _{top} : Temperature on the top center of the package.	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.50		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.75		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		0.90		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		1.01		°C/W
θ_{JC}	Thermal resistance ^a - junction to case for the 128-Pin, LQFP package $\theta_{JC} = (T_J - T_C) / P_{top}$ P _{top} = Power dissipation from the top of the package	JEDEC with no air flow		9.8		°C/W
θ_{JB}	Thermal resistance ^a - junction to board for the 128-Pin, LQFP package $\theta_{JB} = (T_J - T_B) / P_{bottom}$ P _{bottom} = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		15.1		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

4.3.2 Thermal Conditions for 196-pin TFBGA Package

Symbol	Parameter	Condition	Min	Typ	Max	Units
θ_{JA}	Thermal resistance ¹ - junction to ambient for the 196-Pin, TFBGA package $\theta_{JA} = (T_J - T_A) / P$ P = Total power dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		29.16		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		27.05		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		26.23		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		25.70		°C/W
ψ_{JT}	Thermal characteristic parameter ^a - junction to top center of the 196-Pin, TFBGA package $\psi_{JT} = (T_J - T_{top}) / P$ P = Total power dissipation, T _{top} : Temperature on the top center of the package.	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow		0.43		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow		0.54		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow		0.62		°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 3 meter/sec air flow		0.68		°C/W
θ_{JC}	Thermal resistance ^a - junction to case for the 196-Pin, TFBGA package $\theta_{JC} = (T_J - T_C) / P_{top}$ P _{top} = Power dissipation from the top of the package	JEDEC with no air flow		8.94		°C/W
θ_{JB}	Thermal resistance ^a - junction to board for the 196-Pin, TFBGA package $\theta_{JB} = (T_J - T_B) / P_{bottom}$ P _{bottom} = Power dissipation from the bottom of the package to the PCB surface.	JEDEC with no air flow		19.44		°C/W

1. Refer to white paper on TJ Thermal Calculations for more information.

4.4 Current Consumption

4.4.1 Current Consumption AVDD18 + VDDC

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I _{AVDD18} + I _{VDDC}	1.8V Power	AVDD18, VDDC	QSGMII to 1000BASE-T link with traffic		321		mA
			QSGMII to 1000BASE-T EEE		155		mA
			QSGMII to 100BASE-TX link with traffic		171		mA
			QSGMII to 100BASE-TX EEE		129		mA
			QSGMII to 10BASE-T link with traffic		135		mA
			QSGMII to 10BASE-T _e EEE with traffic		132		mA
			QSGMII to Copper Energy Detect		108		mA
			QSGMII to Copper Energy Detect with System Interface Power Down		65		mA
			QSGMII to Copper IEEE Power Down		82		mA
			QSGMII to Copper IEEE Power Down with System Interface Power Down		37		mA
			SGMII to 1000BASE-T link with traffic		358		mA
			SGMII to 1000BASE-T EEE		191		mA
			SGMII to 100BASE-TX link with traffic		207		mA
			SGMII to 100BASE-TX EEE		165		mA
			SGMII to 10BASE-T link with traffic		171		mA
			SGMII to 10BASE-T _e EEE with traffic		168		mA
			SGMII to Copper Energy Detect		150		mA
			SGMII to Copper Energy Detect with System Interface Power Down		87		mA
			SGMII to Copper IEEE Power Down		119		mA
			SGMII to Copper IEEE Power Down with System Interface Power Down		58		mA
			SGMII to Fiber (1000BASE-X/100BASE-FX/SGMII) link with traffic ¹		116		mA
			SGMII to Fiber (1000BASE-X/100BASE-FX/SGMII) IEEE Power Down ¹		77		mA
			SGMII to Fiber (1000BASE-X/100BASE-FX/SGMII) IEEE Power Down with System Interface Power Down ¹		39		mA
			Reset		26		mA

1. Applicable when device is configured as two ports SGMII (system) to Fiber (media) with QSGMII crossover enabled.

4.4.2 Current Consumption AVDD33

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I _{VDDA33}	3.3V Power	AVDD33	QSGMII to 1000BASE-T link with traffic		224		mA
			QSGMII to 1000BASE-T EEE		35		mA
			QSGMII to 100BASE-TX link with traffic		59		mA
			QSGMII to 100BASE-TX EEE		11		mA
			QSGMII to 10BASE-T link with traffic		120		mA
			QSGMII to 10BASE-T _e EEE with traffic		100		mA
			QSGMII to Copper Energy Detect		3		mA
			QSGMII to Copper Energy Detect with System Interface Power Down		3		mA
			QSGMII to Copper IEEE Power Down		3		mA
			QSGMII to Copper IEEE Power Down with System Interface Power Down		3		mA
			SGMII to 1000BASE-T link with traffic		224		mA
			SGMII to 1000BASE-T EEE		35		mA
			SGMII to 100BASE-TX link with traffic		59		mA
			SGMII to 100BASE-TX EEE		11		mA
			SGMII to 10BASE-T link with traffic		120		mA
			SGMII to 10BASE-T _e EEE with traffic		100		mA
			SGMII to Copper Energy Detect		3		mA
			SGMII to Copper Energy Detect with System Interface Power Down		3		mA
			SGMII to Copper IEEE Power Down		3		mA
			SGMII to Copper IEEE Power Down with System Interface Power Down		3		mA
			Reset		3		mA



Note

AVDD33 is not used when the device is in Fiber only mode of operations

4.4.3 Current Consumption DVDD

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I _{DVDD}	Power to digital core at 1.0V	DVDD	QSGMII to 1000BASE-T link with traffic		278		mA
			QSGMII to 1000BASE-T EEE		49		mA
			QSGMII to 100BASE-TX link with traffic		62		mA
			QSGMII to 100BASE-TX EEE		37		mA
			QSGMII to 10BASE-T link with traffic		36		mA
			QSGMII to 10BASE-Te EEE with traffic		33		mA
			QSGMII to Copper Energy Detect		27		mA
			QSGMII to Copper Energy Detect with System Interface Power Down		23		mA
			QSGMII to Copper IEEE Power Down		25		mA
			QSGMII to Copper IEEE Power Down with System Interface Power Down		21		mA
			SGMII to 1000BASE-T link with traffic		280		mA
			SGMII to 1000BASE-T EEE		54		mA
			SGMII to 100BASE-TX link with traffic		64		mA
			SGMII to 100BASE-TX EEE		42		mA
			SGMII to 10BASE-T link with traffic		37		mA
			SGMII to 10BASE-Te EEE with traffic		36		mA
			SGMII to Copper Energy Detect		33		mA
			SGMII to Copper Energy Detect with System Interface Power Down		22		mA
			SGMII to Copper IEEE Power Down		30		mA
			SGMII to Copper IEEE Power Down with System Interface Power Down		19		mA
			SGMII to Fiber (1000BASE-X/100BASE-FX/SGMII) link with traffic ¹		48		mA
			SGMII to Fiber (1000BASE-X/100BASE-FX/SGMII) IEEE Power Down ¹		16		mA
			SGMII to Fiber (1000BASE-X/100BASE-FX/SGMII) IEEE Power Down with System Interface Power Down ¹		16		mA
			Reset		14		mA

1. Applicable when device is configured as two ports SGMII (system) to Fiber (media) with QSGMII crossover enabled.

4.4.4 Current Consumption VDDOL

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I _{VDDOL}	1.8V I/O Supply	VDDOL			1		mA
	2.5V I/O Supply				1		mA
	3.3V I/O Supply				1		mA

4.4.5 Current Consumption VDDOR

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I _{VDDOR}	1.8V I/O Supply	VDDOR			1		mA
	2.5V I/O Supply				1		mA
	3.3V I/O Supply				1		mA

4.4.6 Current Consumption VDDOM

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
I _{VDDOM}	1.2V I/O Supply	VDDOM			1		mA
	1.8V I/O Supply				1		mA
	2.5V I/O Supply				1		mA
	3.3V I/O Supply				1		mA

4.5 DC Operating Conditions

4.5.1 Digital Pins

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VIH	Input high voltage	All digital inputs	VDDO = 3.3V	2.0		VDDO + 0.6V	V
			VDDO = 2.5V	1.75		VDDO + 0.6V	V
			VDDO = 1.8V	1.26		VDDO + 0.6V	V
			VDDO = 1.2V	0.84		VDDO + 0.6V	V
VIL	Input low voltage	All digital inputs	VDDO = 3.3V	-0.3		0.8	V
			VDDO = 2.5V	-0.3		0.75	V
			VDDO = 1.8V	-0.3		0.54	V
			VDDO = 1.2V	-0.3		0.36	V
VOH	High level output voltage	All digital outputs	IOH = -4 mA	VDDO - 0.4V			V
VOL	Low level output voltage	All digital outputs	IOL = 4 mA			0.4	V
I _{ILK}	Input leakage current	With internal pull-up resistor				10 -50	uA
		All others without resistor				10	uA
CIN	Input capacitance	All pins				5	pF

4.5.2 LED Pins

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VOH	High level output voltage	All LED outputs	IOH = -15 mA	VDDO - 0.75V			V
VOL	Low level output voltage	All LED outputs	IOL = 15 mA			0.75	V
I _{MAX}	Total maximum current per port ¹	All LED pins				35	mA
I _{ILK}	Input leakage current	All LED pins				10 -50	uA
CIN	Input capacitance	All LED pins				5	pF

1. Each port can support up to four LED outputs. The maximum current per LED is dependent on the number of LED outputs used per port. For example, when using two LEDs per port, the maximum current per LED is $65/2 = 32.5$ mA.

4.5.3 RESETn Pin

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
VIH	Input high voltage	RESETn	VDDO = 2.5V/3.3V	1.75		VDDO + 0.6V	V
			VDDO = 1.8V	1.26		VDDO + 0.6V	V
VIL	Input low voltage	RESETn	VDDO = 2.5V/3.3V	-0.3		0.75	V
			VDDO = 1.8V	-0.3		0.54	V

4.5.3.1 Internal Resistor Description

Pin #	Pin Name	Resistor
62	TRSTn	Internal Pull-up
58	TDI	Internal Pull-up
55	TMS	Internal Pull-up
54	TCK	Internal Pull-up

4.5.4 IEEE DC Transceiver Parameters

IEEE tests are typically based on template and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications.

-10BASE-T IEEE 802.3 Clause 14

-100BASE-TX ANSI X3.263-1995

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
V _{ODIFF}	Absolute peak differential output voltage	MDIP/N[1:0]	10BASE-T no cable	2.2	2.5	2.8	V
		MDIP/N[1:0]	10BASE-T cable model	585 ¹			mV
		MDIP/N[1:0]	100BASE-TX mode	0.950	1.0	1.050	V
		MDIP/N[3:0]	1000BASE-T ²	0.67	0.75	0.82	V
	Overshoot ²	MDIP/N[1:0]	100BASE-TX mode	0		5%	V
	Amplitude Symmetry (positive/negative)	MDIP/N[1:0]	100BASE-TX mode	0.98x		1.02x	V+/V-
V _{IDIFF}	Peak Differential Input Voltage	MDIP/N[1:0]	10BASE-T mode	585 ³			mV
	Signal Detect Assertion	MDIP/N[1:0]	100BASE-TX mode	1000	460 ⁴		mV peak-peak
	Signal Detect De-assertion	MDIP/N[1:0]	100BASE-TX mode	200	360 ⁵		mV peak-peak

1. IEEE 802.3 Clause 14, Figure 14.9 shows the template for the "far end" wave form. This template allows as little as 495 mV peak differential voltage at the far end receiver.
2. IEEE 802.3ab Figure 40 -19 points A&B.
3. The input test is actually a template test ; IEEE 802.3 Clause 14, Figure 14.17 shows the template for the receive wave form.
4. The ANSI TP-PMD specification requires that any received signal with peak-to-peak differential amplitude greater than 1000 mV should turn on signal detect (internal signal in 100BASE-TX mode). The device will accept signals typically with 460 mV peak-to-peak differential amplitude.
5. The ANSI-PMD specification requires that any received signal with peak-to-peak differential amplitude less than 200 mV should de-assert signal detect (internal signal in 100BASE-TX mode). The Alaska Quad will reject signals typically with peak-to-peak differential amplitude less than 360 mV.

4.5.5 SGMII Interface

SGMII specification is a de-facto standard proposed by Cisco. It is available at the Cisco website <ftp://ftp-eng.cisco.com/sgmii/sgmii.pdf>. It uses a modified LVDS specification based on the IEEE standard 1596.3. Refer to that standard for the exact definition of the terminology used in the following table. The device adds flexibility by allowing programmable output voltage swing and supply voltage option.

4.5.5.1 Transmitter DC Characteristics

Symbol	Parameter ¹	Min	Typ	Max	Units
V _{OH}	Output Voltage High			1600	mV
V _{OL}	Output Voltage Low	700			mV
V _{RING}	Output Ringing			10	%
V _{OD} ²	Output Voltage Swing (differential, peak)	Programmable - see Table 236.			mV peak
V _{OS}	Output Offset Voltage (also called Common mode voltage)	Variable - see 4.5.5.2 for details.			mV
R _O	Output Impedance (single-ended) (50 ohm termination)	40		60	Ωs
Delta R _O	Mismatch in a pair			10	%
Delta V _{OD}	Change in V _{OD} between 0 and 1			25	mV
Delta V _{OS}	Change in V _{OS} between 0 and 1			25	mV
I _{S+} , I _{S-}	Output current on short to VSS			40	mA
I _{S+}	Output current when S_OUT+ and S_OUT- are shorted			12	mA
I _{X+} , I _{X-}	Power off leakage current			10	mA

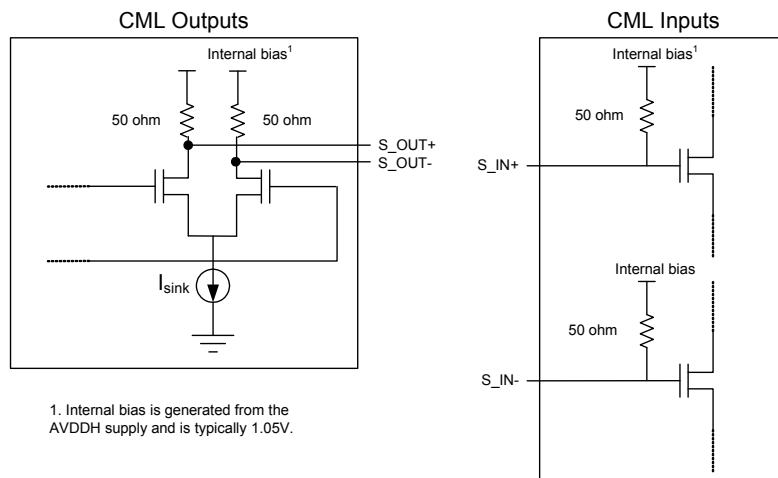
- Parameters are measured with outputs AC connected with 100 ohm differential load.
- Output amplitude is programmable by writing to Register 26_1.2:0.

Table 236: Programming SGMII Output Amplitude

Register 26_1 Bits	Field	Description
2:0	SGMII/Fiber Output Amplitude ¹	Differential voltage peak measured. Note that internal bias minus the differential peak voltage must be greater than 700 mV. 000 = 14 mV 001 = 112 mV 010 = 210 mV 011 = 308 mV 100 = 406 mV 101 = 504 mV 110 = 602 mV 111 = 700 mV

- Cisco SGMII specification limits are |VOD| = 150 mV - 400 mV peak differential.

Figure 35: CML I/Os



4.5.5.2

Common Mode Voltage (Voffset) Calculations

There are four different main configurations for the SGMII/Fiber interface connections. These are:

- DC connection to an LVDS receiver
- AC connection to an LVDS receiver
- DC connection to an CML receiver
- AC connection to an CML receiver

If AC coupling or DC coupling to an LVDS receiver is used, the DC output levels are determined by the following:

- Internal bias. See [Figure 35](#) for details. (If AVDD18 is used to generate the internal bias, the internal bias value will typically be 1.05V.)

**Note**

For QSGMII, internal bias is also generated from the AVDDH supply and is typically 1.38V for output termination, and 1.2V for input termination.

- The output voltage swing is programmed by Register 26_1.2:0 (see [Table 236](#)).

Voffset (i.e., common mode voltage) = internal bias - single-ended peak-peak voltage swing. See [Figure 36](#) for details.

If DC coupling is used with a CML receiver, then the DC levels will be determined by a combination of the MACs output structure and the input structure shown in the CML Inputs diagram in [Figure 37](#). Assuming the same MAC CML voltage levels and structure, the common mode output levels will be determined by:

Voffset (i.e., common mode voltage) = internal bias - single-ended peak-peak voltage swing/2. See [Figure 37](#) for details.

If DC coupling is used, the output voltage DC levels are determined by the AC coupling considerations above, plus the I/O buffer structure of the MAC.

Figure 36: AC connections (CML or LVDS receiver) or DC connection LVDS receiver

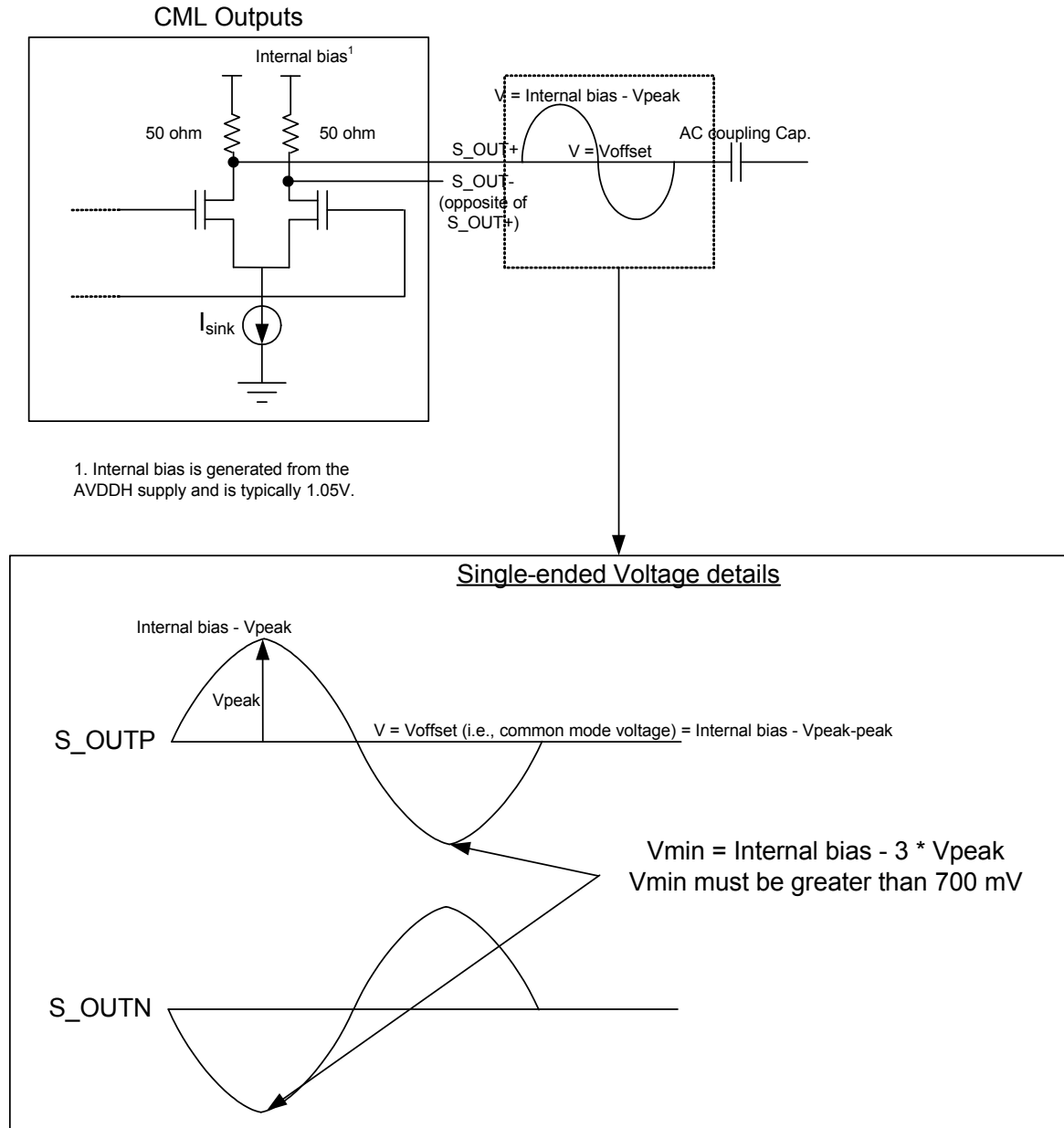
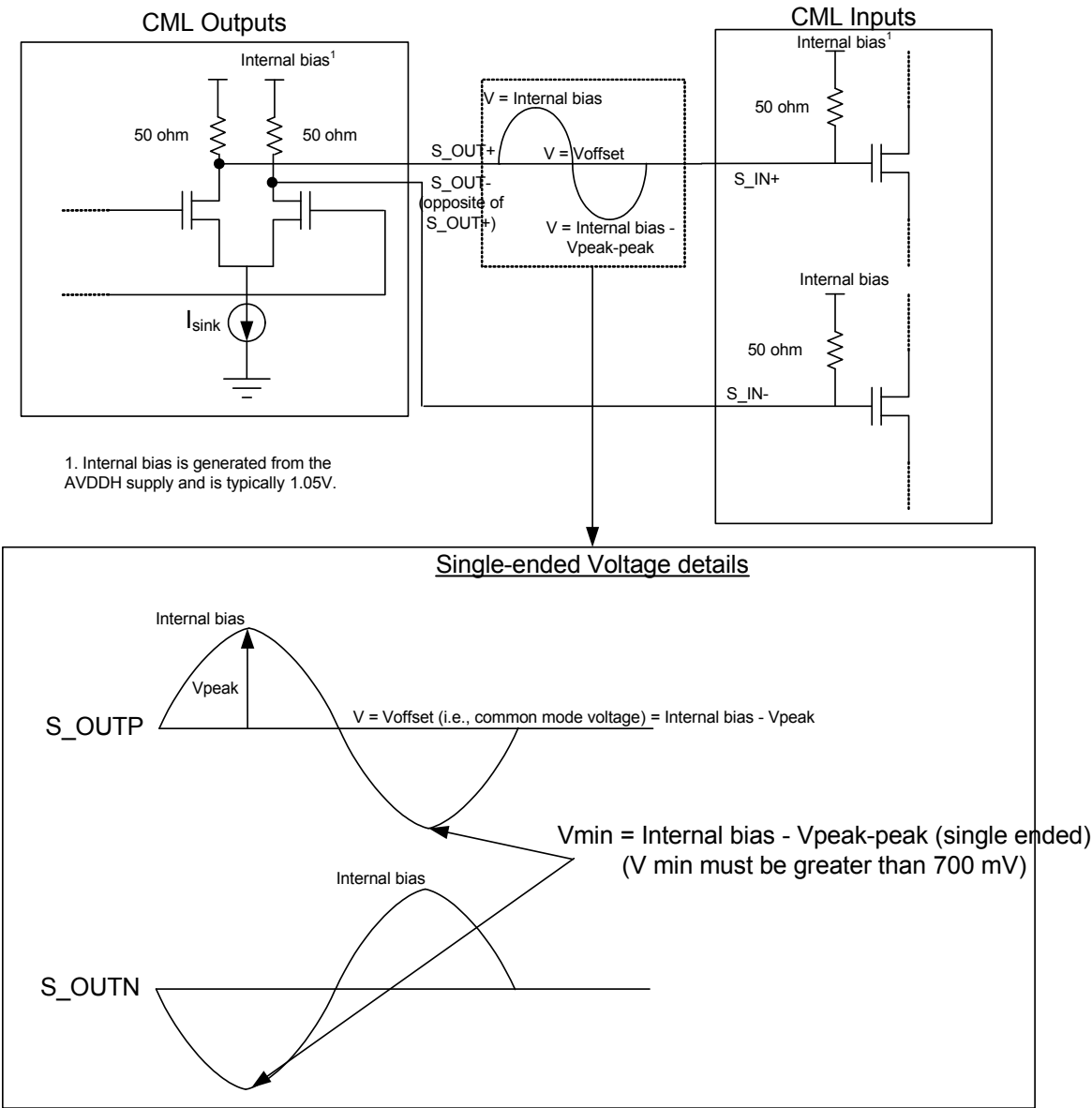


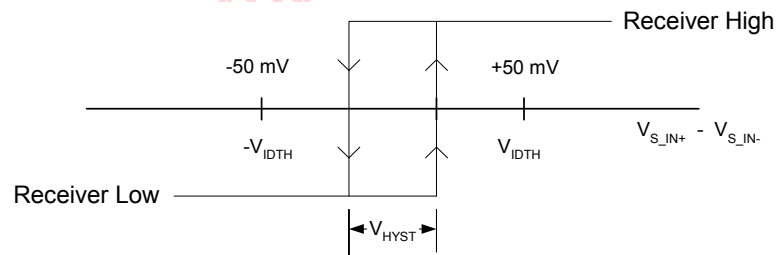
Figure 37: DC connection to a CML receiver



4.5.5.3 Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
V_I	Input Voltage range a or b	675		1725	mV
V_{IDTH}	Input Differential Threshold	-50		+50	mV
V_{HYST}	Input Differential Hysteresis	25			mV
R_{IN}	Receiver 100 Ω Differential Input Impedance	80		120	Ω

Figure 38: Input Differential Hysteresis



4.5.6 QSGMII Interface

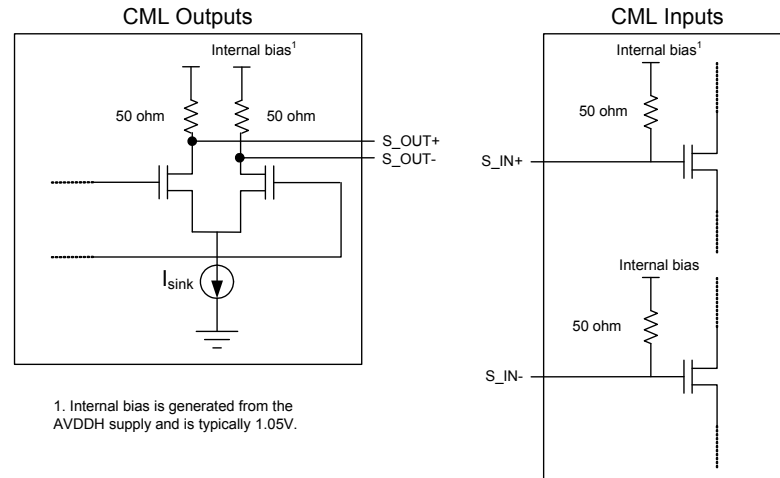
QSGMII specification is a de-facto standard proposed by Cisco. It is available at the Cisco website <ftp://ftp-eng.cisco.com/sgmii/sgmii.pdf>. It uses a modified LVDS specification based on the IEEE standard 1596.3. Refer to that standard for the exact definition of the terminology used in the following table. The device adds flexibility by allowing programmable output voltage swing and supply voltage option.

4.5.6.1 Transmitter DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T_Band	Baud Rate ¹		5000		Gsym/s
T_Vdiff	Output Differential Voltage (into floating Load Rload=100 Ohm) ²	400		900	mVppd
T_Rd	Differential Resistance	80	100	120	Ohms
T_SDD22	Differential Output Return Loss (100 MHz to 2.5 GHz) ³			-8	dB
T_SDD22	Differential Output Return Loss (2.5 GHz to 5 GHz) ⁴				dB
T_SCC22	Common Mode Return Loss (100 MHz to 2.5 GHz) ⁵			-6	dB
T_Ncm	Transmitter Common Mode Noise			5% of T-Vdiff	mVppd
	Output current into or out of driver pins when either SHORT to GND or each other ⁶			100	mA
T_Vcm	Output Common Mode Voltage See Note ⁷ , See Note ⁸ , See Note ⁹	0.0		1.8	V - Load Type0 ¹⁰
		735		1135	mV - Load Type1

- CEI-6G-SR is defined to operate between baud rates of 4.976 and 6.375 Gsym/s, However QSGMII will operate at 5 Gsym/s with a tolerance of +/-100ppm.
- Absolute driver output voltage shall be between -0.1V and 1.9V with respect to local ground. See [Figure 43](#) for details.
- See [Figure 42](#)
- See [Figure 42](#)
- See [Figure 42](#)
- ±100 mA
- For both Load Types: R_Rdin=100 Ohms+/- 20 Ohms. For Vcm definition, see [Figure 43](#).
- For Load Type 1: R_ZVt<30Ohms; Vt is defined follows: Load Type 1: R_Vt =1.2V +5%/-8%
- DC Coupling compliance is Type 1. It is acceptable for a Transmitter to restrict the range of T_Vdiff in order to comply with the specified T_Vcm range. For a transmitter which supports multiple T_Vdiff levels, it is acceptable for a Transmitter to claim DC Compliance if it meets the T_Vcm ranges for at least one of its T_Vdiff setting as long as those settings that are compliant are indicated.
- Load Type 0 with min T_Vdiff, AC Coupling or floating load.

Figure 39: CML I/Os



4.5.6.2 Common Mode Voltage (Voffset) Calculations

There are four different main configurations for the SGMII/Fiber interface connections. These are:

- DC connection to an LVDS receiver
- AC connection to an LVDS receiver
- DC connection to an CML receiver
- AC connection to an CML receiver

If AC coupling or DC coupling to an LVDS receiver is used, the DC output levels are determined by the following:

- Internal bias. See Figure 35 for details. (If AVDD18 is used to generate the internal bias, the internal bias value will typically be 1.05V.)



Note

For QSGMII, internal bias is also generated from the AVDDH supply and is typically 1.38V for output termination, and 1.2V for input termination.

- The output voltage swing is programmed by Register 26_1.2:0 (see Table 236).

Voffset (i.e., common mode voltage) = internal bias - single-ended peak-peak voltage swing. See Figure 36 for details.

If DC coupling is used with a CML receiver, then the DC levels will be determined by a combination of the MACs output structure and the input structure shown in the CML Inputs diagram in Figure 37. Assuming the same MAC CML voltage levels and structure, the common mode output levels will be determined by:

Voffset (i.e., common mode voltage) = internal bias - single-ended peak-peak voltage swing/2. See Figure 37 for details.

If DC coupling is used, the output voltage DC levels are determined by the AC coupling considerations above, plus the I/O buffer structure of the MAC.

Figure 40: AC connections (CML or LVDS receiver) or DC connection LVDS receiver

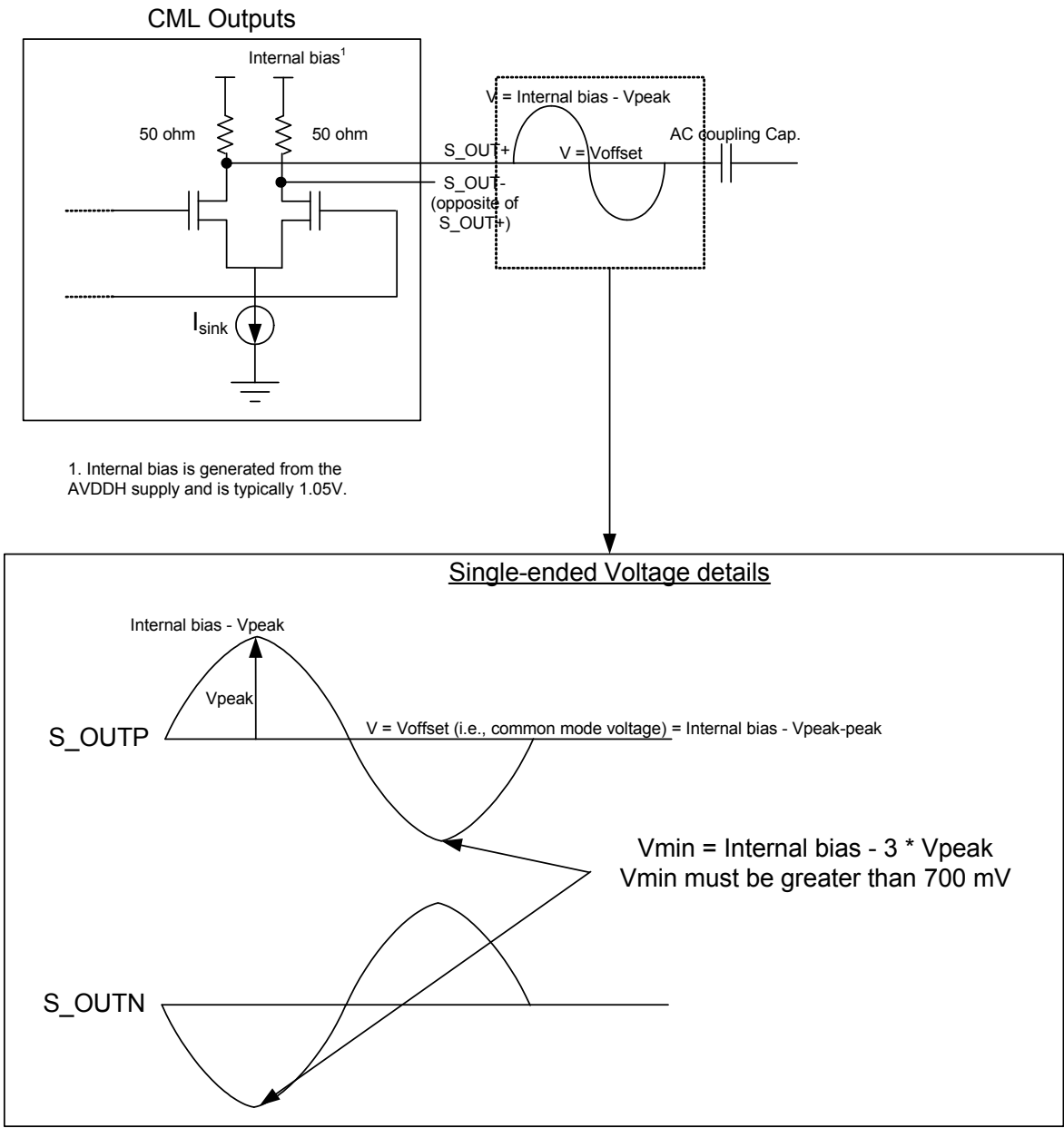
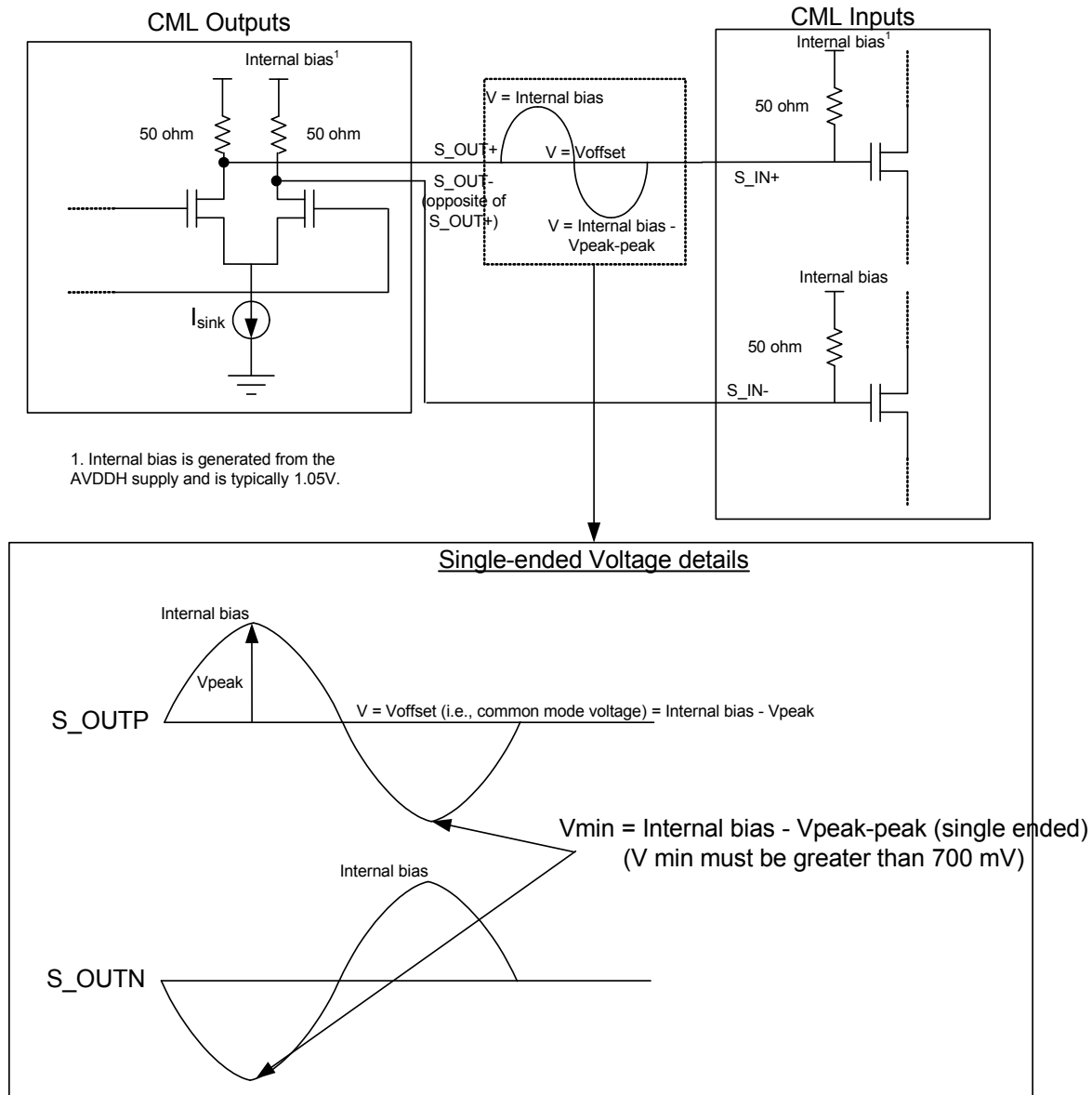


Figure 41: DC connection to a CML receiver



4.5.6.3 Receiver DC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
R_Baud	RX Baud Rate ¹		5.00		GSym/s
R_Vdiff	Input Differential Voltage ²	100		900	mVppd
R_Rdin	Differential Resistance	80	100	120	Ohms
R_Zvtt	Bias Voltage Source Impedance (Load Type 1) ³			30	Ohms
R_SDD1	Differential Input Return Loss (100MHz to 2.5 GHz) ⁴			-8	dB
R_SDD1	Differential Input Return Loss (2.5 GHz to 5 GHz) ⁵				dB
R_SCC1	Common Mode Input Return Loss (100 MHz to 2.5 GHz) ⁶			-6	dB
R_Vtt	Termination Voltage ⁷	Not Specified	Not Specified	Not Specified	⁸ R_Vtt floating, Load Type0
		1.2-8%		1.2+5%	R_Vtt=1.2V Nominal, Load Type1
R_Vrcm	Input Common Mode Voltage ⁹	-0.05		1.85	V
		720		R_Vtt-10	mV
n	Wander Divider ¹⁰			10	

- CEI-6G-SR is defined to operate between baud rates of 4.976 and 6.375 Gsym/s, However QSGMII will operate at 5 Gsym/s with a tolerance of +/-100ppm.
- Min Value is changed from the standard and reduced to 100 mV.
- Load Type 1 is with DC Coupling.
- See [Figure 42](#)
- See [Figure 42](#)
- See [Figure 42](#)
- For floating load, input resistance must be > iK Ohms.
- Input Common Mode voltage for AC-Coupled or floating load input with min T_Vdiff
- For Vcm definition, see [Figure 43](#).
- See Figure 2-27 & Figure 2-28 in CEI-6G-SR document for details

Figure 42: Driver and Receiver Differential Return Loss

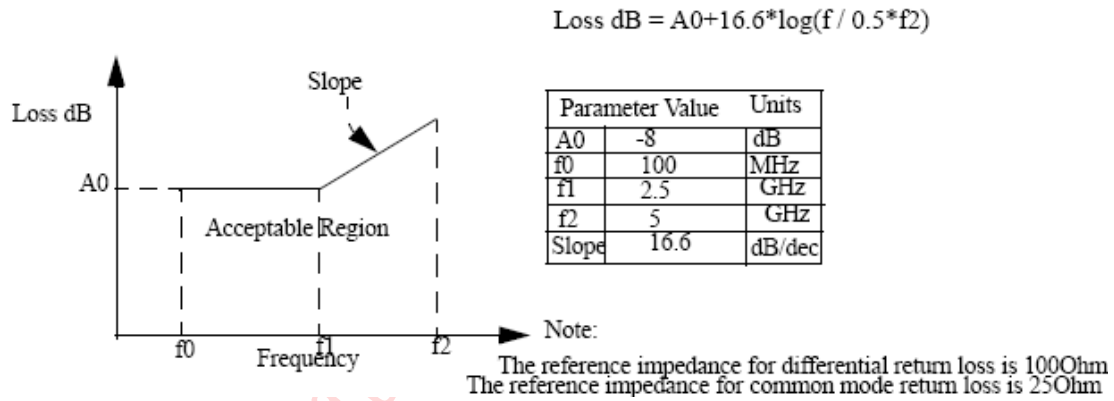
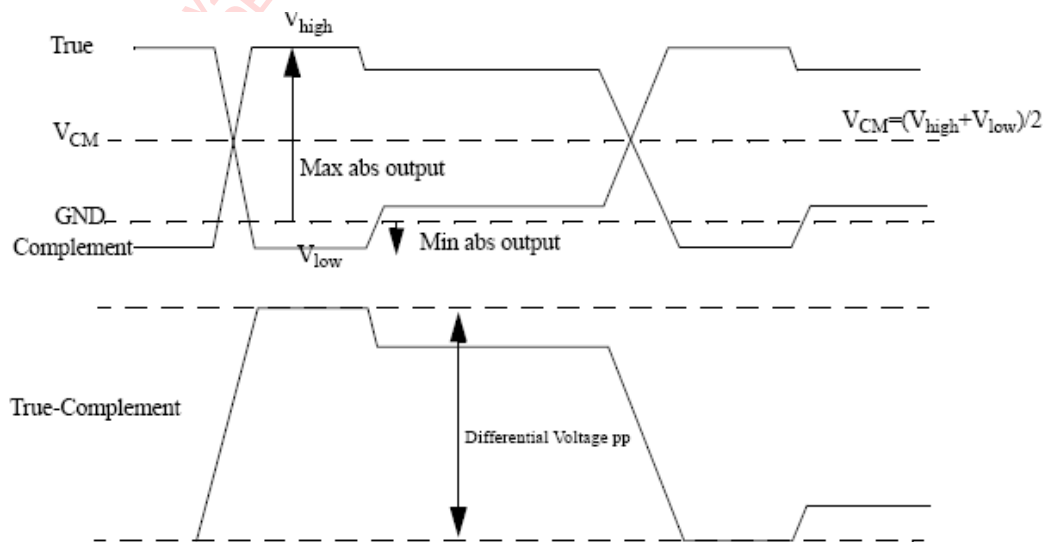


Figure 43: Definition of Driver Amplitude and Swing



4.5.7 REFCLKP/N Receiver Specifications

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)
All voltages are given with respect to receiver circuit ground voltage

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_i	Input voltage range		0		AVDD18	V
V_{icm}	Input common mode voltage range		300		1300	mV
V_{icm_delta}	Variation of Input common mode				50	mV
$V_{id\ p-p}$	Input differential voltage peak-to-peak		200 ¹		1200	mV
R_{in}	Receiver differential input impedance		80	100	120	Ω

- For 125 MHz single-ended clock, the minimum amplitude is 400 mV. The unused pin must be connected to 1 μ F capacitor to ground.

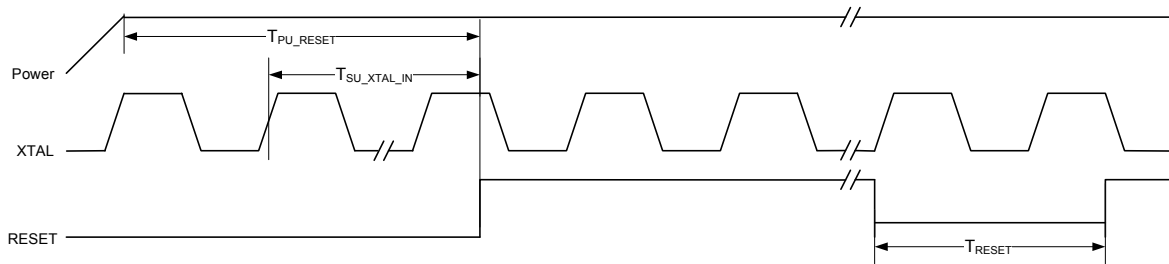
4.6 AC Electrical Specifications

4.6.1 Reset Timing

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{PU_RESET}	Valid power to RESET de-asserted		10			ms
$T_{SU_XTAL_IN}$	Number of valid XTAL_IN cycles prior to RESET de-asserted		10			clks
T_{RESET}	Minimum reset pulse width during normal operation		10			ms
T_{RESET_MDIO}	Minimum wait time from RESET de-assertion to first MDIO access		50			ms

Figure 44: Reset Timing



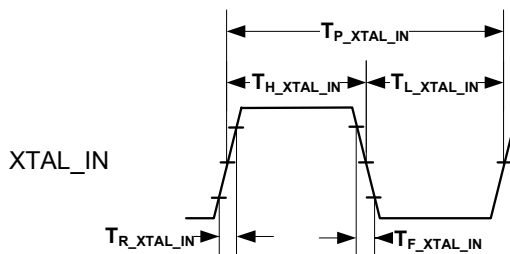
4.6.2 XTAL_IN/XTAL_OUT Timing¹

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P_XTAL_IN}$	XTAL_IN Period		40 -50 ppm	40	40 +50 ppm	ns
$T_{H_XTAL_IN}$	XTAL_IN High time		13	20	27	ns
$T_{L_XTAL_IN}$	XTAL_IN Low time		13	20	27	ns
$T_{R_XTAL_IN}$	XTAL_IN Rise	10% to 90%	-	3.0	5.0	ns
$T_{F_XTAL_IN}$	XTAL_IN Fall	90% to 10%	-	3.0	5.0	ns
$T_{J_XTAL_IN}$	XTAL_IN jitter ² (RMS)	12 kHz - 20 MHz (SGMII to Fiber/ SGMII mode)			3	ps
		12 kHz - 20 MHz (QSGMII to copper/ Fiber/SGMII mode)			1	ps

1. If the crystal option is used, ensure that the frequency is 25 MHz \pm 50 ppm. Capacitors must be chosen carefully - see application note supplied by the crystal vendor.
2. PLL generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.

Figure 45: XTAL_IN/XTAL_OUT Timing



Note

In order to meet the QSGMII transmit and receive jitter specifications, a 125 MHz or 156.25 MHz reference clock input is required. The 25 MHz reference clock input option should not be used for applications using the QSGMII interface.

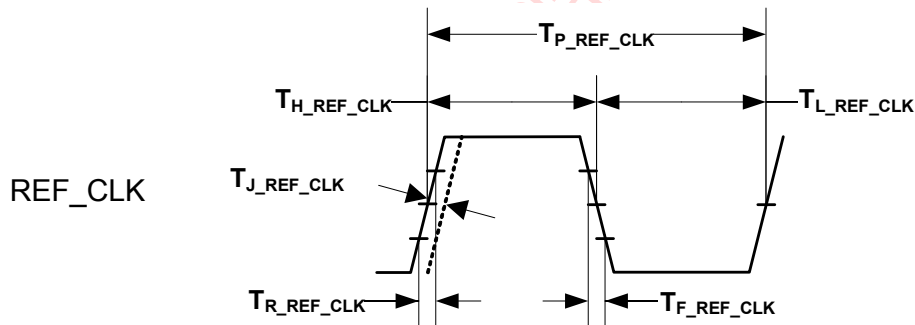
4.6.3 REFCLKP/N Receiver Specifications

(Over Full range of values listed in the Recommended Operating Conditions unless otherwise specified)
All voltages are given with respect to receiver circuit ground voltage

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{P_25_REF_CLK}$	25 MHz REF_CLK Period	CLK_SEL[1:0] = 10 ¹	40 -50 ppm	40	40 +50 ppm	ns
$T_{H_25_REF_CLK}$	25 MHz REF_CLK High Time		13	20	27	ns
$T_{L_25_REF_CLK}$	25 MHz REF_CLK Low Time		13	20	27	ns
T_r/T_f	Rise and Fall Time (10% - 90%)		260	3000	6400	ps
$T_{P_125_REF_CLK}$	125 MHz REF_CLK Period	CLK_SEL[1:0] = 01 ¹	8 -50 ppm	8	8 +50 ppm	ns
$T_{H_125_REF_CLK}$	125 MHz REF_CLK High Time		2.6	4	5.4	ns
$T_{L_125_REF_CLK}$	125 MHz REF_CLK Low Time		2.6	4	5.4	ns
T_r/T_f	Rise and Fall Time (10% - 90%)		260	600	1280	ps
$T_{P_156_REF_CLK}$	156.25 MHz REF_CLK Period	CLK_SEL[1:0] = 00 ¹	6.4 -50 ppm	6.4	6.4 +50 ppm	ns
$T_{H_156_REF_CLK}$	156.25 MHz REF_CLK High Time		2.1	3.2	4.3	ns
$T_{L_156_REF_CLK}$	156.25 MHz REF_CLK Low Time		2.1	3.2	4.3	ns
T_r/T_f	Rise and Fall Time (10% - 90%)		260	480	1024	ps
t_{skew}	Skew tolerable at receiver input to meet setup and hold time requirements				325	ps
$T_{J_REF_CLK}$	REF_CLK Jitter (RMS)	12 kHz - 20 MHz (SGMII mode)			3	ps
		12 kHz - 20 MHz (QSGMII mode)			1	ps

1. See "Configuring the Device" on page 138 for details.

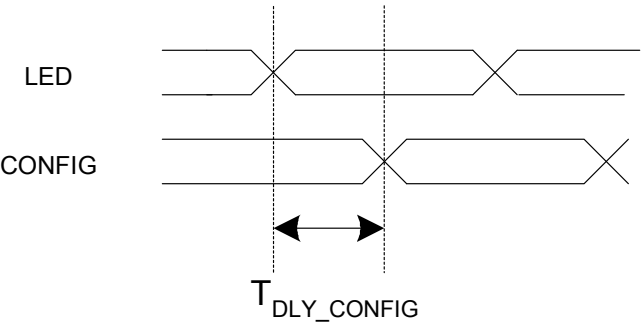
Figure 46: REF_CLK Timing



4.6.4 LED to CONFIG Timing

Symbol	Parameter	Condition	Min	Typ	Max	Units
T _{DLY_CONFIG}	LED to CONFIG Delay		0		25	ns

Figure 47: LED to CONFIG Timing



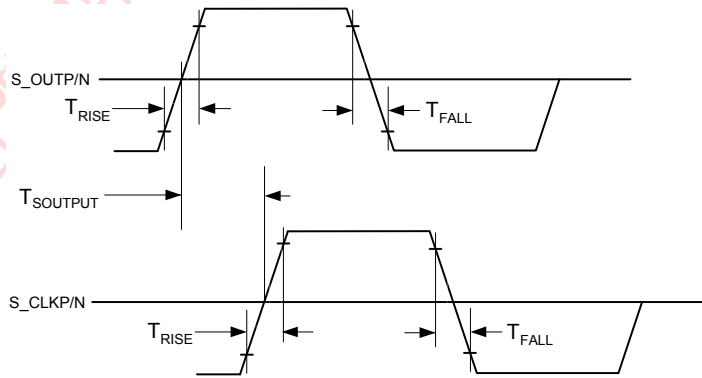
4.7 SGMII Interface Timing

4.7.1 SGMII Output AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T_{FALL}	V_{OD} Fall time (20% - 80%)	100		200	ps
T_{RISE}	V_{OD} Rise time (20% - 80%)	100		200	ps
CLOCK	Clock signal duty cycle @ 625 MHz	48		52	%
T_{SKEW1}^1	Skew between two members of a differential pair			20	ps
$T_{SOUTPUT}^2$	SERDES output to RxClk_P/N	360	400	440	ps
$T_{OutputJitter}$	Total Output Jitter Tolerance (Deterministic + 14*rms Random)		127		ps

1. Skew measured at 50% of the transition.
2. Measured at 50% of the transition.

Figure 48: Serial Interface Rise and Fall Times



4.7.2 SGMII Input AC Characteristics

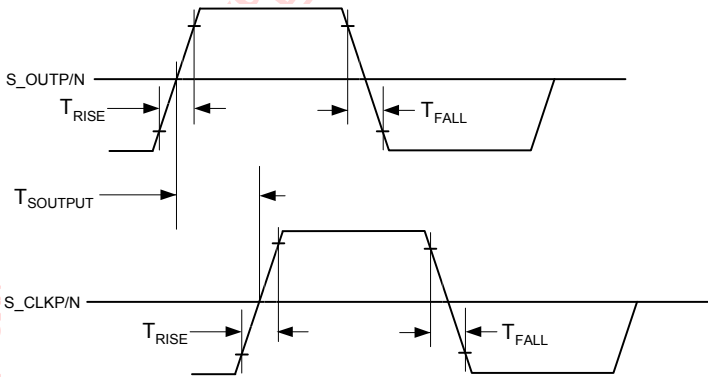
Symbol	Parameter	Min	Typ	Max	Units
$T_{InputJitter}$	Total Input Jitter Tolerance (Deterministic + 14*rms Random)			599	ps

4.8 QSGMII Interface Timing

4.8.1 QSGMII Output AC Characteristics

Symbol	Parameter	Min	Typ	Max	Units
T _{FALL}	V _{OD} Fall time (20% - 80%)	30			ps
T _{RISE}	V _{OD} Rise time (20% - 80%)	30			ps
T _{OutputJitter}	Total Output Jitter Tolerance		60		ps

Figure 49: Serial Interface Rise and Fall Times

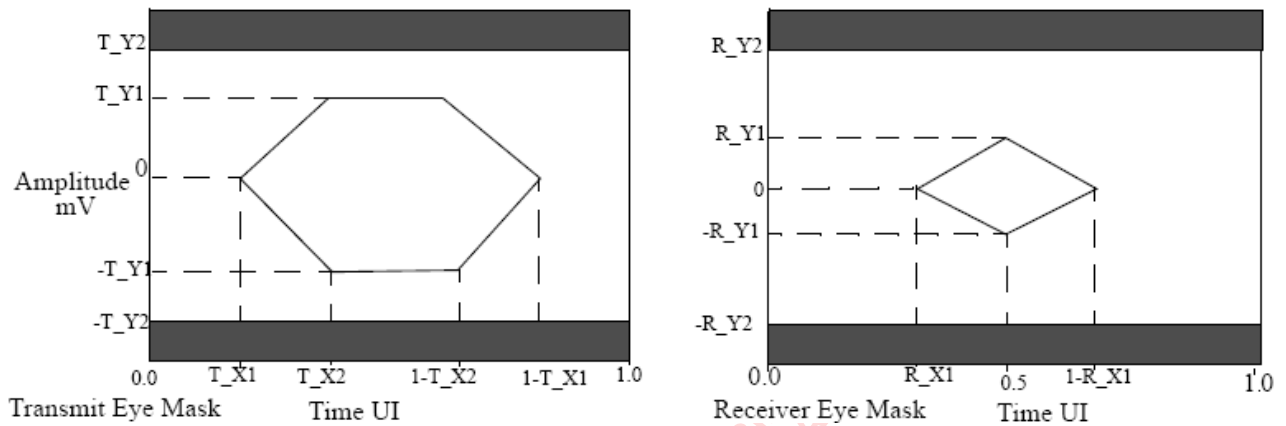


4.8.2 QSGMII Receiver Input Jitter Tolerance Specifications

Symbol	Parameter	Min	Typ	Max	Units
R_BHPJ	Bounded High Probability Jitter ¹			0.45	UIpp
R_SJ-max	Sinusoidal Jitter, maximum			5	UIpp
R_SJ-hf	Sinusoidal Jitter, High Frequency			0.05	UIpp
R_TJ	Total Jitter (does not include Sinusoidal Jitter) ²			0.60	UIpp
R_X1	Eye Mask ³			0.30	UI
R_Y1	Eye Mask ⁴			50	mV
R_Y2	Eye Mask ⁵			450	mV

1. This is the sum of Uncorrelated Bounded High Probability Jitter (0.15 UI) and Correlated Bounded High Probability Jitter (0.30 UI)
Uncorrelated Bounded High Probability Jitter: Jitter distribution where the value of the jitter show no correlation to any signal level being transmitted. Formally defined as deterministic jitter, T_DJ
Correlated Bounded High Probability Jitter: Jitter distribution where the value of the jitter shows a strong correlation to the signal level being transmitted. This jitter may be considered as being equalisable due to its correlation to the signal level
2. The link will operate with a BER or 10^{-15}
3. See Figure 50
4. See Figure 50
5. See Figure 50

Figure 50: Driver and Receiver Eye Mask



4.9 MDC/MDIO Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time		0		20	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time		10			ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time		10			ns
T_{P_MDC}	MDC Period		80			ns ¹
T_{H_MDC}	MDC High		30			ns
T_{L_MDC}	MDC Low		30			ns
V_{HYST}	VDDO Input Hysteresis			360		mV

1. Maximum frequency = 12.5 MHz.

Figure 51: MDC/MDIO Timing

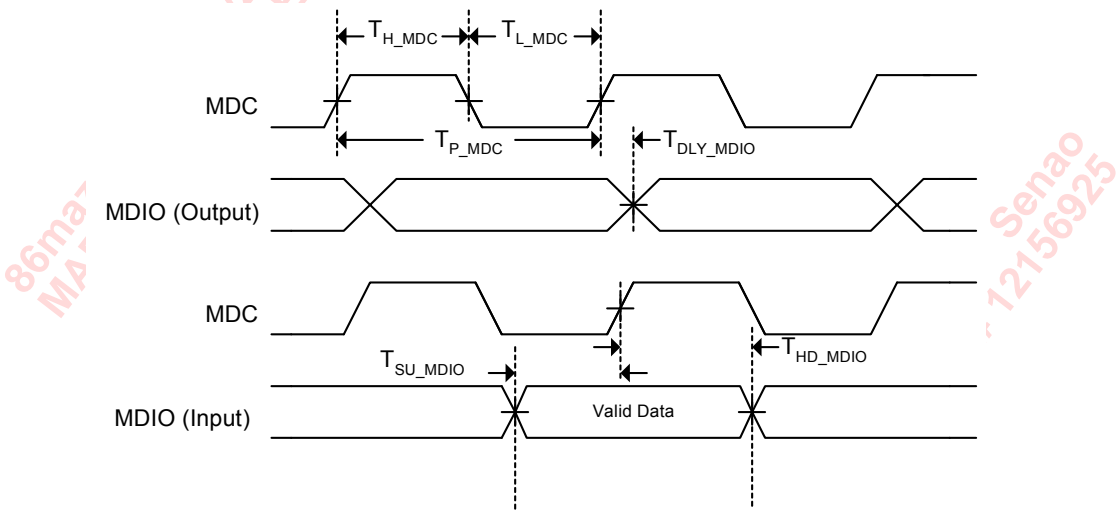
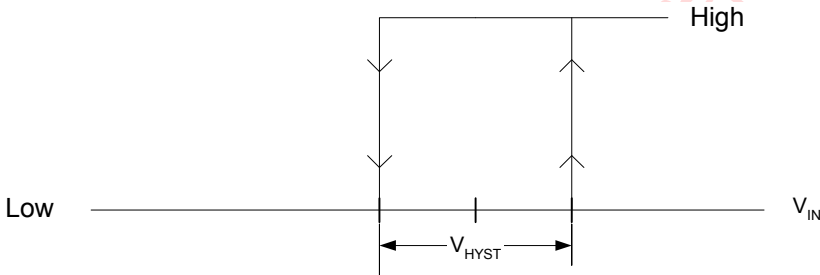


Figure 52: MDC/MDIO Input Hysteresis

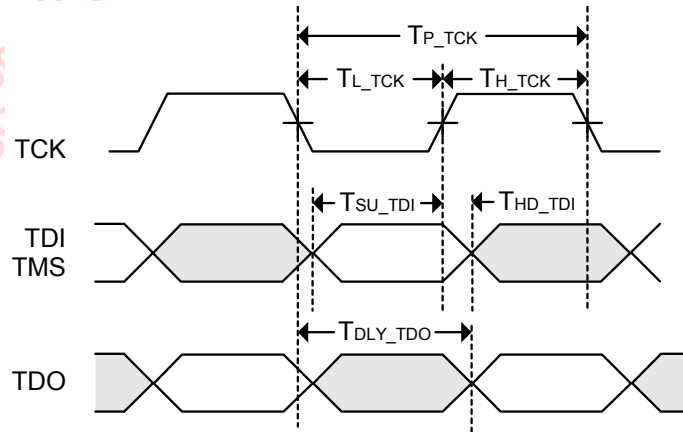


4.9.1 JTAG Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{P_TCK}	TCK Period		60			ns
T_{H_TCK}	TCK High		12			ns
T_{L_TCK}	TCK Low		12			ns
T_{SU_TDI}	TDI, TMS to TCK Setup Time		10			ns
T_{HD_TDI}	TDI, TMS to TCK Hold Time		10			ns
T_{DLY_TDO}	TCK to TDO Delay		0		15	ns

Figure 53: JTAG Timing



4.10 IEEE AC Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by number. For an exact description of the templates and the test conditions, refer to the IEEE specifications:

-10BASE-T IEEE 802.3 Clause 14-2000

-100BASE-TX ANSI X3.263-1995

-1000BASE-T IEEE 802.3ab Clause 40 Section 40.6.1.2 Figure 40-26 shows the template waveforms for transmitter electrical specifications.

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition	Min	Typ	Max	Units
T_{RISE}	Rise time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{FALL}	Fall Time	MDIP/N[1:0]	100BASE-TX	3.0	4.0	5.0	ns
T_{RISE}/T_{FALL} Symmetry		MDIP/N[1:0]	100BASE-TX	0		0.5	ns
DCD	Duty Cycle Distortion	MDIP/N[1:0]	100BASE-TX	0		0.5 ¹	ns, peak-peak
Transmit Jitter		MDIP/N[1:0]	100BASE-TX	0		1.4	ns, peak-peak

1. ANSI X3.263-1995 Figure 9-3

4.11 Latency Timing

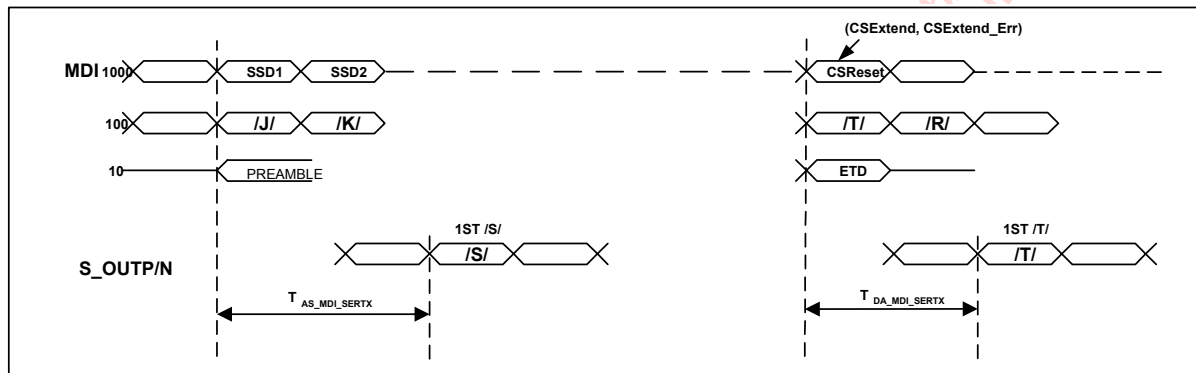
4.11.1 10/100/1000BASE-T to SGMII Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS_MDI_SERT}$ X_{1000}	MDI SSD1 to S_OUTP/N Start of Packet		292 ^{1,2}		336	ns
$T_{DA_MDI_SERT}$ X_{1000}	MDI CSReset, CSExtend, CSExtend_Err to S_OUTP/N /T/		292 ^{1,2,3}		336	ns
$T_{AS_MDI_SERT}$ X_{100}	MDI /J/ to S_OUTP/N Start of Packet		620 ²		732	ns
$T_{DA_MDI_SERT}$ X_{100}	MDI /T/ to S_OUTP/N /T/		620 ^{2,3}		732	ns
$T_{AS_MDI_SERT}$ X_{10}	MDI Preamble to S_OUTP/N Start of Packet		4817 ^{2,4}		5603	ns
$T_{DA_MDI_SERT}$ X_{10}	MDI ETD to S_OUTP/N /T/		4817 ^{2,3,4}		5603	ns

1. In 1000BASE-T the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDIP/N[3:0] is referenced from the latest arriving signal.
2. Assumes Register 16.13:12 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
3. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on MDI and S_OUTP/N. The worst case variation will be outside these limits if there is a frequency difference.
4. Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

Figure 54: 10/100/1000BASE-T to SGMII Latency Timing



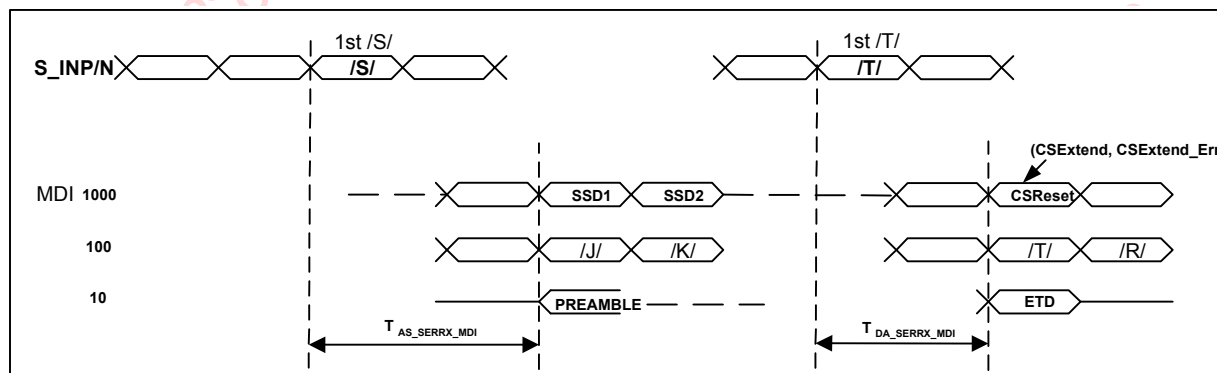
4.11.2 SGMII to 10/100/1000BASE-T Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS_SERRX_MDI_1000}$	S_INP/N Start of Packet /S/ to MDI SSD1		192 ¹		216	ns
$T_{DA_SERRX_MDI_1000}$	S_INP/N /T/ to MDI CSReset, CSExtend, CSExtend_Err		192 ^{1,2}		216	ns
$T_{AS_SERRX_MDI_100}$	S_INP/N Start of Packet /S/ to MDI /J/		528 ¹		612	ns
$T_{DA_SERRX_MDI_100}$	S_INP/N /T/ to MDI /T/		528 ^{1,2}		612	ns
$T_{AS_SERRX_MDI_10}$	S_INP/N Start of Packet /S/ to MDI Preamble		3822 ¹		4634	ns
$T_{DA_SERRX_MDI_10}$	S_INP/N /T/ to MDI ETD		3822 ^{1,2}		4634	ns

1. Assumes register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and the received signal on S_INP/N. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 55: SGMII to 10/100/1000BASE-T Latency Timing



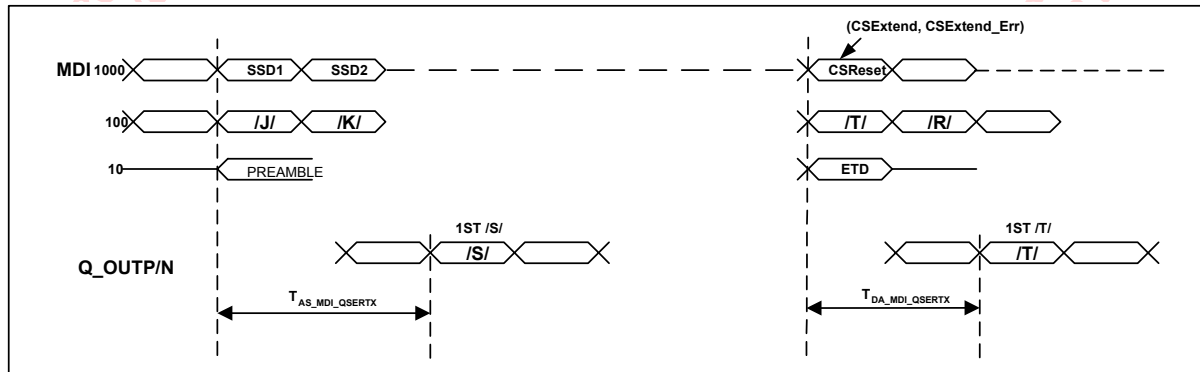
4.11.3 10/100/1000BASE-T to QSGMII Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS_MDI_QSERTX_1000}$	MDI SSD1 to Q_OUTP/N Start of Packet		308 ^{1,2}		356	ns
$T_{DA_MDI_QSERTX_1000}$	MDI CSReset, CSExtend, CSExtend_Err to Q_OUTP/N /T/		308 ^{1,2,3}		356	ns
$T_{AS_MDI_QSERTX_100}$	MDI /J/ to Q_OUTP/N Start of Packet		628 ²		744	ns
$T_{DA_MDI_QSERTX_100}$	MDI /T/ to Q_OUTP/N /T/		628 ^{2,3}		744	ns
$T_{AS_MDI_QSERTX_10}$	MDI Preamble to Q_OUTP/N Start of Packet		4825 ^{2,4}		5615	ns
$T_{DA_MDI_QSERTX_10}$	MDI ETD to Q_OUTP/N /T/		4825 ^{2,3,4}		5615	ns

1. In 1000BASE-T the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDIP/N[3:0] is referenced from the latest arriving signal.
2. Assumes Register 16.13:12 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
3. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on MDI and Q_OUTP/N. The worst case variation will be outside these limits if there is a frequency difference.
4. Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

Figure 56: 10/100/1000BASE-T to QSGMII Latency Timing



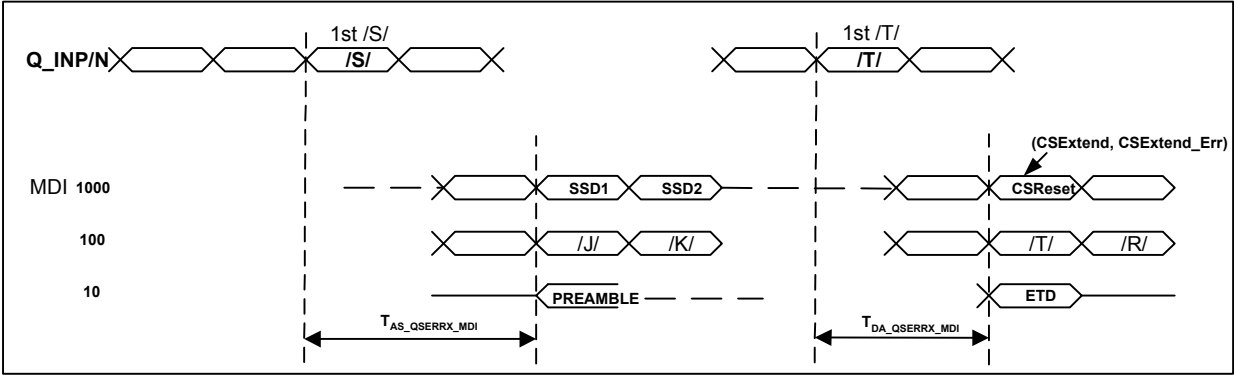
4.11.4 QSGMII to 10/100/1000BASE-T Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T _{AS_QSERRX_MDI_1000}	Q_INP/N Start of Packet /S/ to MDI SSD1		222 ¹		250	ns
T _{DA_QSERRX_MDI_1000}	Q_INP/N /T/ to MDI CSReset, CSExtend, CSExtend_Err		222 ^{1,2}		250	ns
T _{AS_QSERRX_MDI_100}	Q_INP/N Start of Packet /S/ to MDI /J/		506 ¹		614	ns
T _{DA_QSERRX_MDI_100}	Q_INP/N /T/ to MDI /T/		506 ^{1,2}		614	ns
T _{AS_QSERRX_MDI_10}	Q_INP/N Start of Packet /S/ to MDI Preamble		3827 ¹		4644	ns
T _{DA_QSERRX_MDI_10}	Q_INP/N /T/ to MDI ETD		3827 ^{1,2}		4644	ns

1. Assumes register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and the received signal on Q_INP/N. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 57: QSGMII to 10/100/1000BASE-T Latency Timing



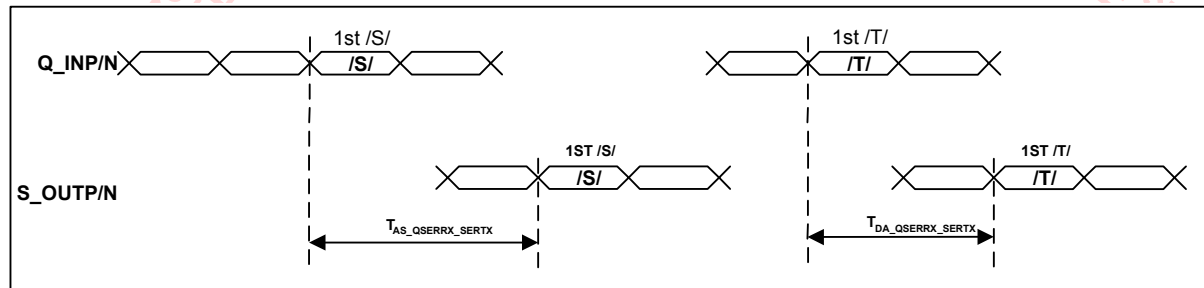
4.11.5 QSGMII to SGMII Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS_QSERRX_SERTX_1000}$	Q_INP/N Start of Packet to S_OUTP/N Start of Packet		156 ¹		232	ns
$T_{DA_QSERRX_SERTX_1000}$	Q_INP/N /T/ to S_OUTP/N /T/		156 ^{1,2}		232	ns
$T_{AS_QSERRX_SERTX_100}$	Q_INP/N Start of Packet to S_OUTP/N Start of Packet		520 ¹		700	ns
$T_{DA_QSERRX_SERTX_100}$	Q_INP/N /T/ to S_OUTP/N /T/		520 ^{1,2}		700	ns
$T_{AS_QSERRX_SERTX_10}$	Q_INP/N Start of Packet to S_OUTP/N Start of Packet		4212 ¹		5472	ns
$T_{DA_QSERRX_SERTX_10}$	Q_INP/N /T/ to S_OUTP/N /T/		4212 ^{1,2}		5472	ns

- Assumes register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
- Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on S_OUTP/N and the received signal on Q_INP/N. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 58: QSGMII to SGMII Latency Timing



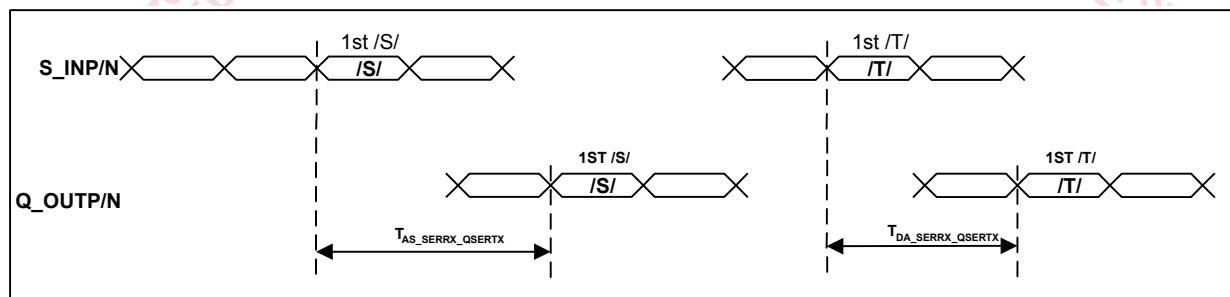
4.11.6 SGMII to QSGMII Latency Timing

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS_SERRX_QSERTX_1000}$	S_INP/N Start of Packet /S/ to Q_OUTP/N Start of Packet /S/		164 ¹		224	ns
$T_{DA_SERRX_QSERTX_1000}$	S_INP/N /T/ to Q_OUTP/N /T/		164 ^{1,2}		224	ns
$T_{AS_SERRX_QSERTX_100}$	S_INP/N Start of Packet /S/ to Q_OUTP/N Start of Packet /S/		472 ¹		636	ns
$T_{DA_SERRX_QSERTX_100}$	S_INP/N /T/ to Q_OUTP/N /T/		472 ^{1,2}		636	ns
$T_{AS_SERRX_QSERTX_10}$	S_INP/N Start of Packet /S/ to Q_OUTP/N Start of Packet /S/		3804 ¹		5048	ns
$T_{DA_SERRX_QSERTX_10}$	S_INP/N /T/ to Q_OUTP/N /T/		3804 ^{1,2}		5048	ns

- Assumes register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
- Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on Q_OUTP/N and the received signal on S_INP/N. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 59: SGMII to QSGMII Latency Timing



4.11.7 SGMII to Auto-media Latency Timing

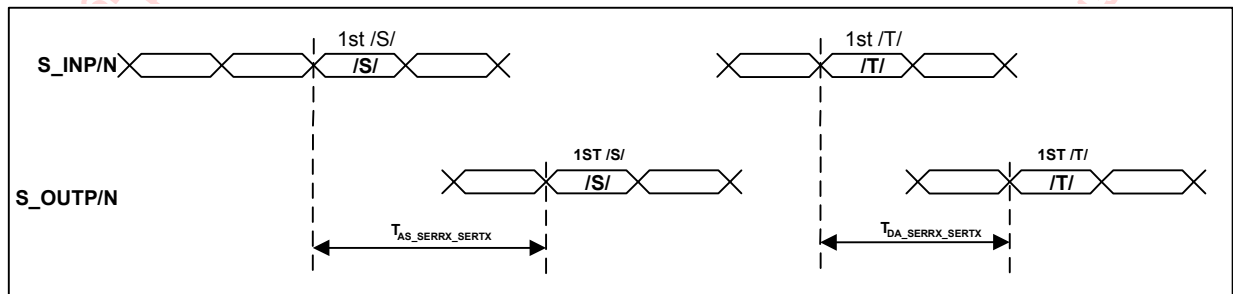
4.11.7.1 SGMII to SGMII/Fiber Latency Timing (Register 27_4.14 = 1¹)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T _{AS_SERRX_SERTX_1000}	S_INP/N Start of Packet /S/ to S_OUTP/N Start of Packet /S/		252 ¹		336	ns
T _{DA_SERRX_SERTX_1000}	S_INP/N /T/ to S_OUTP/N /T/		252 ^{1,2}		336	ns
T _{AS_SERRX_SERTX_100}	S_INP/N Start of Packet /S/ to S_OUTP/N Start of Packet /S/		876 ¹		1172	ns
T _{DA_SERRX_SERTX_100}	S_INP/N /T/ to S_OUTP/N /T/		876 ^{1,2}		1172	ns
T _{AS_SERRX_SERTX_10}	S_INP/N Start of Packet /S/ to S_OUTP/N Start of Packet /S/		7548 ¹		10008	ns
T _{DA_SERRX_SERTX_10}	S_INP/N /T/ to S_OUTP/N /T/		7548 ^{1,2}		10008	ns

- Assumes register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
- Minimum and maximum values on end of packet assume zero frequency drift between the signal on S_OUTP/N and the signal on S_INP/N. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 60: SGMII to SGMII/Fiber Latency Timing (Register 27_4.14 = 1)



1. SGMII to SGMII/Fiber latency timing only applies when QSGMII crossover loopback is enabled. See [Section 2.5.5, QSGMII Crossover Muxing and Loopback](#), on page 77 for details.

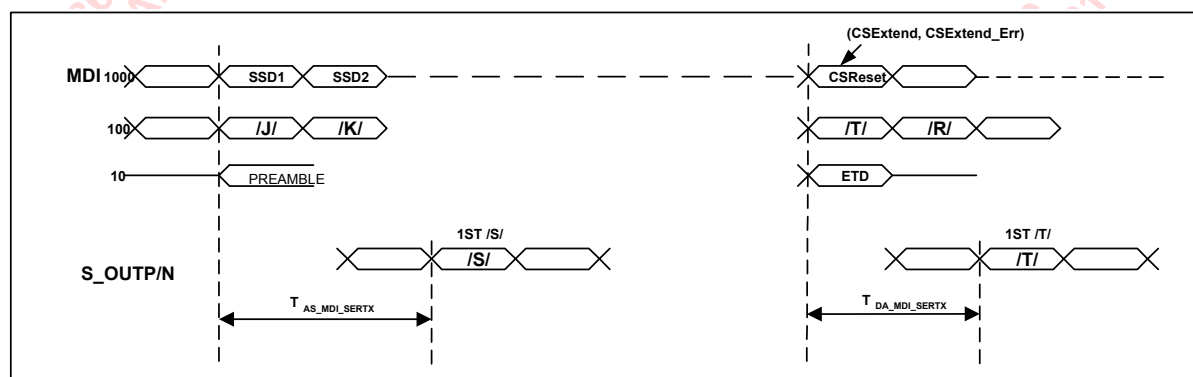
4.11.7.2 10/100/1000BASE-T to SGMII Latency Timing (Register 27_4.14 = 1¹)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
$T_{AS_MDI_SERT}$ X_{1000}	MDI SSD1 to S_OUTP/N Start of Packet		404 ^{1,2}		484	ns
$T_{DA_MDI_SERT}$ X_{1000}	MDI CSReset, CSExtend, CSExtend_Err to S_OUTP/N /T/		404 ^{1,2,3}		484	ns
$T_{AS_MDI_SERT}$ X_{100}	MDI /J/ to S_OUTP/N Start of Packet		1048 ²		1300	ns
$T_{DA_MDI_SERT}$ X_{100}	MDI /T/ to S_OUTP/N /T/		1048 ^{2,3}		1300	ns
$T_{AS_MDI_SERT}$ X_{10}	MDI Preamble to S_OUTP/N Start of Packet		8577 ^{2,4}		10583	ns
$T_{DA_MDI_SERT}$ X_{10}	MDI ETD to S_OUTP/N /T/		8577 ^{2,3,4}		10583	ns

1. In 1000BASE-T the signals on the 4 MDI pairs arrive at different times because of the skew introduced by the cable. All timing on MDIP/N[3:0] is referenced from the latest arriving signal.
2. Assumes Register 16.13:12 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
3. Minimum and maximum values on end of packet assume zero frequency drift between the received signal on MDI and S_OUTP/N. The worst case variation will be outside these limits if there is a frequency difference.
4. Actual values depend on number of bits in preamble and number of dribble bits, since nibbles on MII are aligned to start of frame delimiter and dribble bits are truncated.

Figure 61: 10/100/1000BASE-T to SGMII Latency Timing (Register 27_4.14 = 1)



1. 10/100/1000BASE-T to SGMII latency timing (Register 27_4.14 = 1) only applies when QSGMII crossover loopback is enabled. See Section 2.5.5, QSGMII Crossover Muxing and Loopback, on page 77 for details.

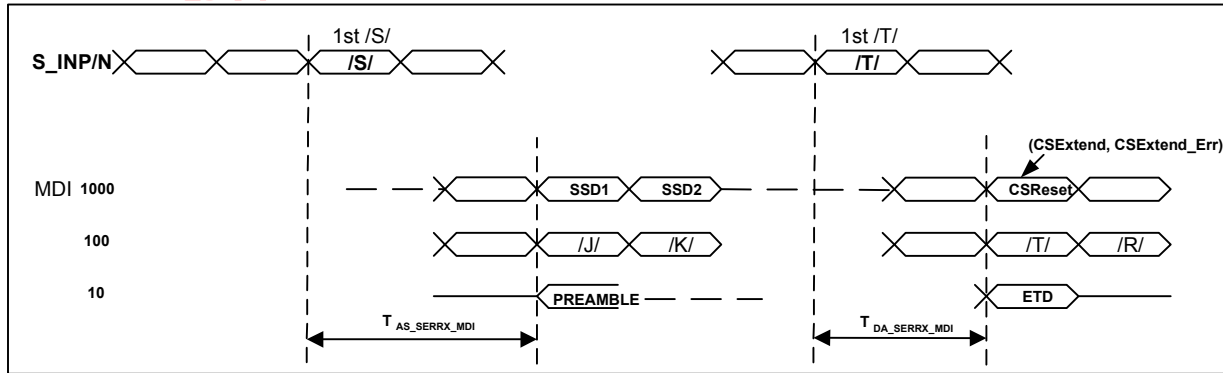
4.11.7.3 SGMII to 10/100/1000BASE-T Latency Timing (Register 27_4.14 = 1¹)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Units
T _{AS_SERRX_MDI_1000}	S_INP/N Start of Packet /S/ to MDI SSD1		304 ¹		364	ns
T _{DA_SERRX_MDI_1000}	S_INP/N /T/ to MDI CSReset, CSExtend, CSExtend_Err		304 ^{1,2}		364	ns
T _{AS_SERRX_MDI_100}	S_INP/N Start of Packet /S/ to MDI /J/		952 ¹		1180	ns
T _{DA_SERRX_MDI_100}	S_INP/N /T/ to MDI /T/		952 ^{1,2}		1180	ns
T _{AS_SERRX_MDI_10}	S_INP/N Start of Packet /S/ to MDI Preamble		7582 ¹		9615	ns
T _{DA_SERRX_MDI_10}	S_INP/N /T/ to MDI ETD		7582 ^{1,2}		9615	ns

1. Assumes register 16.15:14 is set to 00, which is the minimum latency. Each increase in setting adds 8 ns of latency in 1000 Mbps, 40 ns in 100 Mbps, and 400 ns in 10 Mbps.
2. Minimum and maximum values on end of packet assume zero frequency drift between the transmitted signal on MDI and the received signal on S_INP/N. The worst case variation will be outside these limits, if there is a frequency difference.

Figure 62: SGMII to 10/100/1000BASE-T Latency Timing (Register 27_4.14 = 1)



1. SGMII to 10/100/1000BASE-T (Register 27_4.14 = 1) latency timing only applies when QSGMII crossover loopback is enabled. See Section 2.5.5, QSGMII Crossover Muxing and Loopback, on page 77 for details.

5 Mechanical Drawings

5.1 128-Pin LQFP Package Drawing

Figure 63: 128-Pin LQFP Package

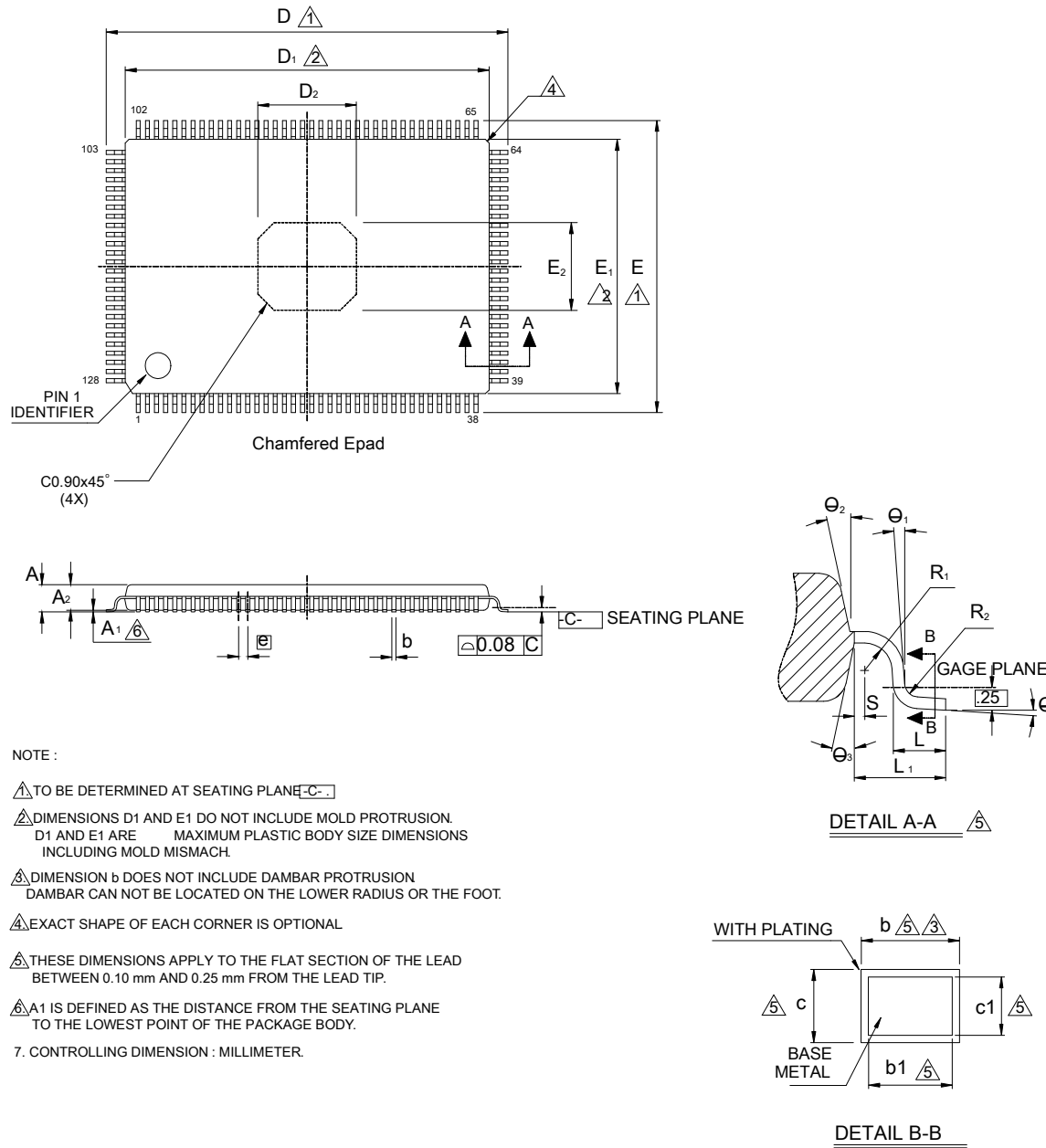


Table 237: 128-Pin LQFP Package Dimensions in mm

Symbol	Dimension in mm		
	Min	Nom	Max
A	--	--	1.60
A ₁	0.05	--	0.15
A ₂	1.35	1.40	1.45
b	0.17	0.22	0.27
b ₁	0.17	0.20	0.23
c	0.09	--	0.20
c ₁	0.09	--	0.16
D	21.90	22.00	22.10
D ₁	19.90	20.00	20.10
E	15.90	16.00	16.10
E ₁	13.90	14.00	14.10
e	0.50 BSC		
L	0.45	0.60	0.75
L ₁	1.00 REF		
R ₁	0.08	--	--
R ₂	0.08	--	0.20
S	0.20	--	--
θ	0°	3.5°	7°
θ ₁	4° TYP		
θ ₂	12° TYP		
θ ₃	12° TYP		

Exposed Pad Size	
D ₂	6.40
E ₂	3.91

5.2 196-Pin TFBGA Package Drawing

Figure 64: 196-Pin TFBGA Package

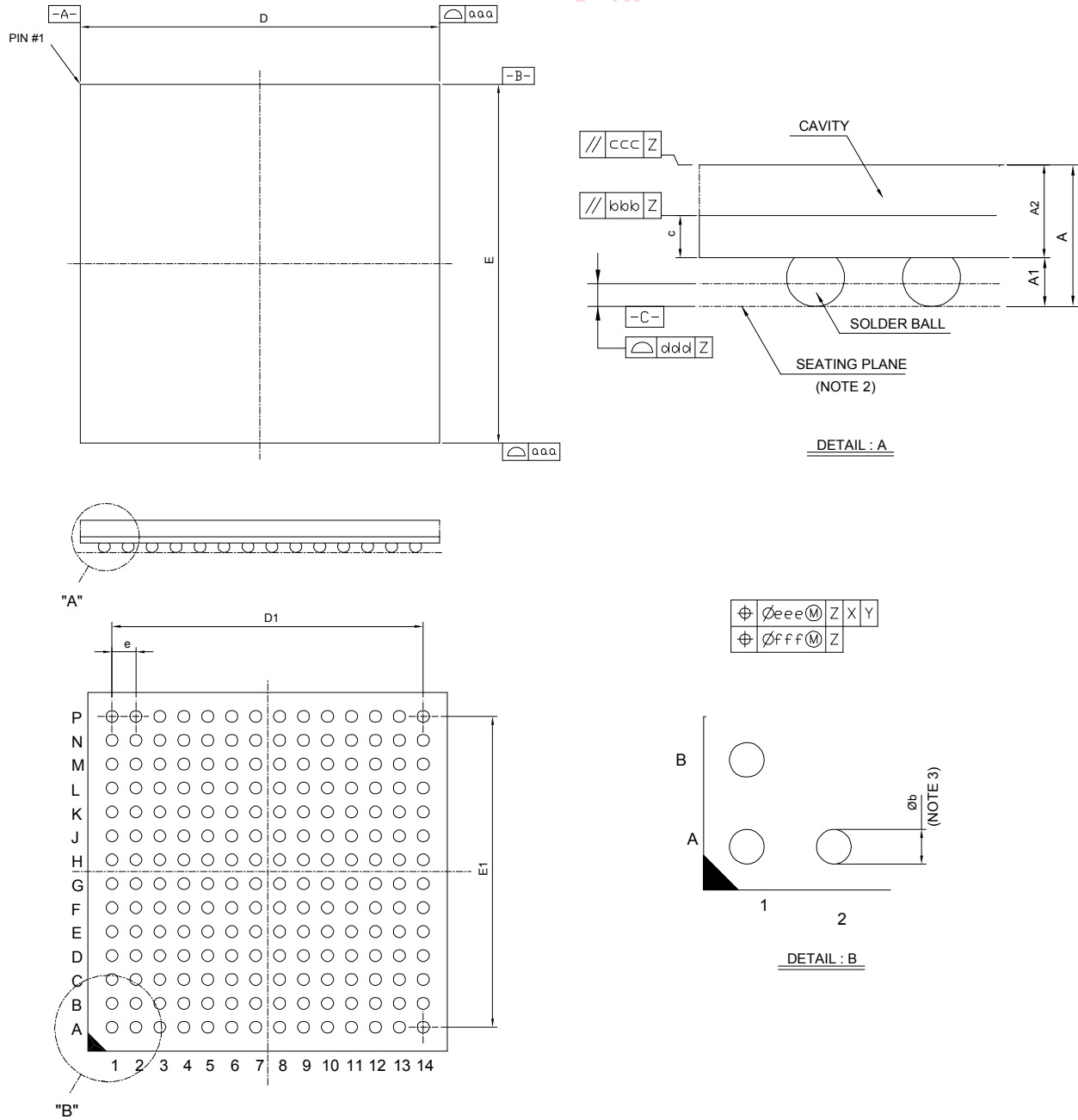


Table 238: 196-Pin TFBGA Package Dimensions (mm)

Symbol	Dimension in mm		
	Min	Nom	Max
A	---	---	1.50
A1	0.30	0.40	0.50
A2	---	0.89	---
c	---	0.36	---
D	14.90	15.00	15.10
E	14.90	15.00	15.10
D1	---	13.00	---
E1	---	13.00	---
e	---	1.00	---
b	0.40	0.50	0.60
aaa	0.20		
bbb	0.25		
ccc	0.35		
ddd	0.12		
eee	0.25		
fff	0.10		
MD/ME	14/14		



Note

1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. THERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.

6 Order Information

6.1 Ordering Part Numbers and Package Markings

Figure 65 shows the ordering part numbering scheme for the device. Contact Marvell® FAEs or sales representatives for complete ordering information.

Figure 65: Sample Part Number

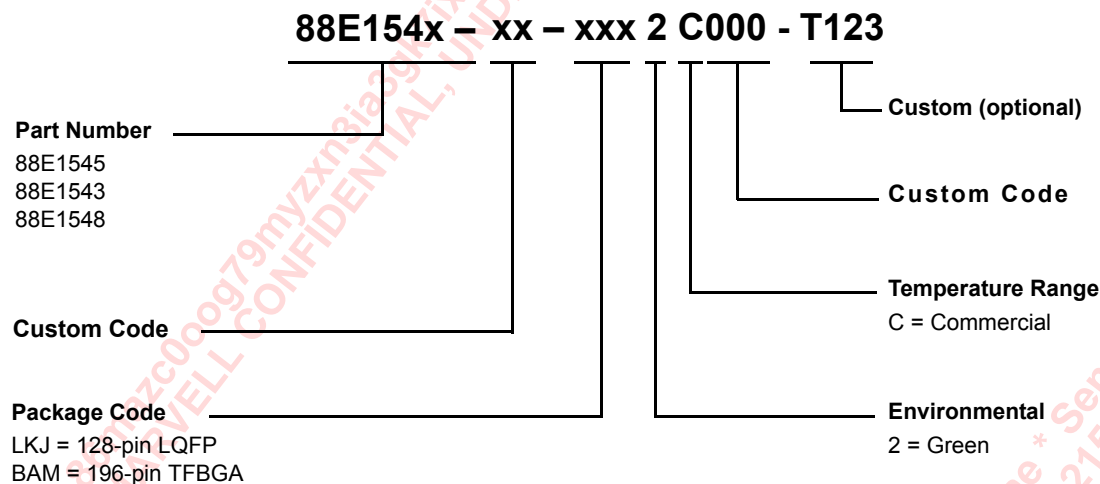


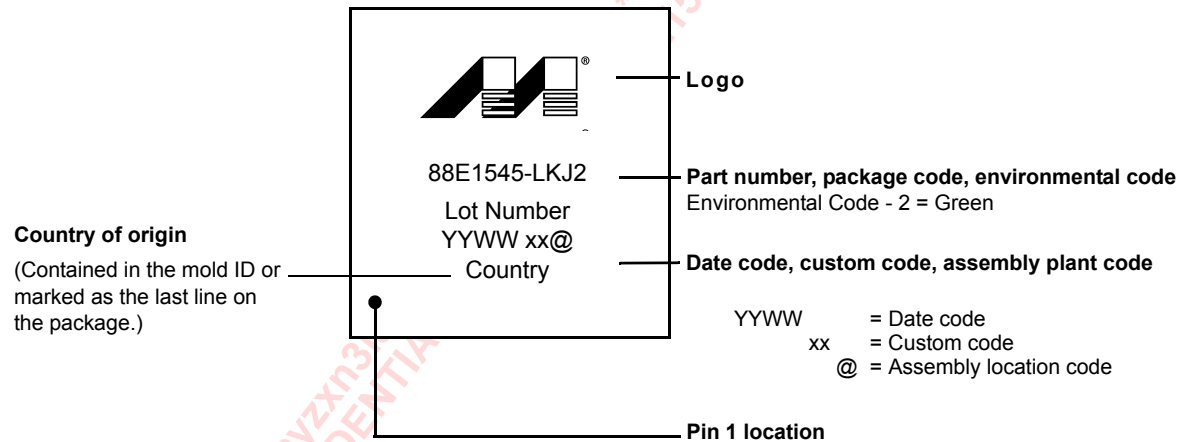
Table 239: Part Order Numbers

Package Type	Part Order Number
88E1545 128-pin LQFP - Commercial	88E1545-XX-LKJ2C000
88E1543 128-pin LQFP - Commercial	88E1543-XX-LKJ2C000
88E1548 196-pin TFBGA - Commercial	88E1548-XX-BAM2C000

6.1.1 Package Marking Examples

Figure 66 is an example of the package marking and pin 1 location for the 88E1545 128-pin LQFP commercial Green package.

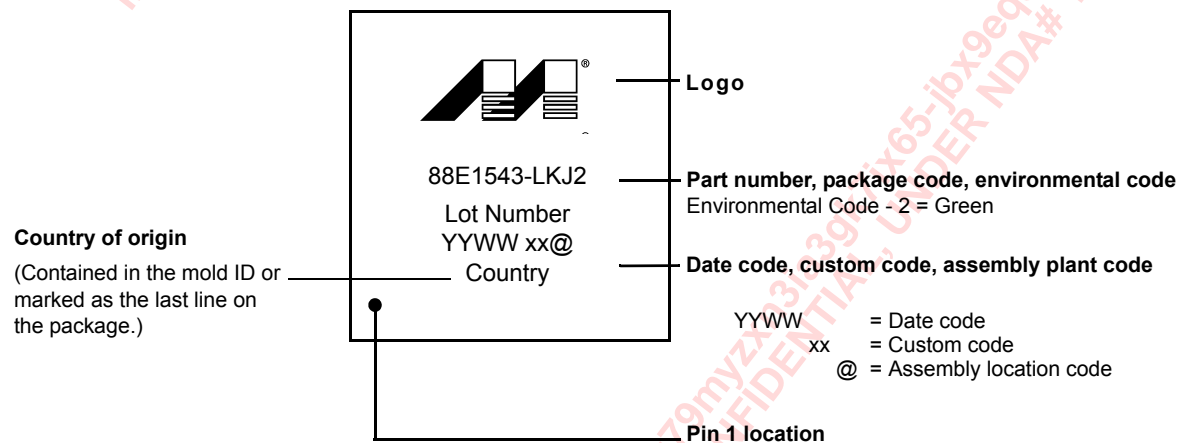
Figure 66: 88E1545 128-pin LQFP Commercial Green Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 67 is an example of the package marking and pin 1 location for the 88E1543 128-pin LQFP commercial Green package.

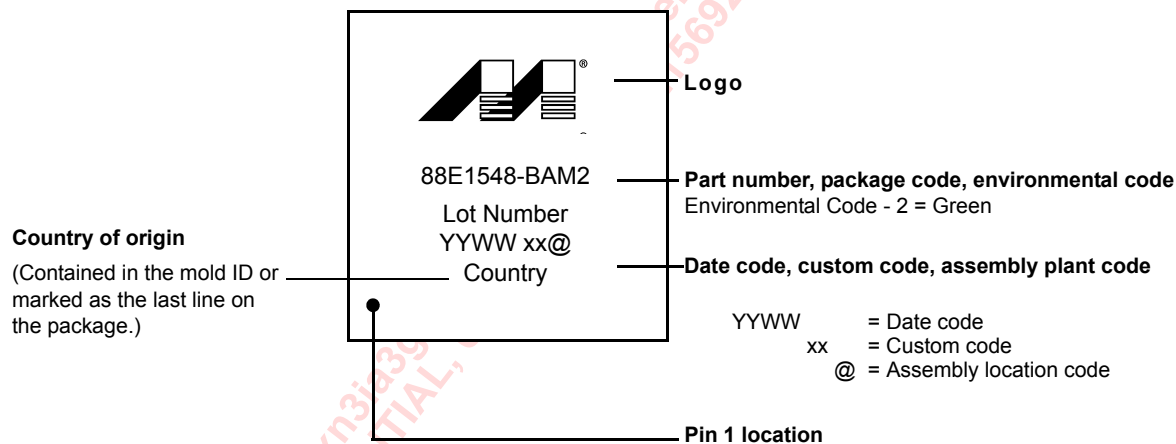
Figure 67: 88E1543 128-pin LQFP Commercial Green Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.

Figure 68 is an example of the package marking and pin 1 location for the 88E1548 196-pin TFBGA commercial Green package.

Figure 68: 88E1548 196-pin TFBGA Commercial Green Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. Location of markings is approximate.



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