# Advanced PHY Features Overview

The new generations of Marvell® 0.13um Gigabit PHYs offer evaluation modes to help evaluate the PHY at the board development stage and production stage. Board developers can make use of the line loopback, packet generator, frame counter, and the CRC counter to evaluate the PHY without the presence of a MAC. For production testing, an external loopback stub can be used to test the complete data path by sending data from the MAC. These features can also be used as a tool for debugging. (Note copper related features do no apply to 88E1143.)

The MAC interface pins have automatic impedance calibration to compensate for process, voltage, and temperature variation. Manual calibration is also available to fine tune and match trace impedance.

This document will discuss the following features:

- Line Loopback
- Packet Generator
- CRC Error Counter and Frame Counter
- Gigabit External Stub Loopback
- Automatic and Manual Impedance Calibration

(Note: Register 29 is a pointer to the different pages of register 30.)

# 1. Line Loopback

## 1.1 Line Loopback Mode

For boards where the MAC ASICs are not ready, line loopback allows a link partner to send frames into the Marvell PHY to test the transmit and receive data path. Frames sent from a link partner into the PHY, before reaching the MAC interface pins, are also looped back and sent out on the line side. See Figure 1. This allows the link partner to receive its own frames.

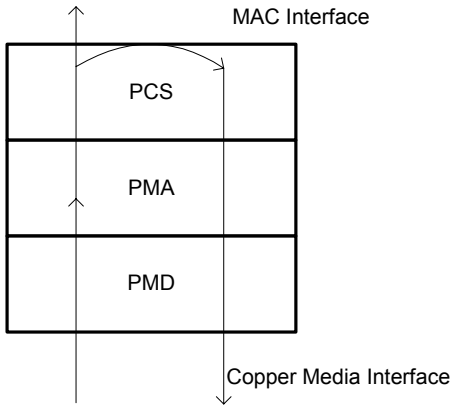


**Figure 1: Line Loopback data path.**

### 1.2 Enabling Line Loopback

Before enabling the line loopback feature, the Marvell® PHY must first establish copper link with another link partner. If Auto negotiation is enabled, both link partners should advertise the same speed and full duplex. If Auto negotiation is disabled, both link partners need to be forced to the same speed and full duplex. Once link is established, enable the line loopback mode by writing to register bit 20.14.

20.14 = 1 (Enable line loopback)

20.14 = 0 (Disables line loopback)

### 1.3 Line Loopback Test Setup

Once the line loopback is enabled, the link partner can send data into the PHY.

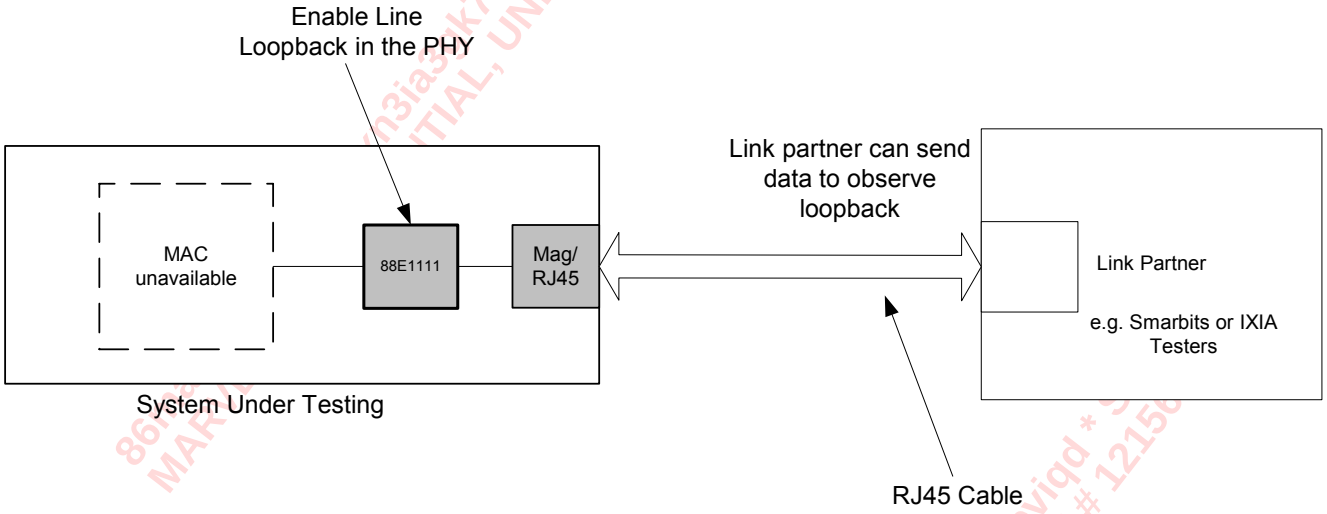


**Figure 2: Test Setup using line loopback**

## 2. Packet Generator

### 2.1 Packet Generation

Without a MAC, the PHY by itself can generate special packets to send out on the media interface. This feature is not available in GBIC mode. You must be in RGMII/GMII or RTBI/TBI mode to use this feature and TX_EN must be low. There must be link with a link partner. If there is no link partner, force to either 10 Mbps or 100 Mbps mode and then apply force good link bit prior to enabling the packet generator.

### 2.2 Packet Generator Register Bits

If Reg29: 0x0012 then Reg30:

Bit 5: 1 = packet generation enable, 0 = disable

Bit 4: 0 = random, 1 = 0x5a (packet pattern select)

Bit 3: 0 = 64 byte, 1 = 1518 byte (packet length select)

Bit 2: 1 = generate error packet, 0 = no error

Register 30 is a read/write register if Reg29 = 0x0012

# 3. CRC Error Counter and Frame Counter

The CRC counter and frame counters, normally found in MACs, are now also available in the Marvell® PHYs. These features are enabled through register writes and each counter is stored in eight register bits. The counters are not cleared on read. They have to be cleared each time after a read; see the disabling and clearing counter section below.

## 3.1 Enabling The CRC Error Counter and Frame Counter

### 3.1.1 Enabling Counters

Writing to the following registers will enable both counters.

Reg29: 0x0010 (points to extended register 0x0010, for register 30 to access)

Reg30 bit 0 = '1' (e.g. 0x0001 enables both CRC error and frame counter)

The CRC error counters should be enabled before reception of packets has started. If the CRC error counter is enabled during reception of a packet, that packet will be counted as a CRC error.

### 3.1.2 Clearing and Disabling Counters

Writing to the following register will clear and disable both counters

Reg29: 0x0010 (points to extended register 0x0010, for register 30 to access)

Reg30 bit 0 = '0' (eg 0x0000, disable and clear CRC error and frame counter)

### 3.1.3 Reading Counter Contents

To read the CRC counter and frame counter, write to the following registers.

Reg29: 0x000C (Points to page 12 of register 30)

Reg30:

Bits 15:8 (Frame count is stored in these bits)

Bits 7:0 (CRC error count is stored in these bits)

The counter does not clear on a read command. To clear the CRC error counter, disable and enable the counters.

# 4. External Gigabit Loopback

## 4.1 External Loopback Modes

For production testing, an external loopback stub allows testing of the complete data path for 10/100/1000 modes. For 10/100 Mbps modes, the loopback test require no register writes. For gigabit mode, a series of register writes will setup the PHY for external gigabit loopback. All modes require an external loopback stub. Additionally, the interrupts should not be used while stub loopback is enabled. To disable the interrupts, write 0x0000 to register 18 (decimal).

## 4.2 Loopback Stub

The loopback stub consists of a plastic RJ-45 header, connecting RJ-45 pair 1,2 to pair 3,6 and connecting pair 4,5 to pair 7,8, as seen in Figure 2.

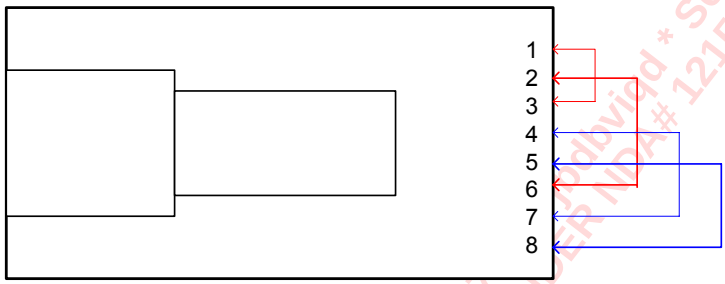


**Figure 3: Loopback Stub (Top view with tab up)**

## 4.3 Enabling Gigabit Stub Loopback

To enable the Gigabit Stub Loopback mode, write to the following registers:

Reg18: 0x0000 (disable all interrupts)

Reg9.12:11 = '11' (force Master, e.g. reg9: 0x1B00)

Reg0.15 = '1' (e.g. reg: 0x9140, to perform soft reset)

Reg29: 0x0007 (points to page 7 of register 30)

Reg30.3 = '1' (e.g. reg 30: 0x0808)

Reg29: 0x0010 (points to page 16 of register 30)

Reg30.1 = '1' (e.g. reg30: 0x0042)

Reg29: 0x0012 (points to page 18 of register 30)

Reg30.0 = '1' (e.g. reg30: 0x8901)

## 4.4 Disabling Gigabit Stub Loopback

To disable the Gigabit Stub Loopback mode, restore the default settings to the related registers above. Note that register 29 is a pointer to different pages of register 30.

Reg9.12:11 = restore original values (e.g. reg9: 0x0300)

Reg0.15 = '1' (e.g. reg: 0x9140, to perform soft reset)

Reg29: 0x0007 (points to page 7 of register 30)

Reg30.3 = '0' (e.g. reg 30: 0x0800)

Reg29 0x0010 (points to page 16 of register 30)

Reg30.1 = '0' (e.g. reg30: 0x0040)

Reg29 0x0012 (points to page 18 of register 30)

Reg30.0 = '0' (e.g. reg30: 0x8900)

Reg18 = restore desired interrupts

## 4.5 External Gigabit Loopback Test Setup

The External loopback test setup requires the presence of a MAC that will originate the frames to be sent out through the PHY. Instead of a normal RJ-45 cable, the loopback stubs allows the PHY to self-link. It also allows the actual external loopback. See Figure 4. The MAC should see the same packets it sent, looped back to it.

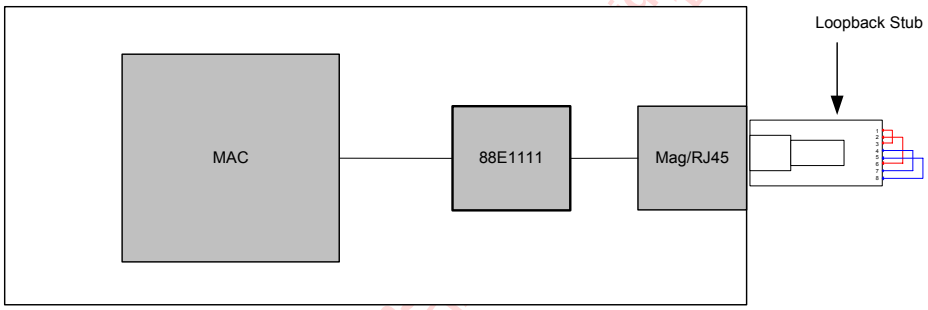


**Figure 4: Test setup for 10/100/1000 modes using an external loopback stub.**

# 5. Automatic and Manual Impedance Calibration

## 5.1 Calibration Circuit

The auto calibration is available for the MAC interface I/Os. The PHY runs the automatic calibration circuit with a 30 ohm impedance target by default after hardware reset. (Some of the newer revisions may have 45 ohm impedance target by default after hardware reset) Other impedance targets are available by changing the impedance target and restarting the auto calibration through register writes. Individual NMOS and PMOS output transistors could be controlled for 22 to 55 ohm targets in various increments.

Manual NMOS and PMOS settings are available if the automatic calibration is not desired. The MAC interface I/O buffers can be manually controlled to meet required board trace impedance that is different from the original 50 ohm target. Users can adjust the NMOS and PMOS driver output strengths to perfectly match the transmission line impedance and eliminate reflections completely.

## 5.2 Calibration Register Definitions

If reg29 = 0x0012, then reg30 is defined as in Table 1.

**Table 1: Auto-Calibration Target Registers**

| Reg bit | Function | Setting description | Mode | HW reset | SW reset |
|---|---|---|---|---|---|
| 11:9 | PMOS Target Value | (2.5V I/O)<br>111 = 22 ohm<br>110 = 24 ohm<br>101 = 25 ohm<br>100 = 30 ohm<br>011 = 32 ohm<br>010 = 36 ohm<br>001 = 45 ohm<br>000 = 52 ohm<br><br>(1.8V)<br>111 = 23 ohm<br>110 = 24 ohm<br>101 = 27 ohm<br>100 = 29 ohm<br>011 = 33 ohm<br>010 = 39 ohm<br>001 = 43 ohm<br>000 = 56 ohm | R/W | E1141/E1143/E1145<br>-Rev C0: '100'<br>-Rev D0 and later: '001'<br><br>E1111<br>Rev B0: '100'<br>Rev B1 and later: '001' | Retain |

| Reg bit | Function | Setting description | Mode | HW reset | SW reset |
|---|---|---|---|---|---|
| 8:6 | NMOS Target Value | (2.5V I/O)<br>111 = 22 ohm<br>110 = 24 ohm<br>101 = 27 ohm<br>100 = 30 ohm<br>011 = 34 ohm<br>010 = 39 ohm<br>001 = 46 ohm<br>000 = 55 ohm<br><br>(1.8V)<br>111 = 23 ohm<br>110 = 25 ohm<br>101 = 27 ohm<br>100 = 29 ohm<br>011 = 32 ohm<br>010 = 41 ohm<br>001 = 48 ohm<br>000 = 58 ohm | R/W | E1141/E1143/E1145<br>-Rev C0: '100'<br>-Rev D0 and later: '001'<br><br>E1111<br>Rev B0: '100'<br>Rev B1 and later: '001' | Retain |

Note: This register of port 0 affects all 4 ports. Writing this register of port 1, 2, or 3 have no effect.

If Reg29 = 0x0003, then Reg30 is defined as in Table 2.

**Table 2: Calibration Control Register**

| Reg bit | Function | Setting description | Mode | HW reset | SW reset |
|---|---|---|---|---|---|
| 15 | Restart Calibration | 0 = Normal, 1 = Restart<br>Bit 15 is a self-clearing register. Calibration will start once the register is cleared. | R/W | 0 | Retain |
| 14 | Calibration Complete | 0 = calibration in progress, 1 = calibration complete | RO | 0 | Retain |
| 13 | Reserved | 0 | R/W | 0 | Retain |
| 12:8 | PMOS Value | 00000 = all fingers off<br>11111 = all fingers on<br>The automatic calibrated values are stored here after calibration completes.<br>Once the LATCH bit is set to 1, the new calibration value is written. The automatic calibrated value is lost. | R/W | Auto calibrated value | Retain |
| 7 | Reserved | 0 | R/W | 0 | Retain |
| 6 | Latch | 1 = Latch in new value. This bit self clears.<br>(Used for manual settings) | R/W, SC | 0 | Retain |
| 5 | PMOS/NMOS select | 1 = PMOS value is written when LATCH is set to 1<br>0 = NMOS value is written when LATCH is set to 1 | R/W | 0 | Retain |

| Reg bit | Function | Setting description | Mode | HW reset | SW reset |
|---|---|---|---|---|---|
| 4:0 | NMOS Value | 00000 = all fingers off<br>11111 = all fingers on<br>The automatic calibrated values are stored here after calibration completes.<br>Once the LATCH bit is set to 1, the new calibration value is written. The automatic calibrated value is lost. | R/W | Auto calibrated value | Retain |

## 5.3 Changing Auto Calibration Targets

The PHY runs the automatic calibration circuit with a 30 ohm impedance target by default after hardware reset. Other impedance targets are available by changing the impedance target and restarting the auto calibration through register writes.

To change the auto calibration targets, write to the following registers:

Write to register 29 = 0x0012

Write to register 30, bit 11:9 = ppp (write new PMOS Target value)

Write to register 30, bit 18:6 = nnn (write new NMOS Target value)

Write to register 29 = 0x0003

Write to register 30 = 0x8000 (Restarts the auto calibration with the new target)

Example: To change to a 60 ohm auto calibration target, write the following:

Reg29 = 0x0012

Reg30, bit 11:9 = '000' and Reg30, bit 8:6 = '000'

Reg29 = 0x0003

Reg30 = 0x8000

## 5.4 Manual Settings to The Calibration Registers

To use manual calibration, write to the following registers:

Write to register 29 = 0x0003

Write to register 30 = b'000P PPPP 011N NNNN -- adjusts PMOS strength

Write to register 30 = b'000P PPPP 010N NNNN -- adjusts NMOS strength

Where PPPPP is the 5 bit value for the PMOS strength.

Where NNNNN is the 5 bit value for the NMOS strength.

The value of PPPPP or NNNNN will depend on your board. The '11111' value enables all fingers for maximum drive strength, for minimum impedance. The '00000' value turns all fingers off for minimum drive strength, for maximum impedance. Use a

scope to monitor the RX_CLK pin close to the destination. Start with the default auto-calibrated value and move in each direction to see how it affects signal integrity on your board.

Example: The automatic calibration has a 50 Ohm target, but if the GMII trace impedance on board was 60 ohms, you see reflections from a scope capture taken at the destination. See Figure 5. After manual calibration, you see that the reflections are eliminated in Figure 6.

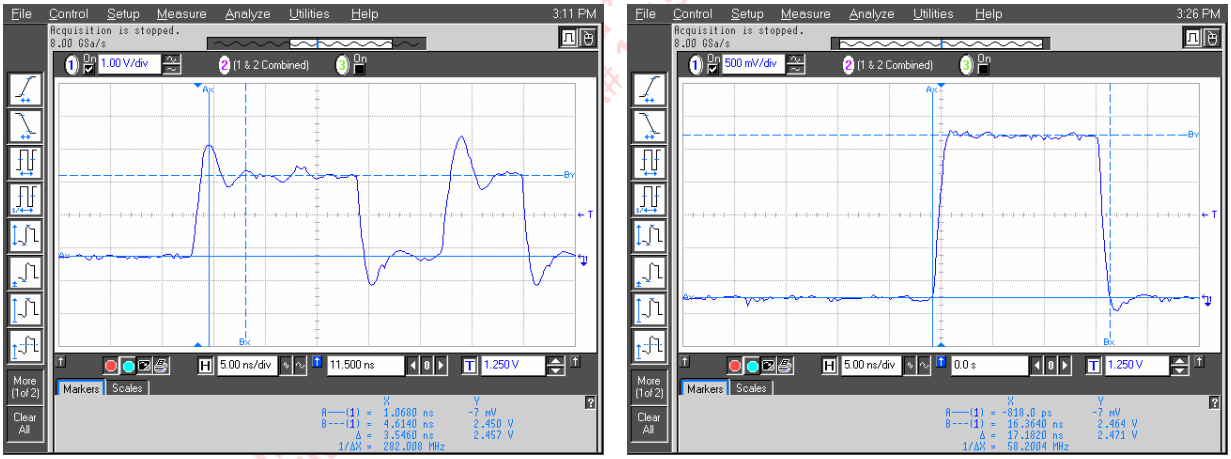

**Figure 5: (left) Signal reflections, using the 50 ohm automatic calibration target, with a 60 ohm line.**

**Figure 6: (right) Clean signal after manual calibration for the 60 ohm.**

**Table 3: Advanced Features Summary For Different Revisions**

| | 88E1111 rev A0/ 88E1141/88E1145/ 88E1143 rev A0/ | 88E1141/88E1145/ 88E1143 rev B0 | 88E1111 rev B0 | 88E1141/45/43 rev C0/D0/E1 |
|---|---|---|---|---|
| Line loopback | yes | yes | yes | yes |
| Packet generator | | yes | yes | yes |
| CRC error counter | Yes[1] | yes | yes | yes |
| Frame counter | | Yes[1] | yes | yes |
| Gigabit stub loopback | Yes[1] | yes | yes | yes |
| Various auto calibration target settings | | | Yes[2] | Yes[2] |
| Manual calibration | yes | yes | yes | yes |

1: For revision A0 of silicon, the register writes to access the CRC error counter and stub loopback are different than what are described in this appnote. See appnote: "Gigabit Advanced PHY Features For 88E1111, 88E114x rev **A0**"

2: Different impedance target settings are available.

**Table 4: Advanced Features Availability Comparison For Different Devices**

| | 88E1011/ 88E104x rev 2.0 | 88E104x rev D1/D2 | 88E1111 rev B0 | 88E1141/45/43 rev C0/D0/E1 |
|---|---|---|---|---|
| Line loopback | no | yes | yes | yes |
| Packet generator | no | yes | yes | yes |
| CRC error counter | no | yes | yes | yes |
| Frame counter | no | yes | yes | yes |
| Gigabit stub loopback | no | yes | yes | yes |
| Various auto calibration target settings | no | No for rev D1<br>yes for rev D2 | yes | yes |
| Manual calibration | no | yes | yes | yes |

Note: An advanced features document exists for the 88E104x rev D1/D2.