COR

Page Description: Cover Sheet			
Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang	
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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Table of Contents

common	Page Description: Table of Contents		
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Revision History

DATE	PHASE	REV #	DESCRIPTION
2018/1/4	EVT	V0.10	**Initial Release**

common	Page Description: Revision History		
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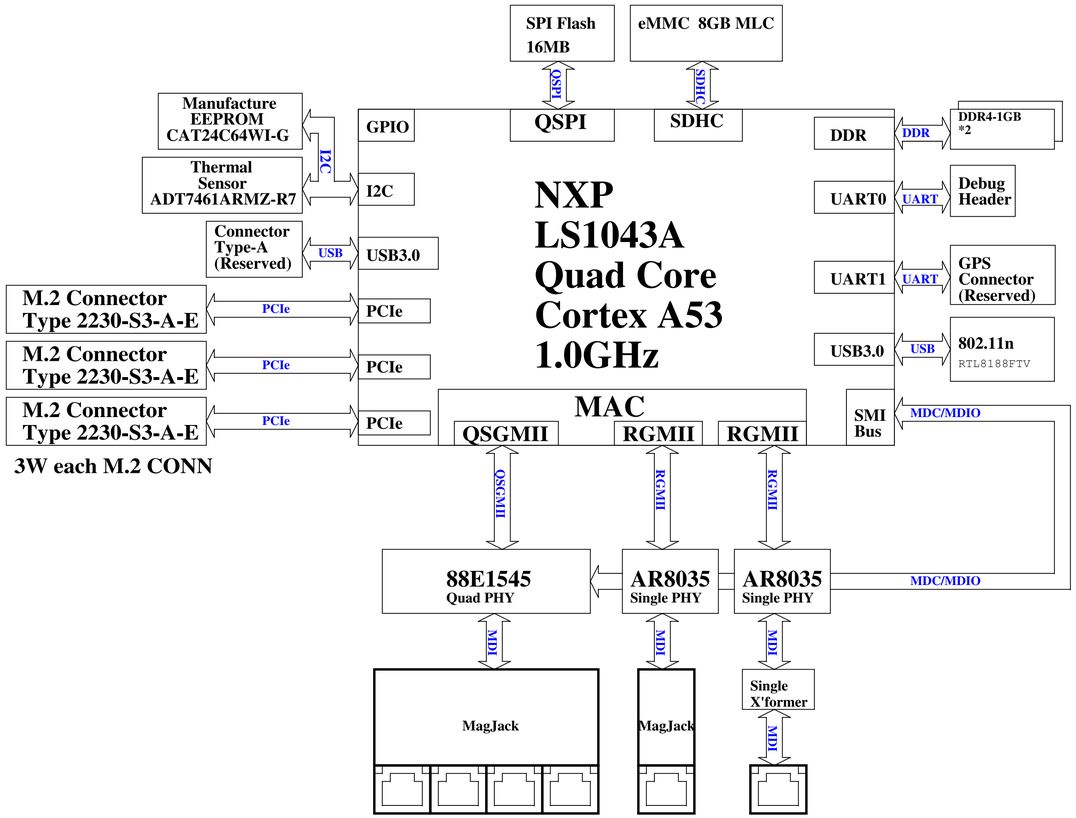
Block Diagram



Page Description: System Block Diagram			
Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang	
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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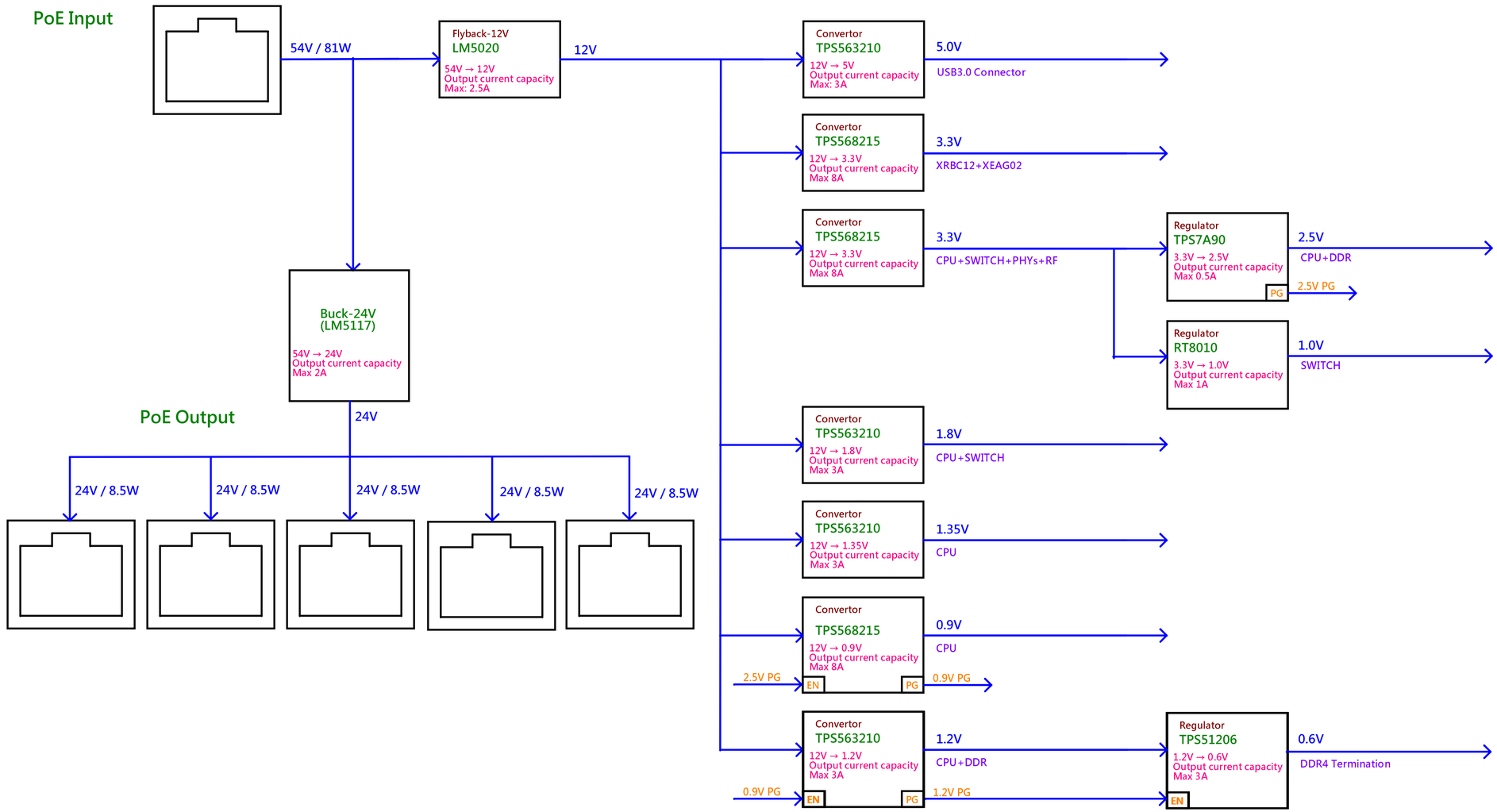
Power Tree



common networks	Page Description: Power Tree		
	Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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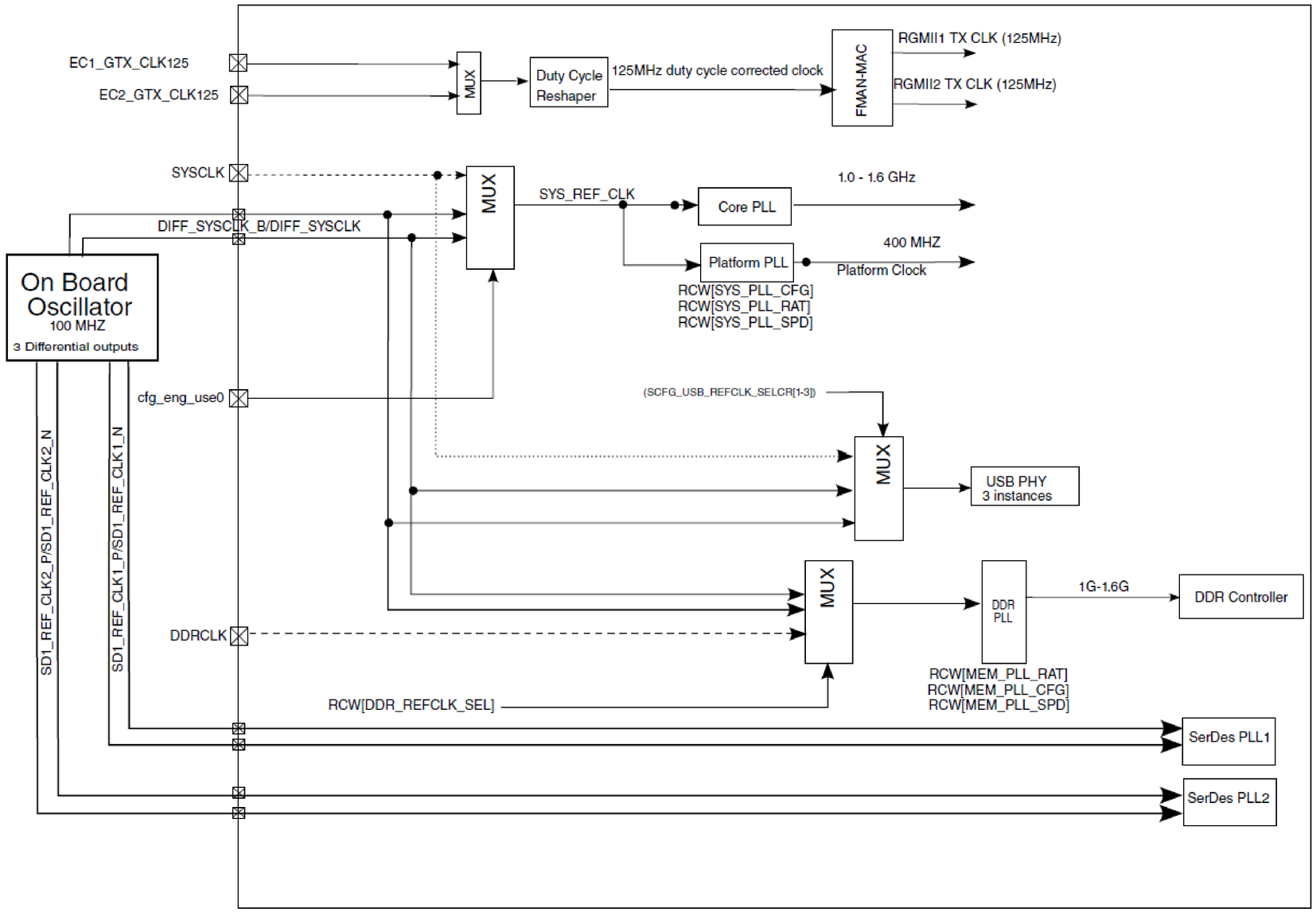
Clock Tree



Page Description: Clock Tree			
Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang	
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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PCB Stackup

layout stackup

Assume Dielectric constant is 4.3

Plane Type/Code	Material	Construction (mil)	40ohm(Single End)			50ohm(Single End)			50ohm(Single End)				50ohm(Single End)				100 ohm(Differential)				100 ohm(Differential)				90 ohm(Differential)				80 ohm(Differential)			
			TRACE	Reference	Impedance	TRACE	Reference	Impedance	TRACE	Gap	Reference	Impedance	TRACE	Gap	Reference	Impedance	TRACE	SPACING	Reference	Impedance	TRACE	SPACING	Reference	Impedance	TRACE	SPACING	Reference	Impedance	TRACE	SPACING	Reference	Impedance
Soldemask		0.80																														
L1 - SIGNAL	0.5oz+plating	1.40							5	10	L2	49.48	9	4	L3	49.72	4	9	L2	102.56	6.3	5	L3	101.76	4	4.5	L2	91.21	5.5	4.5	L2	80.18
1080HRC	Prepreg	3.18																														
L2 - GROUND	1oz Cu	1.30																														
4C-1/1	4mil 1/1	4.00																														
L3 -HS SIGNAL	1oz Cu	1.30				5	L2/L5	48.06									4	9	L2/L5	96.71					4	5	L2/L5	86.42	5	5	L2/L5	79.64
7628*2	Prepreg	15.59																														
L4 - GROUND	1oz Cu	1.30																														
4C-1/1	4mil 1/1	4.00																														
L5 - (3.3)Power	1oz Cu	1.30	7.5	L4/L6	40.44	5	L4/L6	48.06									4	9	L4/L6	96.71					4	5	L4/L6	86.42	4	5	L4/L6	79.64
7628*2	Prepreg	15.59																														
L6 - Power / SIGNAL	1oz Cu	1.30				5	L7/L5	48.06									4	9	L7/L5	96.71					4	5	L7/L5	86.42	5	5	L7/L5	79.64
4C-1/1	4mil 1/1	4.00																														
L7 - GROUND	1oz Cu	1.30																														
1080HRC	Prepreg	3.18																														
L8 - SIGNAL	0.5oz+plating	1.40							5	10	L7	49.48	9	4	L6	49.72	4	9	L7	102.56					4	4.5	L7	91.21	5.5	4.5	L7	80.18
Soldemask		0.80																														
Overall Thickness (mil)		61.74																														
Overall Thickness (mm)		1.568196																														

Layers assigned

- IC pin trace , Differential Pair, Clock signals ,, Control signals , MDI, DDR-SDRAM(DQS/DQM/Data) , Flash, 10GXFI
- Ground
- Differential Pair, DDR-SDRAM(Address,CS,BA,CAS,RAS,CKE) , Clock signals , SGMII , Serdes I/F , MDI,
- Ground
- Power:DDR1.5V , 1V,12V,5V
- Signals : DDR differential clock
  Power : 3.3V, DDRVTT,5V,PLL power
- Ground
- IC pin trace , DDR-SDRAM(DQS/DQM/Data) Clock signals , PCI , Control signals , MDI,HiGi + Differential Pair

GPIO table

common	Page Description: Stackup & GPIO table			
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Reset Circuit

UART Debug Header

Factory Reset Button

CPU Shielding

Page Description:	CPU I/O_Reset_UART_JTAG
Engineer: Howie Shih	Check: Wei Lu
Approval: MT Chang	
Size: D	Project Name: COR
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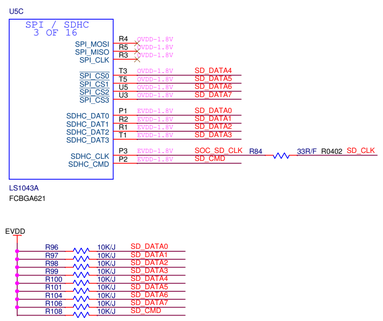
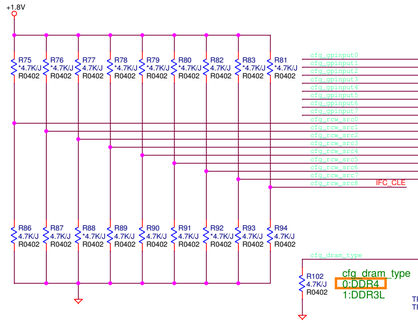
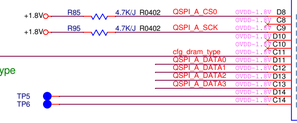
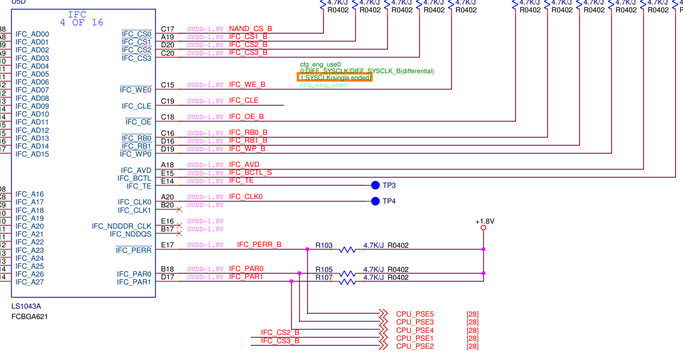


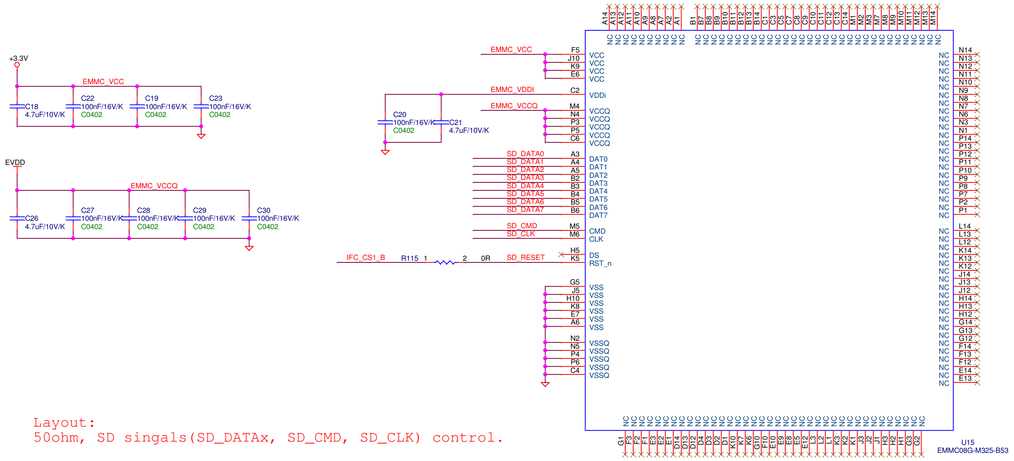
CFG_RCW_SRC[0:8]
SD CARD = 0_0100_0000
QSPI FLASH = 0_0100_010x
NAND FLASH = 1_0000_01xx
8-bit NAND Flash, 512-byte page, 32 pages/block
cfg_rcw_src[7]:
0 Bad Block Indicator in page 0/1
1 Bad Block Indicator in page 0 or last page
cfg_rcw_src[8]:
0 ECC disabled
1 4 bits per 520 bytes





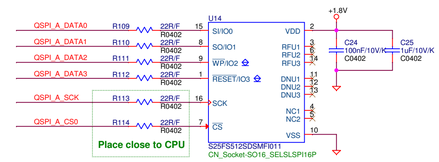


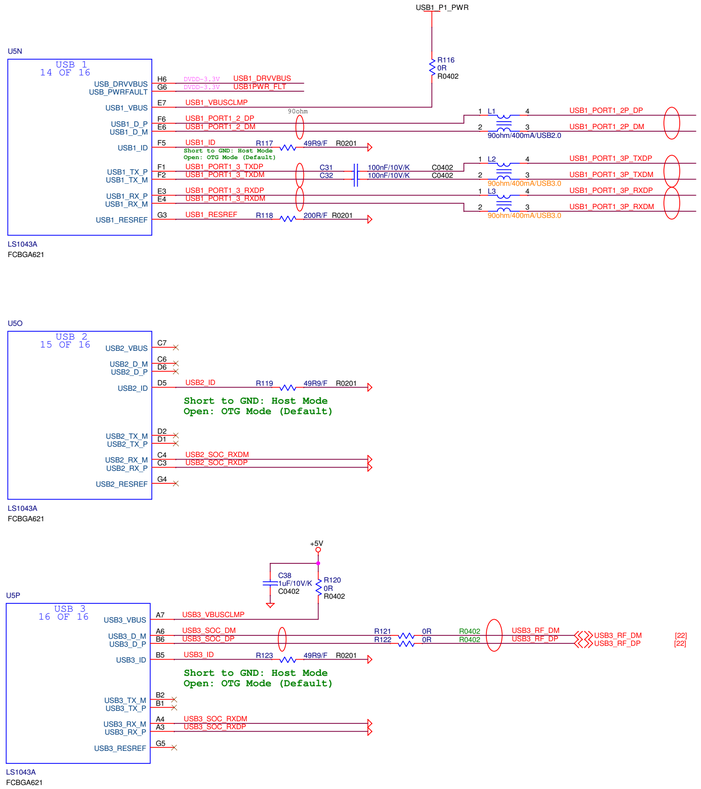
eMMC



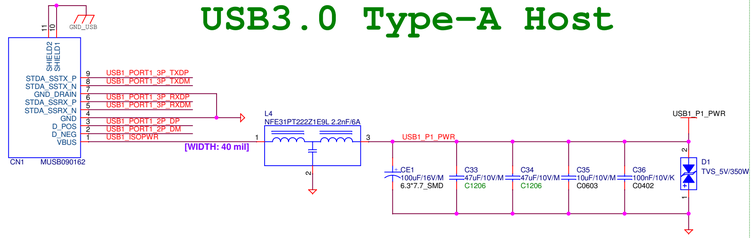
Layout:
50ohm, SD singals(SD_DATAx, SD_CMD, SD_CLK) control.

QSPI FLASH

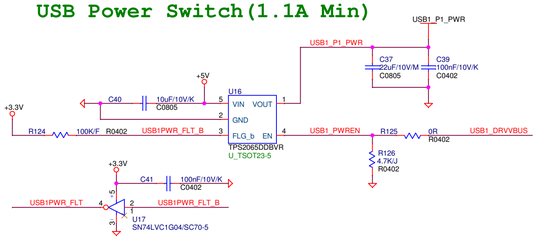




USB3.0 Type-A Host



USB Power Switch(1.1A Min)



Page Description: CPU USB_USB3.0 Connector			
Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang	
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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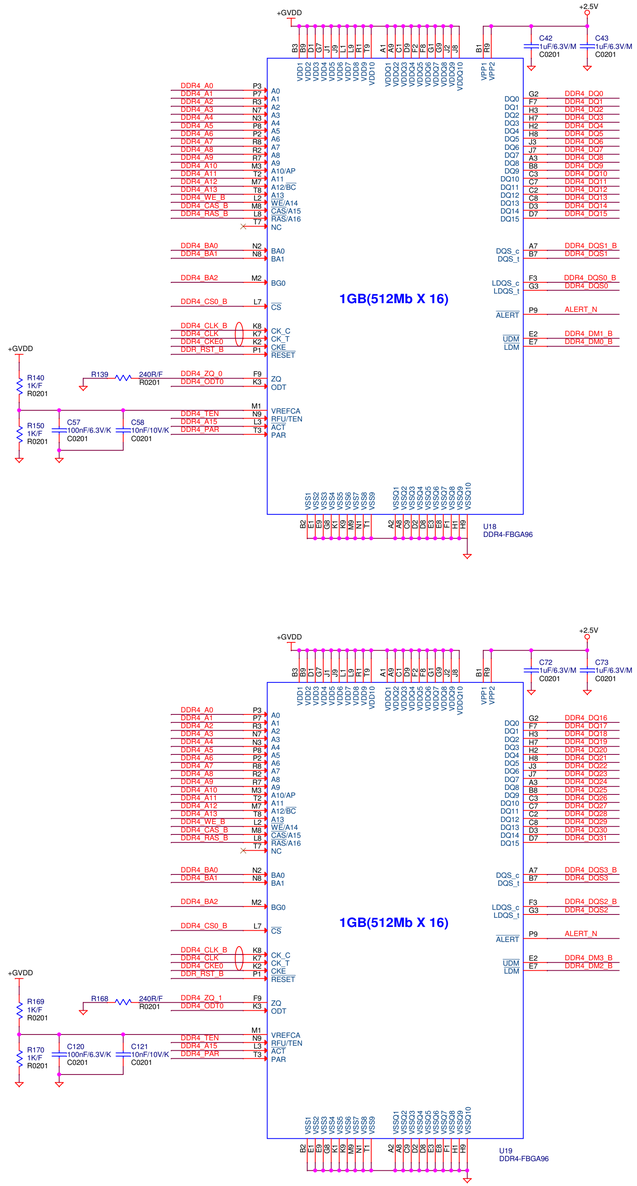
DDR4 bit swap rule

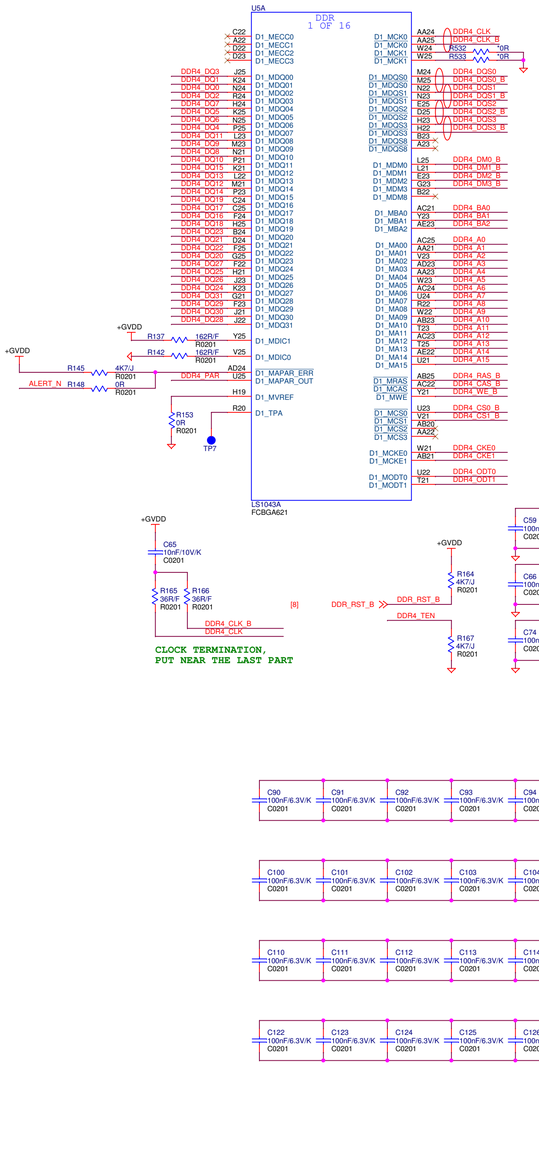
When placing components, optimize placement of the discrete DRAM chips to favor the data bus (analogous to DIMM topologies). Ensure the bit and byte swapping rules listed in following are implemented.

Ensure bit and byte swapping rules are applied:

- Byte-swap is allowed in any order that would best fit the customer's design.
- Bit-swap is only allowed within a nibble.
- Bit-swap across two nibbles is not allowed.
- Bit-swap across byte lanes is not allowed.
- For 32-bit or 16-bit DDR4 data bus, in the ECC byte lane only, the DQ[0], and DQ[1] bit-swap is not allowed.

NOTE: Do not swap individual data bits across different nibbles within a byte lane.





common networks	Page Description: CPU DDR Bus_DDR4		
	Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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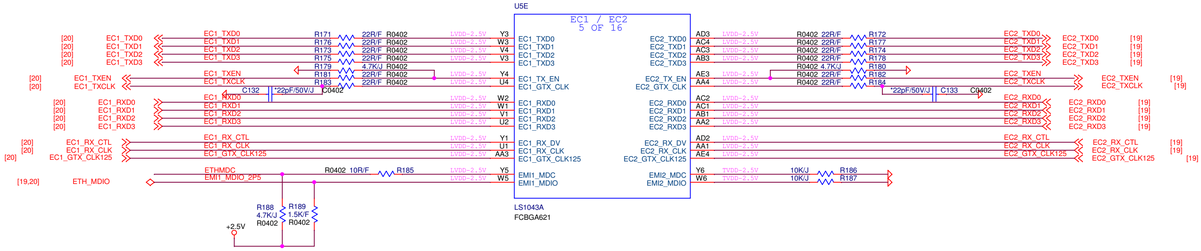

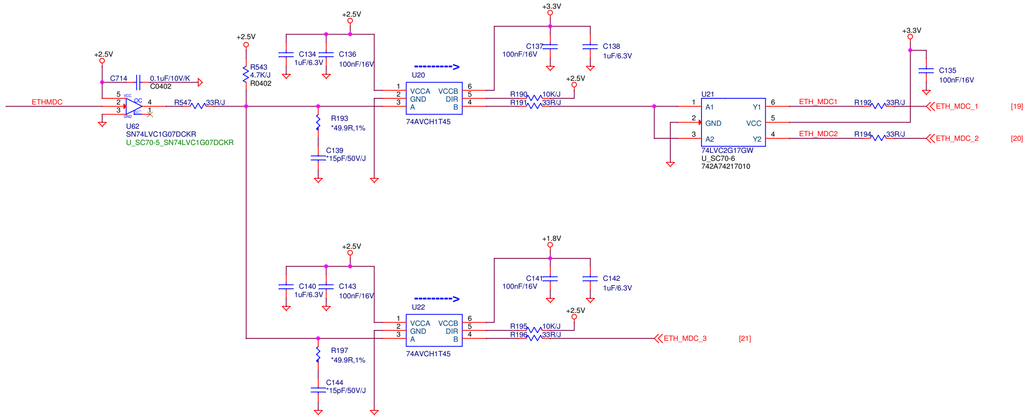

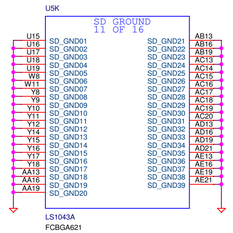

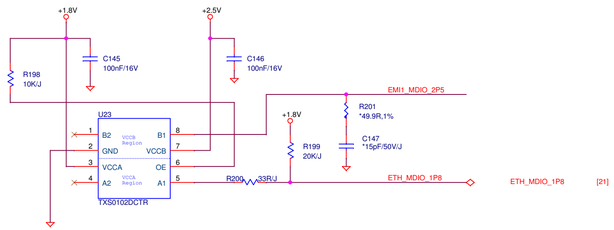

Page Description: CPU RGMII Interface			
Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang	
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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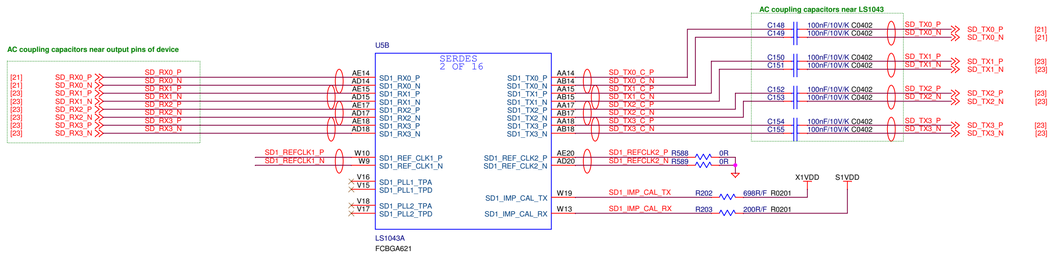

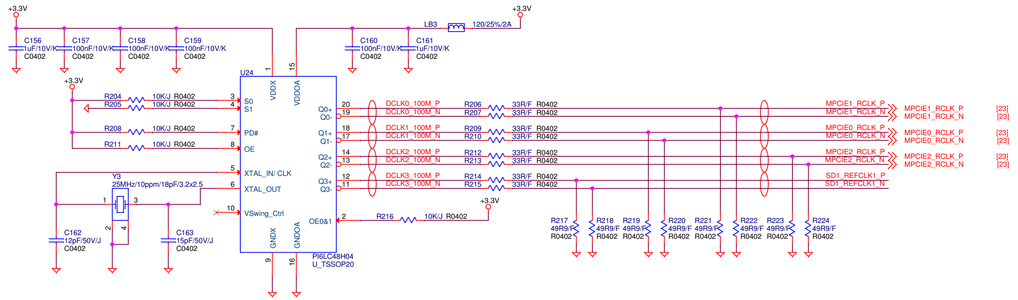

Page Description: CPU SerDes Interface			
Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang	
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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+CPU_VDD

C166 560uF/2V/M

C167 22uF/6.3V/M C0603
C168 22uF/6.3V/M C0603
C169 100nF/6.3V/K C0201
C170 100nF/6.3V/K C0201
C171 100nF/6.3V/K C0201
C172 100nF/6.3V/K C0201
C173 100nF/6.3V/K C0201
C174 100nF/6.3V/K C0201
C175 100nF/6.3V/K C0201
C176 100nF/6.3V/K C0201
C177 100nF/6.3V/K C0201
C178 100nF/6.3V/K C0201
C179 100nF/6.3V/K C0201
C180 100nF/6.3V/K C0201
C181 100nF/6.3V/K C0201

+CPU_VDD

C185 22uF/6.3V/M C0603
C186 22uF/6.3V/M C0603
C187 22uF/6.3V/M C0603
C188 100nF/6.3V/K C0201
C189 100nF/6.3V/K C0201
C190 100nF/6.3V/K C0201
C191 100nF/6.3V/K C0201
C182 100nF/6.3V/K C0201
C192 100nF/6.3V/K C0201
C183 100nF/6.3V/K C0201
C193 100nF/6.3V/K C0201
C194 100nF/6.3V/K C0201
C195 100nF/6.3V/K C0201
C184 100nF/6.3V/K C0201
C196 100nF/6.3V/K C0201
C197 1500pF/16V/K C0201

+CPU_VDD

C206 22uF/6.3V/M C0603
C207 22uF/6.3V/M C0603
C208 22uF/6.3V/M C0603
C209 100nF/6.3V/K C0201
C210 100nF/6.3V/K C0201
C211 100nF/6.3V/K C0201
C212 100nF/6.3V/K C0201
C213 100nF/6.3V/K C0201
C214 1500pF/16V/K C0201
C215 1500pF/16V/K C0201
C216 1500pF/16V/K C0201

+1.8V

R231 5.1R/F R0402
R233 5.1R/F R0402
R235 5.1R/F R0402
R237 5.1R/F R0402

AVDD_CGA1
AVDD_CGA2
AVDD_PLAT
AVDD_DDR1

C225 1uF/6.3V/M C0201
C226 10uF/6.3V/M C0603
C229 1uF/6.3V/M C0201
C230 10uF/6.3V/M C0603
C234 1uF/6.3V/M C0201
C235 10uF/6.3V/M C0603
C239 1uF/6.3V/M C0201
C240 10uF/6.3V/M C0603

+CPU_VDD

C223 47uF/6.3V/M C1206
C224 47uF/6.3V/M C1206

U5L

AVDD 12 OF 16

1.8V +/-90mV
AVDD_CGA1 G12
AVDD_CGA2 G11
AVDD_PLAT G13
AVDD_D1 T19

AVDD_SD1_PLL1 W12
AVDD_SD1_PLL2 V19

1.35V +/-67mV
AVDD_SRDS1_PLL1
AVDD_SRDS1_PLL2

C231 3.3nF/16V/K C0201
C232 4.7uF/10V/K C0603
C233 47uF/6.3V/M C1206
C236 3.3nF/16V/K C0201
C237 4.7uF/10V/K C0603
C238 47uF/6.3V/M C1206

R234 0.33R/F R0402
R236 0.33R/F R0402

X1VDD

LS1043A
FCBGA621

S1VDD
1.0V +/-30mV
T15 S1VDD1
T16 S1VDD2
T17 S1VDD3
T18 S1VDD4
W14 S1VDD5

U5I

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X1VDD1 W15
X1VDD2 W16
X1VDD3 W17
X1VDD4 W18
X1VDD5 Y19

1.35V +/-67mV

C249 100nF/6.3V/K C0201
C250 100nF/6.3V/K C0201
C241 100nF/6.3V/K C0201
C242 100nF/6.3V/K C0201
C243 100nF/6.3V/K C0201
C244 100nF/6.3V/K C0201
C245 100nF/6.3V/K C0201
C246 100nF/6.3V/K C0201
C247 100nF/6.3V/K C0201
C248 100nF/6.3V/K C0201

+CPU_VDD

FL3 NFM18PC225B1A3
FL4 NFM18PC225B1A3

C251 2uF/6.3V/M C0603
C252 2uF/6.3V/M C0603
C253 2uF/6.3V/M C0603
C254 2uF/6.3V/M C0402
C255 2.2uF/6.3V/M C0402
C256 2700pF/16V/K C0201
C257 2700pF/16V/K C0201
C258 2uF/6.3V/M C0402
C259 2uF/6.3V/M C0402
C260 2uF/6.3V/M C0603
C261 2uF/6.3V/M C0603
C262 2uF/6.3V/M C0603

PWR_X1VDD

+GVDD

C264 560uF/2V/M

C265 22uF/6.3V/M C0603
C266 22uF/6.3V/M C0603
C267 22uF/6.3V/M C0603
C268 22uF/6.3V/M C0603
C263 22uF/6.3V/M C0603
C269 22uF/6.3V/M C0603
C270 22uF/6.3V/M C0603
C271 22uF/6.3V/M C0603

C281 100nF/6.3V/K C0201
C282 100nF/6.3V/K C0201
C283 100nF/6.3V/K C0201
C284 100nF/6.3V/K C0201
C285 100nF/6.3V/K C0201
C286 100nF/6.3V/K C0201
C287 100nF/6.3V/K C0201
C288 100nF/6.3V/K C0201
C292 100nF/6.3V/K C0201
C293 100nF/6.3V/K C0201
C294 100nF/6.3V/K C0201

C297 100nF/6.3V/K C0201
C298 100nF/6.3V/K C0201
C299 100nF/6.3V/K C0201
C300 100nF/6.3V/K C0201
C301 100nF/6.3V/K C0201
C302 100nF/6.3V/K C0201
C303 100nF/6.3V/K C0201
C304 100nF/6.3V/K C0201
C305 100nF/6.3V/K C0201
C306 100nF/6.3V/K C0201
C307 100nF/6.3V/K C0201

1.2V +/-60mV
+GVDD

U5G

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G1VDD01 J18
G1VDD02 K18
G1VDD03 K20
G1VDD04 L19
G1VDD05 M18
G1VDD06 M20
G1VDD07 N18
G1VDD08 P18
G1VDD09 P20
G1VDD10 R21
G1VDD11 R23
G1VDD12 T22
G1VDD13 T24
G1VDD14 V22
G1VDD15 V24
G1VDD16 Y22
G1VDD17 Y24
G1VDD18 AA20
G1VDD19 AB22
G1VDD20 AB24
G1VDD21 AD22
G1VDD22 AD25
G1VDD23 AE24

OVDD1 J12
OVDD2 J13
OVDD3 J14
OVDD4 J15
OVDD5 J16
OVDD6 J17
OVDD7 N7

DVDD1 K8
DVDD2 L8

EVDD M8

TA_PROG_SFP F14
PROG_MTR G14
FA_VL R7
TH_VDD T6
TH_TPA P5

1.8V +/-90mV
3.3V +/-165mV
1.8V +/-90mV
1.8V +/-90mV
1.8V +/-90mV
1.0V +/-30mV

C272 100nF/6.3V/K C0201
C273 100nF/6.3V/K C0201
C274 100nF/6.3V/K C0201
C275 100nF/6.3V/K C0201
C276 100nF/6.3V/K C0201
C277 100nF/6.3V/K C0201
C278 100nF/6.3V/K C0201
C279 22uF/6.3V/M C0603
C280 22uF/6.3V/M C0603

C289 100nF/6.3V/K C0201
C290 100nF/6.3V/K C0201
C291 22uF/6.3V/M C0603

C295 100nF/6.3V/K C0201
C296 22uF/6.3V/M C0603

PWR_PROG_SFP
PWR_PROG_MTP

R238 *0R/<0.05 R0402
R239 *0R/<0.05 R0402

C308 100nF/6.3V/K C0201
R240 330R/F R0201
C309 100nF/6.3V/K C0201
R241 330R/F R0201
C310 100nF/6.3V/K C0201
C311 10uF/6.3V/M C0603
R242 *330R/F R0201

LVDD
+2.5V
LB8 120/25%/2A
2.5V +/-125mV

C312 22uF/6.3V/M C0603
C313 1500pF/16V/K C0201
C314 100nF/6.3V/K C0201
C315 100nF/6.3V/K C0201
C316 100nF/6.3V/K C0201

LVDD1
LVDD2
LVDD3

LS1043A
FCBGA621

C317 100nF/6.3V/K C0201
C318 22uF/6.3V/M C0603
C319 100nF/6.3V/K C0201
C320 100nF/6.3V/K C0201
R244 330R/F R0201

VDD_FA_VDD
R243 *0R/<0.05 R0402
+CPU_VDD

1.0V +/-30mV
+CPU_VDD

U5H

POWER 2 8 OF 16

VDD001 K13
VDD002 K15
VDD003 K17
VDD004 L10
VDD005 L12
VDD006 L14
VDD007 L16
VDD008 M9
VDD009 M11
VDD010 M13
VDD011 M15
VDD012 M17
VDD013 N8
VDD014 N10
VDD015 N12
VDD016 N14
VDD017 N16
VDD018 P9
VDD019 P11
VDD020 P13
VDD021 P15
VDD022 P17
VDD023 R8
VDD024 R10
VDD025 R12
VDD026 R14
VDD027 R16
VDD028 R18
VDD029 T9
VDD030 T11
VDD031 T13
VDD032 U8
VDD033 U10

TA_BB_VDD H20

USB_SVDD1 J10
USB_SVDD2 J11
USB_SVDD1 K9
USB_SVDD2 K11
USB_HVDD1 J8
USB_HVDD2 J9
SENSEVDD W7
SENSEGND V7
TVDD V6

1.0V +/-30mV
3.3V +/-165mV
2.5V +/-125mV

LS1043A
FCBGA621

VDD_USB_SVDD
VDD_USB_SDVDD
VDD_USB_HVDD

FL1 NFM18PC225B1A3
FL2 NFM18PC225B1A3

C198 100nF/6.3V/K C0201
C199 100nF/6.3V/K C0201
C200 3.3nF/16V/K C0201
C201 2.2uF/6.3V/M C0402
C202 100nF/6.3V/K C0201
C203 100nF/6.3V/K C0201
C204 3.3nF/16V/K C0201
C205 2.2uF/6.3V/M C0402
C217 100nF/6.3V/K C0201
C218 100nF/6.3V/K C0201
C219 3.3nF/16V/K C0201
C220 2.2uF/6.3V/M C0402

+CPU_VDD
+3.3V
LB5 120/25%/2A

TP8 SENSEVDD
TP9 SENSEGND

TVDD
LB6 120/25%/2A
+2.5V

C227 100nF/6.3V/K C0201
C228 22uF/6.3V/M C0603

U5M

NO CONNECT's 13 OF 16

NC_AA10 AA10
NC_AA11 AA11
NC_AA12 AA12
NC_AA5 AA5
NC_AA6 AA6
NC_AA7 AA7
NC_AA8 AA8
NC_AA9 AA9
NC_AB10 AB10
NC_AB11 AB11
NC_AB12 AB12
NC_AB5 AB5
NC_AB6 AB6
NC_AB7 AB7
NC_AB8 AB8
NC_AB9 AB9
NC_AC10 AC10
NC_AC11 AC11
NC_AC12 AC12
NC_AC5 AC5
NC_AC6 AC6
NC_AC7 AC7
NC_AC8 AC8
NC_AC9 AC9
NC_AD10 AD10
NC_AD11 AD11
NC_AD12 AD12
NC_AD5 AD5
NC_AD6 AD6
NC_AD7 AD7
NC_AD8 AD8
NC_AD9 AD9
NC_AE10 AE10
NC_AE11 AE11
NC_AE12 AE12
NC_AE5 AE5
NC_AE6 AE6
NC_AE7 AE7
NC_AE8 AE8
NC_AE9 AE9
NC_K6 K6
NC_L6 L6
NC_M6 M6
NC_Y13 Y13
NC_Y7 Y7

LS1043A
FCBGA621

U5J

GROUND 10 OF 16

GND001 A2
GND002 A5
GND003 A24
GND004 B3
GND005 B4
GND006 B10
GND007 B13
GND008 B16
GND009 B19
GND010 B21
GND011 B25
GND012 C1
GND013 C2
GND014 C5
GND015 C23
GND016 D3
GND017 D4
GND018 D7
GND019 D9
GND020 D12
GND021 D15
GND022 D18
GND023 D21
GND024 E1
GND025 E2
GND026 E5
GND027 E22
GND028 E24
GND029 F3
GND030 F4
GND031 F7
GND032 F8
GND033 F11
GND034 F12
GND035 F13
GND036 F17
GND037 F20
GND038 G1
GND039 G2
GND040 G22
GND041 G24
GND042 H3
GND043 H4
GND044 H5
GND045 H8
GND046 H9
GND047 H10
GND048 H11
GND049 H12
GND050 H13
GND051 H14
GND052 H15
GND053 H16
GND054 H17
GND055 J7
GND056 J19
GND057 J20
GND058 J24
GND059 K2
GND060 K4
GND061 K7
GND062 K10
GND063 K12
GND064 K14
GND065 K16
GND066 K19
GND067 K22
GND068 L7
GND069 L9
GND070 L11
GND071 L13
GND072 L15
GND073 L17
GND074 L19
GND075 GND076 L20
GND077 L24
GND078 M7
GND079 M10
GND080 M12
GND081 M14
GND082 M16
GND083 M19
GND084 M22
GND085 N2
GND086 N4
GND087 N6
GND088 N9
GND089 N11
GND090 N13
GND091 N15
GND092 N17
GND093 N19
GND094 N20
GND095 P7
GND096 P8
GND097 P10
GND098 P12
GND099 P14
GND100 P16
GND101 P19
GND102 P22
GND103 P24
GND104 R9
GND105 R11
GND106 R13
GND107 R15
GND108 R17
GND109 R19
GND110 R25
GND111 T2
GND112 T4
GND113 T8
GND114 T10
GND115 T12
GND116 T14
GND117 T20
GND118 U6
GND119 U9
GND120 U11
GND121 U20
GND122 V2
GND123 V8
GND124 V9
GND125 V10
GND126 V11
GND127 V12
GND128 V13
GND129 V14
GND130 V20
GND131 W4
GND132 W20
GND133 Y2
GND134 Y20
GND135 AB2
AB4
AD1
AD4
AE2

LS1043A
FCBGA621

common

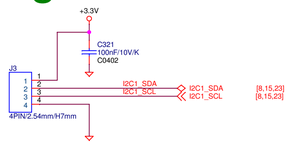
Page Description: CPU Power

Engineer: Howie Shih | Check: Wei Lu | Approval: MT Chang

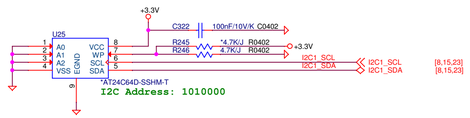
Size	Project Name:	PCB Rev:	Sch.Rev:
D	COR	0.10	0.10

Date: Saturday, January 13, 2018 | Sheet 14 of 28

I2C Debug Header



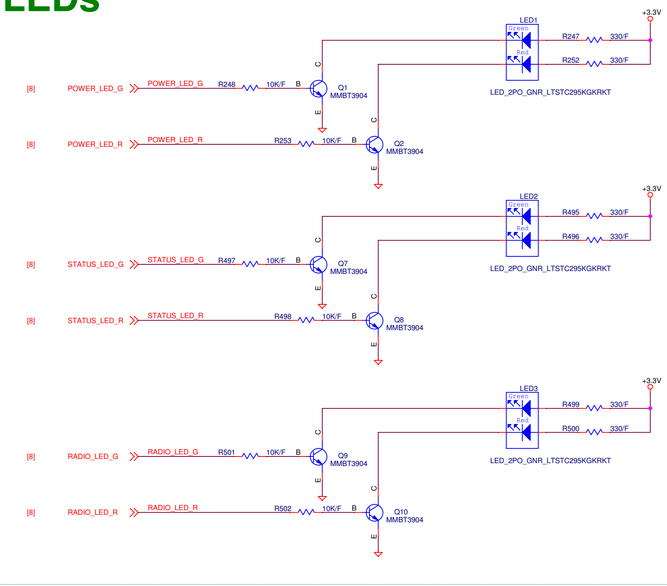
EEPROM



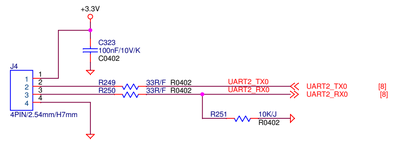
SPD EEPROM

LS1043A	DDR4
MA15	ACT_B
MA14	BG1
MA[13:0]	A[13:0]
MBA2	BG0
MBA[1:0]	BA[1:0]
MRAS_B	RAS_B/A16
MCAS_B	CAS_B/A15
MWE_B	WE_B/A14
MCS_B[0:3]	CS_B[0:3]
MAPAR_ERR_B	ALERT_N
MAPAR_OUT	PAR

LEDs

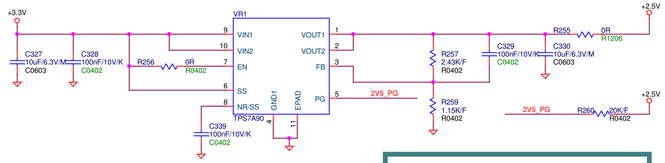


UART => GPS



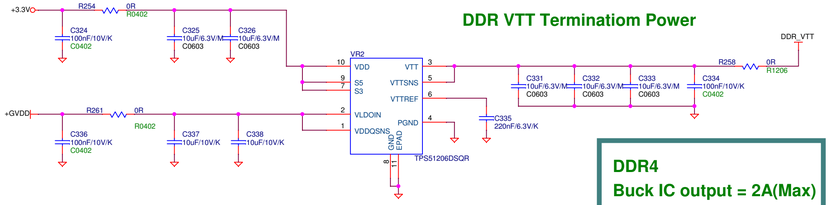
common	Page Description: EEPROM_LEDs_GPS_Con		
	Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
Date: Saturday, January 13, 2018	Sheet 15 of 28		

3.3V -> 2.5V



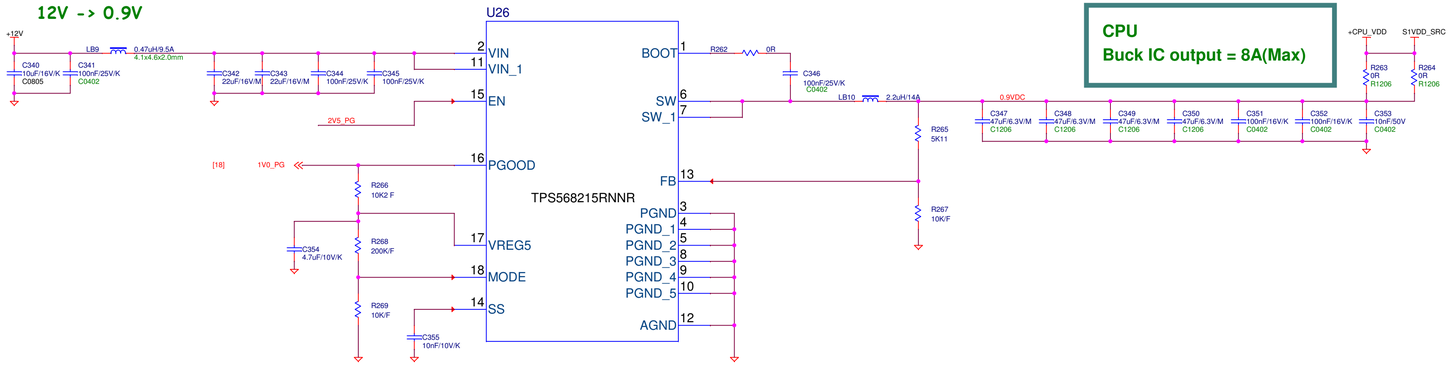
CPU & DDR4
Buck IC output = 500mA(Max)

DDR VTT Terminatiom Power



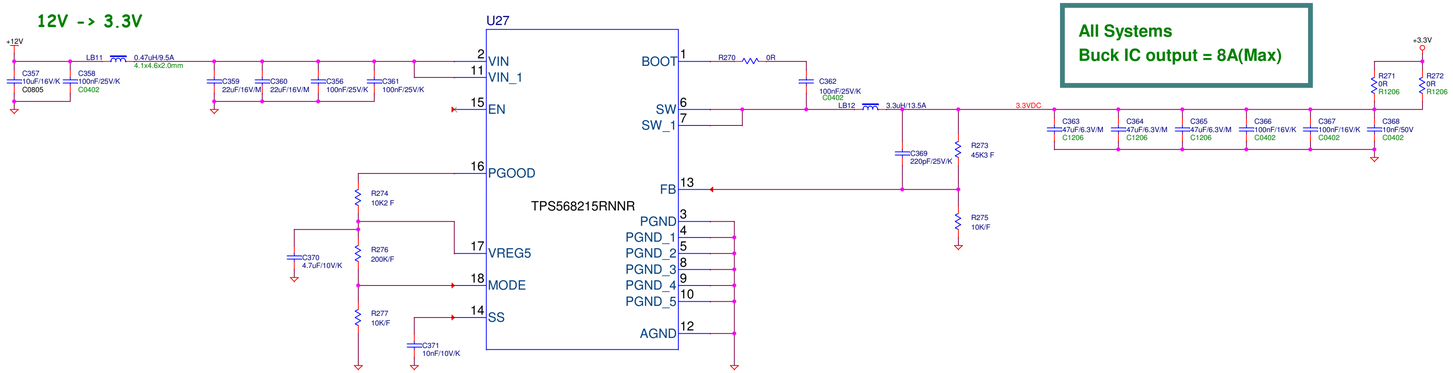
DDR4
Buck IC output = 2A(Max)

12V -> 0.9V



CPU
Buck IC output = 8A(Max)

12V -> 3.3V

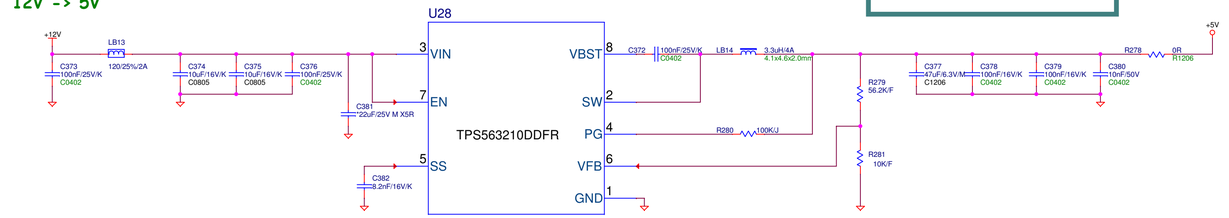


All Systems
Buck IC output = 8A(Max)

common	Page Description: DC to DC_3V3_2V5_0V9_VTT		
	Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
Date: Saturday, January 13, 2018	Sheet 16 of 28		

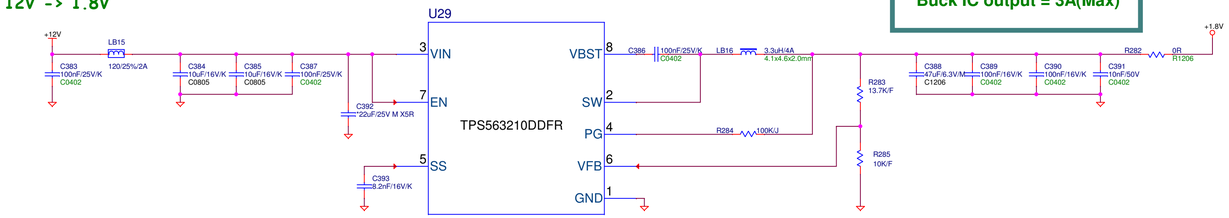
12V -> 5V

USB
Buck IC output = 3A(Max)



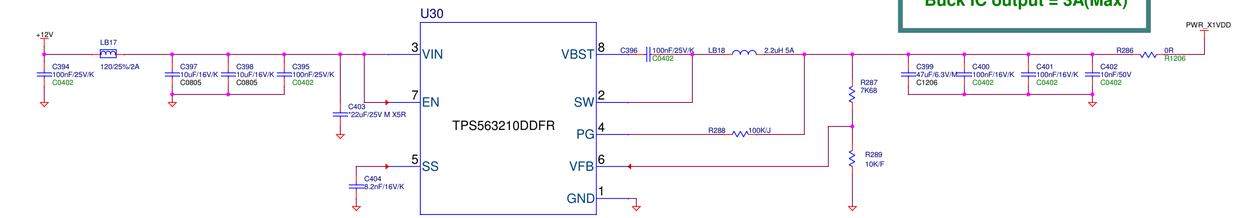
12V -> 1.8V

CPU
Buck IC output = 3A(Max)



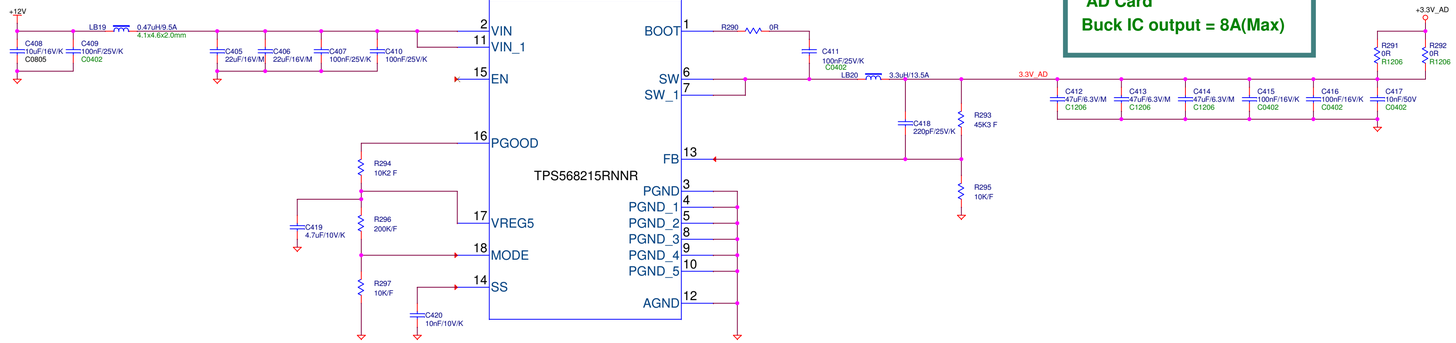
12V -> 1.35V

CPU
Buck IC output = 3A(Max)



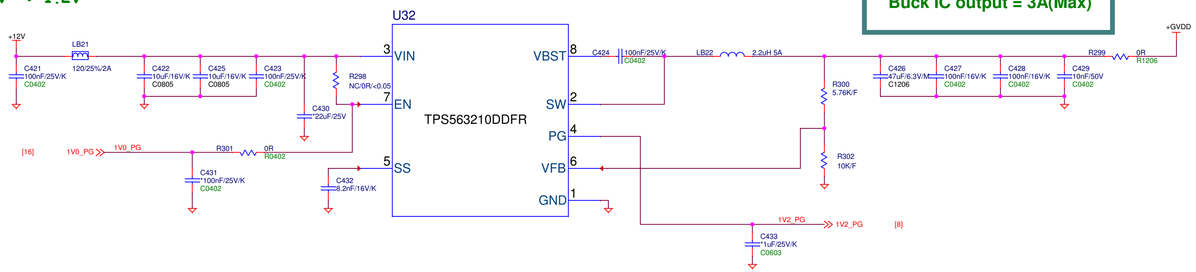
Page Description: DC to DC_5V_1V8_1V35			
Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang	
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
Date: Saturday, January 13, 2018	Sheet 17 of 28		

12V -> 3.3V



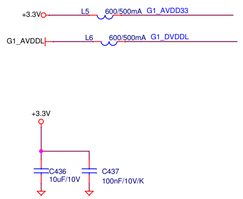
AD Card
Buck IC output = 8A(Max)

12V -> 1.2V

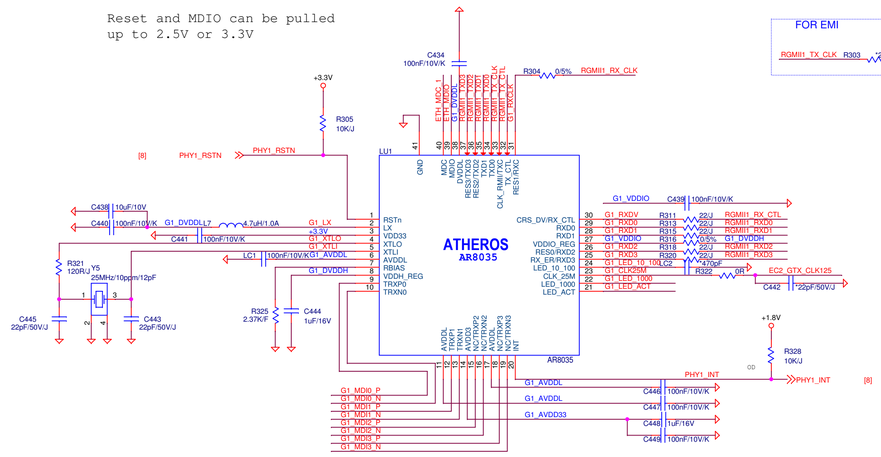


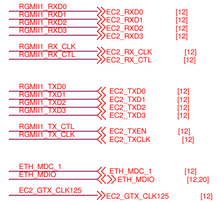
CPU & DDR4
Buck IC output = 3A(Max)

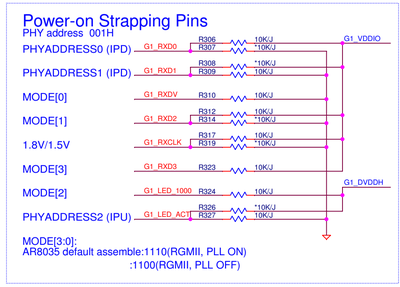
common	Page Description: DC to DC_3V3_AD_1V2		
	Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
Date: Saturday, January 13, 2018	Sheet 18 of 28		



Reset and MDIO can be pulled up to 2.5V or 3.3V



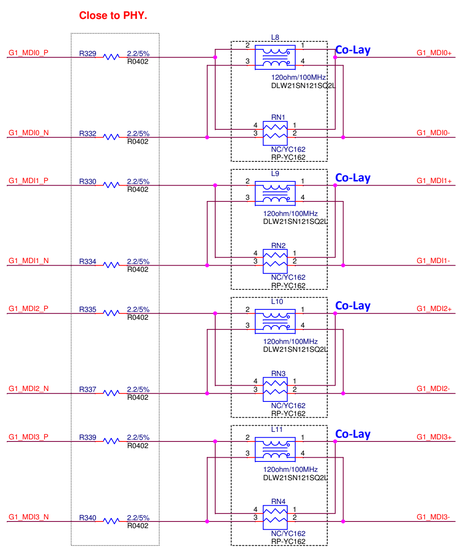




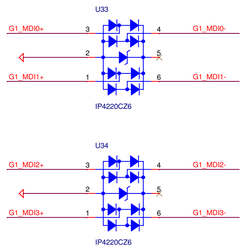
G1_RXCLK	Select the RGMII I/O voltage level
1	1.8V I/O
0	1.5V I/O

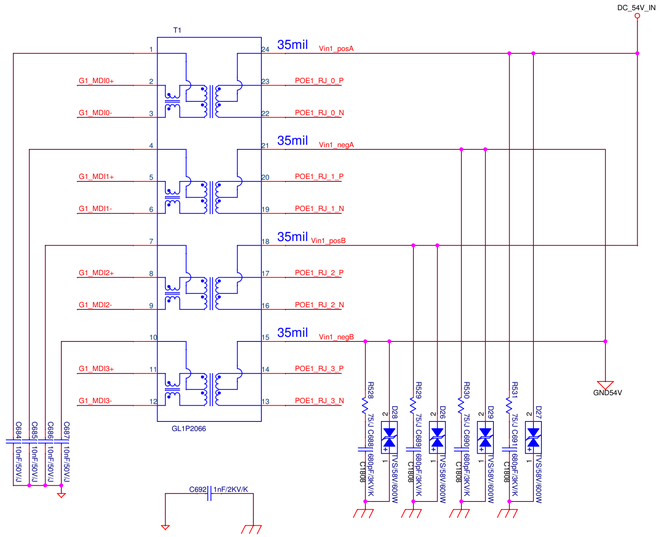
When using 2.5V RGMII I/O voltage level,
G1_RXCLK can be pull-up or pull-down.

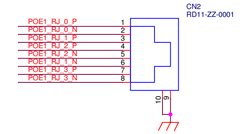
Close to PHY.



Layout: 100 Ohm differential pairs







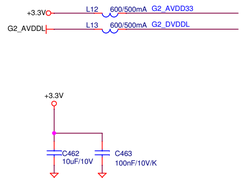
common

Page Description: Ethernet1_AR8035

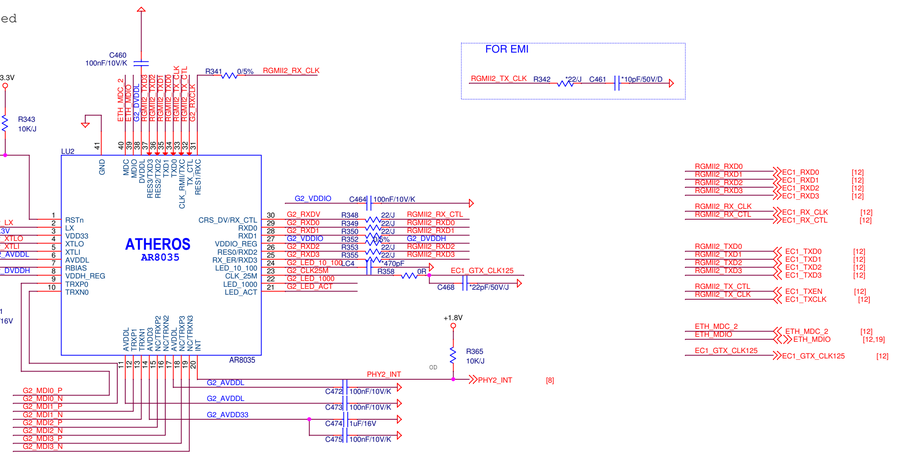
Engineer: Howie Shih | Check: Wei Lu | Approval: MT Chang

Size	Project Name:	PCB Rev:	Sch.Rev:
D	COR	0.10	0.10

Date: Saturday, January 13, 2018 | Sheet 19 of 28



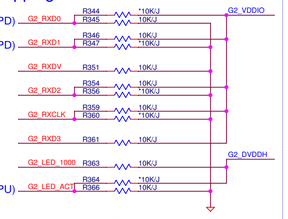
Reset and MDIO can be pulled up to 2.5V or 3.3V



FOR EMI

Power-on Strapping Pins

PHY address 010H

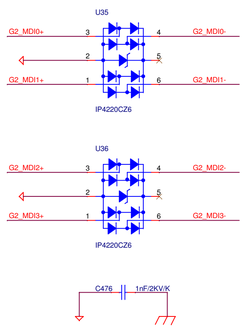


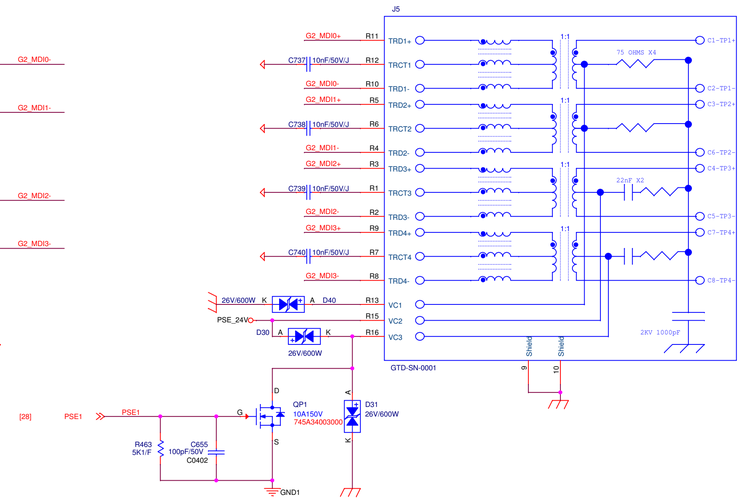
MODE[3:0]:
AR8035 default assemble:1110(RGMII, PLL ON)
:1100(RGMII, PLL OFF)

G2_RXCLK	Select the RGMII I/O voltage level
1	1.8V I/O
0	1.5V I/O

When using 2.5V RGMII I/O voltage level,
G2_RXCLK can be pull-up or pull-down.

Close to PHY.

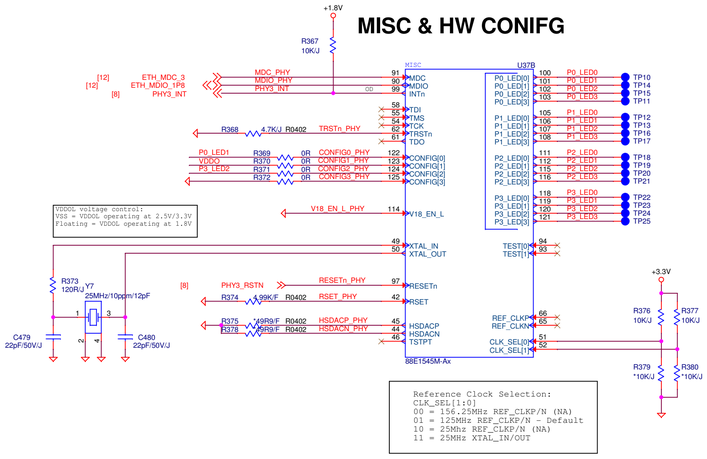




FOUR BIT MAPPING	
PIN	BIT[3:0]
VDDO	1111
P3_LED[2]	1110
P3_LED[1]	1101
P3_LED[0]	1100
P2_LED[3]	1011
P2_LED[2]	1010
P2_LED[1]	1001
P2_LED[0]	1000
P1_LED[3]	0111
P1_LED[2]	0110
P1_LED[1]	0101
P1_LED[0]	0100
P0_LED[3]	0011
P0_LED[2]	0010
P0_LED[1]	0001
VSS	0000

CONFIGURATION MAPPING				
PIN	BIT 3	BIT 2	BIT 1	BIT 0
CONFIG[0]	PHY_ORDER	PHYADR[4]	PHYADR[3]	PHYADR[2]
CONFIG[1]	SEL_MS	ENA_PAUSE	C_ANEG[1]	C_ANEG[0]
CONFIG[2]	S_ANEG	ENA_XC	DIS_SLEEP	PDOWN
CONFIG[3]	PTP_EN	MODE[2]	MODE[1]	MODE[0]

MISC & HW CONIFG



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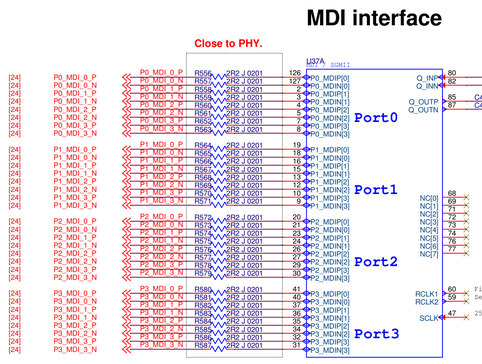

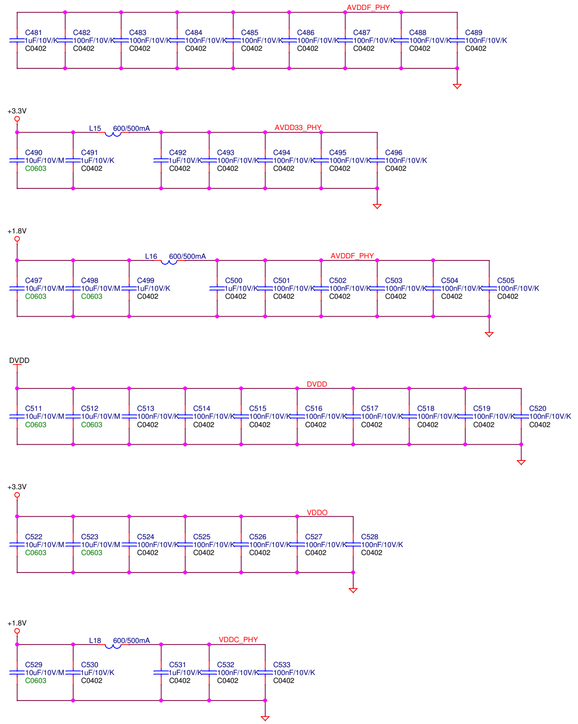

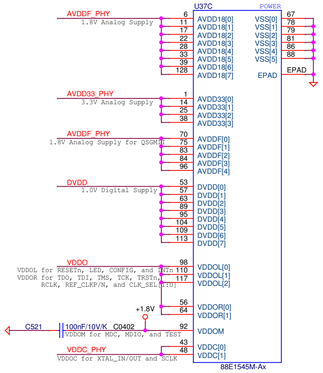

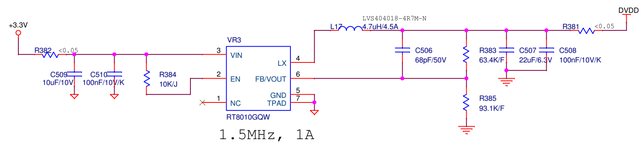

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	Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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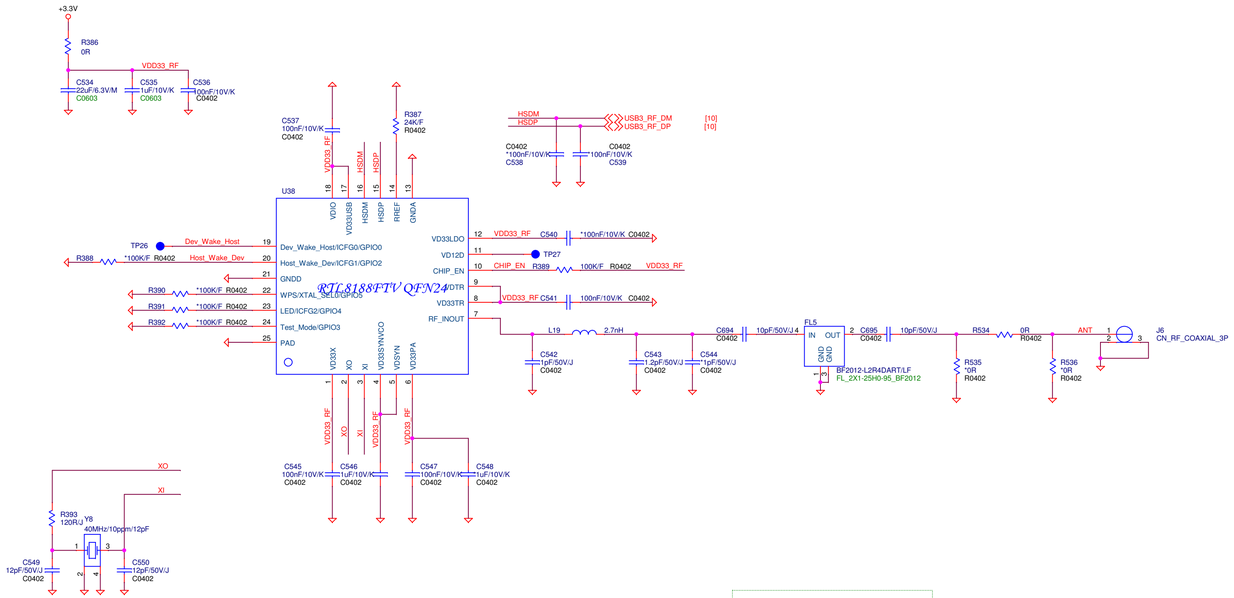

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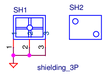

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Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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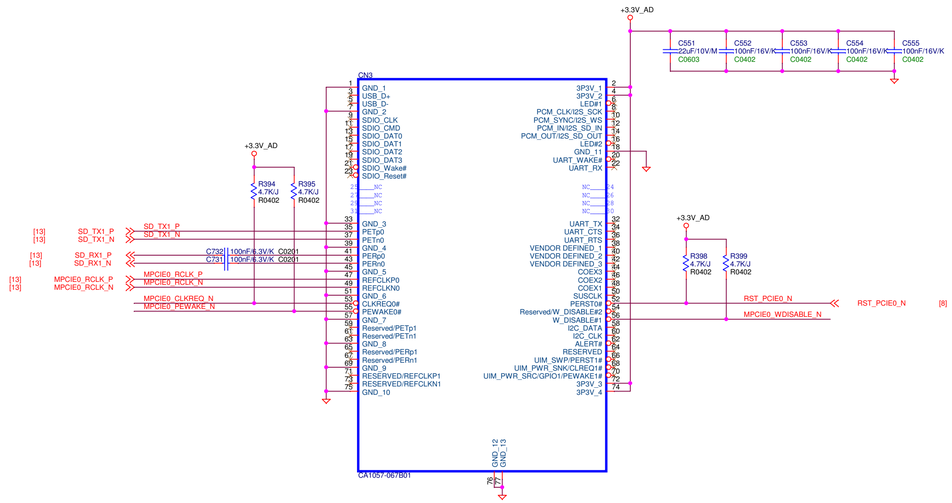
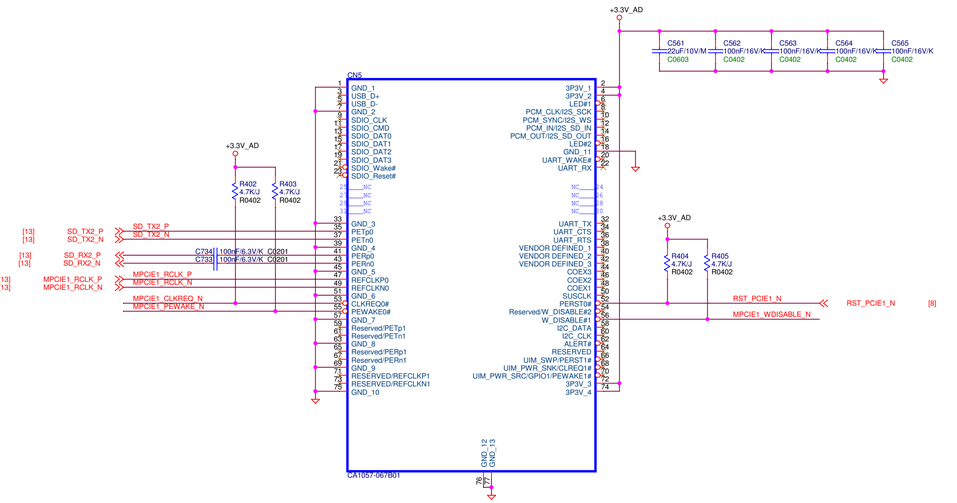
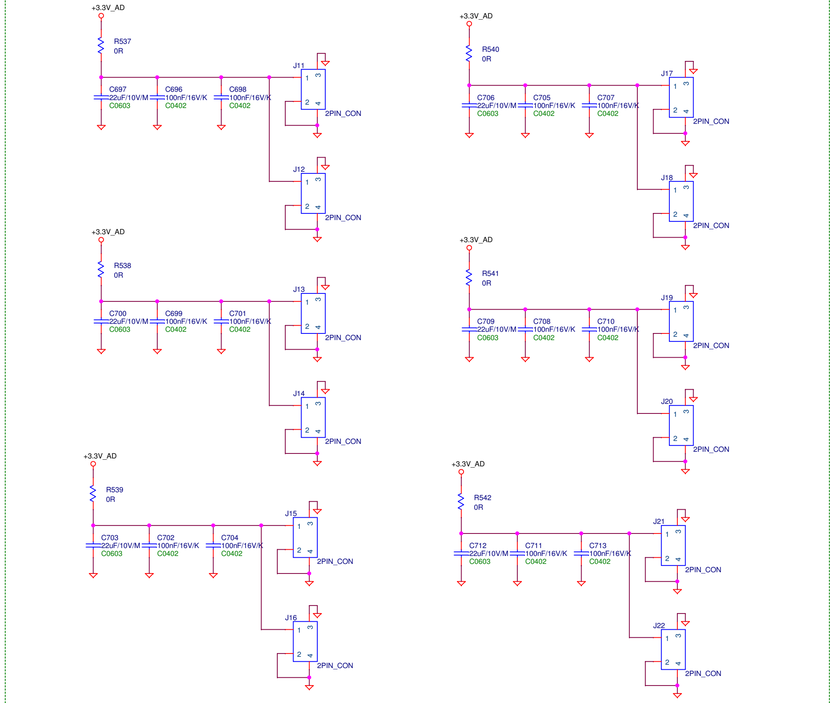
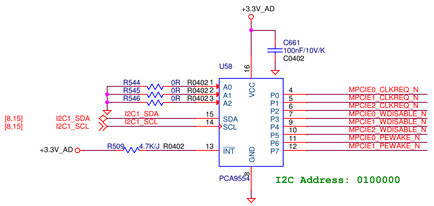
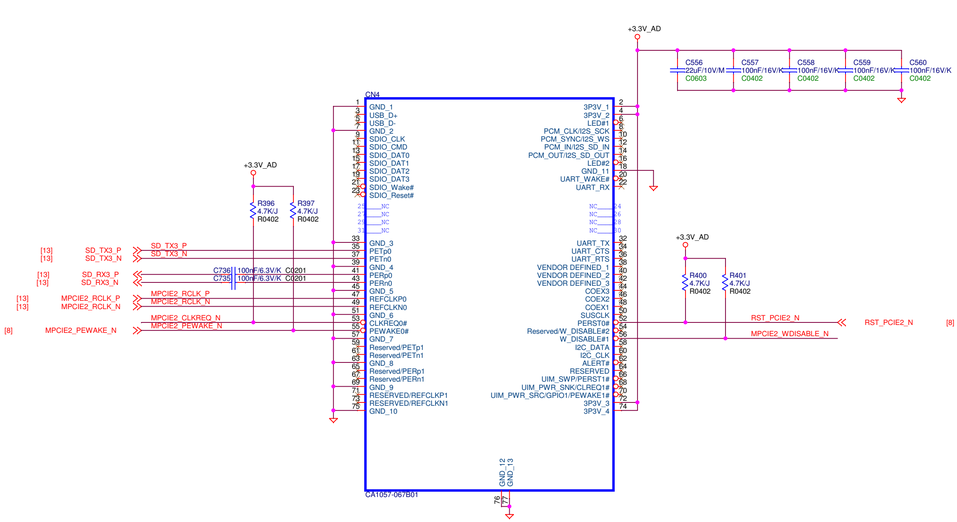




For RF module







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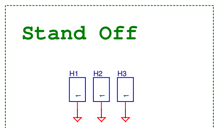

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	Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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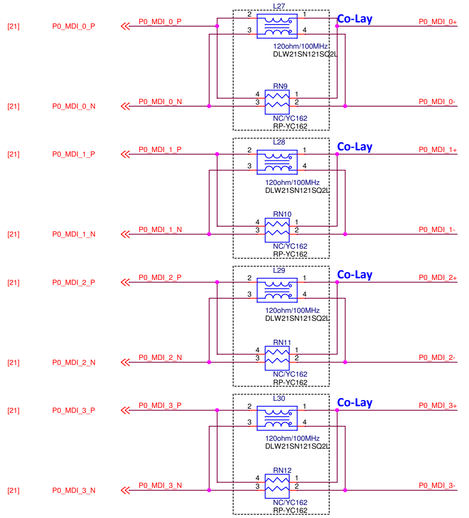

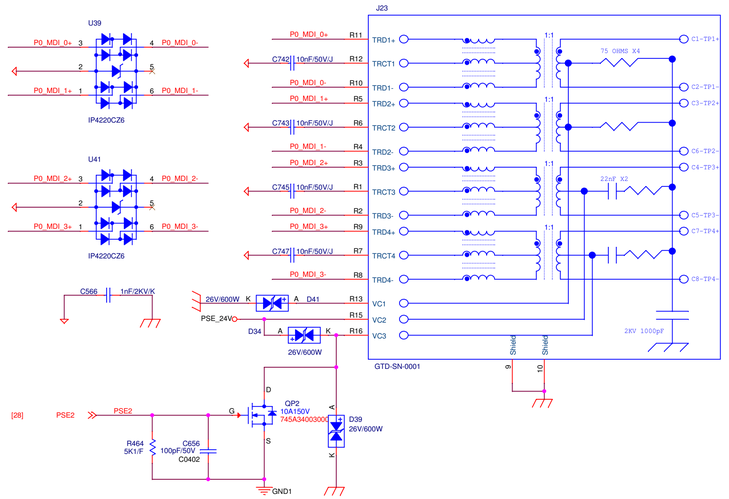

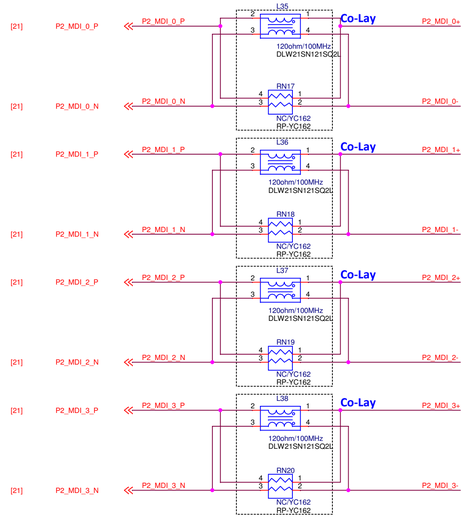

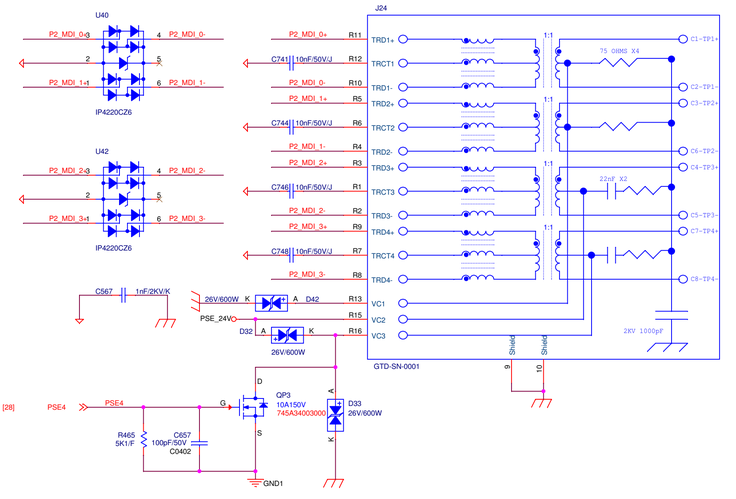

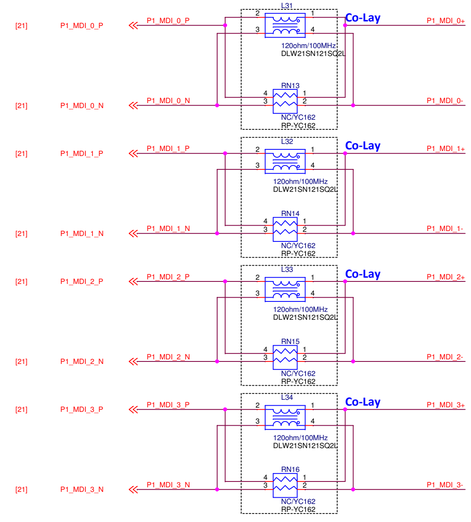

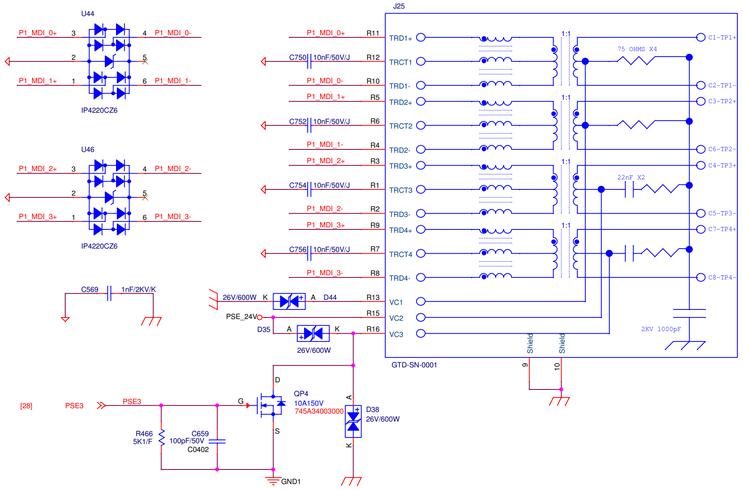

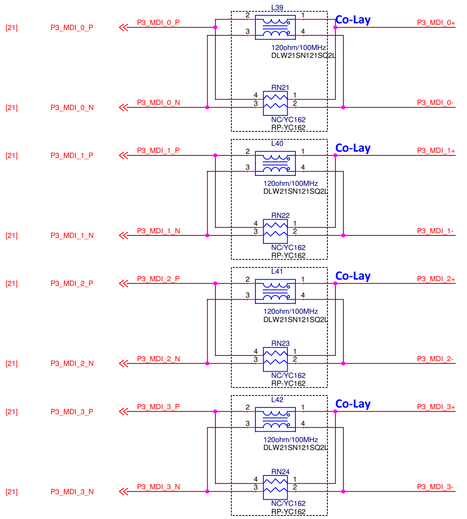

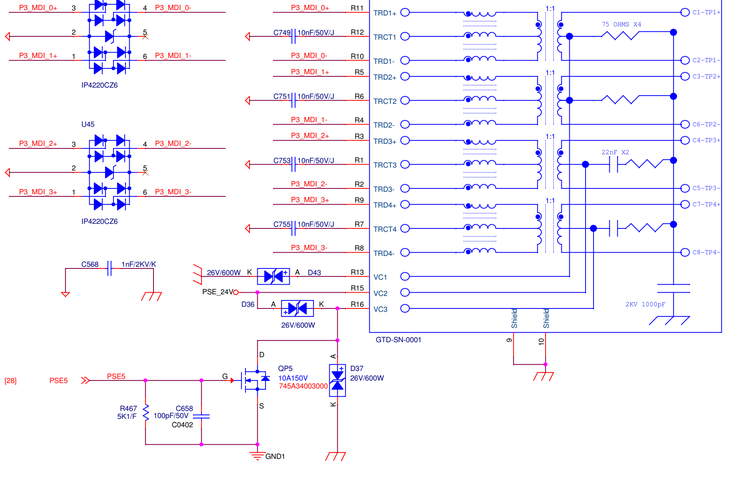

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Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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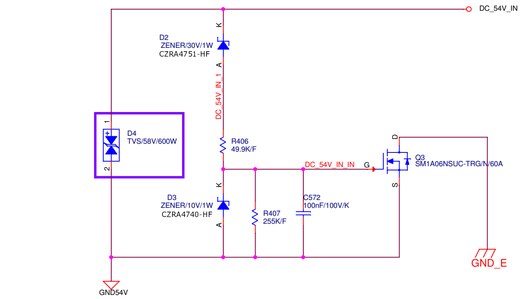

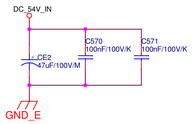

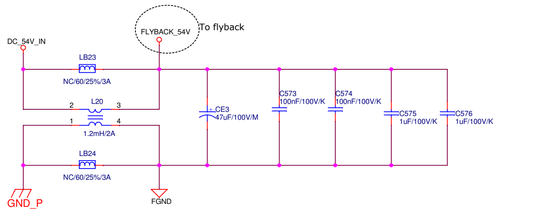

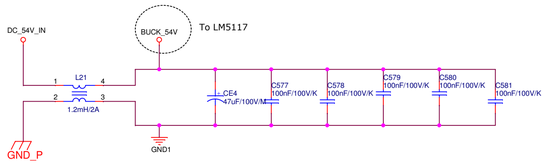

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	Engineer: Howie Shih	Check: Wei Lu	Approval: MT Chang	
Size: D	Project Name: COR		PCB Rev: 0.10	Sch.Rev: 0.10
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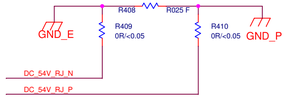

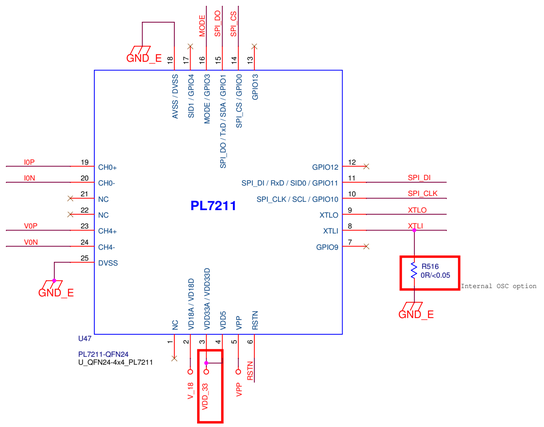

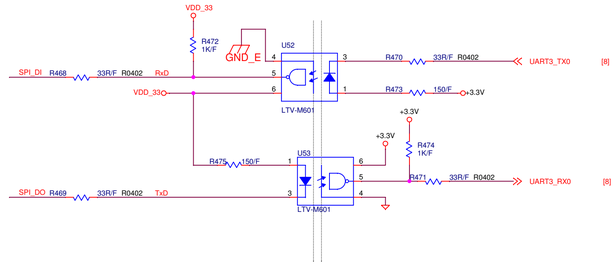

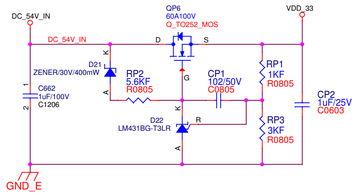

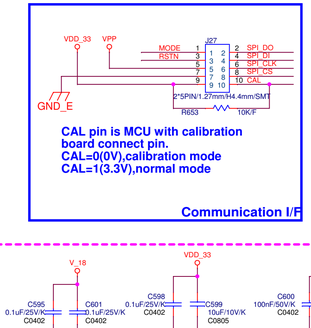

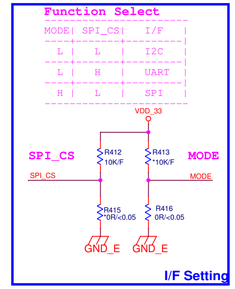

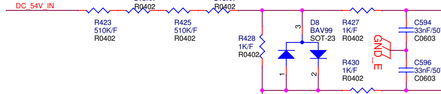

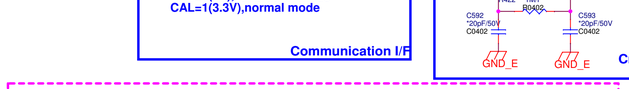

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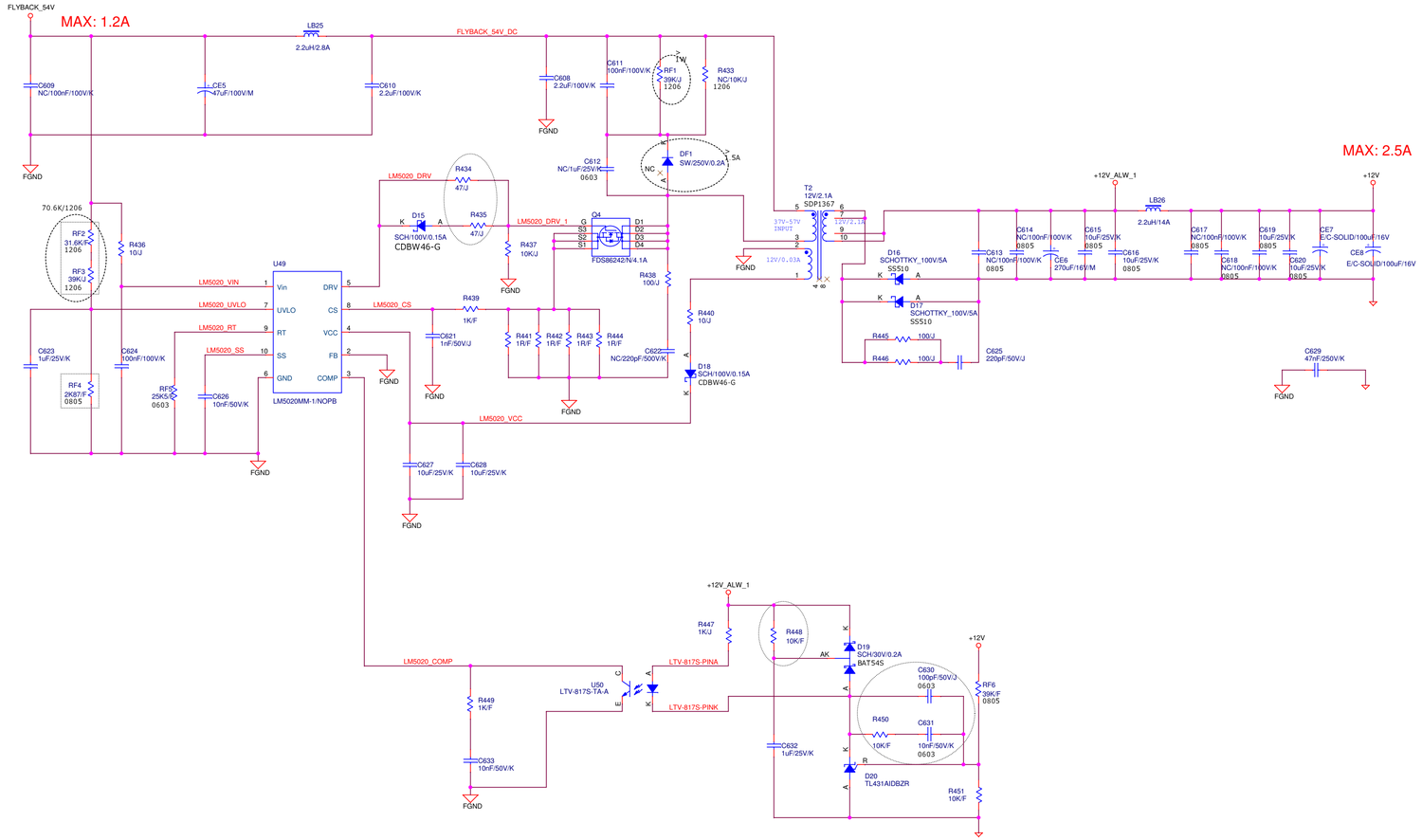
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
Date: Saturday, January 13, 2018	Sheet 26 of 28		



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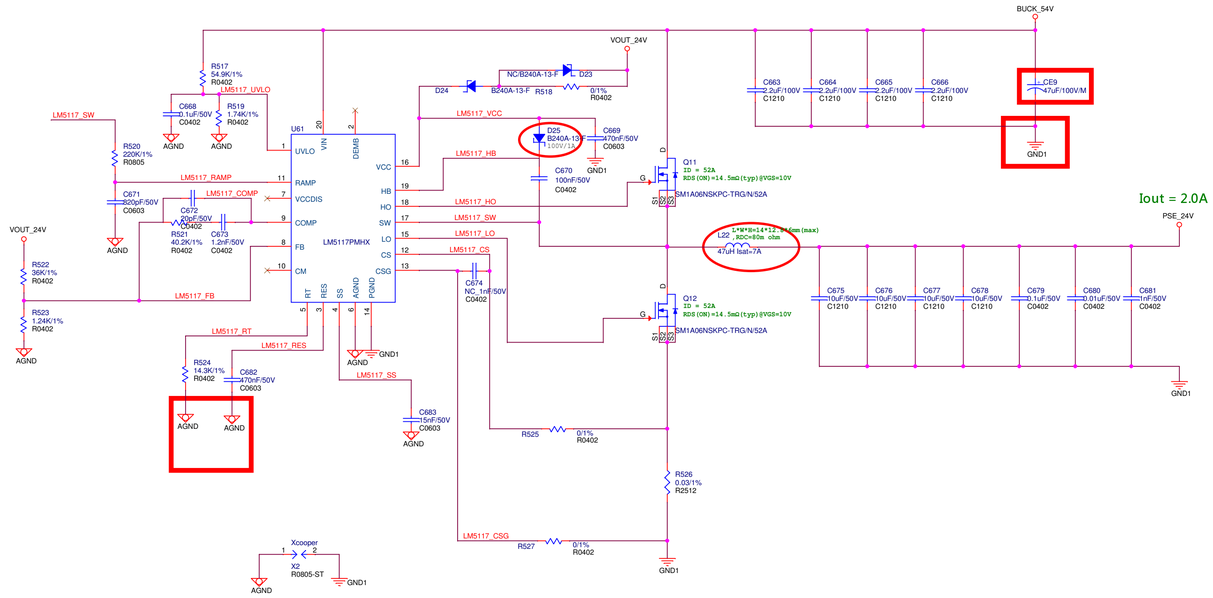
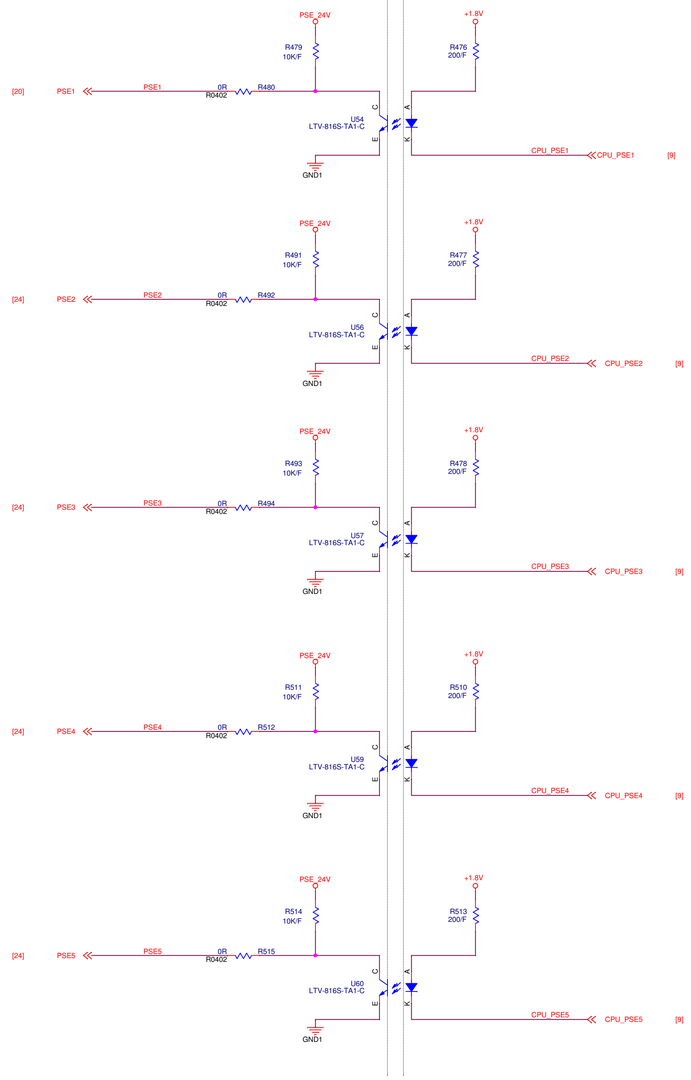
Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
Date: Saturday, January 13, 2018	Sheet 27 of 28		





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Size: D	Project Name: COR	PCB Rev: 0.10	Sch.Rev: 0.10
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