E1q4

Tuesday, October 20, 2020 1:52 PM

Problem 4. (4+6 points):

A. Consider an implementation of a processor where the combinational circuit latency is α ns (nanosecond). You are going to pipeline this implementation, and in your system the latency of each pipeline register is β ns. If you are to divide this entire combinational circuit in k stages, what is the throughput of your pipelined implementation? What about the total latency of a single instruction?

throughput $\frac{1}{\beta}$

latency = β

k stages

Latency: $k\beta$

B. Now, assume that the parameters α, β and k described above have the following relation:

$$\beta = \begin{cases} \alpha/10 & \text{if } k \leq 5, \\ \alpha/10 + k/50 \bullet 9\alpha/10 & \text{if } k > 5. \end{cases} \quad (1)$$

Based on the equation above, clearly present an analysis when would you pipeline this processor. Please consider three different values of k in your analysis: (i) $k = 5$; (ii) $k = 50$; and (iii) $k = 500$.

$\frac{2}{16} + \frac{14}{50} \frac{9x}{10}$

1 - 5

2 - 1

3 - 0