1:52 PM

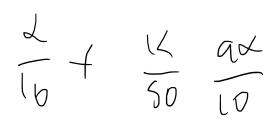
Problem 4. (4+6 points):

A. Consider an implementation of a processor where the combinational circuit latency is α ns (nanosecond). You are going to pipeline this implementation, and in your system the latency of each pipeline register is β ns. If you are to divide this entire combinational circuit in k stages, what is the throughput of your pipelined implementation? What about the total latency of a single instruction?

B. Now, assume that the parameters α , β and k described above have the following relation:

$$\beta = \begin{cases} \alpha/10 & \text{if } k \le 5, \\ \alpha/10 + k/50 \bullet 9\alpha/10 & \text{if } k > 5. \end{cases}$$
 (1)

Based on the equation above, clearly present an analysis when would you pipeline this processor. Please consider three different values of k in your analysis: (i) k = 5; (ii) k = 50; and (iii) k = 500.



1 - 5

2 ~ |

3 - 0