North South University

Department of Electrical & Computer Engineering

LAB REPORT

Course Name: **CSE332L- Computer Organization and Architecture Lab**

Experiment Number: 7

Experiment Name: Build a Full single cycle Datapath with main Control.

Experiment Date: 5-12-2021

Report Submission Date: 5-12-2021

Section: 07

Group Number:

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Remarks:	

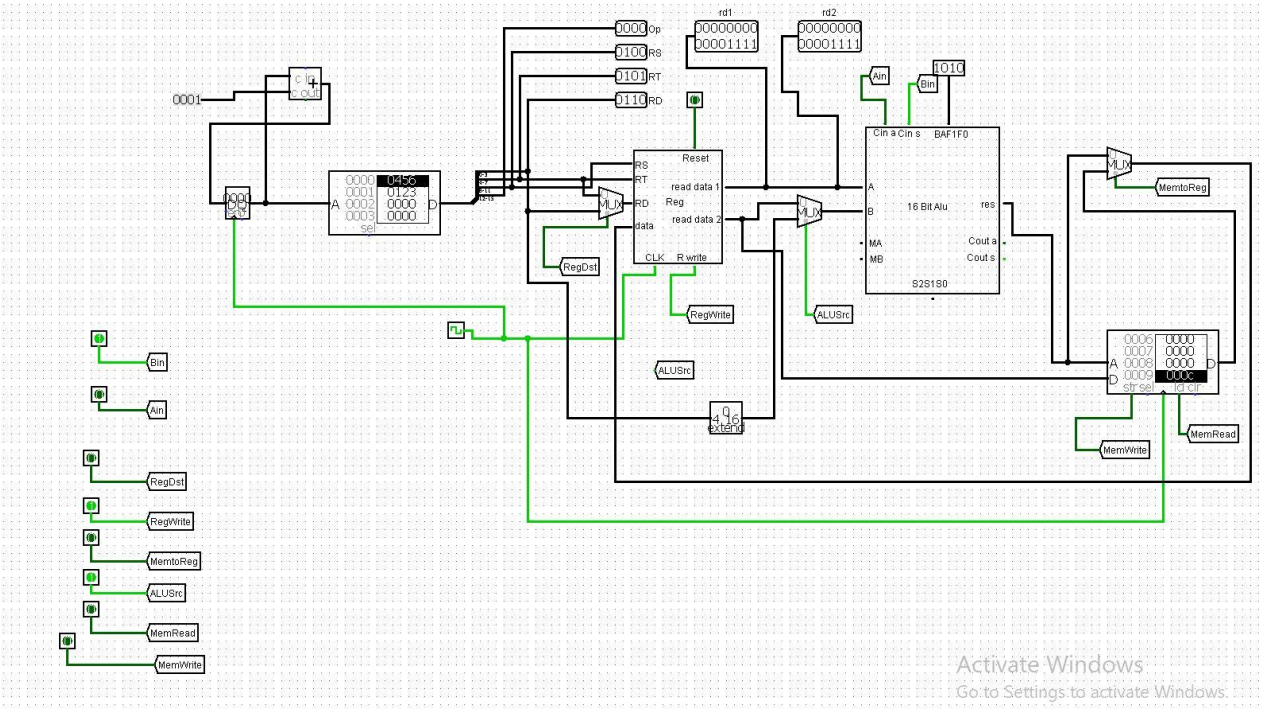
Exp Name: Build a Full single cycle Datapath with main Control.

Objectives:

We will have following objectives to fulfill:

1) Design an Instruction Fetch Unit of the datapath
2) Design an R-format and Load/Store Datapath
3) Compose the datapath segments designed above to yield a complete single cycle datapath.

Circuit Diagrams:



Data table:

Instructions	Opcode	RD/RT(MUX)	Write Enable	R/I-type (MUX)	AluOP(mux)	B.inv/Sub	lw	sw
Add	0000	1	1	0	1000	0	0	0
Sub	0001	1	1	0	1010	1	0	0
Lw	0010	0	1	1	1000	0	1	0
Sw	0011	0	0	1	1000	0	0	1
And	0100	1	1	0	0001	0	0	0
Or	0101	1	1	0	0010	0	0	0
Addi	0110	0	1	1	1000	0	0	0
Subi	0111	0	1	1	1010	1	0	0
Ori	1000	0	1	1	0010	0	0	0
Andi	1001	0	1	1	0001	0	0	0
Mul	1010	1	1	0	1111	0	0	0
Muli	1011	0	1	1	1111	0	0	0
beq	1100	0	0	0	1000	0	0	0

Discussion:

In this expriment,i gather knowledge about Build a full single cycle datapath.Firstly,I take D-mux which has write enable and RD is the part of register.Then,I take 16 register which is connected by enable pin with D-mux.In register,there is two more button for reset and clock.Then I take,two mux for reading data 1 nad 2 and two selector RS and RT which is mainly the part of resgister.

Then I make 3 more file for R type,I type and lw/sw.Then I take a Rom and register for controling the register read and write which consist of OP,RS,RT,RD.Then I take the ic of register file .Then I connect everything like RS,RT,RD. After that I take the ic of 16 bit Alu from my project then I connect the result of Alu with the data input of register file which is used for writing.By the help of clock plus ,I can write the data in register file which is mainly R type.

For making I type,I take a Rom and register for controling the register read and write which consist of OP,RS,RT,RD.Then I take the ic of register file .Then I connect everything like RS,RT,RD.RD for immediate value and Rs is for selecting register which one I use for input. After that I take the ic of 16 bit Alu from my project then I connect the result of Alu with the data input of register file which is used for writing.By the help of clock plus ,I can write the data in register file which is mainly I type.

For doing lw/sw I use same I type,but I add a ram which is connected by AlU output wire and read data two which is use for sw.we use lw for wring value in register and we use lw for storing value in memory.

Then I take another file which is mainly merge the I type,R type,lw/sw file.For doing this task,I use 3 mux,first mux is used for which operation I will do like R type or I type.we will select the 0 for I type and 1 for R type.For 2^{nd} mux which is mainly use for selecting immediate value and read data 2.For seleting read data 2 ,I use 0 and 1 for immediate value.I use mux three for selecting lw and add/sub . if I select 0 which is working for add/sub and other thing and 0 for lw operation.

During the experiment,I face a problem,like my circuit output is showing wrong output .By the help of my lab instructor ,I solve the problem.Then I do the all thing successfully.