2.13 inch
E-paper Display Series

GooDisplay®

GDEM0213U23

Dalian Good Display Co., Ltd.

Specification for 2.13 inch EPD

Model NO. :GDEM0213U23

Good Display's Confirmation:

Prepared by	Checked by	Approved by

Customer approval:

Customer	Approved by	Date

Revision History

Version	Content	Date	Producer
1.0	New release	2016/01/07	
2.0	Add Command Table	2016/01/30	
3.0	Added Part Number Definition	2016/06/12	
4.0	1. Changed the command table 2. Improved the operating Sequence 3. Add the partial update function	2016/12/01	
5.0	Part number change	2017/06/07	
5.1	1.Add the optimal storage environment 2.Change the ESD Gun test	2017/08/08	
5.2	Update Operating temperature and application circuit	2017/12/04	
5.3	Update Features and DC Characteristics and Over View	2018/03/12	
5.4	Update Circuit（Diode type）	2018/03/27	
5.5	Redefine typical test conditions	2018/09/28	

CONTENTS

1. Over View

GDEM0213U23 is an Active Matrix Electrophoretic Display (AM EPD), with interface and a reference system design. The display is capable to display images at 1-bit white ,black and red full display capabilities. The 2.13inch active area contains 250×122 pixels. The module is a TFT-array driving electrophoresis display, with integrated circuits including gate driver, source driver, MCU interface, timing controller, oscillator, DC-DC, SRAM, LUT, VCOM. Module can be used in portable electronic devices, such as Electronic Shelf Label (ESL) System.

2. Features

◆250×122 pixels display
◆High contrast High reflectance
◆Ultra wide viewing angle Ultra low power consumption
◆Pure reflective mode
◆Bi-stable display
◆Commercial temperature range
◆Landscape portrait modes
◆Hard-coat antiglare display surface
◆Ultra Low current deep sleep mode
◆On chip display RAM
◆Waveform can stored in On-chip OTP or written by MCU
◆Serial peripheral interface available
◆On-chip oscillator
◆On-chip booster and regulator control for generating VCOM, Gate and Source driving voltage

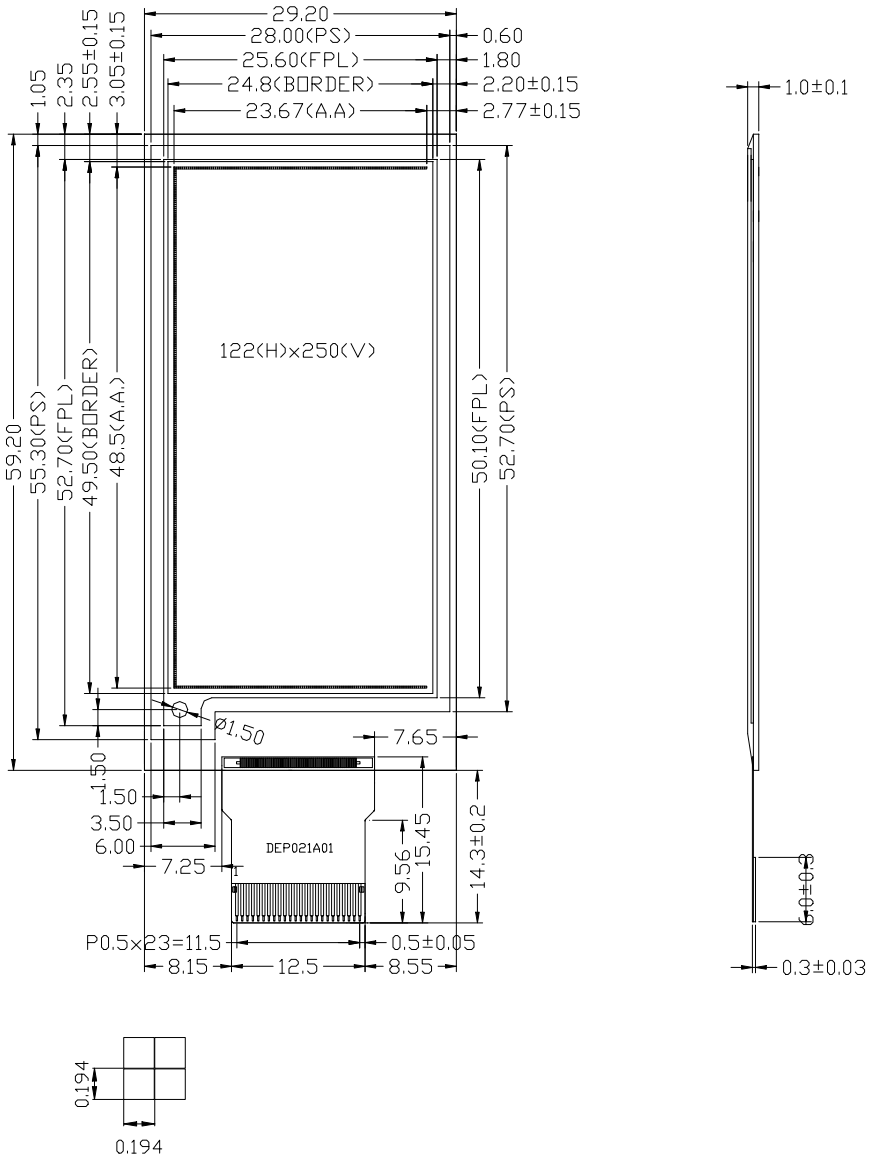
3. Mechanical Specification

Parameter	Specifications	Unit	Remark
Screen Size	2.13	Inch	
Display Resolution	122(H)×250(V)	Pixel	DPI:130
Active Area	23.67×48.50	mm	
Pixel Pitch	0.194×0.194	mm	
Pixel Configuration	Rectangle		
Outline Dimension	29.2(H)×59.2 (V) ×1.05(D)	mm	
Weight	3.2±0.5	g	

4.Mechanical Drawing of EPD Module

Confirmation:

DATE	REV.	MODIFICATION
2017-06-08	A	FIRST ISSUE



NOTE

1 DISPLAY MODE 2.13" ARREY FOR EPD
3 RESOLUTION:250gate*122source
4 PIXEL SIZE:0.194mm*0.194mm
6 Unspecified Tolerance:±0.2mm

RoHS

DALIAN GOOD DISPLAY CO., LTD.

TOLERANCES	TITLE:	PROJECT:		REV.:	DATE:	CUST. P/N:
UNMARKED ANGLES±1° .X=±0.4mm .XX=±0.20mm .XXX=±0.15mm	EPD	GDEM0213U23		A	17.06.08	
	DWN.	CHK.	APPR.	UNIT:	3RD ANGLE:	PAGE:
				mm		1/1

5. Input/output Pin Assignment

No.	Name	I/O	Description	Remark
1	NC		Do not connect with other NC pins	Keep Open
2	GDR	O	N-Channel MOSFET Gate Drive Control	
3	RESE	I	Current Sense Input for the Control Loop	
4	VGL	C	Negative Gate driving voltage	
5	VGH	C	Positive Gate driving voltage	
6	NC		Do not connect with other NC pins	Keep Open
7	Tout1	O	For Test	Keep Open
8	BS1	I	Bus Interface selection pin	Note 5-5
9	BUSY	O	Busy state output pin	Note 5-4
10	RES#	I	Reset signal input. Active Low.	Note 5-3
11	D/C#	I	Data /Command control pin	Note 5-2
12	CS#	I	Chip select input pin	Note 5-1
13	D0	I	Serial Clock pin (SPI)	
14	D1	I	Serial Data pin (SPI)	
15	VDDIO	P	Power Supply for interface logic pins It should be connected with VCI	
16	VCI	P	Power Supply for the chip	
17	VSS	P	Ground	
18	VDD	C	Core logic power pin VDD can be regulated internally from VCI. A capacitor should be connected between VDD and VSS	
19	VPP	P	FOR TEST	Keep Open
20	VSH	C	Positive Source driving voltage	
21	VGH	C	Positive Gate driving voltage	
22	VSL	C	Negative Source driving voltage	
23	PREVGL	C	Power Supply pin for VCOM, VGL and VSL	
24	VCOM	C	VCOM driving voltage	

I = Input Pin, O =Output Pin, /O = Bi-directional Pin (Input/output), P = Power Pin, C = Capacitor Pin

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled LOW.

Note 5-2: This pin is (D/C#) Data/Command control pin connecting to the MCU in 4-wire SPI mode. When the pin is pulled HIGH, the data at SDA will be interpreted as data. When the pin is pulled LOW, the data at SDA will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active low.

Note 5-4: This pin is Busy state output pin. When Busy is High, the operation of chip should not be interrupted, command should not be sent.

Note 5-5: Bus interface selection pin

BS1 State	MCU Interface
L	4-lines serial peripheral interface(SPI) - 8 bits SPI
H	3- lines serial peripheral interface(SPI) - 9 bits SPI

6. Electrical Characteristics

6.1 Absolute Maximum Rating

Parameter	Symbol	Rating	Unit
Logic supply voltage	VCI	-0.5 to +4.0	V
Logic Input voltage	VIN	-0.5 to VCI +0.5	V
Logic Output voltage	VOUT	-0.5 to VCI +0.5	V
Operating Temp range	TOPR	0 to+25	ºC.
Storage Temp range	TSTG	-25 to+70	ºC.
Operating Temp range max	TOPRm	0 to +40	ºC.
Optimal Storage Temp	TSTGo	23±2	ºC.
Optimal Storage Humidity	HSTGo	55±10%	RH

Note:

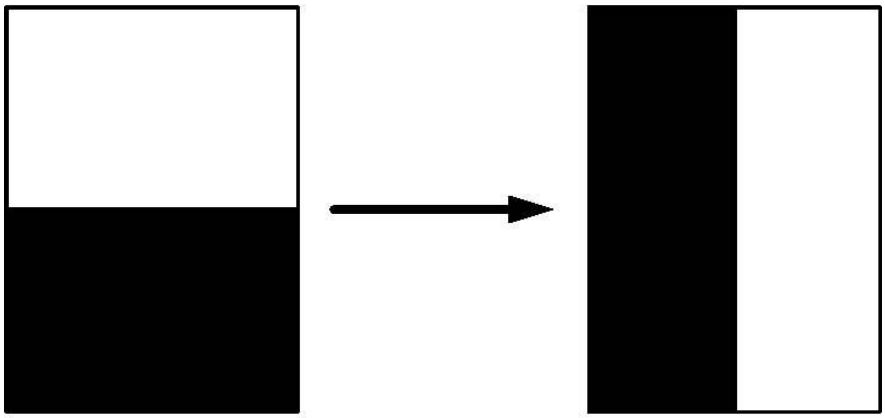
1.Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Panel DC Characteristics tables.

6.2 PanelDC Characteristics

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
Single ground	V_{SS}	-		-	0	-	V
Logic supply voltage	V_{CI}	-	VCI	2.2	3.0	3.7	V
Core logic voltage	V_{DD}		VDD	1.7	1.8	1.9	V
High level input voltage	V_{IH}	-	-	0.8 V_{CI}	-	-	V
Low level input voltage	V_{IL}	-	-	-	-	0.2 V_{CI}	V
High level output voltage	V_{OH}	IOH = -100uA	-	0.9 V_{CI}	-	-	V
Low level output voltage	V_{OL}	IOL = 100uA	-	-	-	0.1 V_{CI}	V
Typical power	P_{TYP}	V_{CI} =3.0V	-	-	12	-	mW
Deep sleep mode	P_{STPY}	V_{CI} =3.0V	-	-	0.003	-	mW
Typical operating current	Iopr_VCI	V_{CI} =3.0V	-	-	4	-	mA
Image update time	-	23 ºC	-	-	12	-	sec
Sleep mode current	Islp_V_{CI}	DC/DC off No clock No input load Ram data retain	-	-	20		uA
Deep sleep mode current	Idslp_V_{CI}	DC/DC off No clock No input load Ram data not retain	-	-	3	5	uA

Notes: 1. The typical power is measured with following transition from horizontal 2 scale pattern to vertical 2 scale pattern.



2. The deep sleep power is the consumed power when the panel controller is in deep sleep mode.

3. The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by Good Display.

6.3 Panel DC Characteristics(Driver IC Internal Regulators)

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.

Parameter	Symbol	Condition	Applicable pin	Min.	Typ.	Max.	Unit
VCOM output voltage	VCOM	-	VCOM	-	TBD	-	V
Positive Source output voltage	V_{SH}	-	S_0~S_{121}	+14.5	+15	+15.5	V
Negative Source output voltage	V_{SL}	-	S_0~S_{121}	-15.5	-15	-14.5	V
Positive gate output voltage	Vgh	-	G_0~G_{249}	+21	+22	+23	V
Negative gate output voltage	Vgl	-	G_0~G_{249}	-21	-20	-19	V

6.4 Panel AC Characteristics

6.4.1 MCU Interface Selection

The pin assignment at different interface mode is summarized in Table 6-4-1. Different MCU mode can be set by hardware selection on BS1 pins. The display panel only supports 4-wire SPI or 3-wire SPI interface mode.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
BS1=L 4-wire SPI	SDIN	SCLK	CS#	D/C#	RES#
BS1=H 3-wire SPI	SDIN	SCLK	CS#	L	RES#

Note: L is connected to **Vss**H is connected to **VCI**

6.4.2 MCU Serial Interface (4-wire SPI)

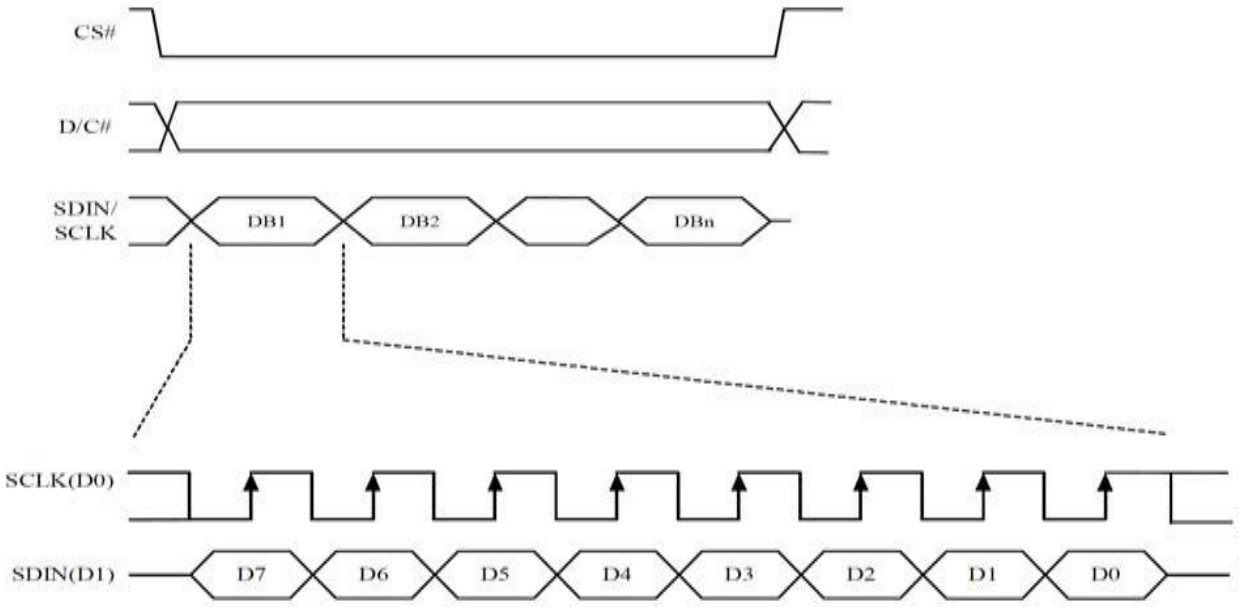
The serial interface consists of serial clock SCL, serial data SDA, D/C#, CS#. This interface supports Write mode and Read mode.

Function	CS#	D/C#	SCL
Write command	L	L	↑
Write data	L	H	↑

Note: ↑ stands for rising edge of signal

SDIN is shifted into an 8-bit shift register on every rising edge of SCLK in the order of D7, D6, ... D0. D/C# is sampled on every eighth clock and the data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

Figure 6-1: Write procedure in 4-wire SPI mode



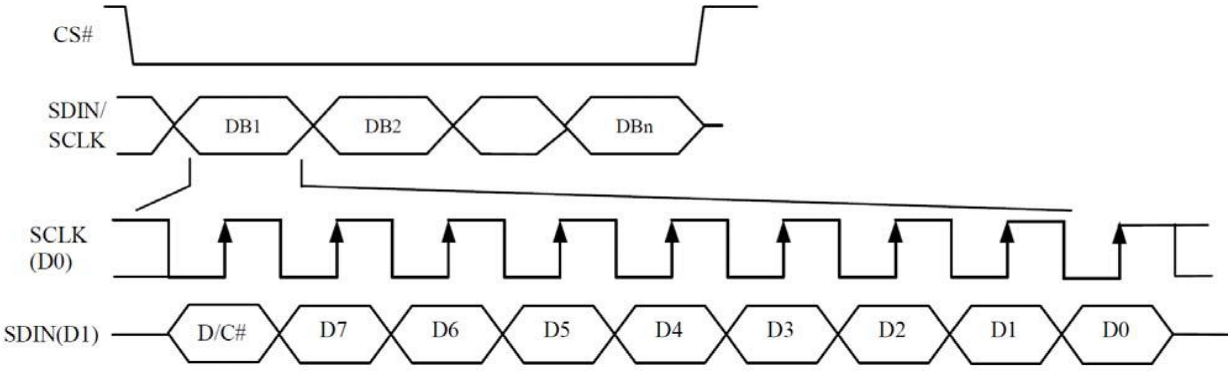
6.4.3 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCL, serial data SDA and CS#. This interface also supports Write mode and Read mode.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).

Function	CS#	D/C#	SCL
Write command	L	Tie	↑
Write data	L	Tie	↑

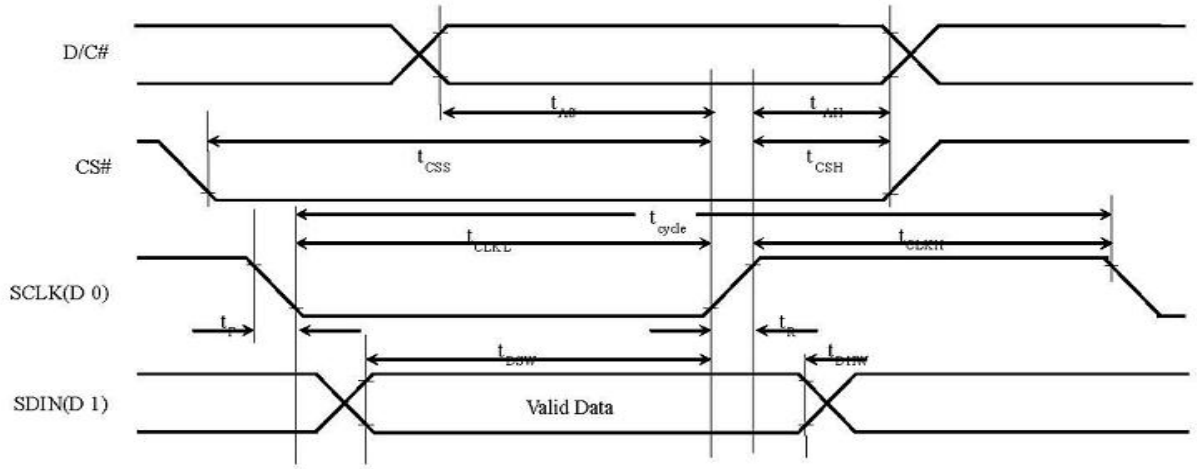
Figure 6-2: Write procedure in 3-wire SPI mode

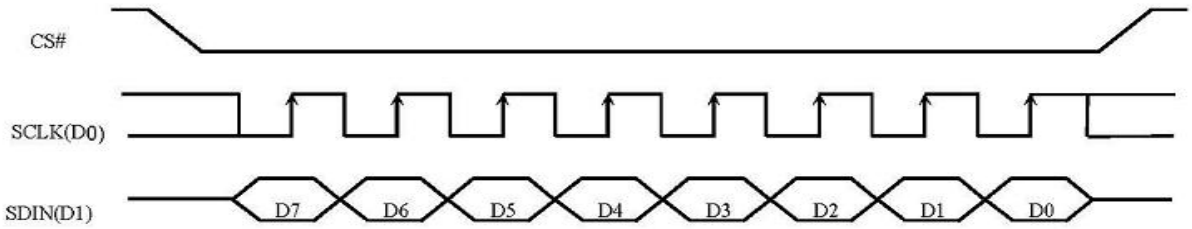


6.4.4 Interface Timing

The following specifications apply for: VSS=0V, VCI=3.0V, TOPR =23ºC.

Symbol	Parameter	Test Condition	Applicable pin	Min.	Typ.	Max.	Unit
Fosc	Internal Oscillator frequency	VCI=2.4 to 3.3V	CL	0.95	1	1.05	MHz





Serial Interface Timing Characteristics

(VCI - VSS = 2.2V to 3.7V, TOPR = 23°C, CL=20pF)

Symbol	Parameter	Min	Typ	Max	Unit
Tcycle	Clock Cycle Time	250	-	-	ns
Tas	Address Setup Time	150	-	-	ns
Tah	Address Hold Time	150	-	-	ns
Tcss	Chip Select Setup Time	120	-	-	ns
Tcsh	Chip Select Hold Time	60	-	-	ns
Tdsw	Write Data Setup Time	50	-	-	ns
Tdhw	Write Data Hold Time	15	-	-	ns
Tclkl	Clock Low Time	100			ns
Tclkh	Clock High Time	100			ns
Tr	Rise Time [20% ~ 80%]			15	ns
Tf	Fall Time [20% ~ 80%]			15	

7. Command Table

R/W#	D/C#	Hex	D7	D6		D4	D3	D1	D0	Command	Description
0	0	01	0	0		0	0	0	1	Driver Output control	Gate setting Set A[7:0]=F9h Set B[7:0]=01h
0	1		A7	A6		A4	A3	A1	A0		
0	1		0	0		0	0	B1	B0		
0	0	03	0	0		0	0	1	1	Gate Driving voltage control	Set Gate Driving voltage In red/black/white region(LUT1) A[4:0]=10h[POR],VGH at 22V[POR] VGH setting from 15V to 22V B[3:0]=0Ah[POR],VGL at 20V[POR] VGL setting from -15V to -20V In red region(LUT2) A[4:0]=02h[POR],VGH at 15V[POR] VGH setting from 15V to 22V B[3:0]=0Ah[POR],VGL at 20V[POR] VGL setting from -15V to -20V
0	1		0	0		A4	A3	A1	A0		
0	1		0	0		0	B3	B1	B0		
0	0	04	0	0		0	0	0	0	Source Driving voltage control	SetSource Driving voltage In red/black/white region(LUT1) A[7:0]=19h[POR],VSH/VSL at +/- 15V In red region (LUT2) A[7:0]=36h[POR],VSH5.4V
0	1		A7	A6		A4	A3	A1	A0		
0	0	05	0	0		0	0	0	1	Red display control	Set analog mode for red display A[7:6]=00 analog mode in red/black/white region(LUT1) A[7:6]=11 analog mode in red region(LUT2)
0	1		A7	A6		0	0	0	0		
0	0	10	0	0		1	0	0	0	Deep Sleep mode	Deep Sleep mode Control A[0] : Description 0 Normal Mode [POR] 1 Enter Deep Sleep Mode
0	1		0	0		0	0	0	A_0		
0	0	11	0	0		1	0	0	1	Data Entry mode setting	Define data entry sequence A [1:0] = ID[1:0]Address automatic increment / decrement setting The setting of incrementing or decrementing of the address counter can be made independently in each upper and lower bit of the address. 00 –Y decrement, X decrement, 01 –Y decrement, X increment, 10 –Y increment, X decrement, 11 –Y increment, X increment [POR] A[2] = AM Set the direction in which the address counter is updated automatically after data are written to the RAM. AM= 0, the address counter is updated in the X direction. [POR] AM = 1, the address counter is updated
0	1		0	0		0	0	A_1	A_0		

<table>
<tr><td>0</td><td>0</td><td>12</td><td>0</td><td>0</td><td></td><td>1</td><td>0</td><td>1</td><td>0</td><td>SWRESET</td><td>It resets the commands and parameters to their S/W Reset default values except R10h-Deep Sleep Mode
Note: RAM are unaffected by this command.</td></tr>
<tr><td>0</td><td>0</td><td>1A</td><td>0</td><td>0</td><td></td><td>1</td><td>1</td><td>1</td><td>0</td><td rowspan="3">Temperature Sensor Control</td><td rowspan="3">Write to temperature register.
A[7:0] – MSByte 01111111[POR]
B[7:0] – LSByte 11110000[POR]</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td></td><td>A4</td><td>A3</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>B6</td><td></td><td>B4</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>0</td><td>20</td><td>0</td><td>0</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>Master Activation</td><td>Activate Display Update Sequence
The Display Update Sequence Option is located at R22h
User should not interrupt this operation to avoid corruption of panel images.</td></tr>
<tr><td>0</td><td>0</td><td>21</td><td>0</td><td>0</td><td></td><td>0</td><td>0</td><td>0</td><td>1</td><td rowspan="2">Display Update Control 1</td><td rowspan="2">Option for Display Update
Bypass Option used for Pattern Display, which is used for display the RAM content
into the DisplayOld RAM Bypass option
A[7] = 1: Enable bypass
A[7] = 0: Disable bypass [POR]
A[4] = 0 [POR]
A[1:0] Initial Update Option – SourceControl
<table><tr><td>A[1:0]</td><td>GSA</td><td>GSB</td></tr><tr><td>01[POR]</td><td>GS0</td><td>GS1</td></tr></table></td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td></td><td>0</td><td>A3</td><td>A1</td><td>A0</td></tr>
<tr><td>0</td><td>0</td><td>22</td><td>0</td><td>0</td><td></td><td>0</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Display Update Control 2</td><td rowspan="2">Display Update Sequence Option:
Enable the stage for Master Activation
<table><tr><td colspan="2">Setting for LUT from MCU</td></tr><tr><td>Enable Clock Signal,
Then Enable Analog
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC</td><td>C7</td></tr><tr><td colspan="2">Setting for LUT from OTP according external Temperature Sensor operatio</td></tr><tr><td>Then Enable Analog
Then Load LUT</td><td>90</td></tr><tr><td>Enable Analog
Then PATTERN DISPLAY
Then Disable Analog
Then Disable OSC</td><td>47</td></tr></table></td></tr>
<tr><td></td><td>1</td><td></td><td>A7</td><td>A6</td><td></td><td>A4</td><td>A3</td><td>A1</td><td>A0</td></tr>
</table>

0	0	24	0	0		0	0	0	0	WriteRAM1	After this command, data entries will be written into theRAM until another command is written. Address pointers will advance accordingly. For Write pixel: Content of write RAM(BW)=1 For Black pixel: Content of write RAM(BW)=0
0	0	26	0	0		0	0	0	0	WriteRAM for Red	After this command, data entries will be written into theRAM until another command is written. Address pointers will advance accordingly. For RED pixel: Content of write RAM(BW)=1 For Black/White pixel: Content of write RAM(BW)=0
0	0	2C	0	0		0	1	0	0	Write VCOM register	Set A[7:0]=7Bh
0	1		A7	A6		A4	A3	A1	A0		
0	0	2D	0	0		0	1	0	1	VCOM Register Read	Read VCOM Register: 1. A[7:0]=00H 2. B[7:0]: VCOM Register
1	1		A7	A6		A4	A3	A1	A0		
1	1		B7	B6		B4	B3	B1	B0		
0	0	2F	0	0		0	1	1	1	Status Bit Read	Read IC status Bit A[1:0]: chip ID [POR=01] A[2] : Busy flog [POR=0]
1	1		0	0		0	0	A1	A0		
0	0	32	0	0		1	0	1	0	Write LUT register	Write LUT register from MCU interface [29 bytes].
0	1		A7	A6		A4	A3	A1	A0		
0	1		B7	B6		B4	B3	B1	B0		
0	1		:	:		:	:	:	:		
0	0	3A	0	0		1	1	1	0	Set dummy line period	Set A[6:0]=04h Default value will give 100Hz Frame frequency
0	1		0	A6		A4	A3	A1	A0		
0	0	3B	0	0		1	1	1	1	Set Gate line width	Set A[3:0]=04h Default value will give 100Hz Frame frequency
0	1		0	0		0	A3	A1	A0		
0	0	3C	0	0		1	1	0	0	Border control	Select border waveform for VBD

<table>
<tr><td>0</td><td>1</td><td></td><td>A7</td><td>A6</td><td></td><td>A4</td><td>0</td><td>A1</td><td>A0</td><td></td><td>A[7] Follow Source at Initial UpdateDisplay
A [7]=0: [POR]
A [7]=1: Follow Source at Initial Update
Display for VBD, A [6:0] setting are beingoverridden at Initial display stage
A [6] Select GS Transition/ Fix Level
A[6]=0: Select GS Transition A[3:0]
A [6]=1: Select FIX level Setting A[5:4]
A [5:4] Fix Level Setting for VBD
<table><tr><td>A[5:4]</td><td>VBD level</td></tr><tr><td>00</td><td>VSS</td></tr><tr><td>01</td><td>VSH</td></tr><tr><td>10</td><td>VSL</td></tr><tr><td>11[POR]</td><td>HiZ</td></tr></table>A [1:0] GS transition setting for VBD (Select waveform like data A[3:2] to data
A[1:0])
<table><tr><td>A[1:0]</td><td>GSC</td><td>GSD</td></tr><tr><td>01[POR]</td><td>GS0</td><td>GS1</td></tr></table></td></tr>
<tr><td>0</td><td>0</td><td>44</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td rowspan="3">Set RAM X - address Start / End position</td><td rowspan="3"></td><td rowspan="3">Specify the start/end positions of the window address in the X direction by an address unit
A[4:0]: XSA[4:0], XStart, POR = 00h
B[4:0]: XEA[4:0], XEnd, POR = 0Fh</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>A_4</td><td>A_3</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>B_4</td><td>B_3</td><td>B_0</td></tr>
<tr><td>0</td><td>0</td><td>45</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td rowspan="3">Set Ram Y- address Start / End position</td><td rowspan="3"></td><td rowspan="3">Specify the start/end positions of the window address in the Y direction by an address unit
A[7:0]: YSA[7:0], YStart, POR = 00h
B[7:0]: YEA[7:0], YEnd, POR = F9h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_4</td><td>A_3</td><td>A_0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B_7</td><td>B_6</td><td>B_4</td><td>B_3</td><td>B_0</td></tr>
<tr><td>0</td><td>0</td><td>4E</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td rowspan="2">Set RAM X address counter</td><td rowspan="2"></td><td rowspan="2">Make initial settings for the RAM X address in the address counter (AC)
A[4:0]: XAD[4:0], POR is 00h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>A_4</td><td>A_3</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>4F</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td rowspan="2">Set RAM Y address counter</td><td rowspan="2"></td><td rowspan="2">Make initial settings for the RAM Y address in the address counter (AC)
A[7:0]: YAD[7:0], POR is 00h</td></tr>
<tr><td>0</td><td>1</td><td></td><td>A_7</td><td>A_6</td><td>A_4</td><td>A_3</td><td>A_0</td></tr>
<tr><td>0</td><td>0</td><td>75</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td rowspan="4">Red Display Control</td><td rowspan="4"></td><td rowspan="4">Set Analog Mode for Red Display
B7=0 Analog Mode inRed/Black/White region
(LUT1).
B7=1 Analog Mode in Red region(LUT2).</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>B7</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>0</td><td>1</td><td></td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table>

8. Optical Specification

Measurements are made with that the illumination is under an angle of 45 degree, the detection is perpendicular unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ.	Max	Units	Notes
R	White Reflectivity	White	30	35	-	%	8-1
CR	Contrast Ratio	indoor	8:1		-		8-2
GN	2Grey Level	-	-	DS+(WS-DS)*n(m-1)			8-3
Tupdate	Image update time	at 23 °C	-	3	-	sec	
Life		Topr		1000000times or 5years			

Notes: 8-1. Luminance meter: Eye-One Pro Spectrophotometer.

8-2. CR=Surface Reflectance with all white pixel/Surface Reflectance with all black pixels.

8-3 WS: White state, DS: Dark state

9. Handling, Safety, and Environment Requirements

Warning

The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

Caution

The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components. Disassembling the display module.

Disassembling the display module can cause permanent damage and invalidates the warranty agreements.

Observe general precautions that are common to handling delicate electronic components. The glass can break and front surfaces can easily be damaged. Moreover the display is sensitive to static electricity and other rough environmental conditions.

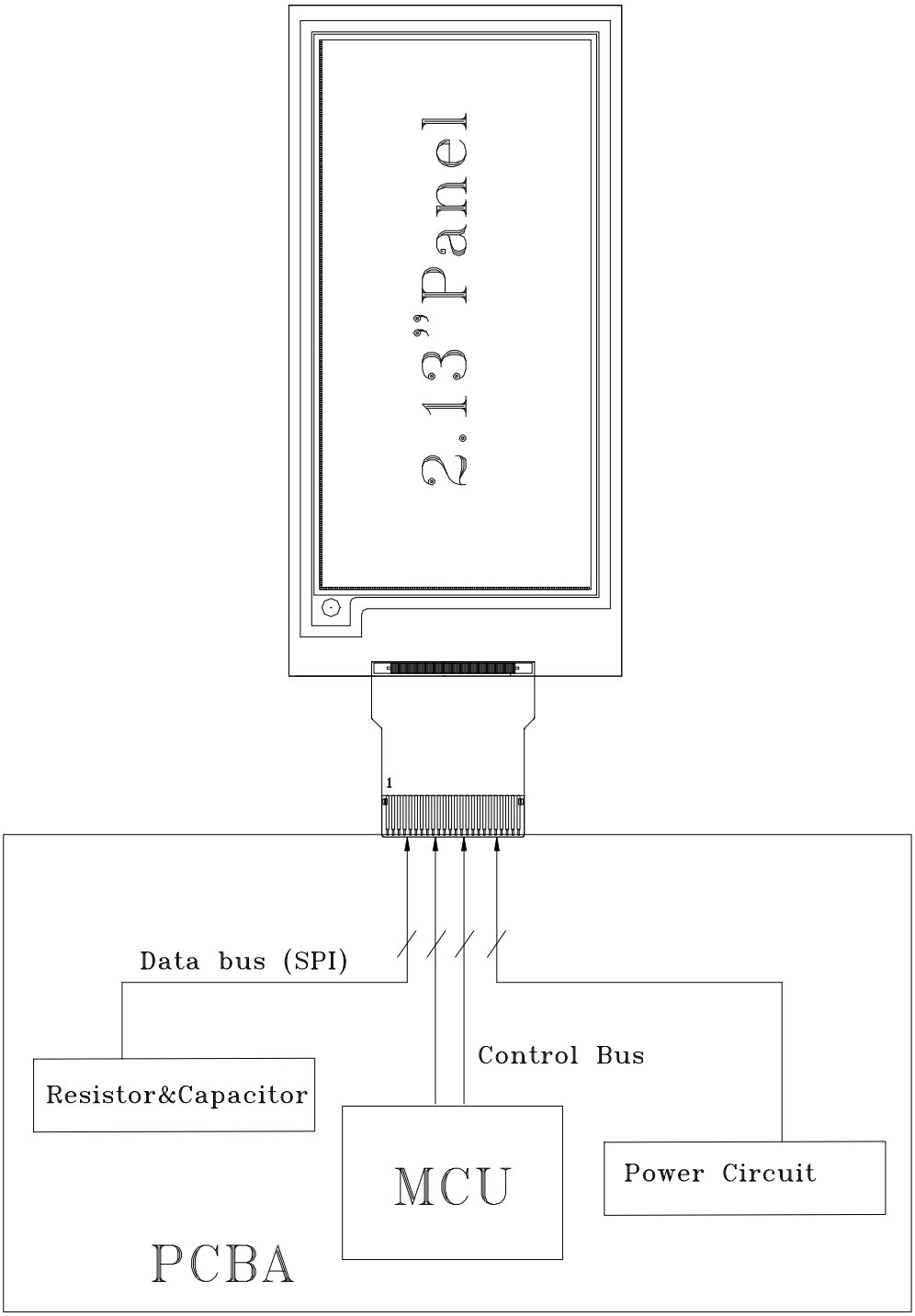
Data sheet status	
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

10. Reliability Test

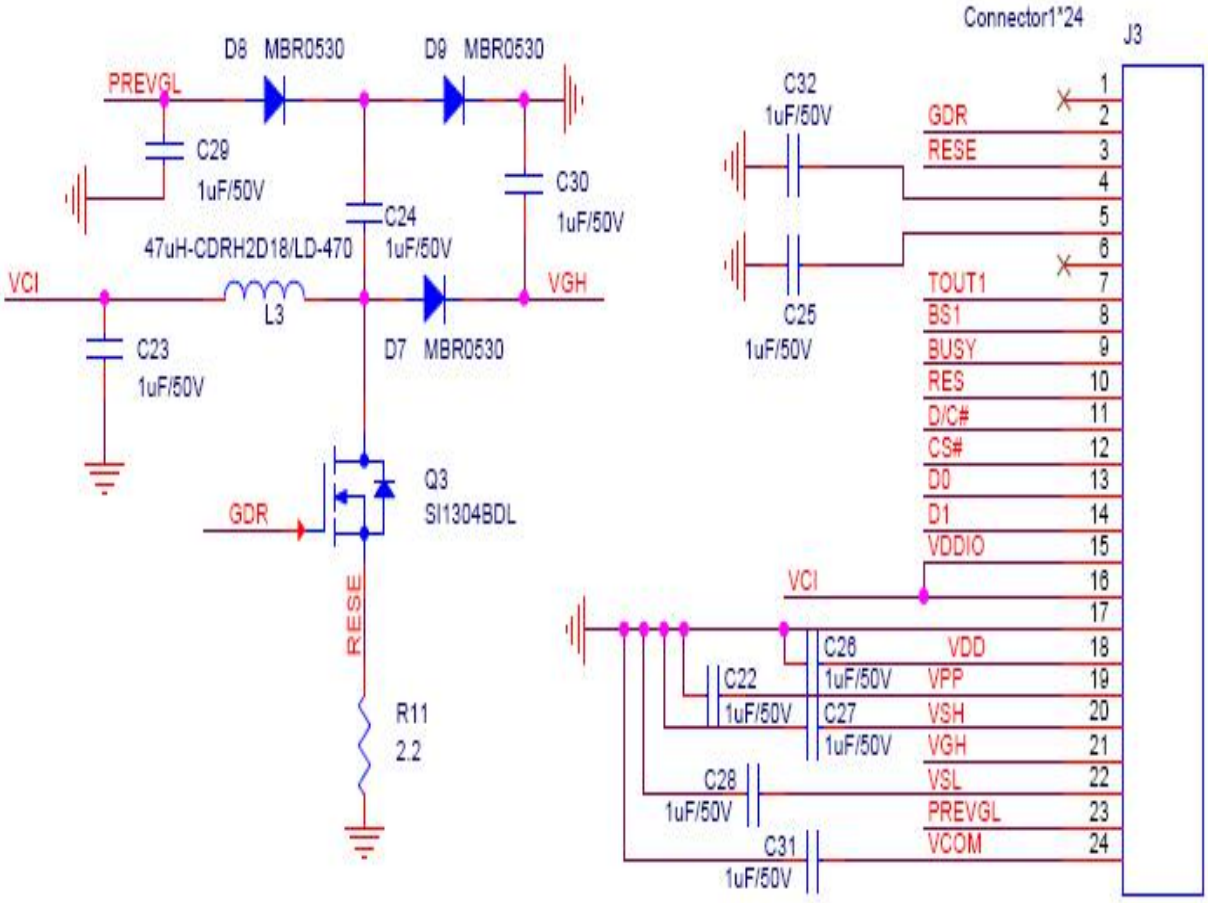
NO	Test items	Test condition
1	Low-Temperature Storage	T = -25°C, 240 h Test in white pattern
2	High-Temperature Storage	T=60ºC，RH=35%，240h Test in white pattern
3	High-Temperature Operation	T=40ºC，RH=35%，240h
4	Low-Temperature Operation	0ºC，240h
5	High-Temperature, High-Humidity Operation	T=40ºC，RH=80%，168h
6	High Temperature, High Humidity Storage	T=50ºC，RH=80%, 240h Test in white pattern
7	Temperature Cycle	1 cycle:[-25°C 30min]→[+60 °C 30 min] : 50 cycles Test in white pattern
8	UV exposure Resistance	765W/m² for 168hrs,40 °C Test in white pattern
9	ESD Gun	Air+/-15KV;Contact+/-8KV (Test finished product shell,not display only) Air+/-8KV;Contact+/-6KV (Naked EPD display,no including IC and FPC area) Air+/-4KV;Contact+/-2KV (Naked EPD display,including IC and FPC area)

Note:Put in normal temperature for 1hour after test finished,display performance is ok.

11. Block Diagram

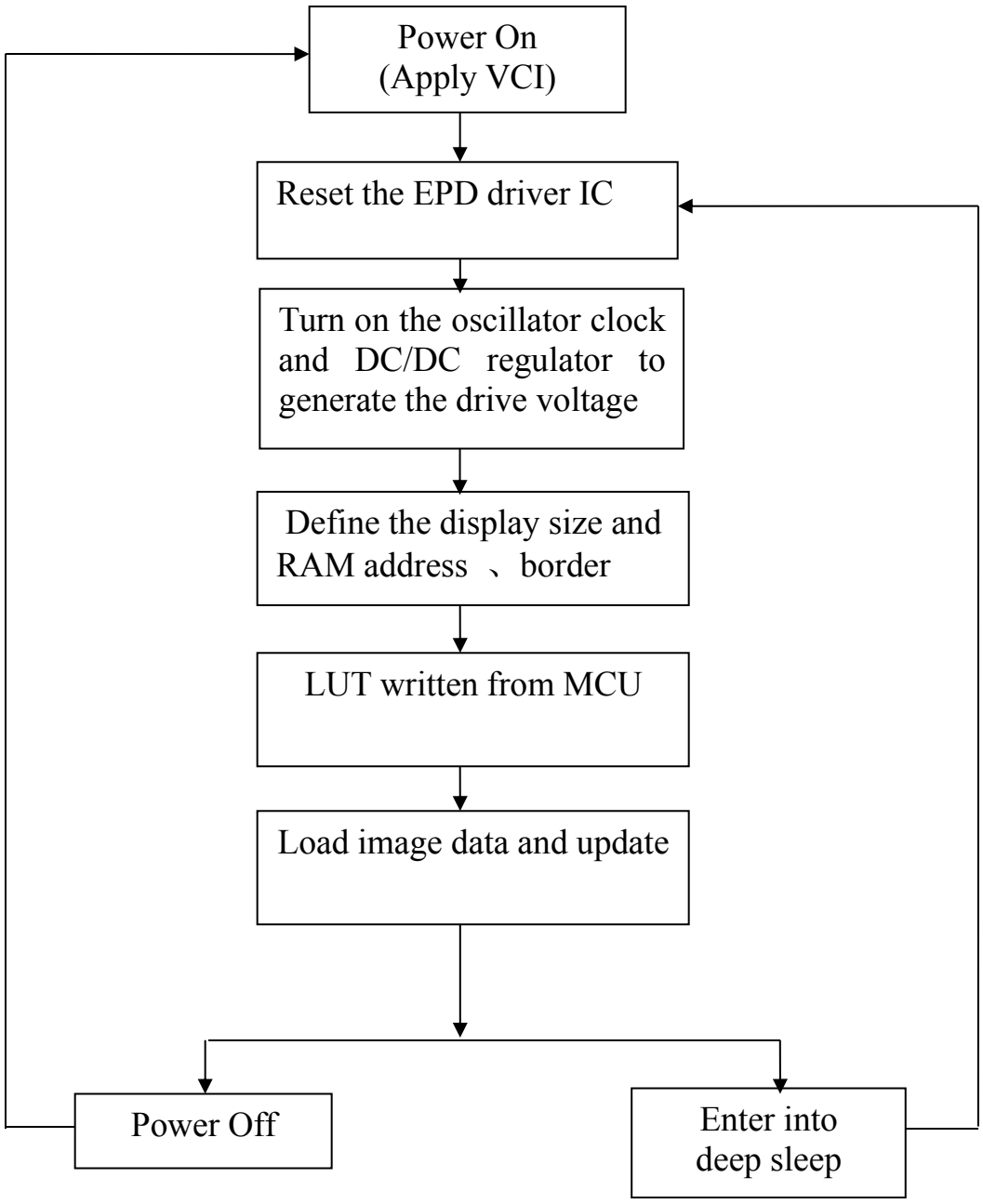


12. Typical Application Circuit with SPI Interface



13 Typical Operating Sequence

13.1Normal Operation Flow



13.2Normal OperationReference Program Code

ACTION	VALUE/DATA	COMMENT
POWER ON		
delay	10ms	
PIN CONFIG		
RESE#	high	Hardware reset
delay	200us	
RESE#	low	
delay	200us	
Read busy pin		Wait for busy low
Command 0x12		Software reset
Read busy pin		Wait for busy low
Command 0x01	Data 0xf9 0x01	Set display size and driver output control
Command 0x11	Data 0x03	Ram data entry mode
Command 0x44	Data 0x00 0x0F	Set Ram X address
Command 0x45	Data 0x00 0XF9	Set Ram Y address
Command 0x3A	Data 0x04	Frame setting 100hz
Command 0x3B	Data 0x04	
Command 0x3C	Data 0x01	Set border
Command 0x2C	Data 0x7B	Set VCOM value
LOAD IMAGE		
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x00	Set Ram Y address counter
Command 0x24	4000bytes	Load B/Wimage (128/8*250)
Command 0x4E	Data 0x00	Set Ram X address counter
Command 0x4F	Data 0x00	Set Ram Y address counter
Command 0x24	4000bytes	Load REDimage (128/8*250)
SET VOLTAGE / LOAD LUT/ UPDATE		
Command 0x03	Data 0x10 0x0A	Gate voltage setting for B/W
Command 0x04	Data 0x19	Source voltage setting for B/W
Command 0x05	Data 0x00	B/W mode
Command 0x32	Write 29bytes LUT for B/W	Load B/W LUT
Command 0x75	Data 0x00 0x00 0x00	B/W mode
Command 0x22	Data 0XC7	Image B/W update
Command 0x20		
Read busy pin		
Command 0x03	Data 0x02 0x0A	Gate voltage setting for RED
Command 0x04	Data 0x36	Source voltage setting for RED
Command 0x05	Data 0xC0	RED mode
Command 0x32	Write 29bytes LUT for B/W	Load RED LUT
Command 0x75	Data 0x00 0x80 0x00	RED mode
Command 0x22	Data 0XC7	Image RED update
Command 0x20		
Read busy pin		
Command 0x10	Data 0X01	Enter deep sleep mode
POWER OFF		

14. Inspection condition

14.1 Environment

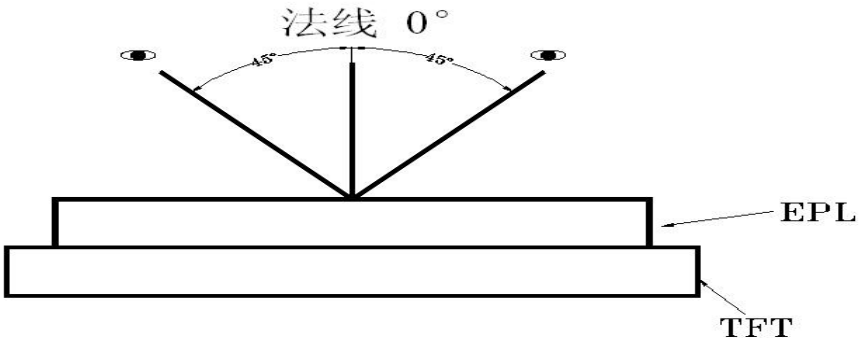
Temperature： 25±3℃

Humidity： 55±10%RH

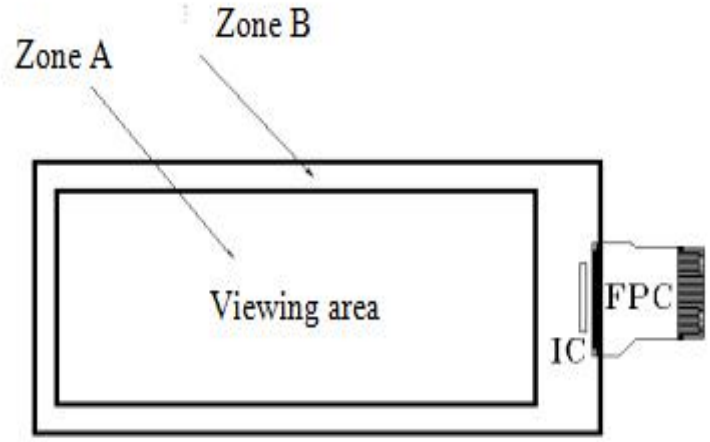
14.2 Illuminance

Brightness:1200～1500LUX;distance:20-30CM;Angle:Relate 30°surround.

14.3 Inspect method

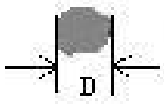
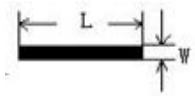


14.4 Display area



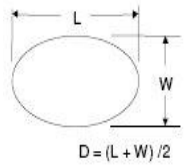
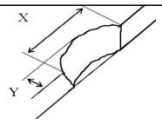
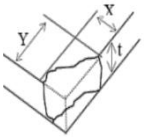
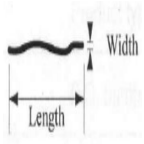
14.5 Inspection standard

14.5.1 Electric inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	Display	Display complete Display uniform	MA	Visual inspection Visual/ Inspection card	Zone A
2	Black/White spots	 D≤0.25mm，Allowed 0.25mm＜D≤0.4mm。N≤3， and Distance≥5mm 0.4mm＜D Not Allow	MI		
3	Black/White spots (No switch)	 L≤0.6mm，W≤0.2mm，N≤1 L≤2.0mm,W＞0.2mm，Not Allow L＞0.6mm，Not Allow			

4	Ghost image	Allowed in switching process	MI	Visual inspection	
5	Flash spots/ Larger FPL size	Flash spots in switching,Allowed FPL size larger than viewing area,Allowed	MI	Visual/ Inspection card	Zone A Zone B
6	Display wrong/Missing	All appointed displays are showed correct	MA	Visual inspection	Zone A
6	Shortcircuit/ Circuit break/ Display abnormal	Not Allow			

14.5.2 Appearance inspection standard

NO.	Item	Standard	Defect level	Method	Scope
1	B/W spots /Bubble/ Foreign bodies/ Dents	 D≤0.25mm，Allowed 0.25mm＜D≤0.4mm，N≤3 D＞0.4mm，Not Allow	MI	Visual inspection	Zone A
2	Glass crack	Not Allow	MA	Visual / Microscope	Zone A Zone B
3	Dirty	Allowed if can be removed	MI		Zone A Zone B
4	Chips/Scratch/ Edge crown	 X≤3mm,Y≤0.5mm  2mm≤X or 2mm≤Y Allow  W≤0.1mm,L≤5mm, n≤ 2 Edge crown：X≤0.3mm，Y≤3mm	MI	Visual / Microscope	Zone A Zone B
5	Substrate color difference	Allowed			
6	FPC broken/ Goldfingers ›xidation/ scratch	  Not Allow	MA	Visual / Microscope	Zone B

7	PCB damaged/ Poor welding/ Curl	PCB（Circuit area）damaged Not Allow PCB Poor welding Not Allow PCB Curl≤1%	MI	Visual / Ruler	Zone B
8	Edge Adhesives height/FPL/ Edge adhesives bubble	Edge Adhesives height≤Display surface Edge adhesives seep in≤1/2 Margin width FPL tolerance ±0.3mm Edge adhesives bubble：bubble Width ≤1/2 Margin width；Length ≤0.5mm。n≤3			
9	Protect film	Surface scratch but not effect protect function, Allow		Visual Inspection	

15.Packaging

EPD PACKING INSTRUCTION

DATE	2016.11.30
DESIGN	
CHECKED	
APPROVED	

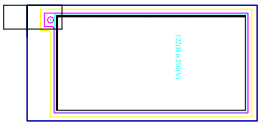
P/N	Customer Code	Ref.P/N
GDEM0213U23		

Type	PKG Method	Printing	Surface Marks	Pull Tape	Bar.Code
GLASS	Blister	BACK	None	YES	None

Marks instruction:

print on the back of the product
Contents: model+Lot#

Pull tape:



Packing Materials List

List	Model	Materials	Q'ty	Unit
Carton	7#	corrugate	1	Piece
BOX	7#(INNER)	corrugate	2	Piece
Blister	GDEM0213U23	PET	22	Piece
Thin foam	301.6*265.73*T1.8-2.0	EPE	20	Piece
Vaccum bag	430.0*590.0*0.075		2	Piece
Foam board	GD2251-10	EPE	4	Piece

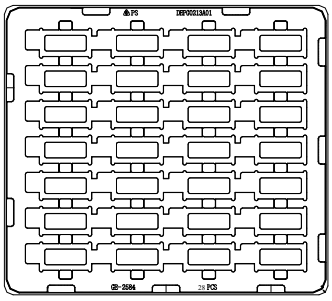
28PCS/LAYER,2 INNER BOX/CTN,TOTAL 560PCS/CTN.

Barcode Instruction:

Detail:

Blister box:

NOTE:
TOTAL 10 LAYERS PER INNER BOX WITH ONE MORE EMPTY BLISTER ON THE TOP OF THE PRODUCTS.



Quantity:4*7=28PCS