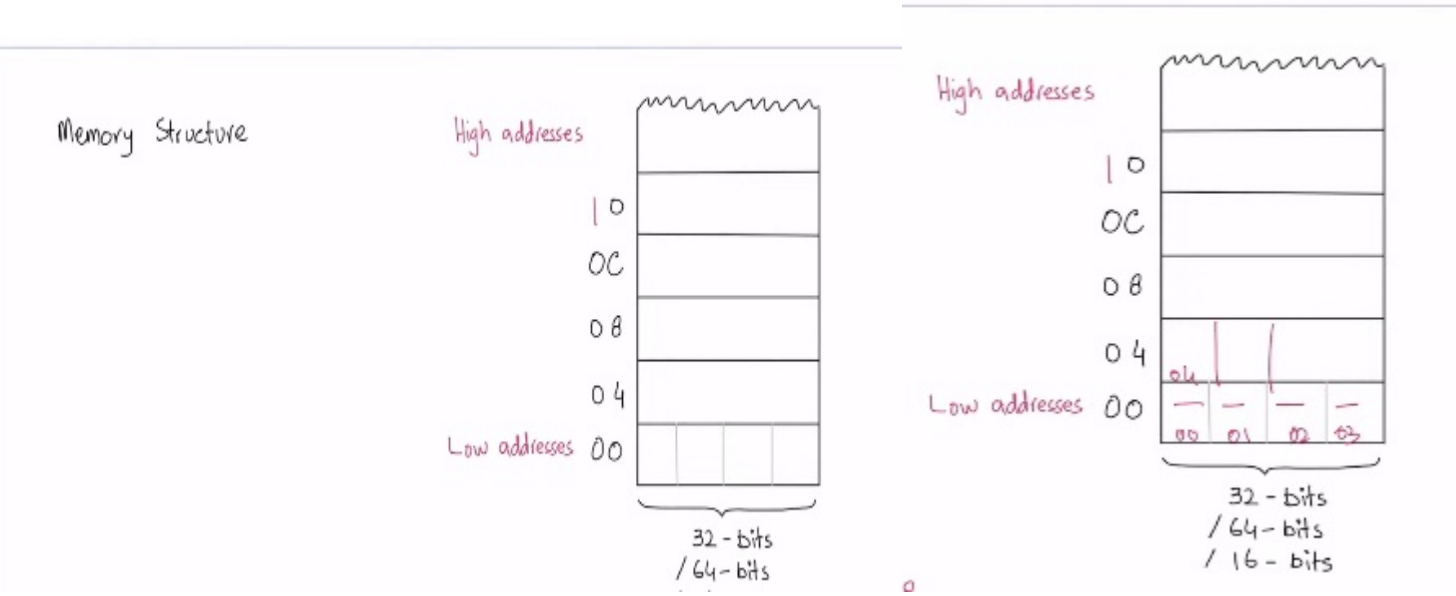
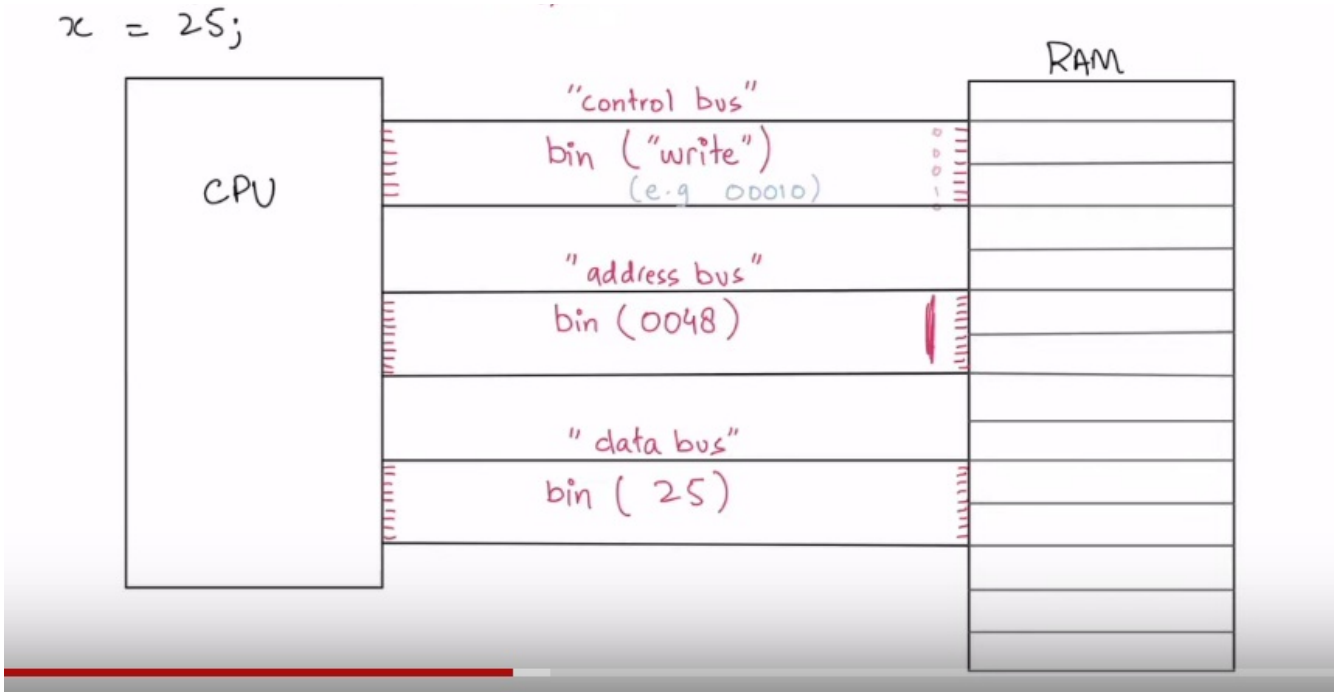
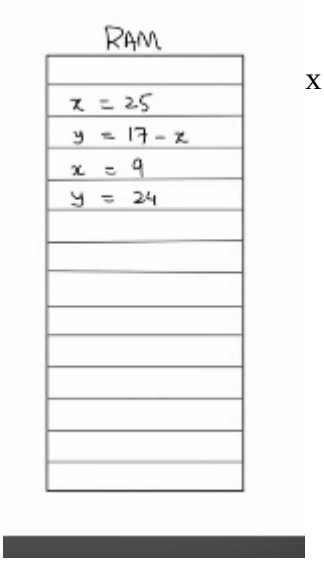
COAL
LECTURE 2



RAM →
LOW ADDRESSES (BELOW) TO HIGH
we split into 4 → 32 bits
8 → 64 bits
2 → 16 bits

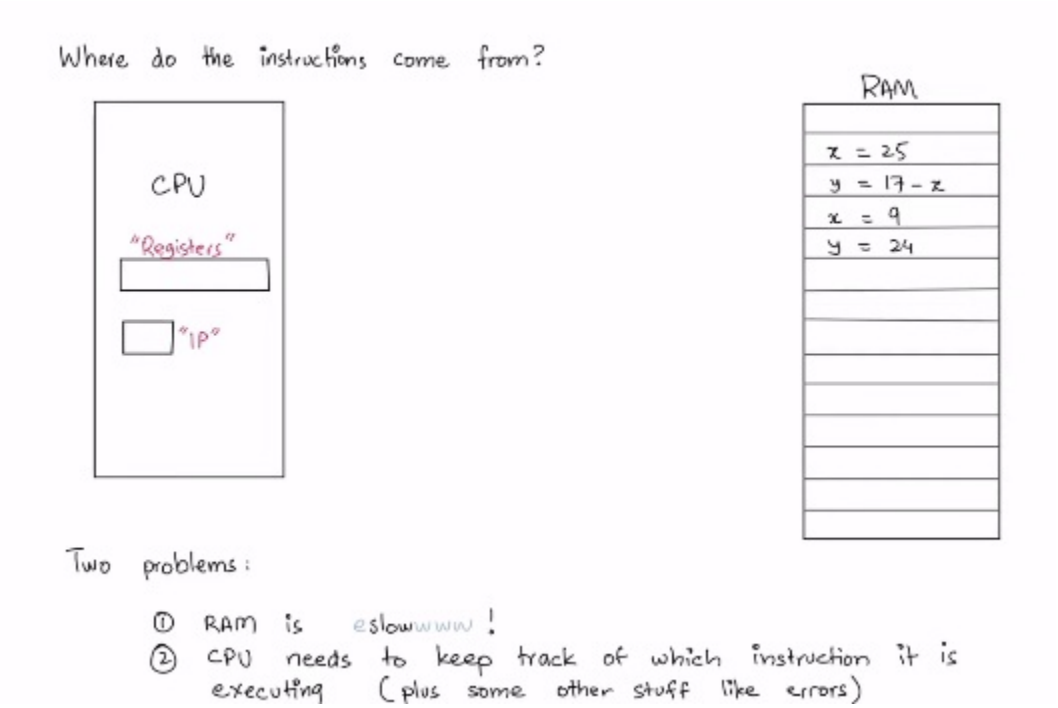


CPU does **three** works
→ first it tells what to read or write on ram (physical wire → contain 32 wires) specific pattern send to ram
→ set of wires contain address (address where to write/from where to read)
→ data (what to write/read)

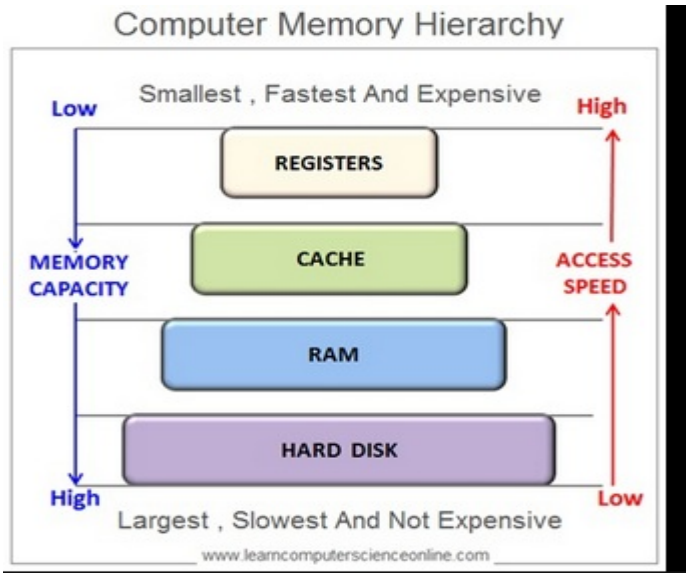


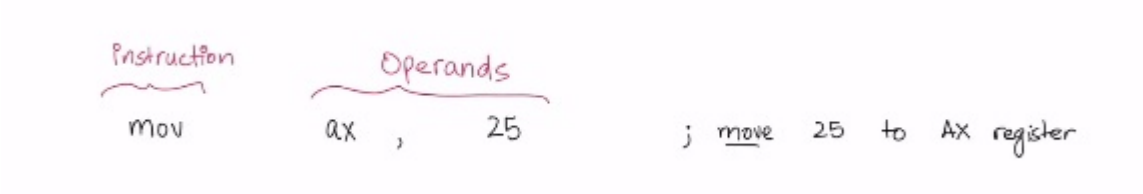
x value will be 25 bcz we see it from low to high

here comes the prob CPU is very fast but everything else is slow

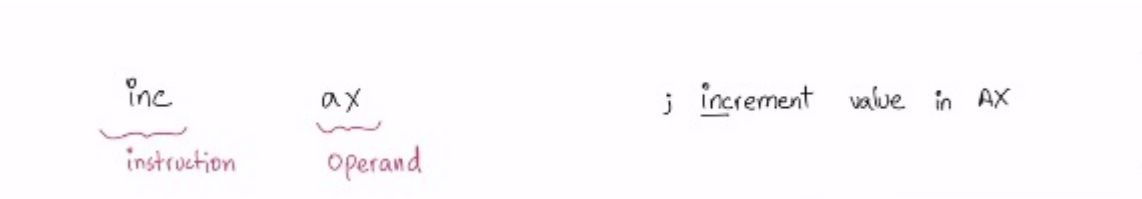


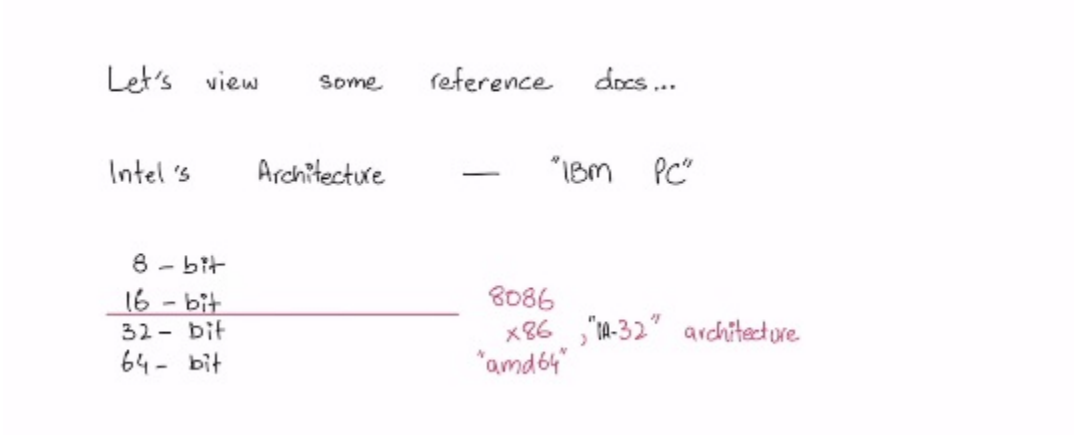
CPU → working area → register(register **stores data and instructions for quick processing**.)
cpu goes to ram → fetch data from ram → decode→ execute



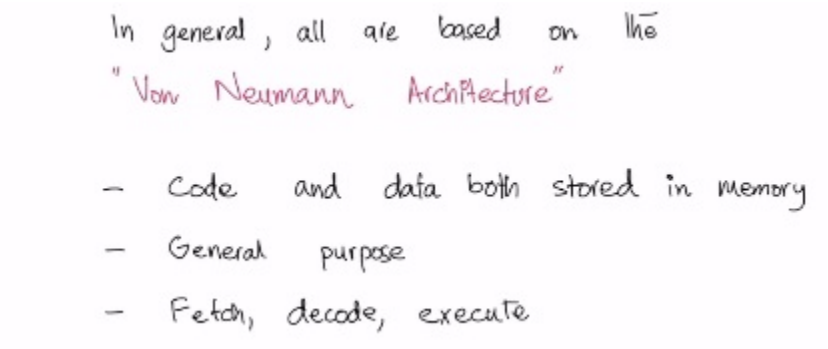


ax is the name of register
→ mov 25 to ax register





machine size depends on the size of accumulator register



intel architecture manual → https://www.intel.com/content/www/us/en/developer/articles/technical/intel-sdm.html
pg -55

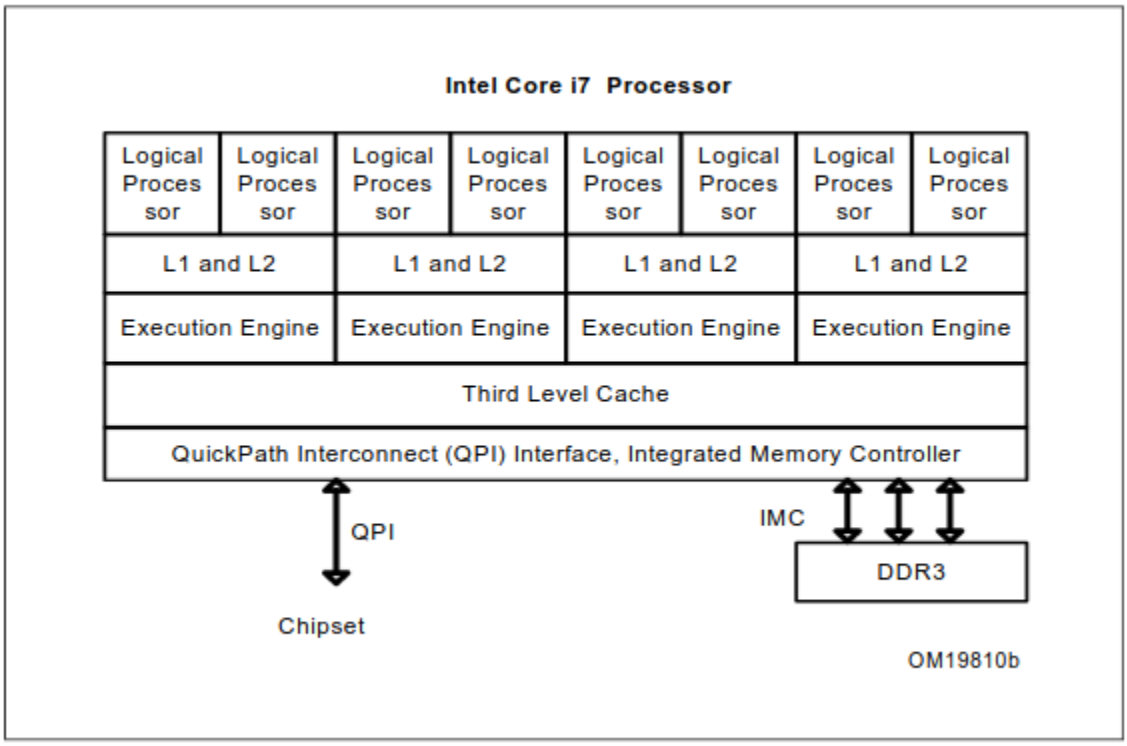


Figure 2-8. Intel® Core™ i7 Processor

DDR 3 → RAM
8 PROCESSORS
L1 AND L2 → CACHE

RAM

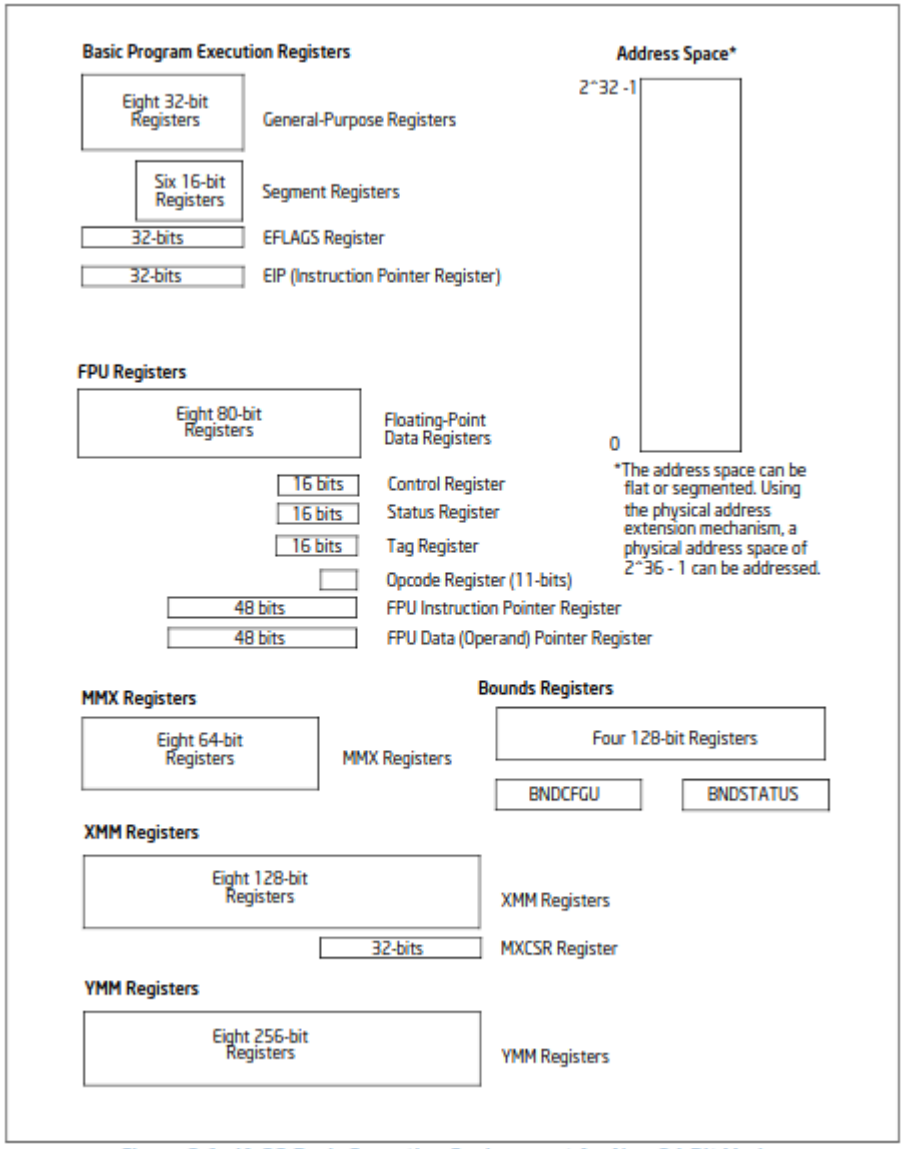


Figure 3-1. IA-32 Basic Execution Environment for Non-64-Bit Modes

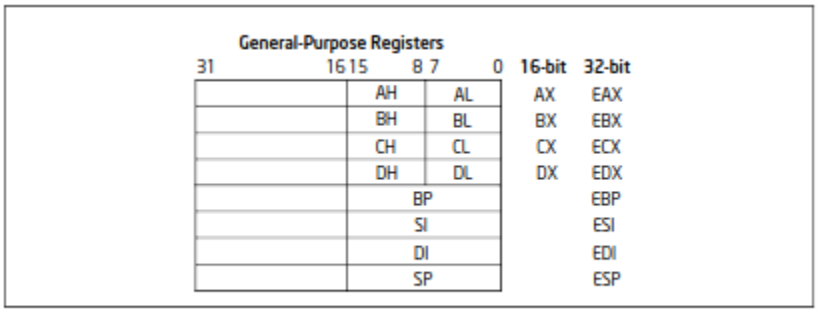


Figure 3-5. Alternate General-Purpose Register Names