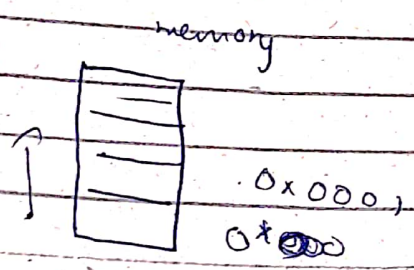
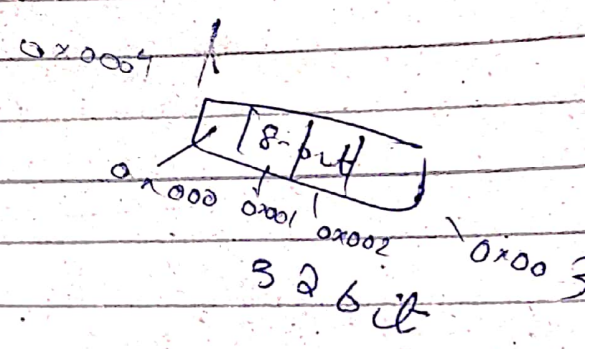
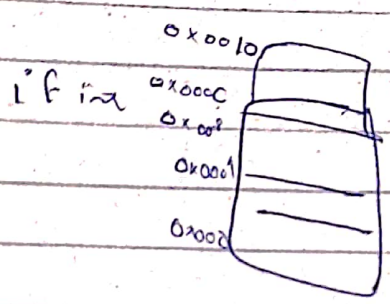




gmac 102



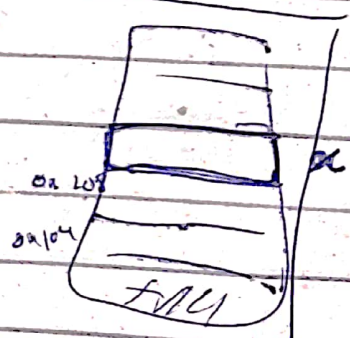
32-bit  
if it is 8 bit  
addressable  
then



- nibble - 4-bit
- byte - 8-bit
- word - 16-bit
- double-word - 32-bit
- quad word - 64-bit

Stack → sequential

```
int x;  
int *p;  
x = 15;  
p = &x;
```



$x = 2^{10} \rightarrow 0 - 1023$   
if negative  
 $-512 \rightarrow -1, 0 - 511$

Van Neumann → Data Code → same memory

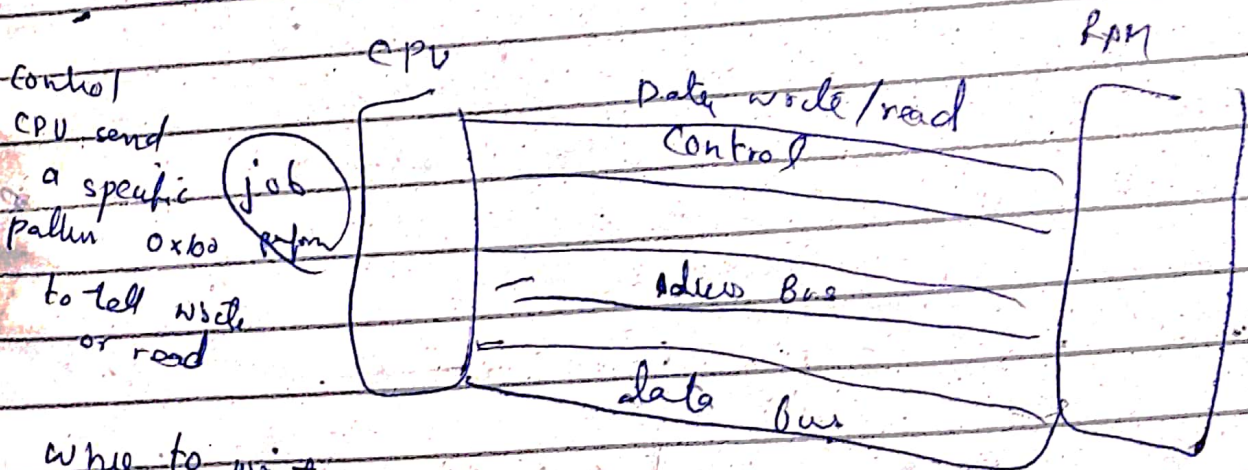
Harvard → code data → separate memory

GPUR  
General  
purpose  
register

SFR  
Specific

Place at the top  
of the memory  
bcz memory  
start from 0 to High

Fetch Decode Execute  
Computation



Control  
CPU send  
a specific  
path 0x60  
to tell write  
or read

job  
from

when to write  
Address bus / memory slots

what data  
data bus



instruction  
operator  
operands  
mnemonic  
mov, inc  
ax, 25; moves 25 into ax register  
ax

max 3 operands

Add ax, bx

destination source

chip  
for  
code

ATmega328P

32KB

[org 0x0100] →

10 wires

2<sup>8</sup> - 1

bit

byte addressable

|                 |
|-----------------|
| GPR             |
| SFR             |
| Heap            |
| Stack           |
| bit addressable |

interrupt  
or  
register

memory

bit  
addressable  
slot

byte  
addressable  
slot

A → Accumulator

B → base

C → count

D →

arithmetic →

accumulator  
register



org → directive

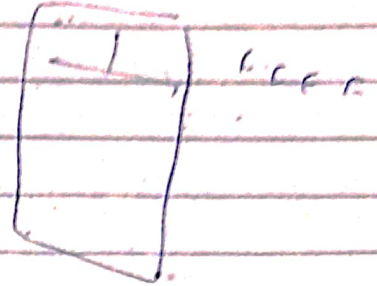
ret → directive

↓

return

Coal

SP FFFC



mov [FFFC], 40000

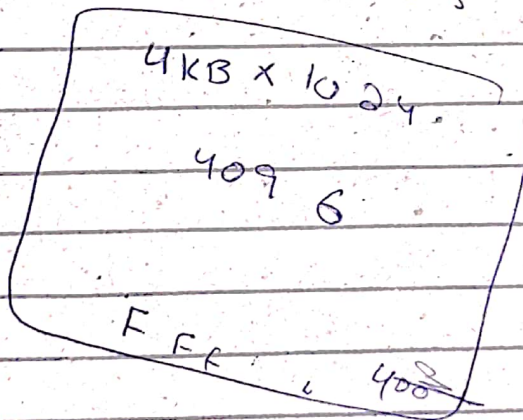
word = 2-byte

$$\frac{65536}{1024} = 64 \text{ kbytes}$$

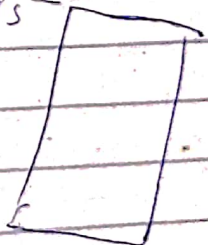
kbytes ←  $2^{16} = 65536$

$$2^8 = 256$$

0 - 255



0xFFFF 4095  
4KB



0000 0000 0000 0000  
16 bits

0000 0000 0000 0000

regular



Flags

7202

