Shafiur Rahman

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Education

University of California, Riverside **Sep 2016 – Present**
PhD Candidate in Computer Science
Research Area: Hardware Accelerators, Parallel Computing, Heterogeneous Architecture
Relevant Courses: Advanced Computer Architecture, GPU Architecture & Programming, Compiler Construction, High Performance Computing, Machine Learning, Artificial Intelligence

Bangladesh University of Engineering and Technology **Mar 2009 – Jun 2014**
B.Sc. in Electrical and Electronics Engineering

Professional Experience

Software Engineer **Jul 2014 – Dec 2015**
Therap Services LLC, Dhaka, Bangladesh
Responsibilities: Developing test automation frameworks, Test scripts, Load testing

Selected Publications

- **Incremental Graph Processing Accelerator using an Event-Driven Approach**
  Shafiur Rahman, Nael Abu-Ghazaleh, Rajiv Gupta *[Under Revision]*
- **PDES-A: Accelerators for Parallel Discrete Event Simulation implemented on FPGAs**
  Shafiur Rahman, Nael Abu-Ghazaleh, Walid Najjar; ACM Transactions on Modeling and Computer Simulation, Volume 29 Issue 2, April 2019. *[Invited paper]*
- **PDES-A: a Parallel Discrete Event Simulation Accelerator for FPGAs**
  Shafiur Rahman, Nael Abu-Ghazaleh, Walid Najjar; ACM SIGSIM Conference on Principles of Advanced Discrete Simulation (PADS), 2017. *[Best paper nominee]*
- **A Template Matching Approach of One-Shot-Learning Gesture Recognition**
  Upal Mahbub, Hafiz Imtiaz, Tonmoy Roy, Shafiur Rahman, Md Atiqur Rahman Ahad; Pattern Recognition Letters, Elsevier, Nov. 2013.
- **One-Shot-Learning Gesture Recognition Using Motion History Based Gesture Silhouettes**
  Upal Mahbub, Tonmoy Roy, Shafiur Rahman, Hafiz Imtiaz, Seiichi Serikawa, Md Atiqur Rahman Ahad; International Conference on Industrial Application Engineering, 2013.

Selected Projects

Event-Driven Graph Processing Framework:

- Developed an event-driven processing model to support graph processing algorithms.
- Designed a hardware accelerator architecture for scalable and optimized event-driven graph processing on FPGA and ASIC.
- Developed an MPI-driven cycle-accurate hardware simulator on top of Structural Simulation Toolkit (SST) for fast prototyping and scalability analysis of the framework on large graphs.

Parallel Discrete Events Simulation Accelerator:

- Designed a generalized and modular architectural framework for fast development of Parallel Discrete Events Simulators on reconfigurable platforms.
- Implemeted the framework using Verilog and Chisel on a Convey Wolverine Coprocessor.

One-shot Gesture Recognition:

- Developed novel algorithms for detection of individual gestures from video with depth data.
- Extracted and characterized distinguishing features from motion-history-image of a gesture.
- Developed algorithms for real-time gesture recognition using one-shot learning techniques.

Technical Skills

- **Programming Languages & APIs:** C, C++, Python, Scala, MATLAB, CUDA
- **Hardware Design & Verification:** Verilog HDL, Chisel, ModelSim, Xilinx Vivado
- **Simulation Platforms:** Structural Simulation Toolkit (SST), Gem5

Awards and Honors

- **Dean's Distinguished Fellowship**, University of California, Riverside (2015–2016)
- **Winner of Cadence Design Contest 2014 – Tensilica Design Project**, Cadence Design Systems India Ltd.