Shafiur Rahman

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Education

University of California, Riverside **Sep 2016 – Sep 2021**
PhD in Computer Science
MS in Computer Science
Research Area: Hardware Accelerators, Parallel Computing, Heterogeneous Architecture

Bangladesh University of Engineering and Technology **Mar 2009 – Jun 2014**
BS in Electrical and Electronic Engineering

Professional Experiences

Research Scientist **Oct 2021 – Present**
Facebook, System Infrastructure. Menlo Park, CA.

Software Engineering Intern **Apr 2021 – Sep 2021**
Micron Technology, Advanced Computing and Emerging Memory Systems Group. Allen, TX.
Project: Developed and profiled simulators for near-memory computing architectures.

Hardware Engineering Intern **Jun 2020 – Aug 2020**
Western Digital Research, Platforms and Systems Concepts. Milpitas, CA.
Project: Developed RTL components for a prototype Fast-CNN accelerator

Software Engineer **Jul 2014 – Dec 2015**
Therap Services LLC, Dhaka, Bangladesh.
Responsibilities: Developing test automation framework with Selenium, Load testing

Selected Research Projects

Event-Driven Graph Processing Framework:

- Developed an event-driven processing model to support graph processing algorithms.
- Designed an accelerator architecture for scalable and optimized graph processing on FPGA and ASIC.
- Developed an MPI-driven cycle-accurate hardware simulator on top of Structural Simulation Toolkit (SST) for fast prototyping and scalability analysis of the framework on large graphs.

Parallel Discrete Events Simulation Accelerator:

- Designed a generalized and modular architectural framework for fast development of Parallel Discrete Events Simulators on reconfigurable platforms.
- Implemented the framework for FPGA using Verilog and Chisel on a Convey Wolverine Coprocessor.

One-shot Gesture Recognition:

- Extracted and characterized distinguishing features from motion-history-image of a gesture.
- Developed algorithms for real-time gesture recognition using one-shot learning techniques.

Selected Publications

- **JetStream: Graph Analytics on Streaming Data with Event-Driven Hardware Accelerator**
  Shafiur Rahman, Mahabod Afarin, Nael Abu-Ghazaleh, Rajiv Gupta; International Symposium on Microarchitecture, October 2021.
- **GraphPulse: An Event-Driven Hardware Accelerator for Asynchronous Graph Processing**
  Shafiur Rahman, Nael Abu-Ghazaleh, Rajiv Gupta; International Symposium on Microarchitecture, 2020.
- **BOW: Breathing Operand Windows to Exploit Bypassing in GPUs**
  Hodjat Asghari Esfeden, Amirali Abdolrashidi, Shafiur Rahman, Daniel Wong, Nael Abu-Ghazaleh; International Symposium on Microarchitecture, October 2020.
- **PDES-A: a Parallel Discrete Event Simulation Accelerator for FPGAs**
  Shafiur Rahman, Nael Abu-Ghazaleh, Walid Najjar; ACM SIGSIM Conference on Principles of Advanced Discrete Simulation (PADS), 2017. *[Best paper nominee]*
- **A Template Matching Approach of One-Shot-Learning Gesture Recognition**
  Upal Mahbub, Hafiz Imtiaz, Tonmoy Roy, Shafiur Rahman, Md Atiqur Rahman Ahad; Pattern Recognition Letters, Elsevier, Nov. 2013.

Technical Skills

- **Programming Languages & APIs:** C, C++, Python, MATLAB, CUDA
- **Hardware Design & Verification:** Verilog HDL, Chisel, ModelSim, Xilinx Vivado