Shafiur Rahman

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Education

University of California, Riverside **Sep 2016 – Sep 2021**
PhD in Computer Science *Riverside, CA*
MS in Computer Science
Dissertation: *Hardware Acceleration of Irregular Applications Using Event-Driven Execution.*
Specialization: Parallel Computing, Distributed Systems, High Performance Computing, Graph Processing, Computer Architecture, Hardware Accelerators.

Bangladesh University of Engineering and Technology **Mar 2009 – Jun 2014**
BS in Electrical and Electronic Engineering *Dhaka, Bangladesh*

Professional Experiences

Meta **Oct 2021 – Nov 2022**
Research Scientist (Software Engineering), Video Infrastructure *Menlo Park, CA*

- Worked in the development and maintenance of a multi-tenant compute farm for video transcoding.
- Built micro-services in C++ for video transformation and transcoding using FFmpeg.
- Worked with containerized execution of services in a large-scale distributed system.
- Contributed to the design and implementation of service APIs (C++ and PHP).
- Carried out performance profiling and load testing for reliability analysis and disaster recovery.
- Collaborated with cross-functional teams and internal clients for defining specifications and roadmaps.

Micron Technology **Apr 2021 – Sep 2021**
Software Engineering Intern, Advanced Computing and Emerging Memory Systems. *Allen, TX*

- Built cycle-accurate simulators in C++ for modeling x86 processor and near-memory compute architectures.
- Worked closely with processor architecture and operating system kernel for simulator implementation.
- Implemented cache coherence and data prefetching capabilities for the cycle-accurate simulators.
- Micro-architectural performance profiling (perf-tools) of x86 processors to validate simulator performance.

Western Digital Research **Jun 2020 – Aug 2020**
Next Generation Technology Intern, Platforms and Systems Concepts. *Milpitas, CA*

- Designed modules from specification for a prototype Neural Network (Fast-CNN) hardware accelerator.
- Profiled and analyzed common CNN architectures for guiding accelerator design.

Therap Services LLC **Jul 2014 – Dec 2015**
Software Engineer *Dhaka, Bangladesh*

- Developed test automation and load testing framework with Ruby and Selenium Webdriver.

Selected Research Project

Event-Driven Graph Processing Framework

- Developed an event-driven processing model to support graph algorithms efficiently in hardware.
- Designed an accelerator architecture for scalable and optimized graph processing on FPGA and ASIC.
- Developed an MPI-driven cycle-accurate hardware simulator using Structural Simulation Toolkit (SST) framework for fast prototyping and scalability analysis of the architecture on large graphs.

Technical Skills

- **Programming Languages:** C, C++, Python, MATLAB
- **Programming Frameworks**: CUDA, MPI for parallel computing.