INTEGRATED CIRCUITS

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT00Quad 2-input NAND gate

Product specification
File under Integrated Circuits, IC06

December 1990





Quad 2-input NAND gate

74HC/HCT00

FEATURES

· Output capability: standard

I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT00 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT00 provide the 2-input NAND function.

QUICK REFERENCE DATA

 $GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns$

SYMBOL	PARAMETER	CONDITIONS	TYI	UNIT		
SYMBOL	PARAWETER	CONDITIONS	нс	нст	UNII	
t _{PHL} / t _{PLH}	propagation delay nA, nB to nY	$C_L = 15 \text{ pF}; V_{CC} = 5 \text{ V}$	7	10	ns	
C _I	input capacitance		3.5	3.5	pF	
C _{PD}	power dissipation capacitance per gate	notes 1 and 2	22	22	pF	

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:

 f_i = input frequency in MHz

 f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

$$\Sigma (C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs}$$

2. For HC the condition is V_I = GND to V_{CC} For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

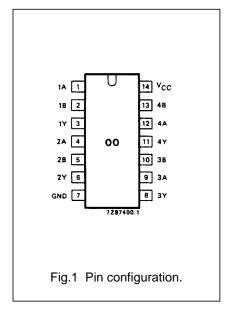
See "74HC/HCT/HCU/HCMOS Logic Package Information".

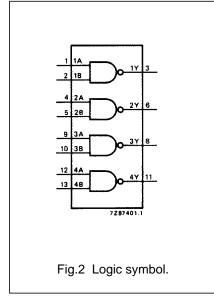
Quad 2-input NAND gate

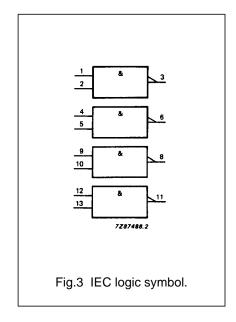
74HC/HCT00

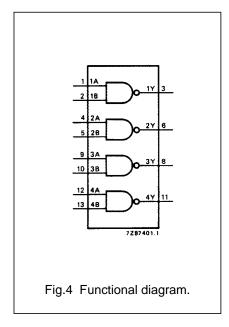
PIN DESCRIPTION

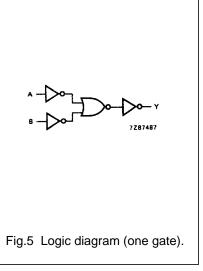
PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V _{CC}	positive supply voltage











FUNCTION TABLE

INP	OUTPUT			
nA	nY			
L	L	Н		
L	Н	Н		
H	L	Н		
Н	Н	L		

Note

H = HIGH voltage level
 L = LOW voltage level

Quad 2-input NAND gate

74HC/HCT00

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

I_{CC} category: SSI

AC CHARACTERISTICS FOR 74HC

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

SYMBOL	PARAMETER	T _{amb} (°C)								TEST CONDITIONS	
		74HC									
		+25			−40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS
		min.	typ.	max.	min.	max.	min.	max.		(3)	
t _{PHL} / t _{PLH}	propagation delay nA, nB to nY		25 9 7	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.6
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "74HC/HCT/HCU/HCMOS Logic Family Specifications".

Output capability: standard

 I_{CC} category: SSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nA, nB	1.50

AC CHARACTERISTICS FOR 74HCT

 $GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF$

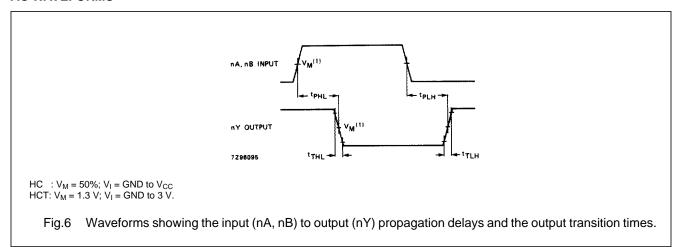
SYMBOL	PARAMETER	T _{amb} (°C)							LIMIT	TEST CONDITIONS	
		74HCT									
		+25		-40 to +85		-40 to +125		UNIT	V _{CC} (V)	WAVEFORMS	
		min.	typ.	max.	min.	max.	min.	max.		(1)	
t _{PHL} / t _{PLH}	propagation delay nA, nB to nY		12	19		24		29	ns	4.5	Fig.6
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6

Philips Semiconductors Product specification

Quad 2-input NAND gate

74HC/HCT00

AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".