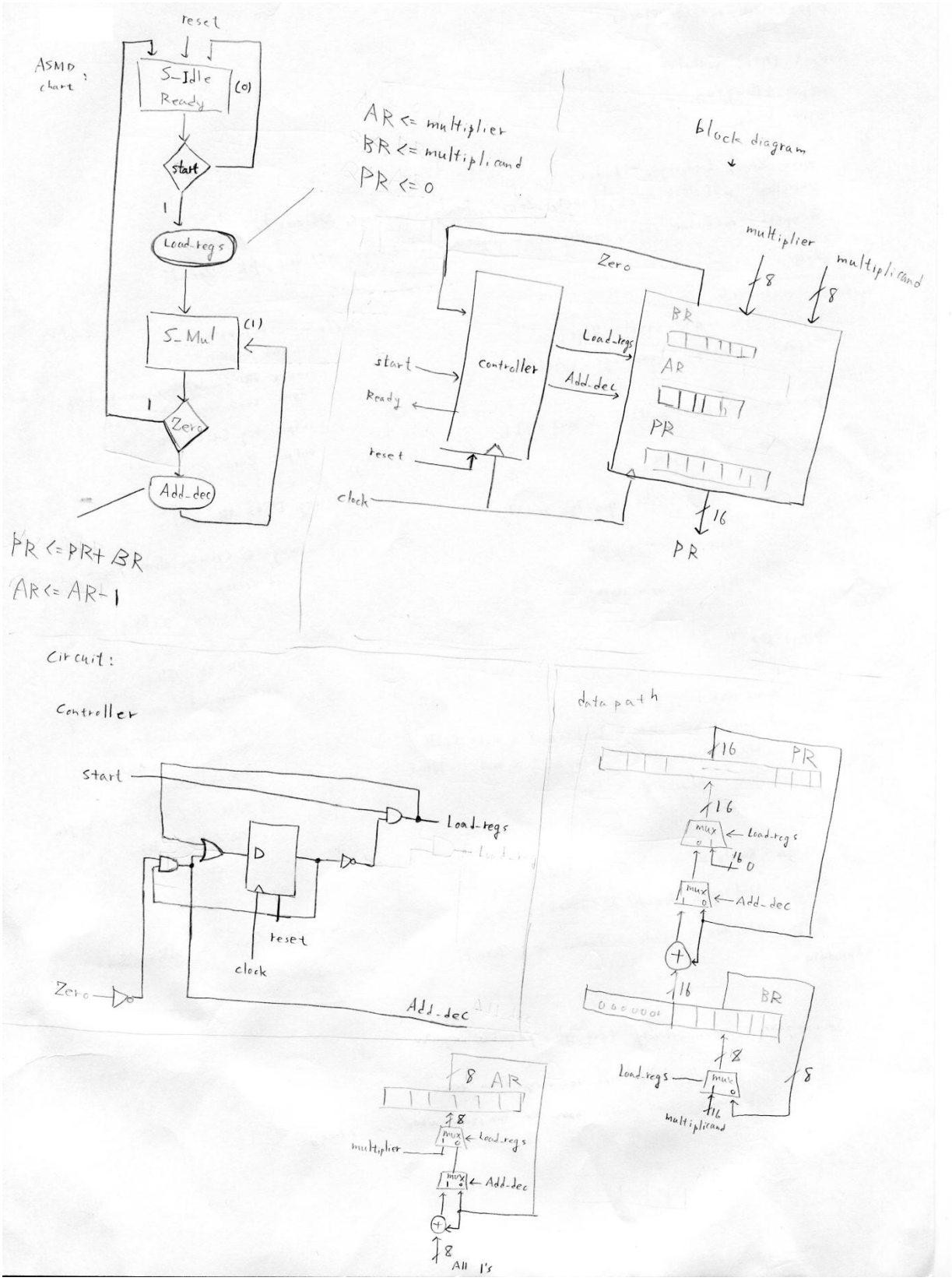
Dlab Homework 1

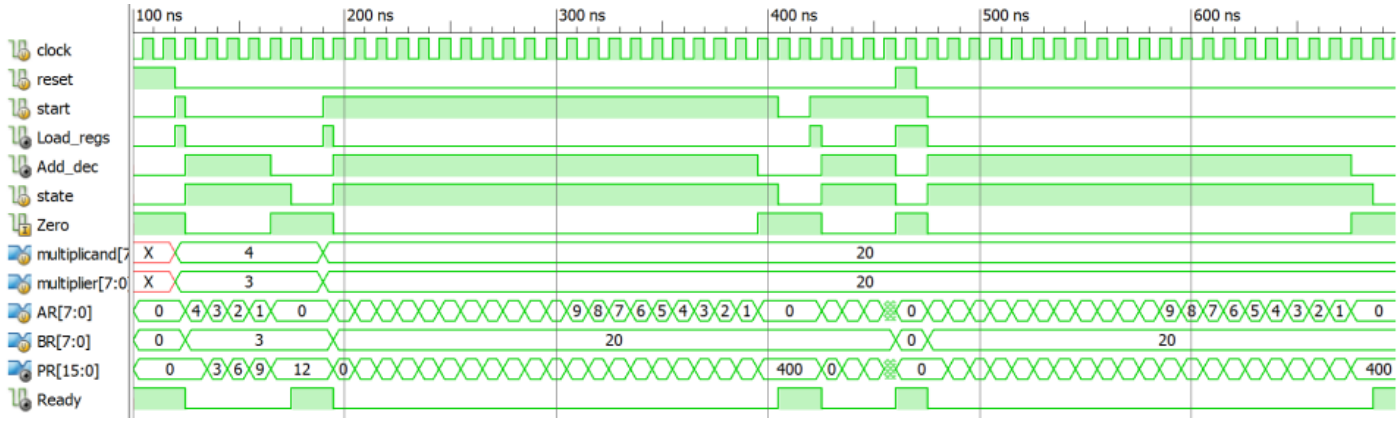
8.16



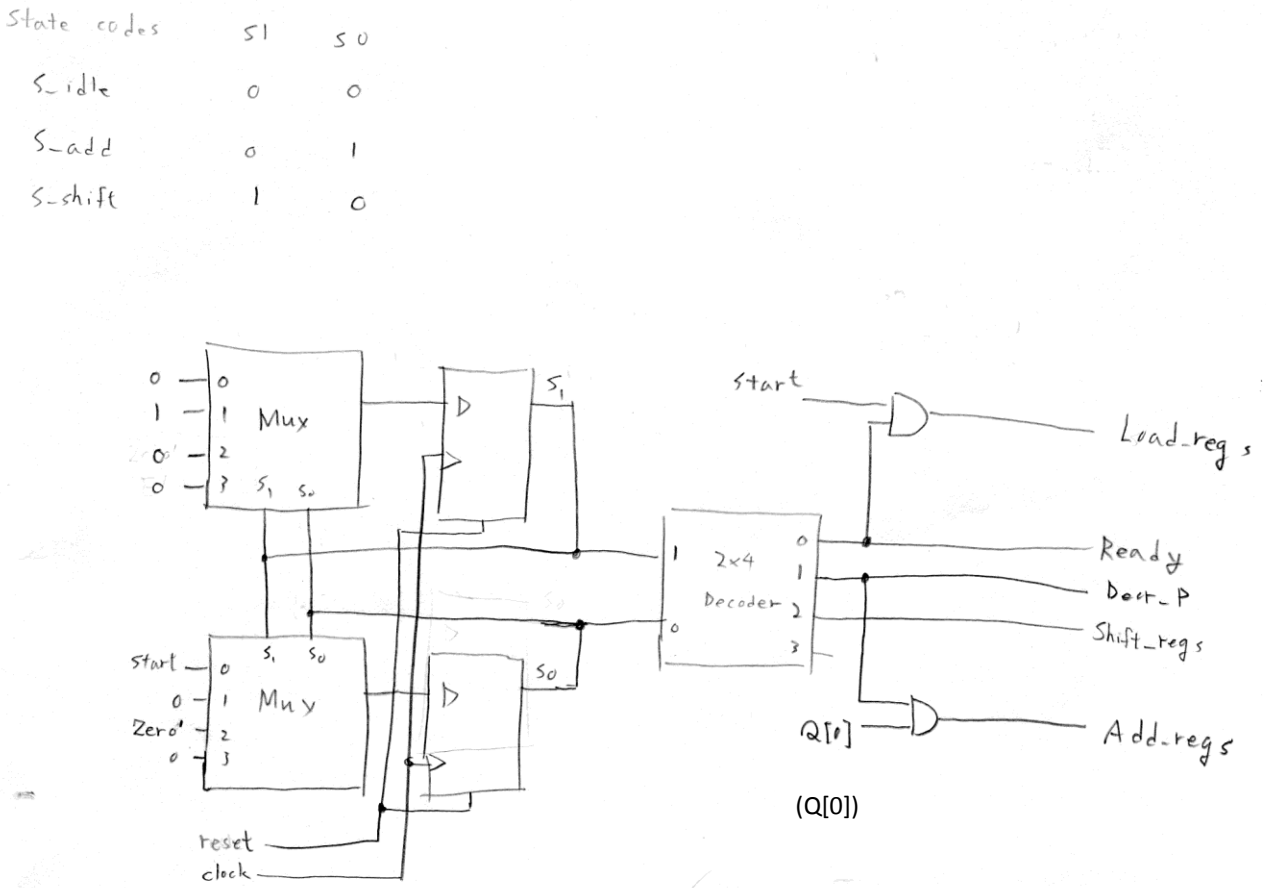
The Verlilog behavioral model is included in **multiply.v** (three modules in one file.)

The testbench is **t_multiply.v**, it tests the recovery from reset, verifies that start have no function when not ready and exhaustively tests all combinations of inputs.

Partial simulation results:



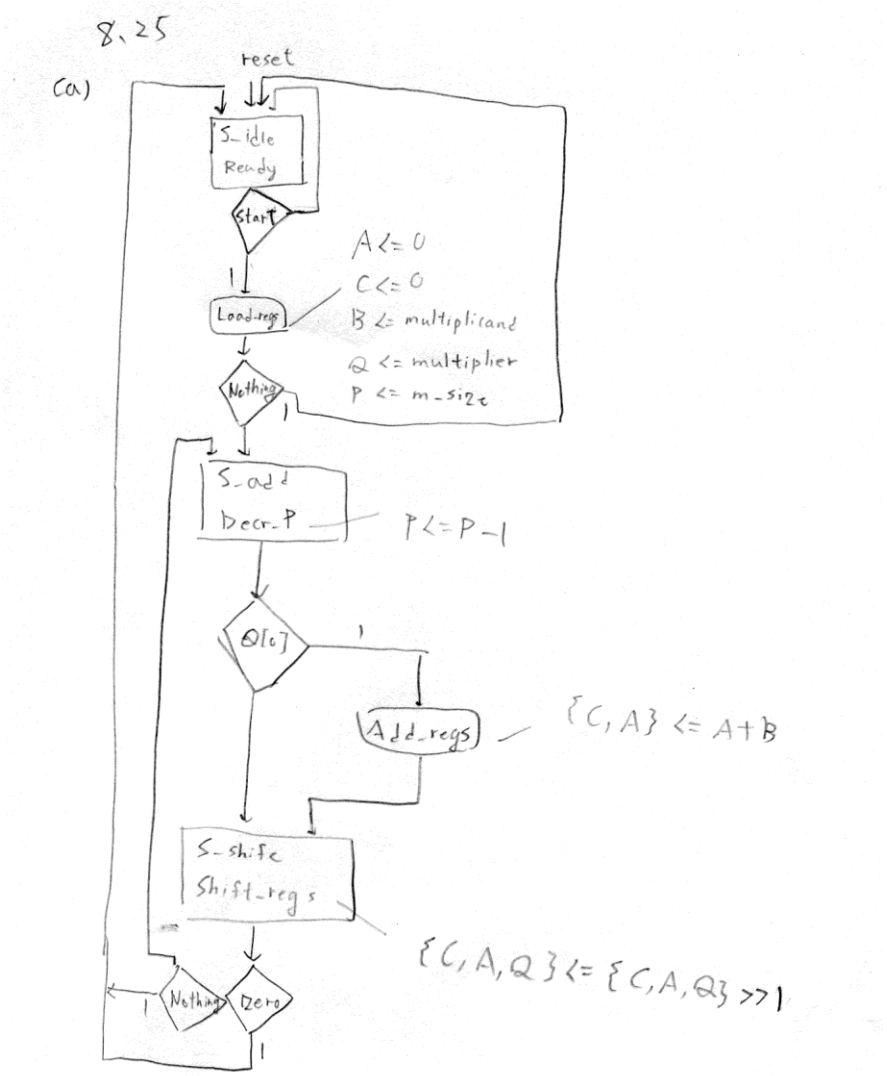
8.21



(Q[0])

8.25

(a)



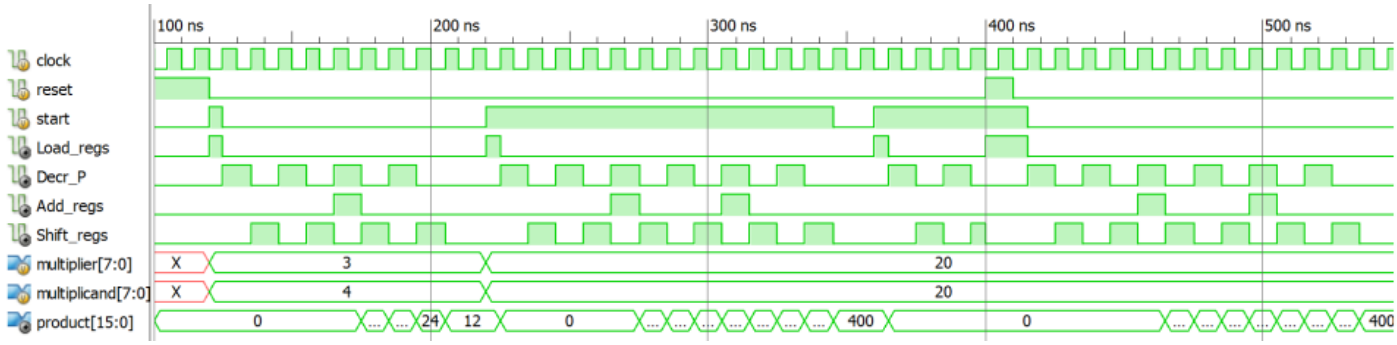
(b)

The Verlilog behavioral model is included in **binary_multiplier.v** (three modules in one file.)

(c)

The testbench is **t_binary_multiplier.v**, it tests the recovery from reset, verifies that start have no function when not ready, checks that the operation does terminates early and exhaustively tests all combinations of inputs.

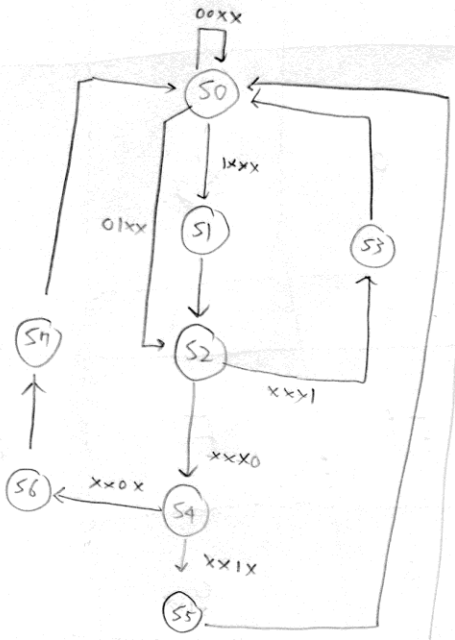
Partial simulation results:



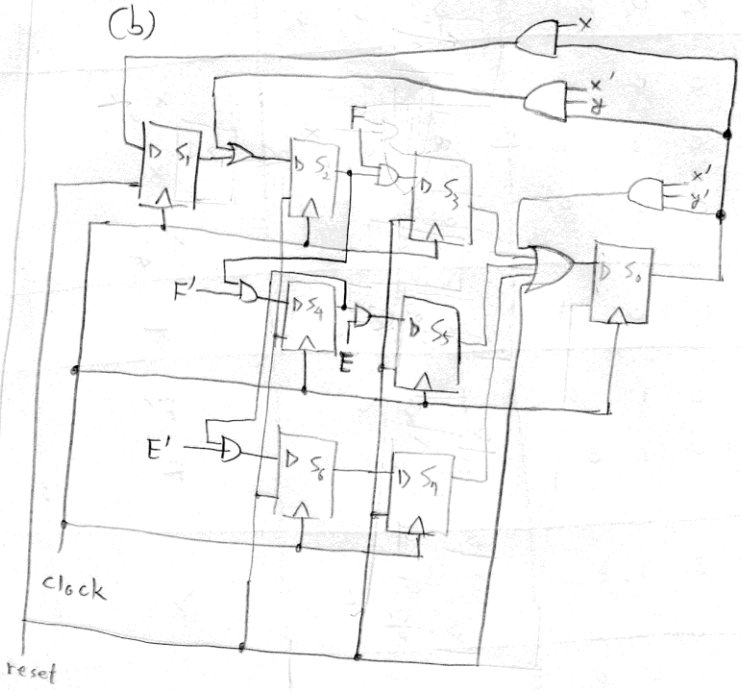
8.29

(a)

Inputs: xyEF



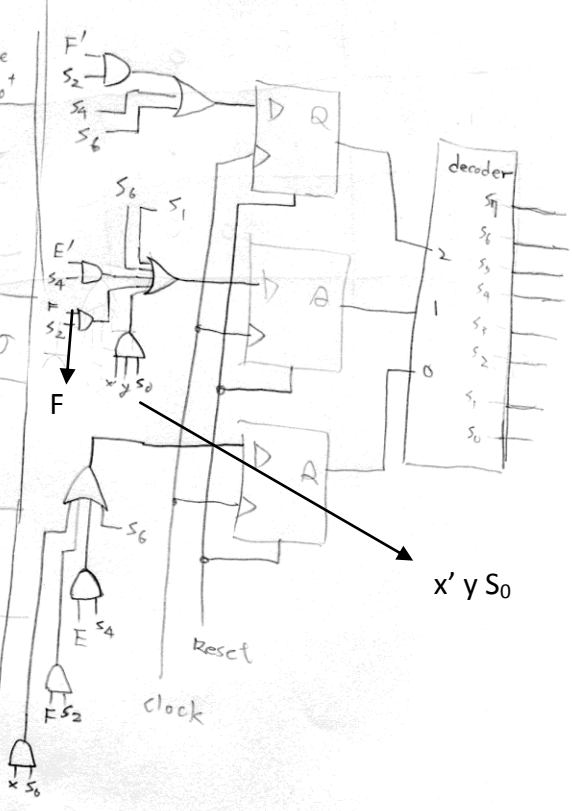
(b)



(c) by using three flip flops

Output	Present state D_2 D_1 D_0	Inputs x	y	E	F	Next state D_2^+ D_1^+ D_0^+
S_0	0 0 0	0	0	x	x	0 0 0
	0 0 0	1	x	x	x	0 0 1
	0 0 0	0	1	x	x	0 1 0
S_1	0 0 1	x	x	x	x	0 1 0
S_2	0 1 0	x	x	x	0	1 0 0
	0 1 0	x	x	x	1	0 1 1
S_3	0 1 1	x	x	x	x	0 0 0
S_4	1 0 0	x	x	0	x	1 1 0
	1 0 0	x	x	1	x	1 0 1
S_5	1 0 1	x	x	x	x	0 0 0
S_6	1 1 0	x	x	x	x	1 1 1
S_7	1 1 1	x	x	x	x	0 0 0

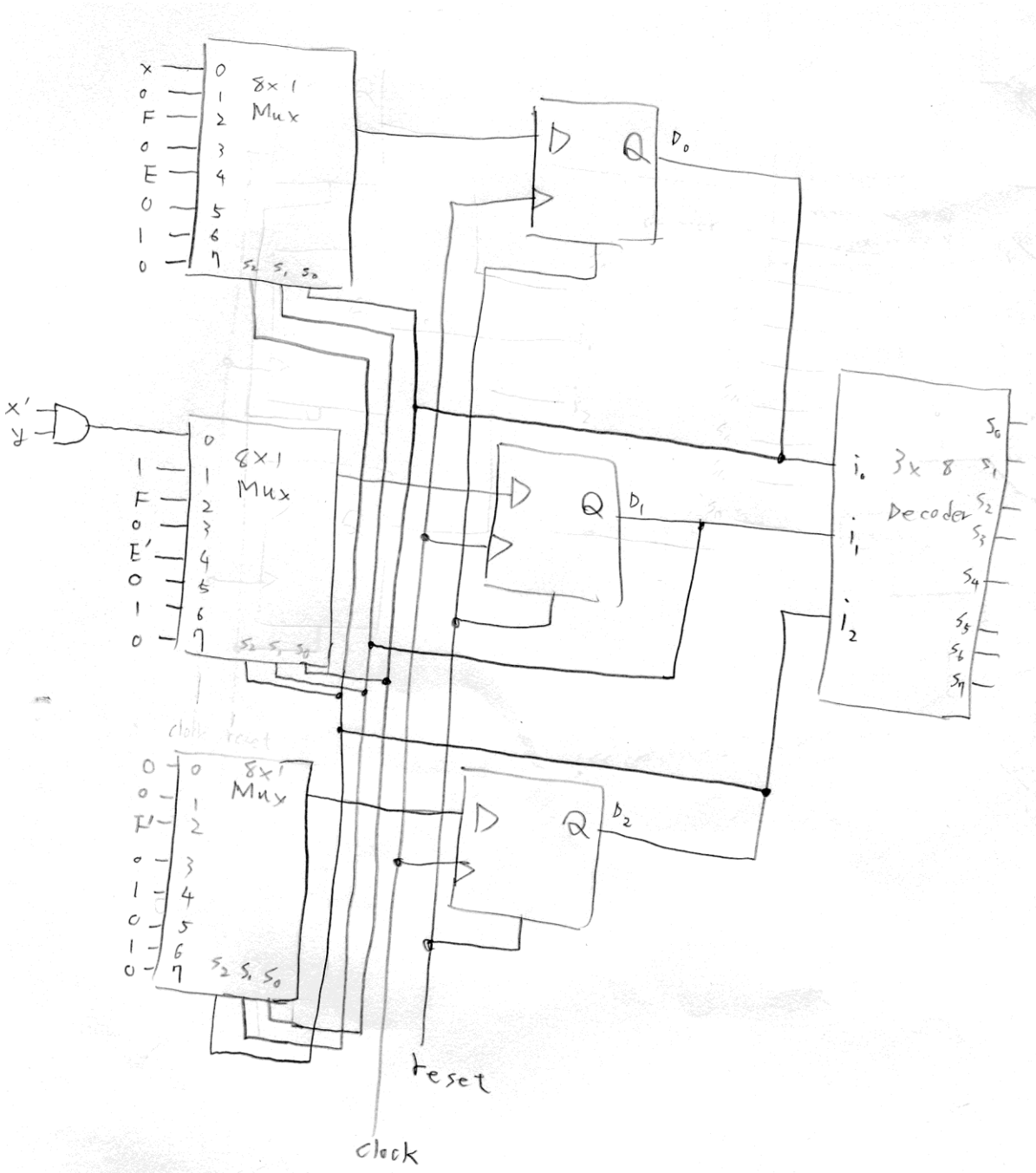
(d)



(e)

Present State			Next State			Input Conditions	Mux2	Mux1	Mux0
D_2	D_1	D_0	D_2^+	D_1^+	D_0^+				
0	0	0	0	0	0	x'y'	0	x'y	x
0	0	0	0	0	1	x			
0	0	0	0	1	0	x'y			
0	0	1	0	1	0	-	0	1	0
0	1	0	1	0	0	F'	F'	F	F
0	1	0	0	1	1	F			
0	1	1	0	0	0	-	0	0	0
1	0	0	1	1	0	E'	1	E'	E
1	0	0	1	0	1	E			
1	0	1	0	0	0	-	0	0	0
1	1	0	1	1	1	-	1	1	1
1	1	1	0	0	0	-	0	0	0

(f)

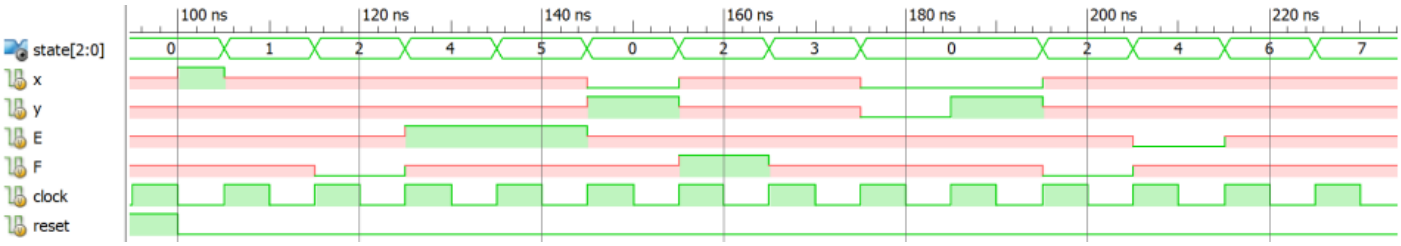

8x1 Mux
D0
D1
D2
3x 8 Decoder
S0
S1
S2
S3
S4
S5
S6
S7
i0
i1
i2
x'
y
E'
F
E
reset
clock

(g)

The Verlilog structural model is included in **controller_struct_29.v**.

The testbench is **t_ controller_struct_29.v** with **t_ controller_struct_29_comp.v**, it tests all the state transitions.

Simulation results:



(h)

The Verlilog structural model is included in **controller_rtl_29.v**.

The testbench is **t_ controller_rtl_29.v**, it tests all the state transitions.

Simulation results (identical with g):