Fully Integrated, Hall Effect-Based Linear Current Sensor IC with 3 kVRMS Voltage Isolation and a Low-Resistance Current Conductor

Features and Benefits

- Industry-leading noise performance through proprietary amplifier and filter design techniques
- Total output error 0.8% at T_A = 25°C
- Small package size, with easy mounting capability
- Monolithic Hall IC for high reliability
- Ultra-low power loss: 130 µΩ internal conductor resistance
- 3 kV_{RMS} minimum isolation voltage from pins 1-3 to pins 4-5
- 3.0 to 5.0 V, single supply operation
- 3 µs output rise time in response to step input current
- 20 or 40 mV/A output sensitivity
- Output voltage proportional to AC or DC currents
- Factory-trimmed for accuracy
- Extremely stable output offset voltage
- Nearly zero magnetic hysteresis

TÜV America
Certificate Number:
U8V 09 05 54214 021

Package: 5 pin package (suffix PFF)

Additional leadforms available for qualifying volumes

Description

The Allegro ACS756 family of current sensor ICs provides economical and precise solutions for AC or DC current sensing in industrial, automotive, commercial, and communications systems. The device package allows for easy implementation by the customer. Typical applications include motor control, load detection and management, power supplies, and overcurrent fault protection.

The device consists of a precision, low-offset linear Hall circuit with a copper conduction path located near the die. Applied current flowing through this copper conduction path generates a magnetic field which the Hall IC converts into a proportional voltage. Device accuracy is optimized through the close proximity of the magnetic signal to the Hall transducer. A precise, proportional voltage is provided by the low-offset, chopper-stabilized BiCMOS Hall IC, which is programmed for accuracy at the factory.

The output of the device has a positive slope (>V_{CC}/2) when an increasing current flows through the primary copper conduction path (from terminal 4 to terminal 5), which is the path used for current sampling. The internal resistance of this conductive path is 130 µΩ typical, providing low power loss.

The thickness of the copper conductor allows survival of the device at up to 5× overcurrent conditions. The terminals of the

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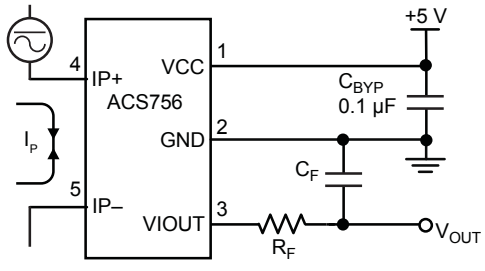
Typical Application



Application 1. The ACS756 outputs an analog signal, V_{OUT}, that varies linearly with the uni- or bi-directional AC or DC primary sampled current, I_P, within the range specified. C_F is for optimal noise management, with values that depend on the application.

Description (continued)

conductive path are electrically isolated from the signal leads (pins 1 through 3). This allows the ACS756 family of sensor ICs to be used in applications requiring electrical isolation without the use of opto-isolators or other costly isolation techniques.

The device is fully calibrated prior to shipment from the factory. The ACS75x family is lead (Pb) free. All leads are plated with 100% matte tin, and there is no Pb inside the package. The heavy gauge leadframe is made of oxygen-free copper.

Selection Guide

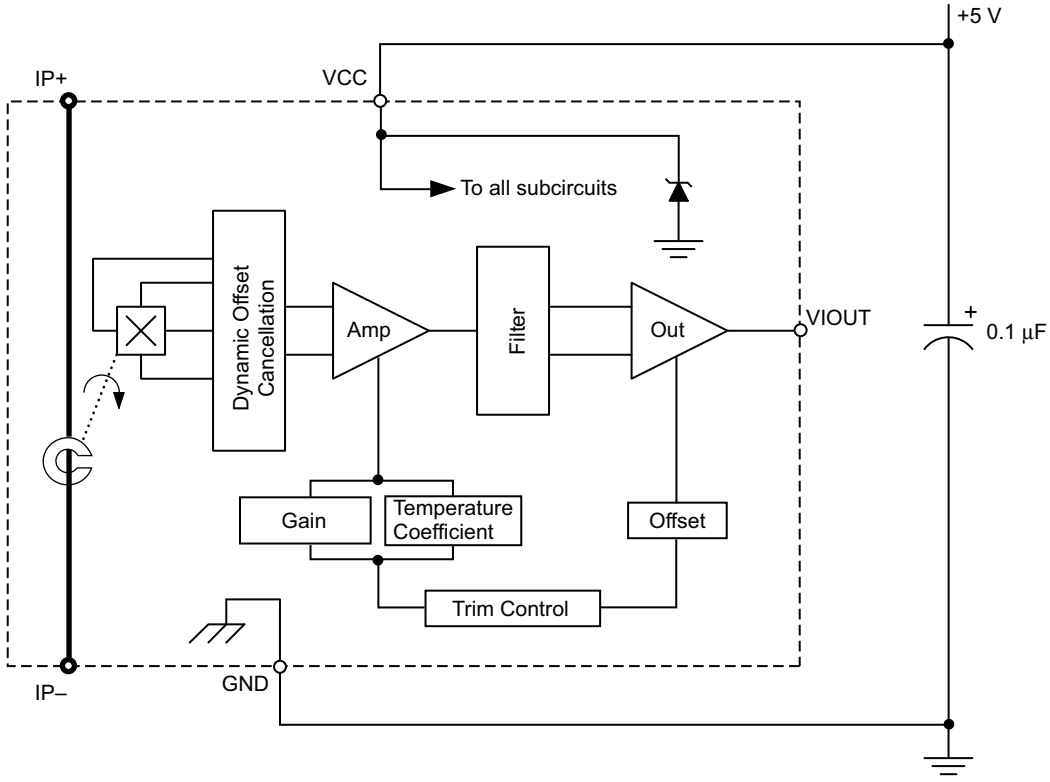
Part Number[1]	T_{OP} (°C)	Primary Sampled Current , I_P (A)	Packing[2]
ACS756SCA-050B-PFF-T	–20 to 85	±50	34 per tube
ACS756SCA-100B-PFF-T	–20 to 85	±100	
ACS756KCA-050B-PFF-T	–40 to 125	±50	

[1]Additional leadform options available for qualified volumes
[2]Contact Allegro for additional packing options.

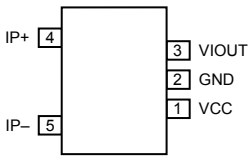
Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Forward Supply Voltage	V_{CC}		8	V
Reverse Supply Voltage	V_{RCC}		–0.5	V
Forward Output Voltage	V_{IOUT}		28	V
Reverse Output Voltage	V_{RIOUT}		–0.5	V
Working Voltage for Reinforced Isolation	$V_{WORKING-R}$	Voltage applied between pins 1-3 and 4-5; tested at 3000 VAC for 1 minute according to UL standard 60950-1	353	VDC / V_{pk}
Working Voltage for Basic Isolation	$V_{WORKING-B}$	Voltage applied between pins 1-3 and 4-5; tested at 3000 VAC for 1 minute according to UL standard 60950-1	500	VDC / V_{pk}
Output Source Current	$I_{OUT(Source)}$	VIOUT to GND	3	mA
Output Sink Current	$I_{OUT(Sink)}$	VCC to VIOUT	1	mA
Nominal Operating Ambient Temperature	T_{OP}	Range K	–40 to 125	°C
		Range S	–20 to 85	°C
Maximum Junction	T_J(max)		165	°C
Storage Temperature	T_{stg}		–65 to 165	°C

Functional Block Diagram



Pin-out Diagram



Terminal List Table

Number	Name	Description
1	VCC	Device power supply terminal
2	GND	Signal ground terminal
3	VIOUT	Analog output signal
4	IP+	Terminal for current being sampled
5	IP–	Terminal for current being sampled

COMMON OPERATING CHARACTERISTICS[1] over full range of T_{OP}, and V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Supply Voltage[2]	V_{CC}		3	5.0	5.5	V
Supply Current	I_{CC}	V_{CC} = 5.0 V, output open	–	10	14	mA
Power On Time	t_{PO}	T_A = 25°C	–	35	–	µs
Rise Time	t_r	I_P = three-quarter scale of I_P+, T_A = 25°C, C_{OUT} = 0.47 nF	–	3	–	µs
Internal Bandwidth[3]	BW_i	–3 dB; I_P is 10 A peak-to-peak; 100 pF from VIOUT to GND	–	120	–	kHz
Output Load Resistance	$R_{LOAD(MIN)}$	VIOUT to GND	4.7	–	–	kΩ
Output Load Capacitance	$C_{LOAD(MAX)}$	VIOUT to GND	–	–	10	nF
Primary Conductor Resistance	$R_{PRIMARY}$	T_A = 25°C	–	130	–	µΩ
Symmetry	E_{SYM}	Over half-scale of Ip	98.5	100	101.5	%
Bidirectional 0 A Output	$V_{OUT(QBI)}$	I_P = 0 A, T_A = 25°C	–	V_{CC}/2	–	V
Magnetic Offset Error	I_{ERROM}	I_P = 0 A, after excursion of 100 A	–	±0.23	–	A
Ratiometry	V_{RAT}	V_{CC} = 4.5 to 5.5 V	–	100	–	%
Propagation Time	t_{PROP}	T_A = 25°C, C_{OUT} = 100 pF,	–	1	–	µs

[1]Device is factory-trimmed at 5 V, for optimal accuracy.
[2]Devices are programmed for maximum accuracy at 5.0 V V_{CC} levels. The device contains ratiometry circuits that accurately alter the 0 A Output Voltage and Sensitivity level of the device in proportion to the applied V_{CC} level. However, as a result of minor nonlinearities in the ratiometry circuit additional output error will result when V_{CC} varies from the 5 V V_{CC} level. Customers that plan to operate the device from a 3.3 V regulated supply should contact their local Allegro sales representative regarding expected device accuracy levels under these bias conditions.
[3]Guaranteed by design.

*X*050 PERFORMANCE CHARACTERISTICS over Range K[1]: T_{OP} = –40°C to 125°C, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Primary Sampled Current	I_P		–50	–	50	A
Sensitivity	$Sens_{TA}$	Half scale of I_P applied for 5 ms, T_A = 25°C	–	40	–	mV/A
	$Sens_{TOP}$	Half scale of I_P applied for 5 ms	37.2	–	42.8	mV/A
Noise[2]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	10	–	mV
Nonlinearity	$E_{LIN(HT)}$	Up to full scale of I_P, I_P applied for 5 ms, T_{OP} = 25°C to 125°C	– 1	–	1	%
	$E_{LIN(LT)}$	Up to full scale of I_P, I_P applied for 5 ms, T_{OP} = –40°C to 25°C	– 1.8	–	1.8	%
Electrical Offset Voltage[3]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±2	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 125°C	–30	–	30	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –40°C to 25°C	–60	–	60	mV
Total Output Error[4]	$E_{TOT(HT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = 25°C to 125°C	–7.5	–	7.5	%
	$E_{TOT(LT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = –40°C to 25°C	–7.5	–	7.5	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_{OP}, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.
[2]6σ noise voltage.
[3]$V_{OE(TOP)}$ drift is referred to ideal V_{OE} = 2.5 V at 0 A.
[4]Percentage of I_P, with I_P = 25 A. Output filtered.

*X*050 PERFORMANCE CHARACTERISTICS over Range S[1]: T_{OP} = –20°C to 85°C, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Primary Sampled Current	I_P		–50	–	50	A
Sensitivity	$Sens_{TA}$	Half scale of I_P applied for 5 ms, T_A = 25°C	–	40	–	mV/A
	$Sens_{TOP}$	Half scale of I_P applied for 5 ms	38.3	–	41.7	mV/A
Noise[2]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	10	–	mV
Nonlinearity	$E_{LIN(HT)}$	Up to full scale of I_P, I_P applied for 5 ms, T_{OP} = 25°C to 85°C	– 1	–	1	%
	$E_{LIN(LT)}$	Up to full scale of I_P, I_P applied for 5 ms, T_{OP} = –20°C to 25°C	– 1	–	1	%
Electrical Offset Voltage[3]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±2	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 85°C	–30	–	30	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –20°C to 25°C	–30	–	30	mV
Total Output Error[4]	$E_{TOT(HT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = 25°C to 85°C	–5	–	5	%
	$E_{TOT(LT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = –20°C to 25°C	–5	–	5	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_{OP}, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.
[2]6σ noise voltage.
[3]$V_{OE(TOP)}$ drift is referred to ideal V_{OE} = 2.5 V at 0 A.
[4]Percentage of I_P, with I_P = 25 A. Output filtered.

_X_100 PERFORMANCE CHARACTERISTICS over Range S[1]: T_{OP} = –20°C to 85°C, V_{CC} = 5 V, unless otherwise specified

Characteristic	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Primary Sampled Current	I_P		–100	–	100	A
Sensitivity	$Sens_{TA}$	Half scale of I_P applied for 5 ms, T_A = 25°C	–	20	–	mV/A
	$Sens_{TOP}$	Half scale of I_P applied for 5 ms	18.2	–	21.8	mV/A
Noise[2]	V_{NOISE}	T_A= 25°C, 10 nF on VIOUT pin to GND	–	6	–	mV
Nonlinearity	$E_{LIN(HT)}$	Up to full scale of I_P, I_P applied for 5 ms, T_{OP} = 25°C to 85°C	– 1.75	–	1.75	%
	$E_{LIN(LT)}$	Up to full scale of I_P, I_P applied for 5 ms, T_{OP} = –20°C to 25°C	– 1	–	1	%
Electrical Offset Voltage[3]	$V_{OE(TA)}$	I_P = 0 A, T_A = 25°C	–	±2	–	mV
	$V_{OE(TOP)HT}$	I_P = 0 A, T_{OP} = 25°C to 85°C	–30	–	30	mV
	$V_{OE(TOP)LT}$	I_P = 0 A, T_{OP} = –20°C to 25°C	–30	–	30	mV
Total Output Error[4]	$E_{TOT(HT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = 25°C to 85°C	–8	–	8	%
	$E_{TOT(LT)}$	Over full scale of I_P, I_P applied for 5 ms, T_{OP} = –20°C to 25°C	–7	–	7	%

[1]Device may be operated at higher primary current levels, I_P, and ambient temperatures, T_{OP}, provided that the Maximum Junction Temperature, T_J(max), is not exceeded.
[2]6σ noise voltage.
[3]$V_{OE(TOP)}$ drift is referred to ideal V_{OE} = 2.5 V at 0 A.
[4]Percentage of I_P, with I_P = 25 A. Output filtered.

Definitions of Accuracy Characteristics

Sensitivity (Sens). The change in device output in response to a 1 A change through the primary conductor. The sensitivity is the product of the magnetic circuit sensitivity (G/A) and the linear IC amplifier gain (mV/G). The linear IC amplifier gain is programmed at the factory to optimize the sensitivity (mV/A) for the half-scale current of the device.

Noise (V_{NOISE}). The noise floor is derived from the thermal and shot noise observed in Hall elements. Dividing the noise (mV) by the sensitivity (mV/A) provides the smallest current that the device is able to resolve.

Nonlinearity (E_{LIN}). The degree to which the voltage output from the IC varies in direct proportion to the primary current through its half-scale amplitude. Nonlinearity in the output can be attributed to the saturation of the flux concentrator approaching the half-scale current. The following equation is used to derive the linearity:

$$100\left\{1-\left[\frac{\Delta\text{ gain}\times\%\text{ sat}\,(V_{\text{IOUT\_half-scale amperes}}-V_{\text{IOUT(Q)}})}{2\,(V_{\text{IOUT\_quarter-scale amperes}}-V_{\text{IOUT(Q)}})}\right]\right\}$$

where

Δ gain = the gain variation as a function of temperature changes from 25ºC,
% sat = the percentage of saturation of the flux concentrator, which becomes significant as the current being sampled approaches half-scale $\pm I_P$, and
$V_{\text{IOUT\_half-scale amperes}}$ = the output voltage (V) when the sampled current approximates half-scale $\pm I_P$.

Symmetry (E_{SYM}). The degree to which the absolute voltage output from the IC varies in proportion to either a positive or negative half-scale primary current. The following equation is used to derive symmetry:

$$100\left(\frac{V_{\text{IOUT\_+ half-scale amperes}}-V_{\text{IOUT(Q)}}}{V_{\text{IOUT(Q)}}-V_{\text{IOUT\_–half-scale amperes}}}\right)$$

Ratiometry. The device features a ratiometric output. This means that the quiescent voltage output, V_{IOUTQ}, and the magnetic sensitivity, Sens, are proportional to the supply voltage, V_{CC}.

The ratiometric change (%) in the quiescent voltage output is defined as:

$$\Delta V_{\text{IOUTQ}(\Delta V)} = \frac{V_{\text{IOUTQ}(V_{CC})}/V_{\text{IOUTQ}(5V)}}{V_{CC}/5\text{ V}}\times 100\%$$

and the ratiometric change (%) in sensitivity is defined as:

$$\Delta Sens_{(\Delta V)} = \frac{Sens_{(V_{CC})}/Sens_{(5V)}}{V_{CC}/5\text{ V}}\times 100\%$$

Quiescent output voltage ($V_{IOUT(Q)}$). The output of the device when the primary current is zero. For a unipolar supply voltage, it nominally remains at $V_{CC}/2$. Thus, V_{CC} = 5 V translates into $V_{IOUT(Q)}$ = 2.5 V. Variation in $V_{OUT(Q)}$ can be attributed to the resolution of the Allegro linear IC quiescent voltage trim, magnetic hysteresis, and thermal drift.

Electrical offset voltage (V_{OE}). The deviation of the device output from its ideal quiescent value of $V_{CC}/2$ due to nonmagnetic causes.

Magnetic offset error (I_{ERROM}). The magnetic offset is due to the residual magnetism (remnant field) of the core material. The magnetic offset error is highest when the magnetic circuit has been saturated, usually when the device has been subjected to a full-scale or high-current overload condition. The magnetic offset is largely dependent on the material used as a flux concentrator. The larger magnetic offsets are observed at the lower operating temperatures.

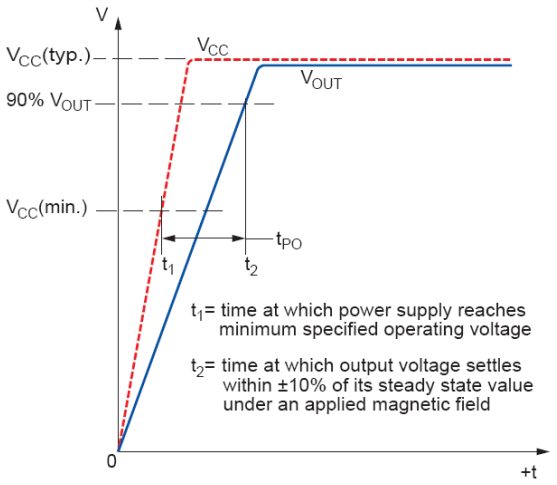
Total Output Error (E_{TOT}). The maximum deviation of the actual output from its ideal value, also referred to as *accuracy*, illustrated graphically in the output voltage versus current chart on the following page.

E_{TOT} is divided into four areas:

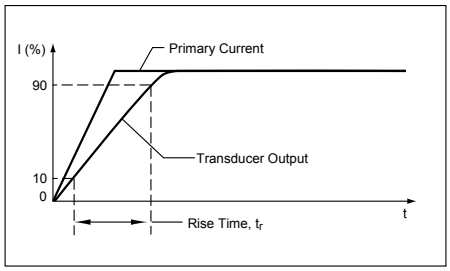
- **0 A at 25°C.** Accuracy at the zero current flow at 25°C, without the effects of temperature.
- **0 A over Δ temperature.** Accuracy at the zero current flow including temperature effects.
- **Half-scale current at 25°C.** Accuracy at the the half-scale current at 25°C, without the effects of temperature.
- **Half-scale current over Δ temperature.** Accuracy at the half-scale current flow including temperature effects.

Definitions of Dynamic Response Characteristics

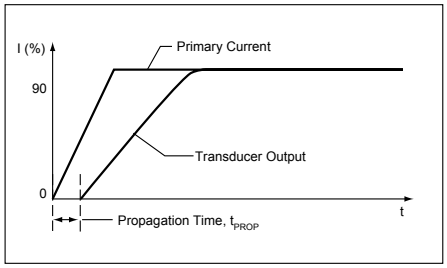
Power-On Time (t_{PO}). When the supply is ramped to its operating voltage, the device requires a finite time to power its internal components before responding to an input magnetic field. Power-On Time, t_{PO} , is defined as the time it takes for the output voltage to settle within ±10% of its steady state value under an applied magnetic field, after the power supply has reached its minimum specified operating voltage, V_{CC}(min), as shown in the chart at right.



Rise time (t_r). The time interval between a) when the device reaches 10% of its full scale value, and b) when it reaches 90% of its full scale value. The rise time to a step response is used to derive the bandwidth of the device, in which $f(-3\ dB) = 0.35 / t_r$. Both t_r and $t_{RESPONSE}$ are detrimentally affected by eddy current losses observed in the conductive IC ground plane.

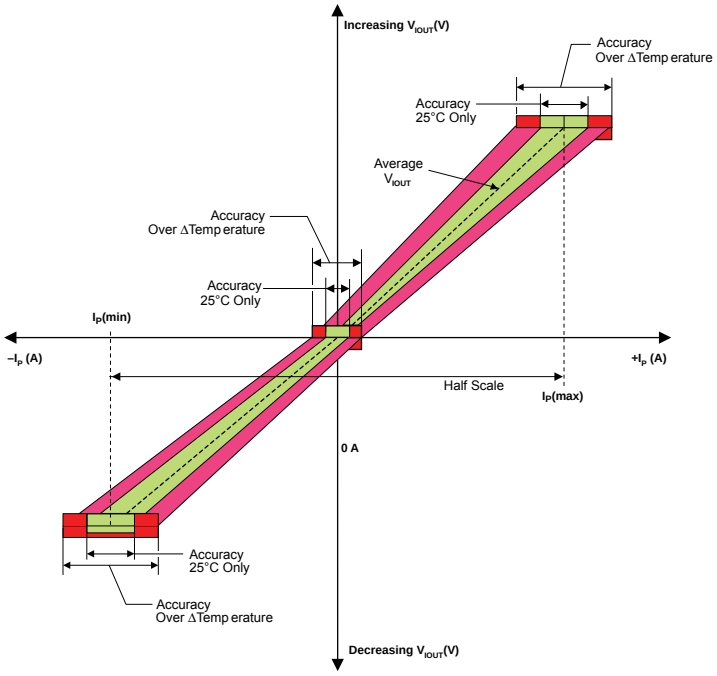


Propagation delay (t_{PROP}). The time required for the device output to reflect a change in the primary current signal. Propagation delay is attributed to inductive loading within the linear IC package, as well as in the inductive loop formed by the primary conductor geometry. Propagation delay can be considered as a fixed time offset and may be compensated.



Output Voltage versus Sampled Current

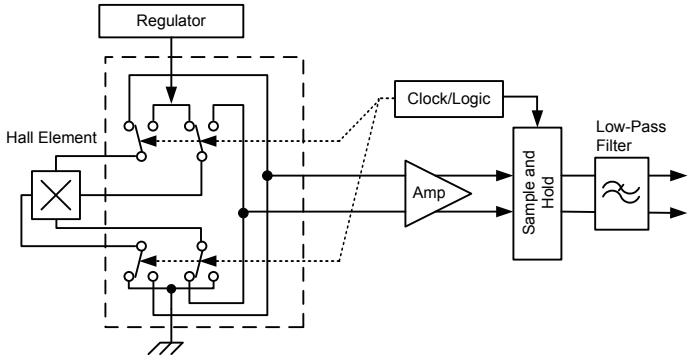
Total Output Error at 0 A and at Half-Scale Current



Chopper Stabilization Technique

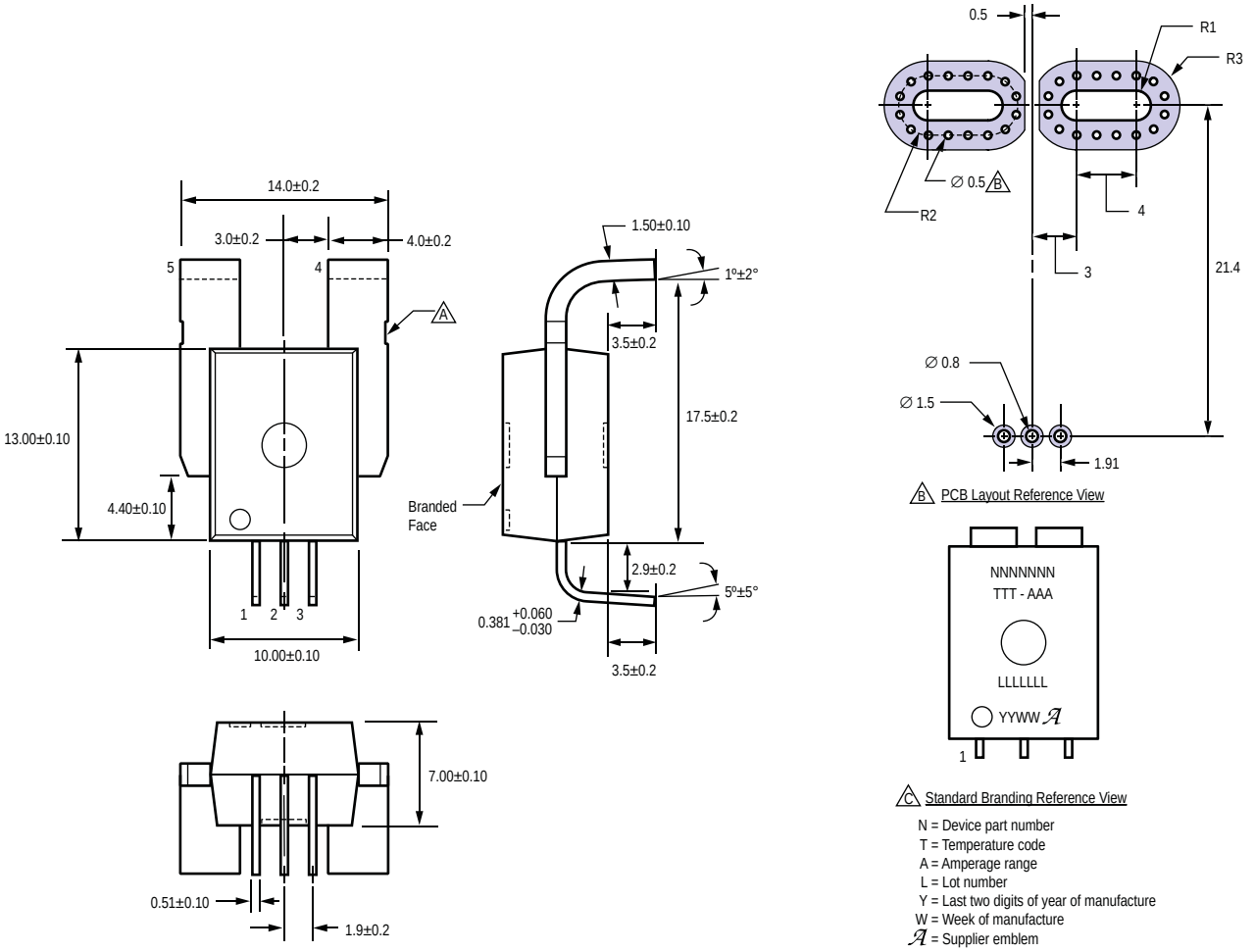
Chopper Stabilization is an innovative circuit technique that is used to minimize the offset voltage of a Hall element and an associated on-chip amplifier. Allegro patented a Chopper Stabilization technique that nearly eliminates Hall IC output drift induced by temperature or package stress effects. This offset reduction technique is based on a signal modulation-demodulation process. Modulation is used to separate the undesired DC offset signal from the magnetically induced signal in the frequency domain. Then, using a low-pass filter, the modulated DC offset is suppressed while the magnetically induced signal passes through the filter. As a result of this chopper stabilization approach, the output voltage from the Hall IC is desensitized to the effects of temperature and mechanical stress. This technique produces devices that have an extremely stable Electrical Offset Voltage, are immune to thermal stress, and have precise recoverability after temperature cycling.

This technique is made possible through the use of a BiCMOS process that allows the use of low-offset and low-noise amplifiers in combination with high-density logic integration and sample and hold circuits.



Concept of Chopper Stabilization Technique

Package CA, 5-pin package, leadform PFF



N = Device part number
T = Temperature code
A = Amperage range
L = Lot number
Y = Last two digits of year of manufacture
W = Week of manufacture
A = Supplier emblem

A Dambar removal intrusion
B Perimeter through-holes recommended
C Branding scale and appearance at supplier discretion

For Reference Only; not for tooling use (reference DWG-9111, DWG-9110)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

Revision History

Revision	Revision Date	Description of Revision
Rev. 6	March 25, 2011	Augment V_{CC} specification

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