1T01234 - S.E.(Information Technology Engineering)(SEM-IV)(Choice Base Credit Grading System) (R- 20-21) (C Scheme) /
41025 - Computer Organization & Architecture   QP CODE: 10015940   DATE: 19/12/2022

Duration: 3hrs   **[Max Marks:80]**

N.B. : (1) Question No 1 is Compulsory.
        (2) Attempt any three questions out of the remaining five.
        (3) All questions carry equal marks.
        (4) Assume suitable data, if required and state it clearly.

1   Attempt any FOUR   **[20]**
   a   Discuss any five arithmetic instructions of 8086 with examples.
   b   Explain Memory hierarchy with diagram.
   c   Minimize the following boolean function using K map
        $F(A, B, C) = \Sigma m(0, 1, 6, 7) + \Sigma d(3, 5)$
   d   Explain full adder with diagram
   e   Convert $(-1259.125)_{10}$ in the IEEE 754 single precision standard.

2   a   Explain concept of DMA in detail with diagram   **[10]**
    b   Discuss various cache memory mapping techniques with advantages and   **[10]**
        disadvantages of it.

3   a   Draw Flowchart of Restoring division technique and divide 13 by 5 using **[10]**
        Restoring division technique.
    b   List and explain Key Characteristics of Computer memory.   **[10]**

4   a   Write 8086 Assembly Language Program to count the number of 0's and 1's **[10]**
        in given 8-bit numbers.
    b   Discuss various Pipeline Hazards with examples.   **[10]**

5   a   Draw flowchart of Booth's algorithm. Using Booth's algorithm demonstrate **[10]**
        multiplication of (-11)*(-5).
    b   Discuss various addressing modes of 8086 microprocessor with example. **[10]**

6   a   Write short note on Flip Flops   **[10]**
    b   Minimize the following boolean function using K map   **[10]**
        $F(A, B, C, D) = \Sigma m(0, 2, 8, 10, 14) + \Sigma d(5, 15)$

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Paper / Subject Code: 41004 / Computer Oraganization and Architecture

13-Dec-2019   1T01224 - S.E.(Information Technology Engineering)(SEM-IV)(Choice Based) / 41004 - Computer Oraganization and Architecture 55465

(3 Hours)   **[Total Marks: 80]**

N.B.   1. Question No 1 is compulsory.
2. Solve any **three** questions out of remaining five questions.
3. Assume suitable data if necessary.
4. Figures to right indicate marks.

Q. 1. Solve any **four** out of five.   (4*5=20)

a) Draw and explain memory hierarchy.

b) Differentiate between MIN and MAX mode of 8086 Microprocessor.

c) Discuss the importance of Nano Programming.

d) Express $(15.125)_{10}$ in IEE 754 single precision floating point representation.

e) Explain following instructions of 8086 microprocessor – OR, DAA, INC, JNZ, POP

Q. 2 a) Draw and explain internal architecture of 8086 microprocessor. .   [10]

b) Draw the flowchart of Booths algorithm and perform -7 X 3.   [10]

Q. 3 a) Perform 18 divided by 5 using Restoring division algorithm.   [10]

b) What is the need of DMA in computer system? Explain in detail its

operation in various modes..   [10]

Q. 4 a) Discuss various memory characteristics in detail.   [10]

b) Compare Hardwired and Microprogrammed Control Unit.   [10]

Q. 5 a) Explain Direct Cache Memory mapping in detail with example.   [10]

b) Write assembly language program for 8086 microprocessor to find whether a

8 bit number stored at 1000H is even or odd number. Store the 00H or

01H at 1001H if the number is even or odd respectively.   [10]

Q. 6 a) Explain with example addressing modes of 8086 microprocessor   [10]

b) Draw and explain the various pipeline hazards.   [10]

Paper / Subject Code: 41004 / Computer Oraganization and Architecture

Thursday, May 23, 201902:30 pm - 05:30 pm   1T01224 - S.E.(INFORMATION TECHNOLOGY) (Sem IV)
(Choice Based) / 41004 - COMPUTER ORGANIZATION & ACHITECTURE   55466

(3 Hours)   [**Total Marks: 80**

N.B.: (1) Question No. **1** is **compulsory.**

      (2) Solve any **three** questions out of remaining **five.**

      (3) Figures to **right** indicate **full** marks.

      (4) Assume suitable **data** where **necessary.**

1. Solve any four out of five sub questions.   [04 x 05=20]
    a) Compare Computer Organization and Computer Architecture.
    b) Explain various pipeline hazards.
    c) Differentiate between Hardwired and Micro programmed control unit.
    d) Discuss various characteristics of memory.
    e) Explain following instructions of 8086 microprocessor –ADC, DAA, MOVSB, LEA, ROL

2. a) Discuss various addressing modes of 8086 microprocessor with example.   10
    b) Using Booth's algorithm demonstrates multiplication of (-7)*(-6).   10

3. a) Explain concept of DMA in detail.   10
    b) Describe various cache memory mapping techniques.   10

4. a) Describe Flynn's classification in detail.   10
    b) Divide 13 by 4 using restoring division algorithms.   10

5. a) Describe Minimum modes of 8086 microprocessor in detail.   10
    b) Express $(-10.100)_{10}$ in IEEE 754 single & double precision standard of floating
       point number representation.   10

6. Write short notes on: (**any four**)   [04 x 05=20]
    a) Segmentation concept of 8086 microprocessor.
    b) Cache coherency
    c) Von Neumann architecture
    d) Programmed I/O
    e) Six stage instruction pipeline
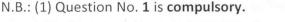
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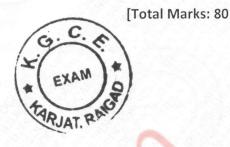32D6CAE73823A2A9FE2C2E7C15BB4E67

(3 Hours) [Total Marks: 80]

Note : Q1 is compulsory.
Attempt any THREE out of the remaining questions.
Assume suitable data if necessary.

Q1. Attempt any 4 sub questions

    a) Explain six stage instruction pipeline with suitable diagram.   5
    b) Write a note on 8288 bus controller.   5
    c) Explain memory hierarchy.   5
    d) Draw the flowchart of unsigned binary restoring division algorithm.
    e) Explain any five instructions of 8086 microprocessor with   5
       suitable examples.

Q2. a) What is DMA? Explain working of DMA.   10
    b) List and explain key characteristics of computer memory.   10

Q3 a) Draw the flowchart of Booths algorithm and multiply (-3)*(4)   10
     using Booths algorithm.
    b) Explain micro-programmed control unit with suitable diagram.   10

4 a) Explain addressing modes of 8086 microprocessor with suitable examples.   10
    b) Explain single and double precision IEEE 754 binary floating point   10
      representation formats.

Q5. a) Explain with suitable diagram maximum mode of operation of 8086   10
     Micro processor.
    b) Write 8086 Assembly Language Program to count number of 0's   10
     and 1's in a given 8 bit number.

Q6 Write notes on (any two)   20
    a) Cache memory mapping techniques.
    b) Flynn's classification of parallel computers.
    c) Programmed I/O.

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Q.P.Code: 37701

(3 Hours) [Total Marks: 80]

N.B.: (1) Question No. **1** is **compulsory**.
    (2) Solve any **three** questions out of remaining **five**.
    (3) Figures to **right** indicate **full** marks.
    (4) Assume suitable **data** where **necessary**.

1. Solve any four out of five sub questions. [04 x 05=20]
    a) Differentiate between minimum and maximum mode of operation of 8086 microprocessor.
    b) Explain any five arithmetic instructions of 8086 microprocessor with suitable examples.
    c) Draw and explain basic instruction execution cycle.
    d) Describe Nano programming.
    e) Explain the hierarchical organization of computer memory.

2. a) Explain with suitable diagram architecture of 8086 microprocessor. 10
    b) Explain hardwired approach to the design of a control unit. 10

3. a) Represent the number $(-0.125)_{10}$ in single and double precision IEEE 754 binary floating
    point representation formats. 10
    b) Write 8086 Assembly Language Program to convert two digit packed BCD number 10
    to unpacked BCD number.

4. a) Identify the addressing modes of following instructions and explain their meaning. 10
        I. MOV AX, 1000
        II. MOV AX, [1000]
        III. MOV AX, BX
        IV. MOV [BX], AX
        V. MOV AX, [SI+200]
    b) Draw the flowchart of Booths algorithm and multiply (-7)*(3)using Booths algorithm. 10

5. a) Explain working of DMA and its different configurations. 10
    b) Explain different cache memory mapping techniques. 10

6 Write notes on (**any two**) 20
    a) Interleaved and Associative memory.
    b) Interrupt driven I/O
    c) Pipeline Hazards

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