



UNIVERSITY OF TEHRAN

College of Engineering

Electrical and Computer Engineering Department

Digital Systems I, ECE 894

Computer Assignment 5

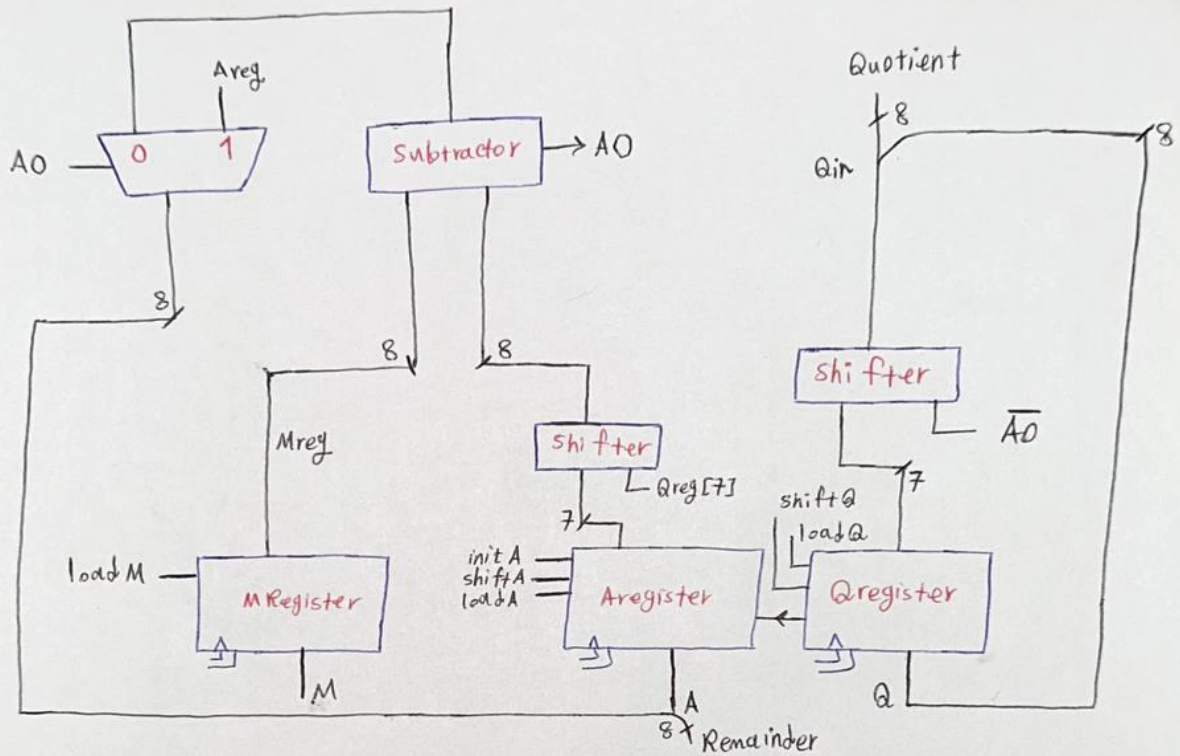
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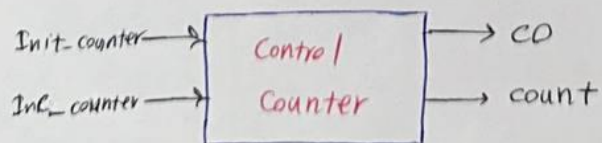
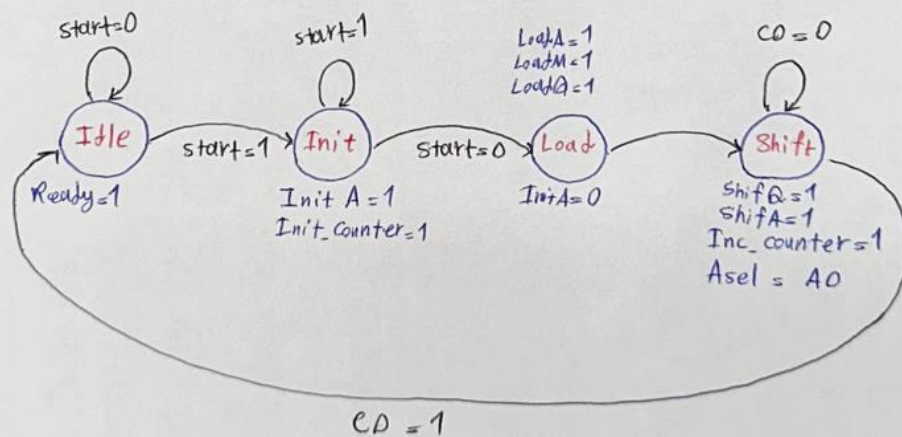
Spring 1402-03

Design:

Datapath:



Controller:



Pre-Synthesis

```

1 | `timescale 1ns/1ns
2 | module DivDp (input [7:0]Q, M, input loadM, loadA, loadQ, InitA, Asel, shiftA, shiftQ, clk, rst, output logic [7:0]Quotient, output logic [7:0]Remainder, output logic A0);
3 |
4 | logic [7:0]Qreg, Mreg, Qin, Akin, Areg, Ares, SubResult, MKXResult;
5 |
6 | always @(posedge clk, posedge rst) begin
7 |
8 |     if(rst) begin
9 |         Areg <= 8'b0;
10 |     end
11 |     else if(InitA) begin
12 |         A <= 8'b0;
13 |     end
14 |     else if(loadA) begin
15 |         Areg <= A;
16 |     end
17 |     else if(shiftA) begin
18 |         Areg <= Ares;
19 |     end
20 | end
21 |
22 | always @(posedge clk, posedge rst) begin
23 |     if(rst)
24 |         Qreg <= 8'b0;
25 |     else begin
26 |         if(loadQ)
27 |             Qreg <= Q;
28 |         else
29 |             if(shiftQ)
30 |                 Qreg <= Qin;
31 |     end
32 | end
33 |
34 | always @(posedge clk, posedge rst) begin
35 |     if(rst)
36 |         Mreg <= 8'b0;
37 |     else begin
38 |         if(loadM)
39 |             Mreg <= M;
40 |     end

```

```

1 | `timescale 1ns/1ns
2 | module DivCV (input clk, rst, start, A0, output logic ready, loadA, loadM, loadQ, shiftA, shiftQ, InitA, Asel);
3 |
4 | logic Co;
5 | logic Init_Counter, Inc_Counter;
6 | logic [1:0]pstate, nstate;
7 | logic [2:0] Count;
8 |
9 | parameter [1:0]
10 | Idle = 0, Init = 1, Load = 2, Shift = 3;
11 | always @(pstate, start, A0, Co) begin
12 |     nstate = 0;
13 |     (loadA, loadM, loadQ, shiftA, shiftQ, InitA, Asel, ready) = 8'b0;
14 |     (Init_Counter, Inc_Counter) = 2'b0;
15 |     case (pstate)
16 |     Idle: begin nstate = start ? Init : Idle; ready = 1'b1; end
17 |     Init: begin nstate = start ? Init:Load; Init_Counter = 1'b1; InitA = 1'b1; end
18 |     Load: begin nstate = Shift; InitA = 1'b0; loadM = 1'b1; loadQ = 1'b1; loadA = 1'b1; end
19 |     Shift: begin nstate = Co ? Idle : Shift; shiftQ = 1'b1; shiftA = 1'b1; Inc_Counter = 1'b1; Asel = A0; end
20 |     default: nstate = Idle;
21 |     endcase
22 | end
23 |
24 | always @(posedge clk, posedge rst) begin
25 |     if(rst)
26 |         pstate <= Idle;
27 |     else
28 |         pstate <= nstate;
29 |     end
30 |
31 | always @(posedge clk, posedge rst) begin
32 |     if(rst) Count <= 3'b0;
33 |     else
34 |         if(Init_Counter) Count <= 3'b1;
35 |         else
36 |             if(Inc_Counter) Count <= Count+1'b1;
37 |     end
38 |
39 | assign Co = #Count;
40 |

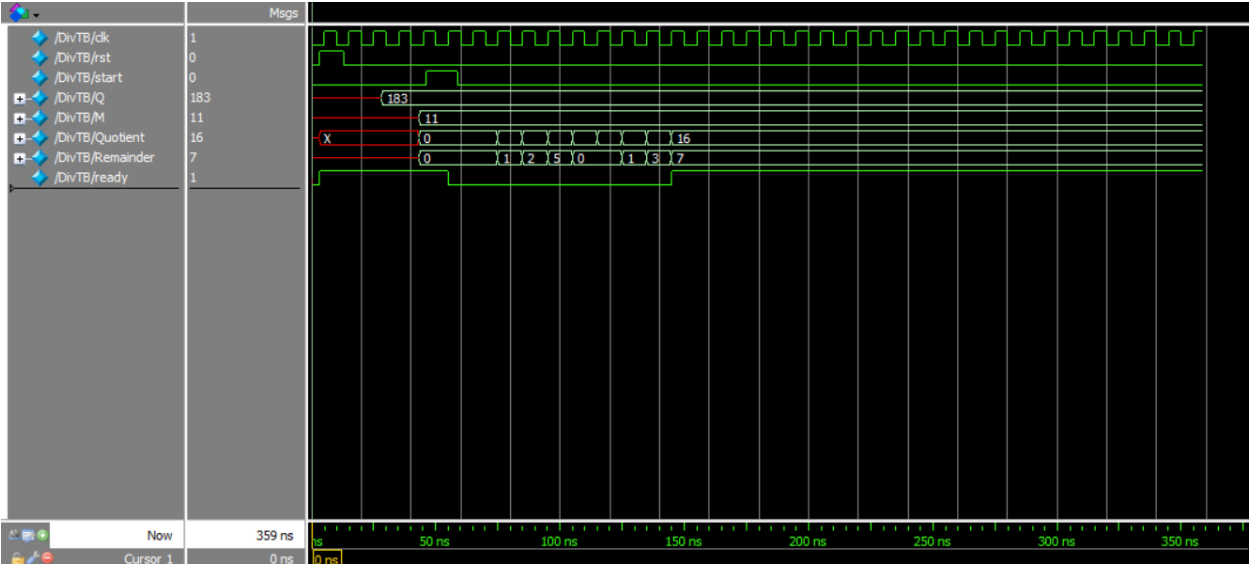
```

```

1 | `timescale 1ns/1ns
2 | module top (input clk, rst, start, input[7:0] Q, M, output[7:0] Quotient, Remainder, output ready);
3 | logic loadA, loadM, loadQ, shiftA, shiftQ, InitA, Asel, A0;
4 | DivDp dp (Q, M, loadM, loadA, loadQ, InitA, Asel, shiftA, shiftQ, clk, rst, Quotient, Remainder, A0);
5 | DivCV cu (clk, rst, start, A0, ready, loadA, loadM, loadQ, shiftA, shiftQ, InitA, Asel);
6 | endmodule

```

06/12/2024 05:08:17 ...	Test.sv	✓	Syst... 2
06/12/2024 05:03:00 ...	Controller.sv	✓	Syst... 0
06/12/2024 05:01:16 ...	Top.sv	✓	Syst... 3
06/12/2024 05:00:55 ...	Datapath.sv	✓	Syst... 1



Post-Synthesis:

The screenshot displays the Quartus Prime IDE interface during the post-synthesis phase. The top window shows the 'Flow Summary' for the 'Div_Top' project, indicating a successful compilation on June 11, 2024. The summary lists various metrics such as logic elements, registers, and pins. The bottom window shows the 'Messages' pane with a list of compilation messages, including warnings and errors. The code editor at the bottom shows a Verilog snippet for a combinatorial logic block.

Flow Summary

Flow Status	Successful - Tue Jun 11 18:57:48 2024
Quartus Prime Version	20.1.0 Build 711 06/05/2020 SJ Lite Edition
Revision Name	Div_Top
Top-level Entity Name	top
Family	Cyclone IV E
Device	EP4CE6E22A7
Timing Models	Final
Total logic elements	43
Total registers	22
Total pins	36
Total virtual pins	0
Total memory bits	0
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Messages

- 18236 Command: quartus_map --read_settings_files-on --write_settings_files-off Div_Top -c Div_Top
- 20030 Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment NUM_PARALLEL_PROCESSORS in your QSF to an appropriate value.
- 20030 Parallel compilation is enabled and will use 4 of the 4 processors detected
- 12021 Found 1 design units, including 1 entities, in source file /uni/semester 4/digital systems 1/ca/ca5/top.sv
- 12021 Found 1 design units, including 1 entities, in source file /uni/semester 4/digital systems 1/ca/ca5/datapath.sv
- 12021 Found 1 design units, including 1 entities, in source file /uni/semester 4/digital systems 1/ca/ca5/controller.sv
- 12127 Elaborating entity "top" for the top level hierarchy
- 12128 Elaborating entity "Divdp" for hierarchy "Divdp"
- 10036 Verilog HDL or VHDL warning at datapath.sv(4): object "Mreg" assigned a value but never read
- 12128 Elaborating entity "Divcv" for hierarchy "Divcv:cu"
- 286030 Timing-Driven Synthesis is running
- 170492 registers lost all their fanouts during netlist optimizations.
- 16010 Generating hard_block partition "hard_block:auto.generated_inst"
- 21057 Implemented 79 device resources after synthesis - the final resource count might be different
- Quartus Prime Analysis & Synthesis was successful. 0 errors, 2 warnings

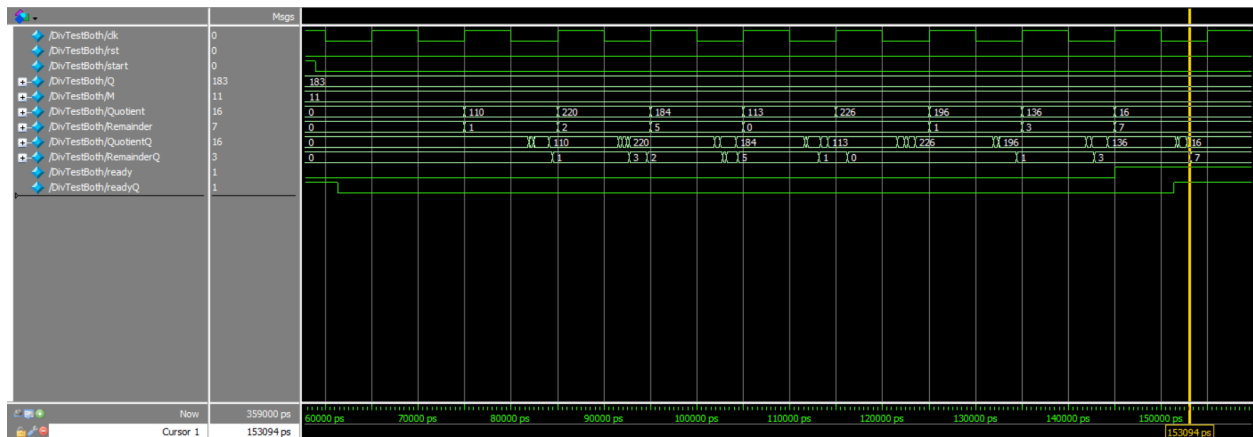
```
701 .cout());
702 // synopsys translate_off
703 defparam \cu|Selector2-0 .lut_mask = 16'h70F0;
704 defparam \cu|Selector2-0 .sum_lutc_input = "dataac";
705 // synopsys translate_on
706
707 // Location: LCCOMB_X20_Y20_N14
708 cycloneive_lcell_comb \cu|Selector2-1 (
709 // Equation(s):
710 // \cu|Selector2-1_combout = (\cu|pstate.Load-q) # (\cu|Selector2-0_combout )
711
712 .dataa(gnd),
713 .datab(gnd),
714 .datac(\cu|pstate.Load-q ),
715 .datad(\cu|Selector2-0_combout ),
716 .cin(gnd),
717 .combout(\cu|Selector2-1_combout ),
718 .cout());
719 // synopsys translate_off
720 defparam \cu|Selector2-1 .lut_mask = 16'hFFF0;
721 defparam \cu|Selector2-1 .sum_lutc_input = "dataac";
722 // synopsys translate_on
723
724 // Location: FF_X20_Y20_N15
725 dfffeas \cu|pstate.Shift (
726 .clk(\clk-inputclkctrl_outclk ),
727 .d(\cu|Selector2-1_combout ),
728 .asdata(vcc),
729 .clrn(!\rst-inputclkctrl_outclk ),
730 .aload(gnd),
731 .sclr(gnd),
732 .aload(mdi)
```


Test-Both:

```

1  `timescale 1ns/1ns
2  module DivTestBoth();
3  logic clk = 1'b0;
4  logic rst=1'b0;
5  logic start =1'b0;
6  logic [7:0] Q, M, Quotient, Remainder;
7  logic ready;
8  DivTop cut (clk, rst, start, Q, M, Quotient, Remainder, ready);
9  top cut2 (clk, rst, start, Q, M, QuotientQ, RemainderQ, readyQ);
10 always #5 clk <= ~clk;
11 initial begin
12     #3 rst = 1;
13     #10 rst = 0;
14     #15 Q = 8'd183;
15     #15 M = 8'd11;
16     #3 start =1;
17     #13 start =0;
18     #300 $stop;
19 end
20 endmodule

```



This assignment involves designing a divider circuit using bit shifting.

Datapath:

- The datapath consists of three registers: A , Q , and M .
- The algorithm utilizes these registers to calculate the quotient and remainder of a division operation over a period of 8 clock cycles. This is achieved by shifting registers A and Q in a specific sequence.

Controller:

- The controller employs a 2-bit state variable that defines four distinct states for the divider.
- The controller asserts a "ready" signal upon completing the division operation.
- **(Optional:** You can mention additional details about the state transitions at first.)

Control Counter:

- The control counter has two inputs and two outputs:
 - Inputs: These might be clock and reset signals.
 - Outputs:
 - co : This is likely the "carry out" signal, which represents the combined overflow from all counter bits.
 - $count$: This represents the current count value of the counter.

Asynchronous Reset:

- The design incorporates an asynchronous reset mechanism to initialize the circuit.

Overall Design:

- These components, the datapath, controller, control counter, and reset, work together to form the complete divider circuit!