King Saud University
College of Computer and Information Sciences
Computer Science Department

CSC 220 - Project

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Section: 44174

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1. Introduction:

In this project I have multiple operations that have to perform in one circuit, so I designed an Arithmetic-Logic-Unit (ALU) that preforms many different arithmetic operations such as: adding, subtracting, transferring, incrementing, decrementing. and other logic operations such as complementing, and other operations using AND, OR, XOR gates.

2. Design:

I designed a 4-bit Arithmetic Logic Unit (ALU) that contain (X,Y) as 4 bits input,(G) as 4 bits output, and Cout as a carry out output. It also contains 4 selectors (S0,S1,S2,S3).

The circuit performs 14 different operations.

It has an arithmetic unit that can compute 8 functions on 4-bit inputs. and a logic unit that can perform 6 functions on 4-bit inputs

My circuit has 12 multiplexers:

Arithmetic part has (3) 2x1 multiplexers:

2 of the multiplexers take the output of each adder as an input and S1 as a selector, depending on the select signal, the output is connected to either of the inputs.

The outputs of these two multiplexers are the inputs of another multiplexer and its selector is S2.

Which is the last multiplexer for the arithmetic part.

Logic part has (5) 2x1 multiplexers:

One multiplexer takes as an input the output of AND and OR gates to perform one operation depending on the selector(S0).

Another multiplexer takes as an input the output of XOR gate and the complement of X to perform one operation depending on the selector (S0).

The outputs of these two multiplexers go as inputs in another multiplexer (selector S1).

There is other multiplexer that performs the last two logic operations which take Y and Y' as inputs and S0 as a selector.

The outputs of these two multiplexers go as inputs in another multiplexer which its selector is S2. This multiplexer chooses which operation to perform depending on its selector.

This multiplexer is last multiplexer in the logic part.

Four 2x1 multiplexers left, 3 of them are for the Carry Out output:

2 of the multiplexers take the carry out of the four adders as inputs and S1 as a selector. The output of these two multiplexers are the input for another multiplexer and the selector of it is S2 and it has an enable which is the complement of S3. The output of this multiplexer is the (Cout)carry out output of the circuit. (depending on the carry out of each adder, and then the multiplexer's output).

One multiplexer left which is the Last multiplexer:

This multiplexer takes the output of the last multiplexer of the arithmetic part and the last multiplexer of the logic part as inputs and S3 as a selector, this multiplexer determines the output of the whole circuit(G).

There are four adders:

The first two adders perform the first four arithmetic operations depending on the carry in. Which are: transferring, incrementing, adding.

The second two adders perform the second four arithmetic operations depending on the carry in.Which are: subtracting, decrementing, transferring

The carry in for all the adders is S0.

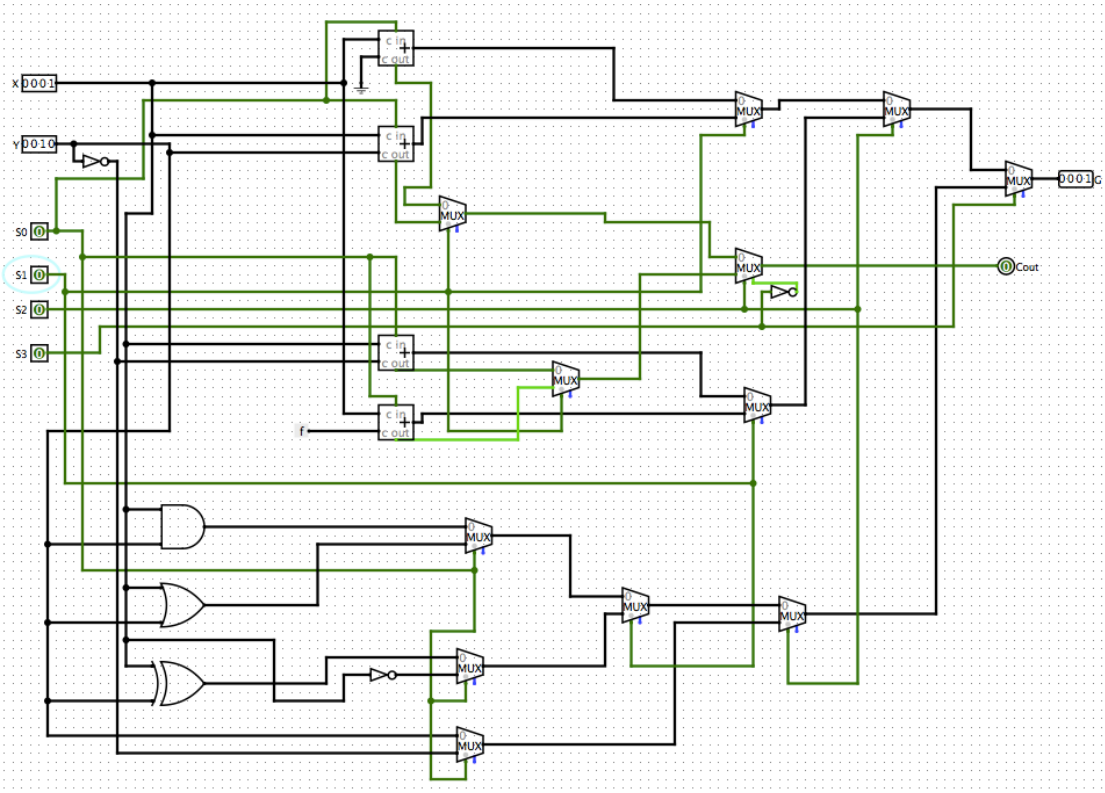
3. Test cases:

X=0001

Y=0010

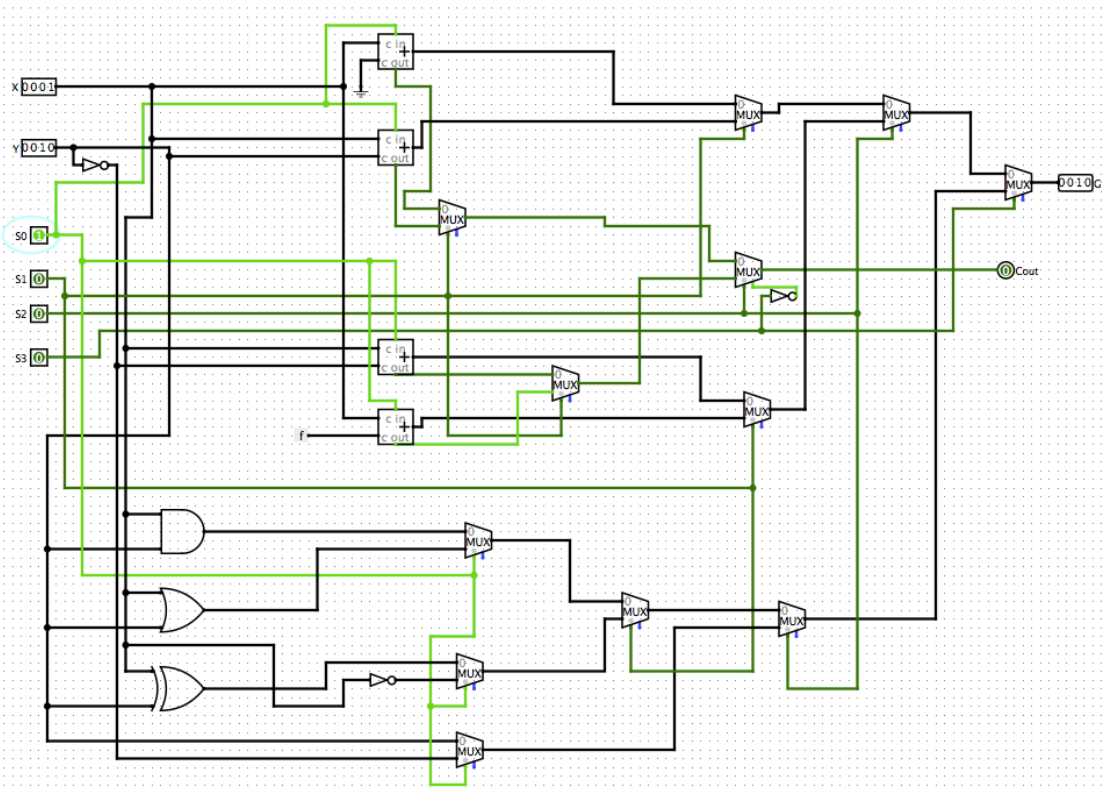
1:

S3	S2	S1	S0	Operation
0	0	0	0	G=X



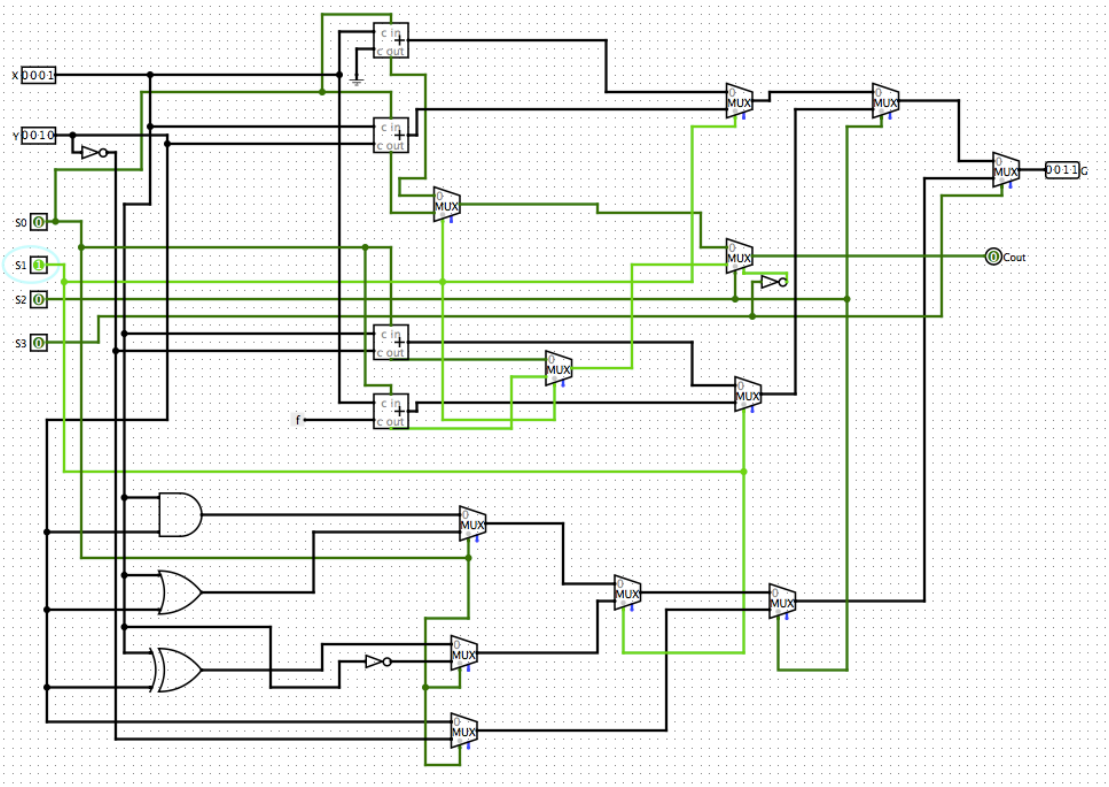
2:

S3	S2	S1	S0	Operation
0	0	0	1	G=X+1



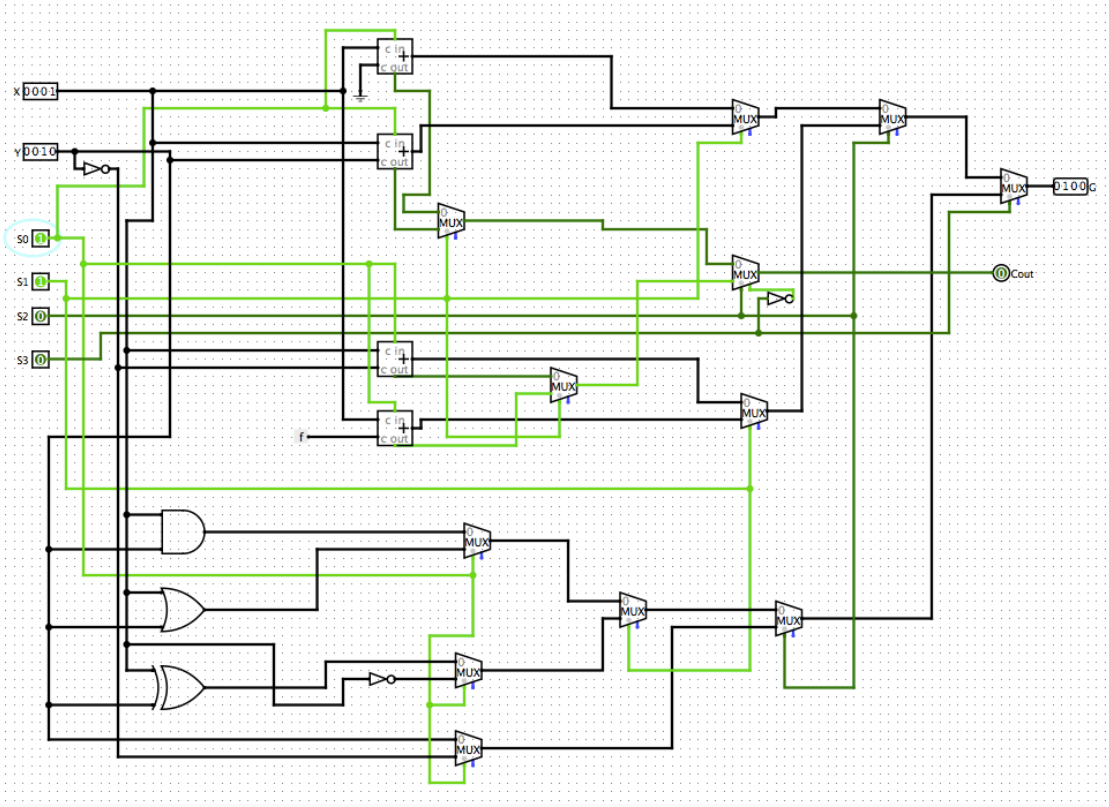
3:

S3	S2	S1	S0	Operation
0	0	1	0	G=X+Y



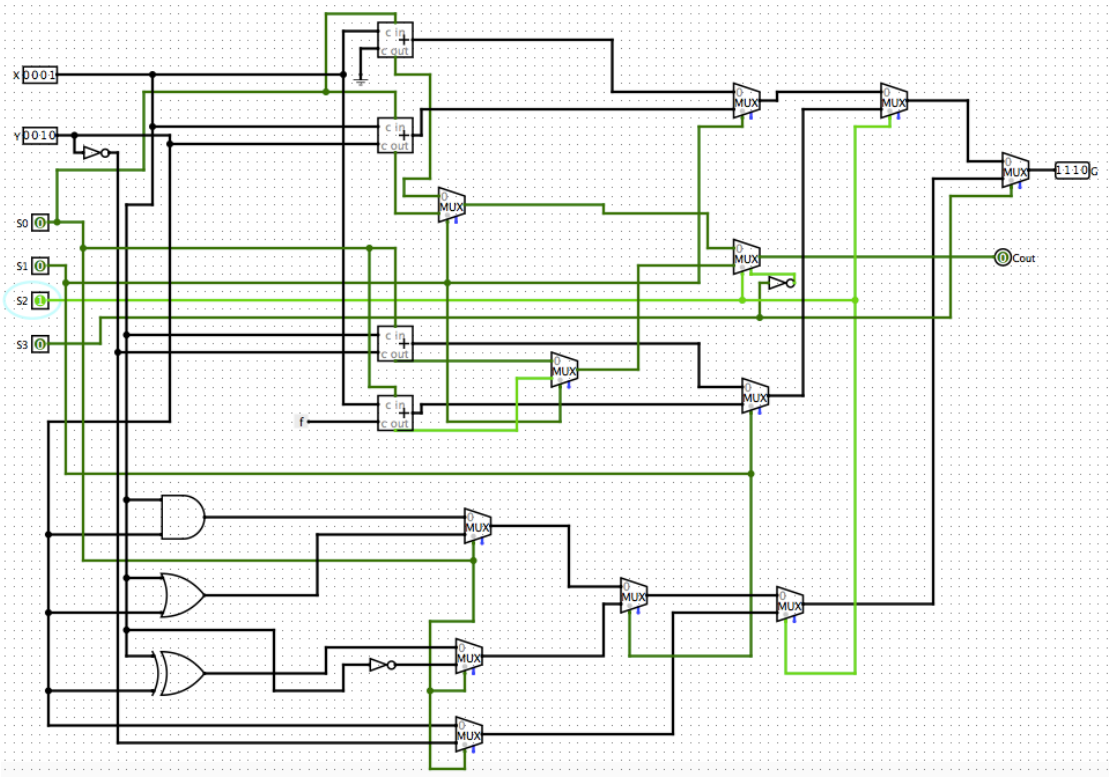
4:

S3	S2	S1	S0	Operation
0	0	1	1	G=X+Y+1



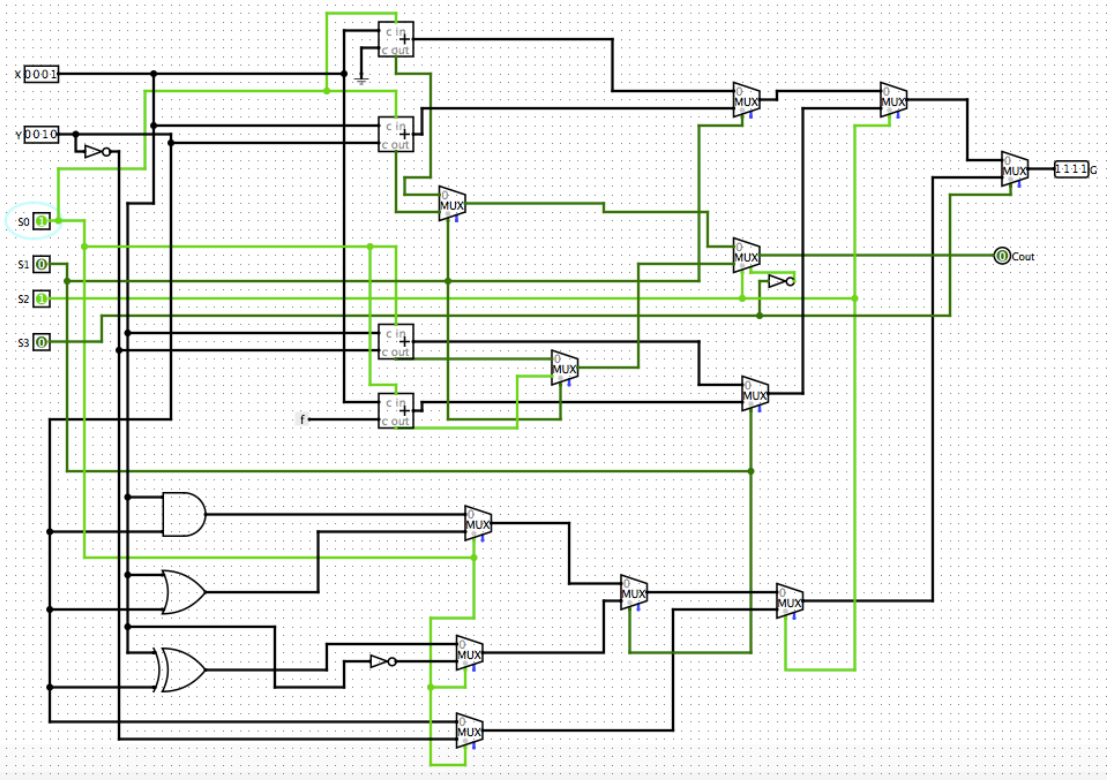
5:

S3	S2	S1	S0	Operation
0	1	0	0	G=X+Y’



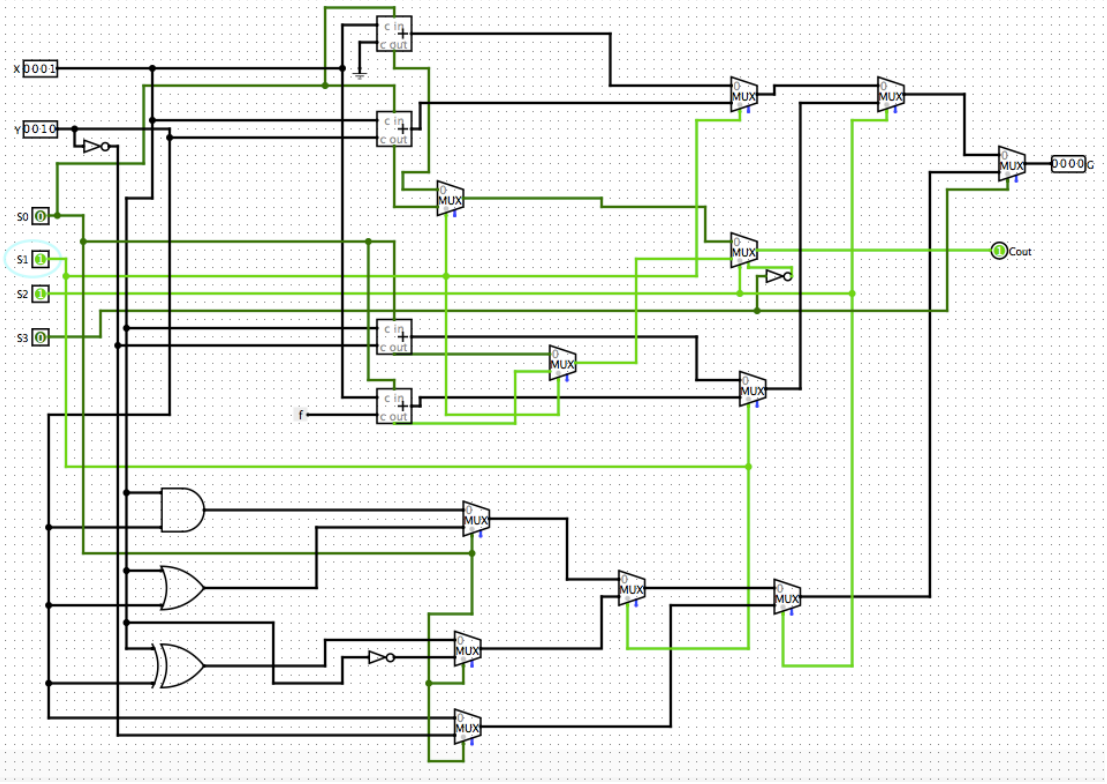
6:

S3	S2	S1	S0	Operation
0	1	0	1	G=X+Y’ +1



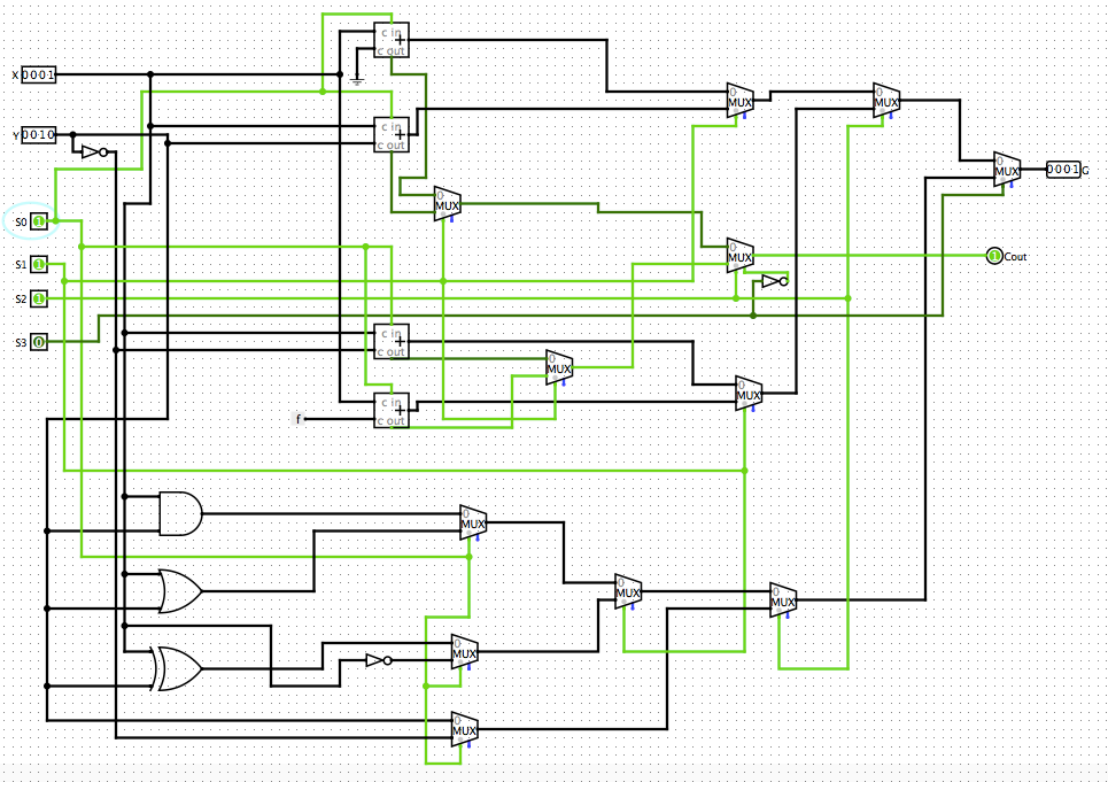
7:

S3	S2	S1	S0	Operation
0	1	1	0	G=X-1



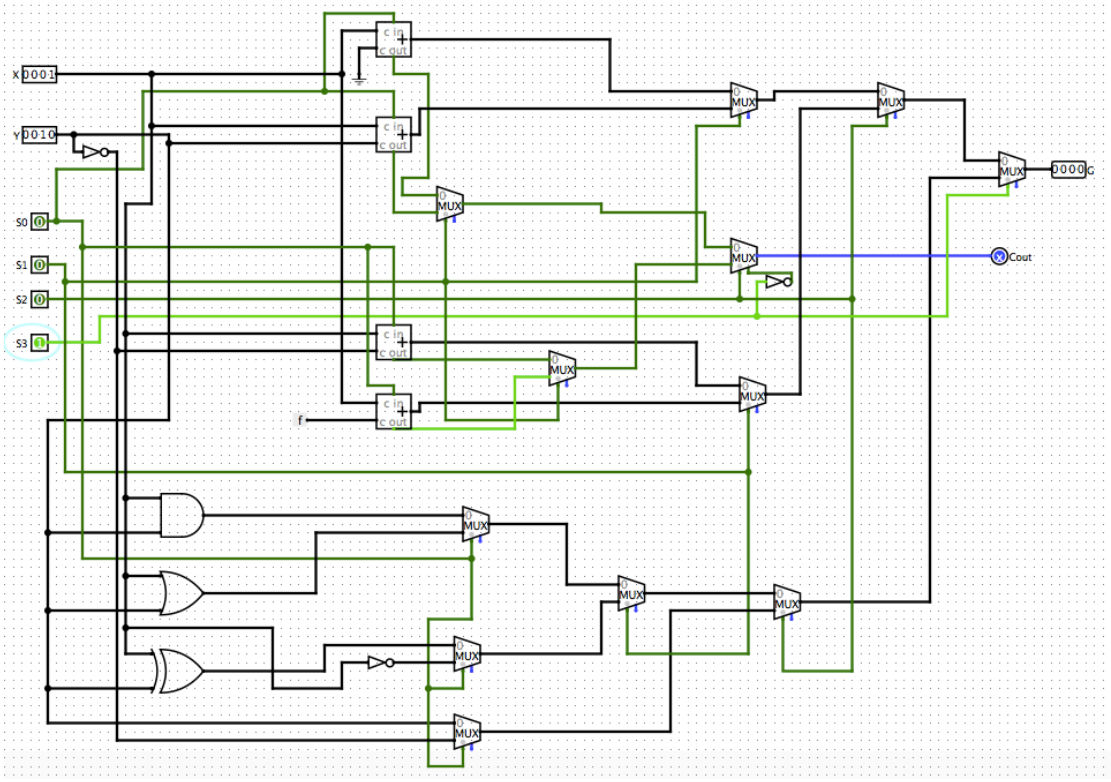
8:

S3	S2	S1	S0	Operation
0	1	1	1	G=X



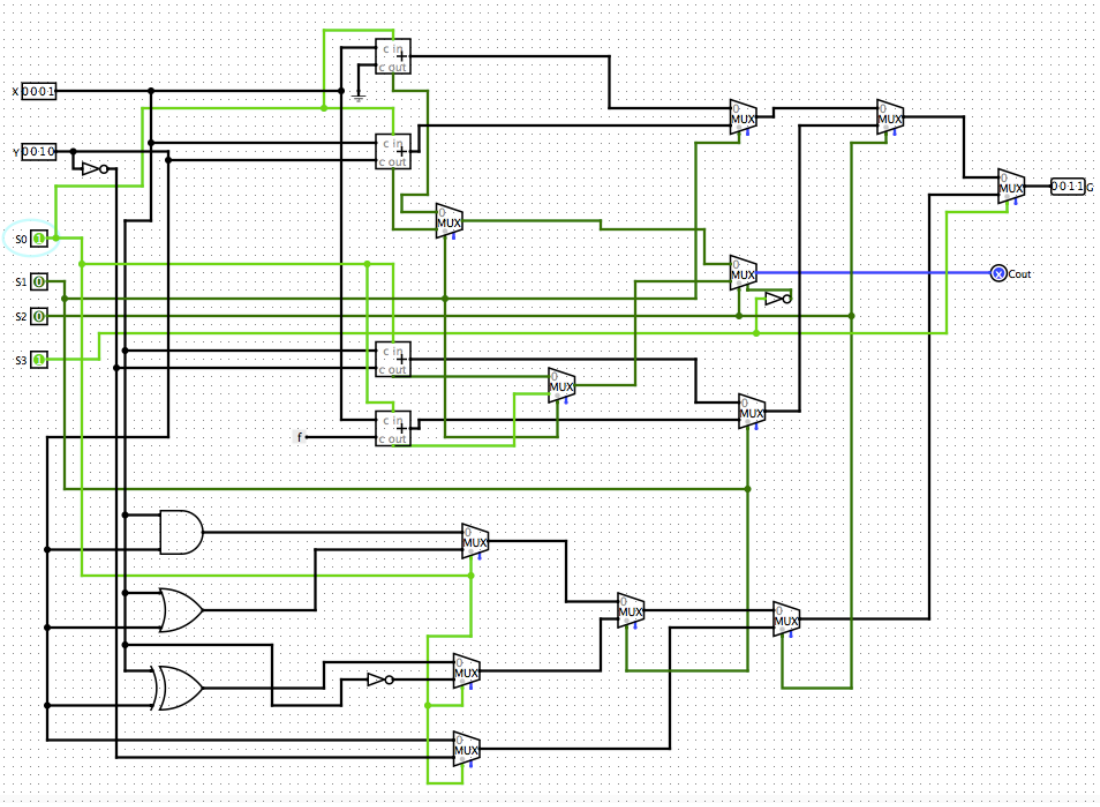
9:

S3	S2	S1	S0	Operation
1	0	0	0	G=X and Y



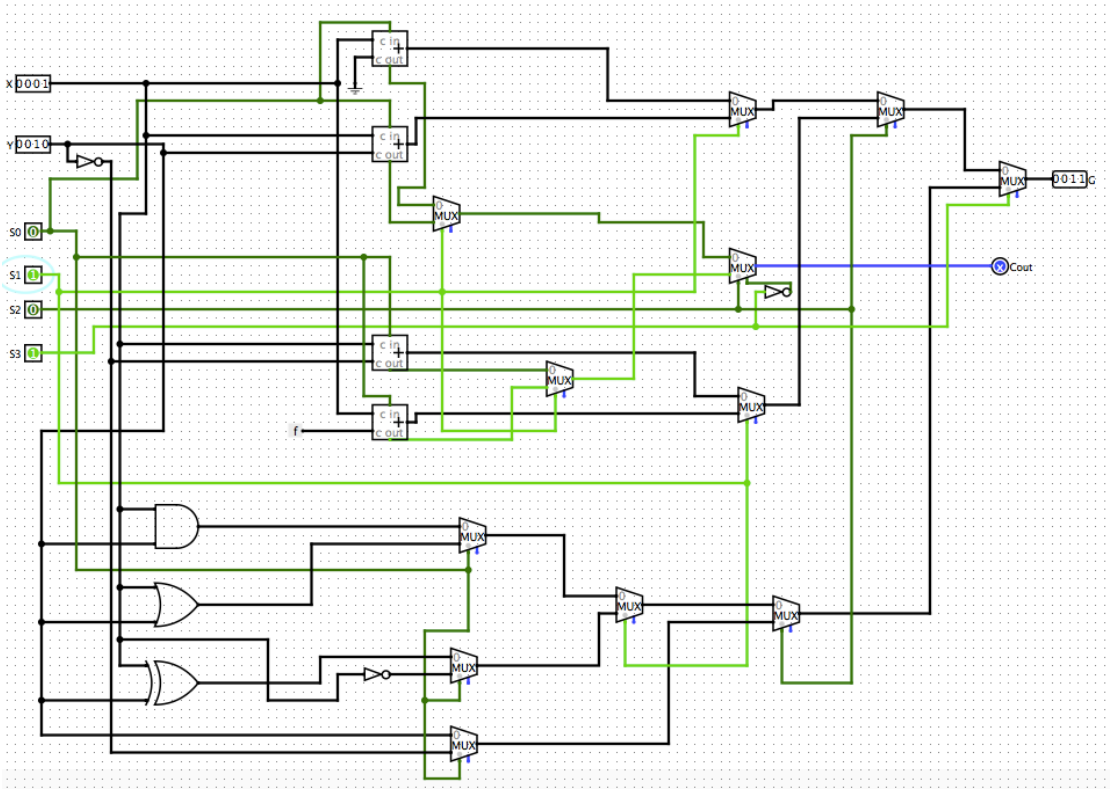
10:

S3	S2	S1	S0	Operation
1	0	0	1	G=X or Y



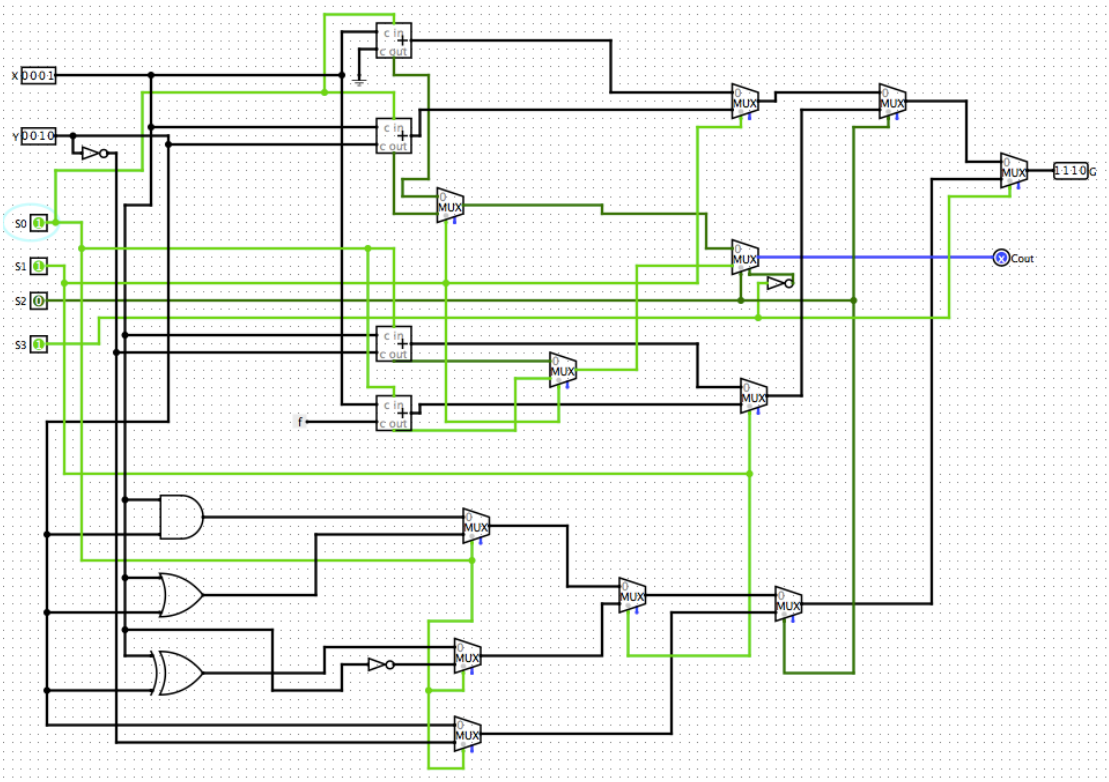
11:

S3	S2	S1	S0	Operation
1	0	1	0	G=X XOR Y



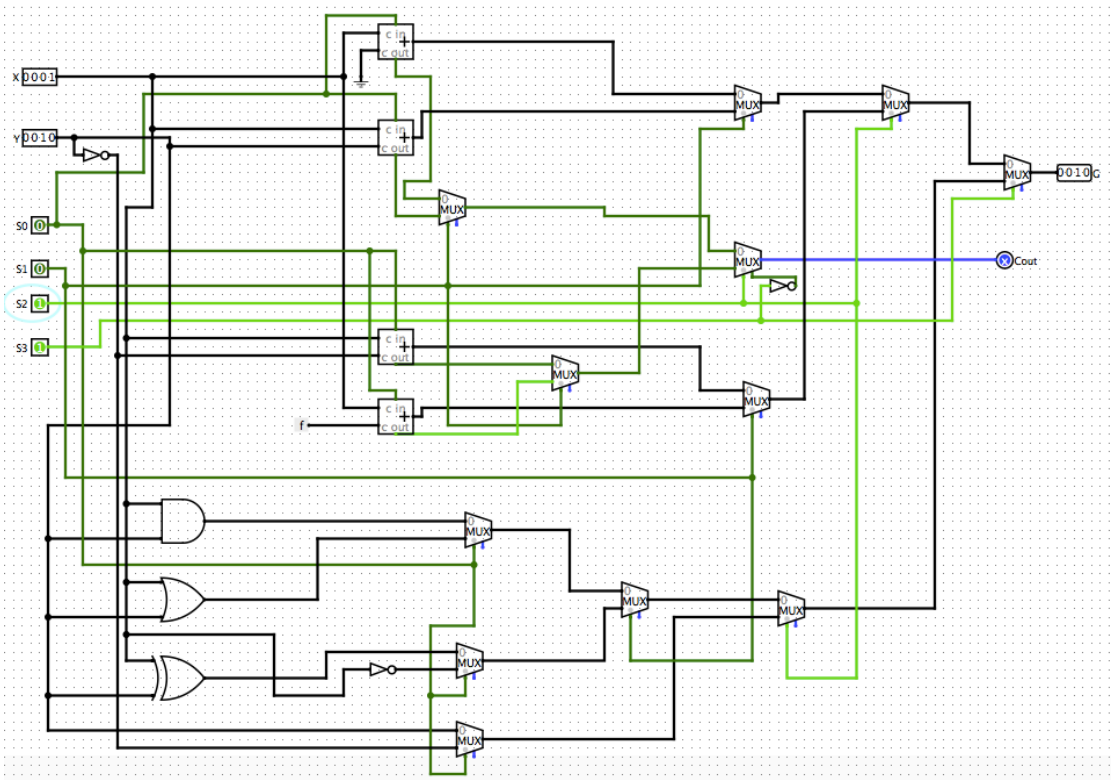
12:

S3	S2	S1	S0	Operation
1	0	1	1	G=X’



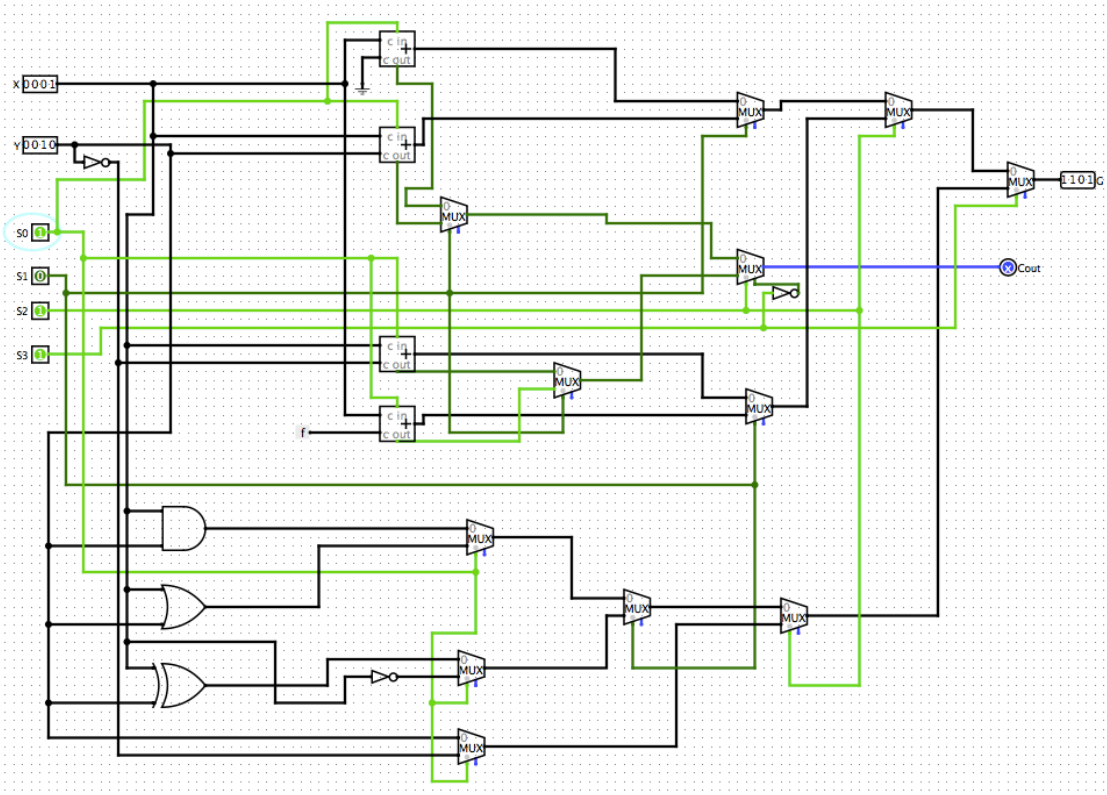
13:

S3	S2	S1	S0	Operation
1	1	0	0	G=Y



14:

S3	S2	S1	S0	Operation
1	1	0	1	G=Y’



The Whole Circuit :