1.

a. Define half adder.

The half adder is a type of combinational logic circuit that adds two of the 1-bit binary digits. It generates carry and sum of both the inputs. The full adder is also a type of combinational logic that adds three of the 1-bit binary digits for performing an addition operation.

b. Draw a truth table for the sum and carry of half adder.

Truth table

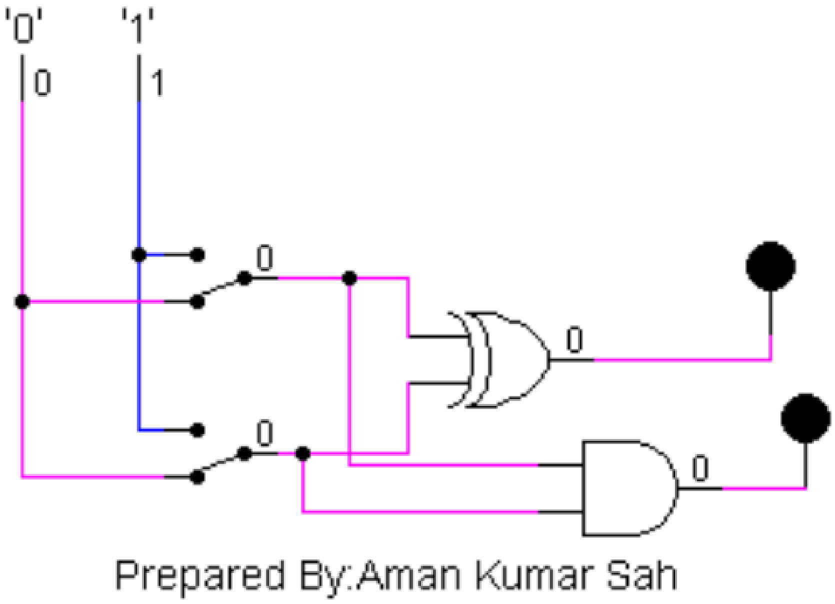
-Input A	-input B	-S(Sum)
0	0	0
0	1	1
1	0	1
1	1	0

c. Write the sop expression from the truth table.

-SOP expresssion sum=AB'+A'B

-SOP expressioin carry=A'B

d. Draw the circuit using logsim.



2.

a. Draw the truth table for the outputs of the full adder

e. Write the corresponding sop expression for sum and carry of full adder and simplify the expression

-A full adder circuit is central to most digital circuit that perform addition or subtraction. It is so called because it adds together two binary digits, plus a carry-in digit to produce a sum and carry-out digit. 1. It therefore has three inputs and two outputs. Truth Table for full Adder:

A	B	C	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	1	1

SOP expression carry =A'BC-AB'C-ABC'+A'B'C'

=A'BC +ABC+ABC+AB'C+ABC'+ABC'

=BC(A+A) +AC(B-B')+AB(C-C')

=AB+BC+AC

SOP expression sum =A'B'C+AB'C+A'BC'+ABC

=A'(B'C+BC')+A(B'C'+BC)

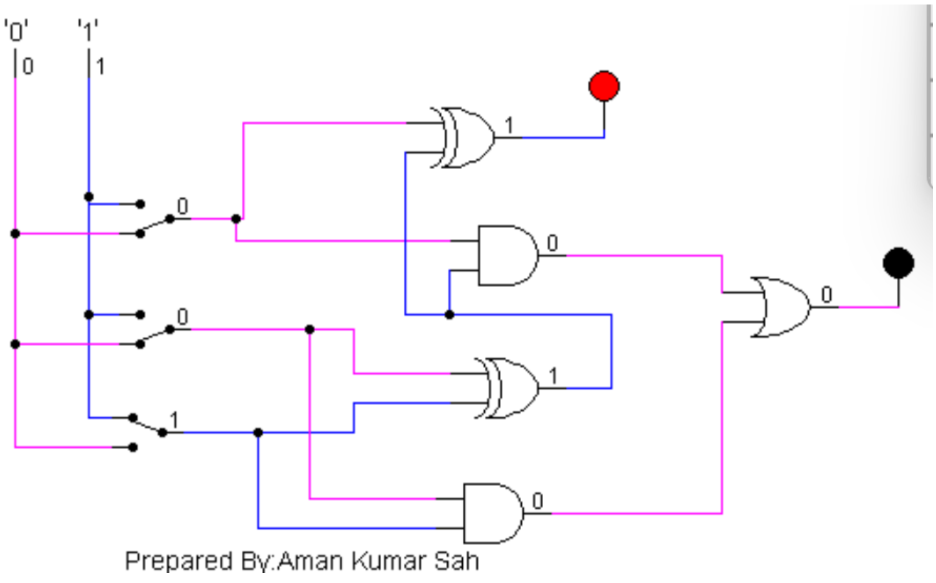
=A'X+AX'

=A OR B OR C

= (B'C+BC-B OR C)

=(B OR C-X)

Draw full adder using two half adder and an OR gate



3. Using the three stages of design, construct the circuits for the following input /output values. Here A, B and C are the inputs whereas D, E, F, G, H and I are outputs. *Note: Draw circuit diagram using logsim corresponding to the simplified expression of outputs D, E, F, G, H and I.*

A	B	C	D	E	F	G	H	I
0	0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	0	1
0	1	0	1	0	1	1	1	1
1	0	0	1	0	0	1	0	1
1	1	1	1	1	1	1	1	1
1	1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	1	0
0	1	1	0	0	0	1	1	1

1) *D=A+B’+C’*

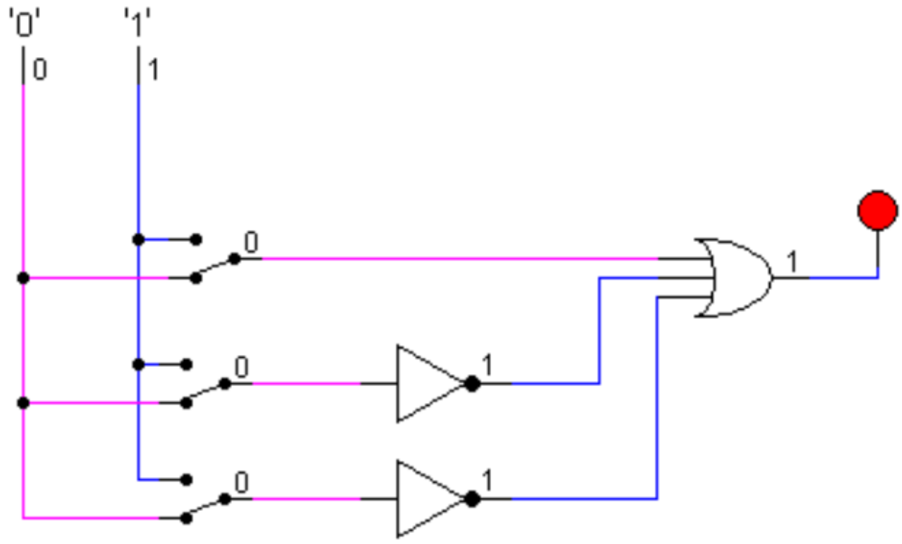


Fig:D=A+B'+C'

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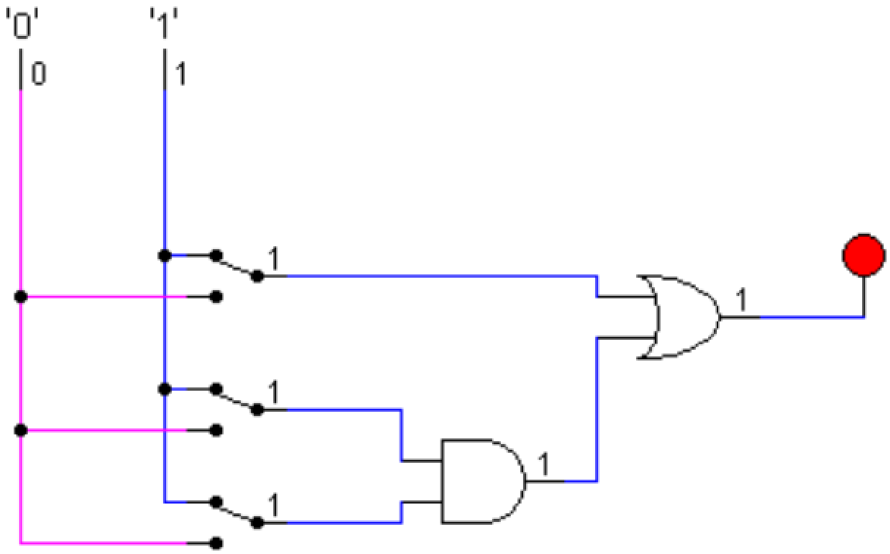
2) E=ABC+ABC'+AB'C

=ABC+ABC'+ABC+AB'C

=AB+AC

=A(B+C)



E=A(B+C)

Prepared By:Aman Kumar Sah

3)F=A'BC'+AB'C=A'BC'+AB'C

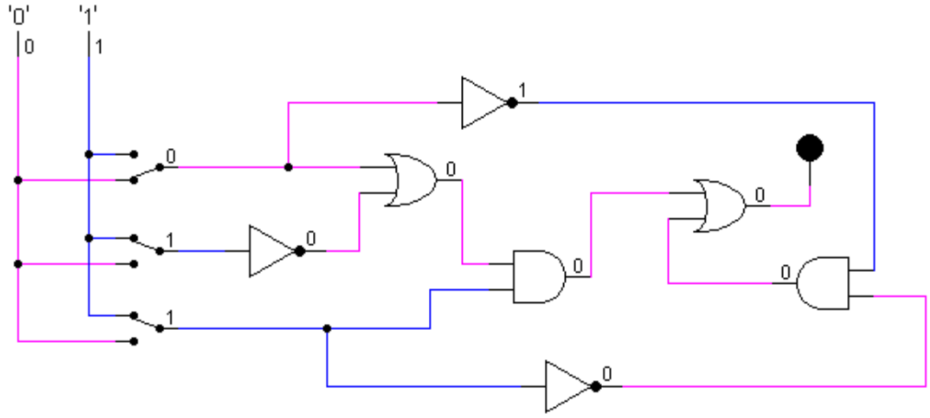
=A'C'(B'+B)+B'C(A'+A)+ABC

=A'C'+B'C+ABC

=A'C'+C'(B+AB)

=A’C’+C(B’+A)(B’+B)

=A’C’+(B’+A)



F:A'C'+C(B'A)

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4)G=A+B+C

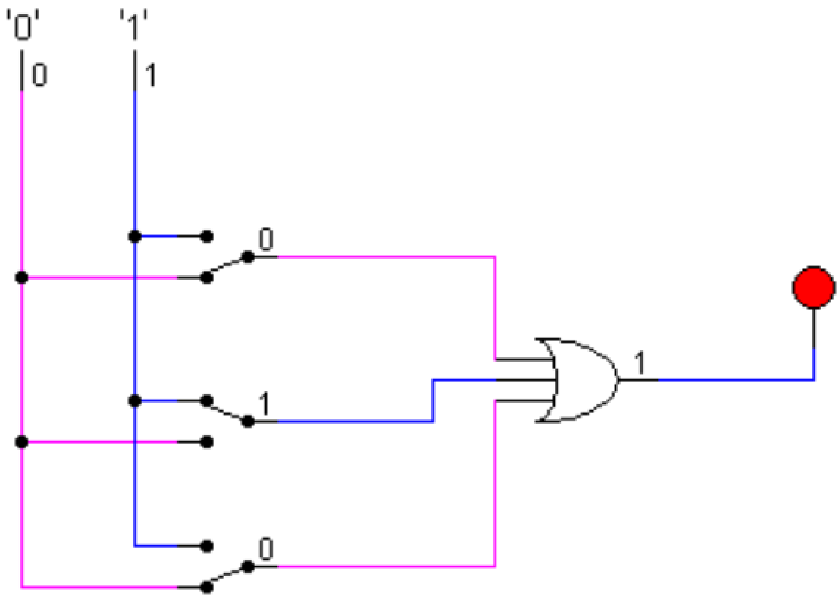

FIG:A+B+C

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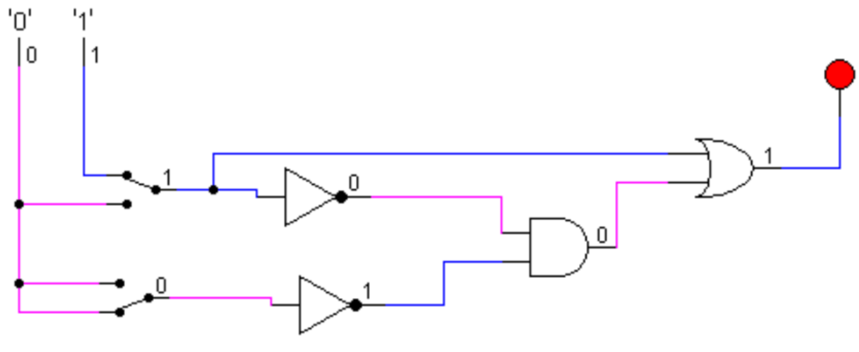
5)H =A’B’C’+A’BC’+ABC+AB’C+AB’C’

=A’C’(B+B’)+AC(B+B’)+A(B’C+BC)

=A’C’+A



H:A'C'+A
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6)I=A’+B+C’

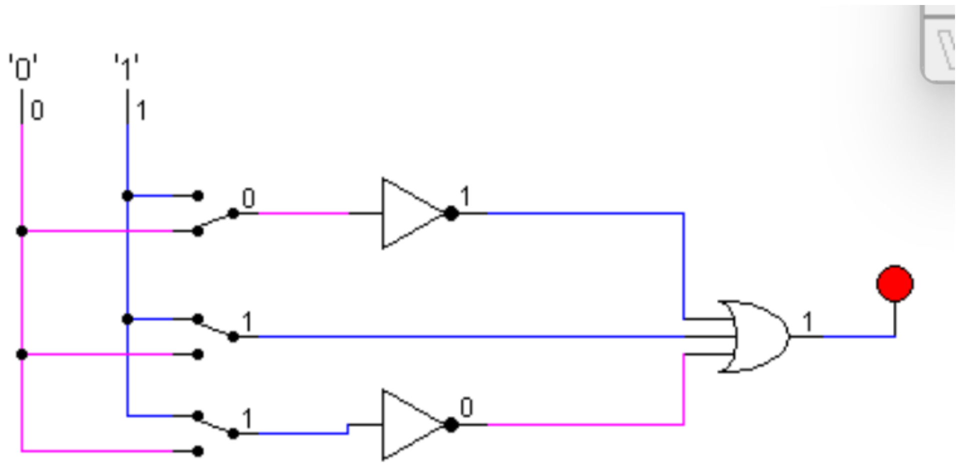

Fig:A'+B+C'
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