1.

a. Define half adder.

The half adder is a type of combinational logic circuit that adds two of the 1-bit binary digits. It generates carry and sum of both the inputs. The full adder is also a type of combinational logic that adds three of the 1-bit binary digits for performing an addition operation.

b. Draw a truth table for the sum and carry of half adder.

Truth table

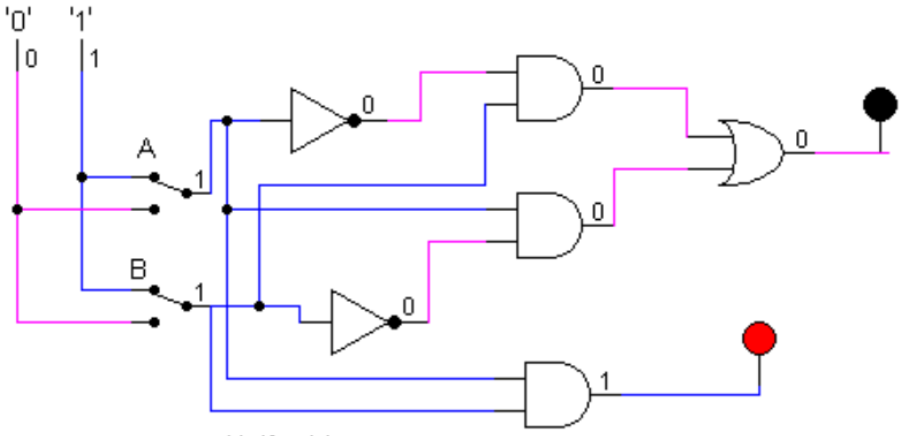
-Input A	-input B	-S(Sum)	Carry
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

c. Write the sop expression from the truth table.

-SOP expresssion sum=A'B+AB'

-SOP expressioin carry=A.B

d. Draw the circuit using logsim.



2.

a. Draw the truth table for the outputs of the full adder

A	B	C	Sum	Carry Out
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	1	1
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	1	1

Write the corresponding sop expression for sum and carry of full adder and simplify the expression

SOP expression sum =A'B’C+A’BC’+AB’C’+ABC

=A’B’C+A’BC’+AB’C’+ABC

=A’(B’C+BC’)+A(B’C’+BC)

=A’(B+C)+A(B+C)

=A’X+AX

=+A+X

Sum=A+B+C

SOP expression carry=A'B'C+AB'C+A'BC'+ABC

=A'BC+AB’C+ABC’+ABC+ABC

=BC(A’+B)+AC(B’+B)+AB(C’+C)

Carry+BC+AC+AB

Draw full adder using two half adder and an OR gate

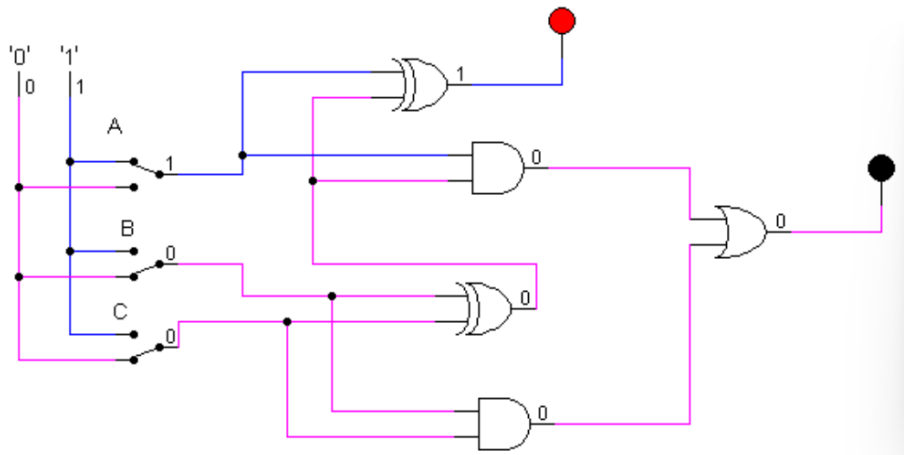


Fig:Full adder
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3. Using the three stages of design, construct the circuits for the following input /output values. Here A, B and C are the inputs whereas D, E, F, G, H and I are outputs. *Note: Draw circuit diagram using logsim corresponding to the simplified expression of outputs D, E, F, G, H and I.*

A	B	C	D	E	F	G	H	I
0	0	0	1	0	1	0	1	1
0	0	1	1	0	1	1	0	1
0	1	0	1	0	1	1	1	1
1	0	0	1	0	0	1	0	1
1	1	1	1	1	1	1	1	1
1	1	0	1	1	0	1	0	1
1	0	1	1	1	1	1	1	0
0	1	1	0	0	0	1	1	1

1) POS Of D=A+B'+C'

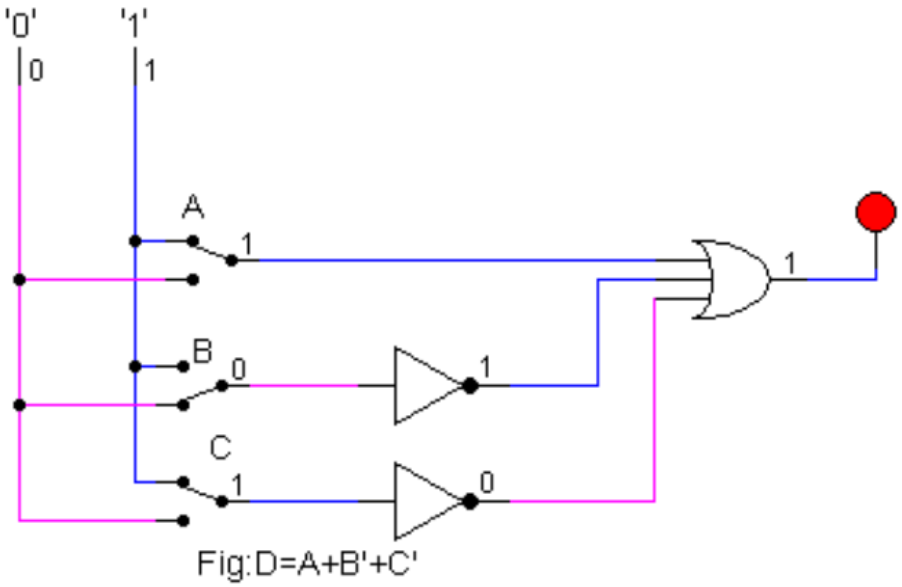

Fig:D=A+B'+C'

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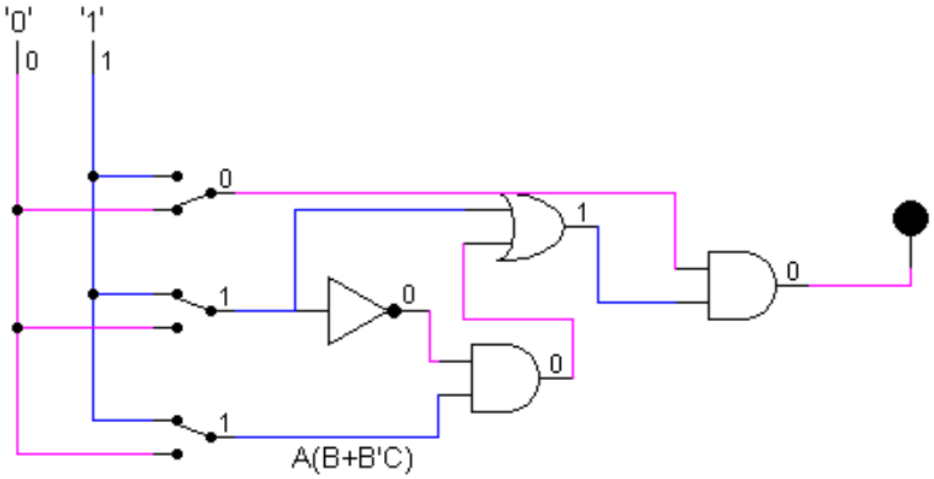
2) E =ABC+ABC'+AB'C

=AB(C+C')+AB'C

=AB+AB'C

=A(B+B'C)



A(B+B'C)

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For F result:

3)F=A'BC'+AB'C=A'BC'+AB'C

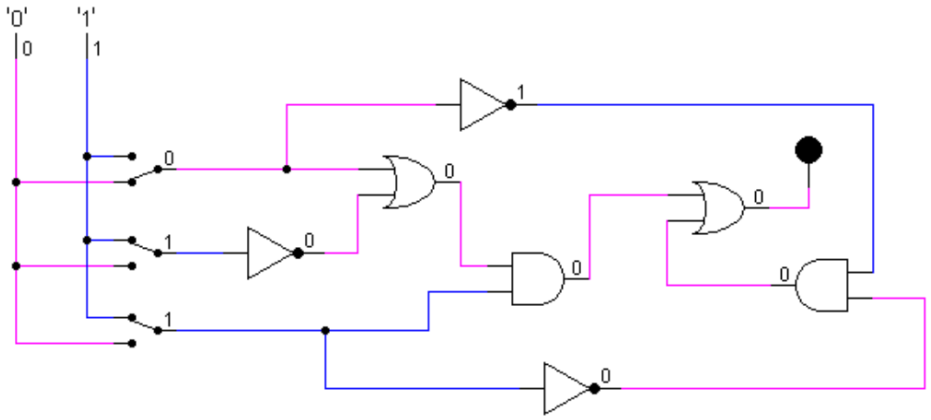
=A’C’(B’+B)+B’C(A’+A)+ABC

=A’C’+B’C+ABC

=A’C’+C’(B+AB)

=A’C’+C(B’+A)(B’+B)

=A’C’+(B’+A)



F:A'C'+C(B'A)

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4)POS of G=A+B+C

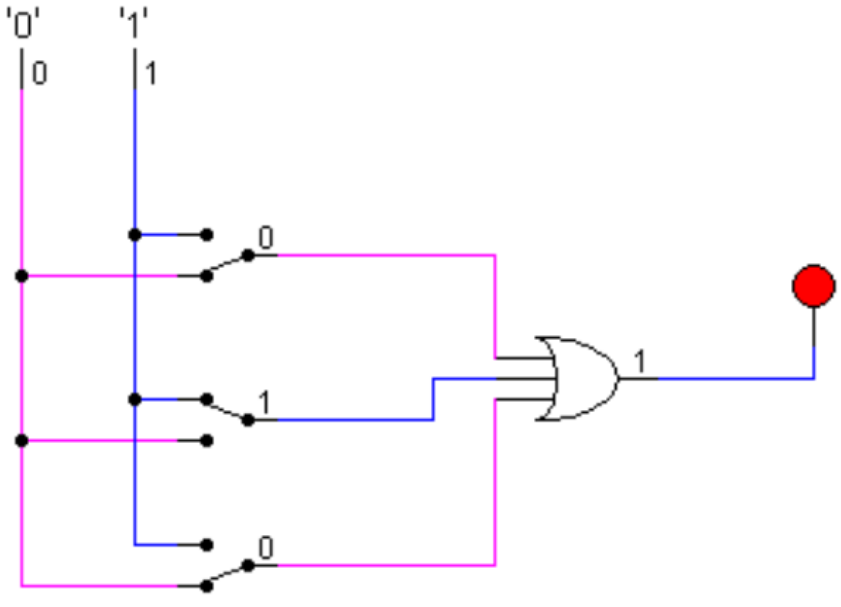

FIG:A+B+C

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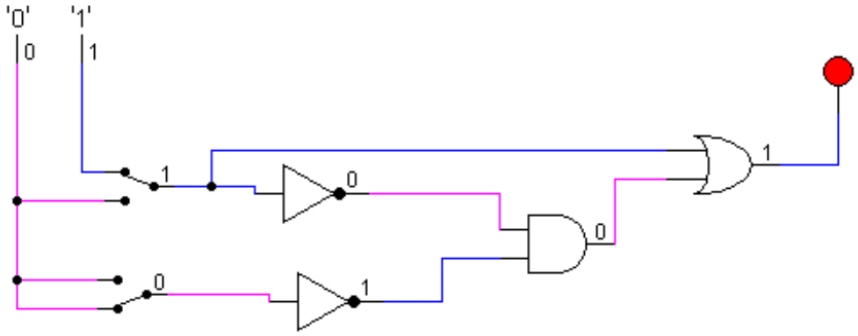
5)H =A’B’C’+A’BC’+ABC+AB’C+AB’C’

=A’C’(B+B’)+AC(B+B’)+A(B’C+BC)

=A’C’+A



H:A'C'+A

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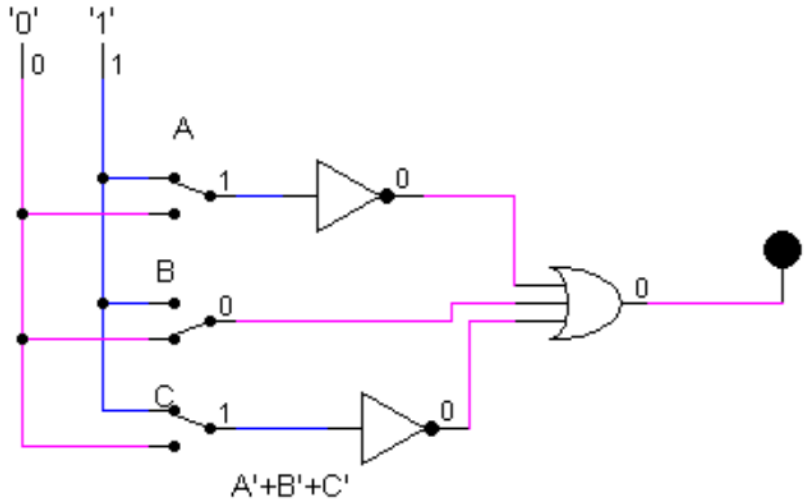
6)POS of I=A’+B+C’



A'+B'+C'

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