**Tests CoolSiC**

סדר בבדיקות שיש לעשות לכל טרנזיסטור:

Core Set of Tests for CoolSiC  
(PWM\_1kHz\_Arduino\_UNO\_R3\_for\_CoolSiC\_V4)

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| Test 1: Gate-Source Voltage (Vgs) Switching Test | |
| Purpose | Verify correct gate drive voltages and switching behavior. |
| Why Important | Ensures proper ON/OFF control of the SiC; prevents damage if wrong voltages are applied. |
| What to Measure | Vgs (Gate–Source voltage) using oscilloscope |
| How to Measure | Probe between Gate and Source. **Not simultaneously** (TP10 to PHASE for HS and TP20 to HV- for LS) OR Safer (use TP10 to GP10 for HS and TP20 to GP20 for LS) |
| What to Expect | Clear square waveform toggling between:  - ON-state: ~+15 V  - OFF-state: ~−2 V  Sharp rising and falling edges. |
| Results | HS shows expected swing from +15 V (ON) to 0.4 V (OFF), and not -2 V as expected (but this happened for the IGBTs as well, the voltage goes somewhere).    LS shows expected swing from +15 V (ON) to −2 V (OFF) Appears symmetric with correct complementary pattern  יש תמונות נוספות עם מתח גבוה פועל, זה משנה – יש overshoot בעיקר לHS. |

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| Test 2: Drain-Source Voltage (Vds) Switching Test | | |
| Purpose | Confirm that the transistor properly switches high voltage side. | |
| Why Important | Vds behavior directly shows if the SiC is conducting or blocking correctly. | |
| What to Measure | Vds (Drain–Source voltage) using oscilloscope. | |
| How to Measure | Probe between Drain (HV+ node) and Source (PHASE) for HS, Drain (PHASE node) and Source (HV-) for LS. | |
| What to Expect | - When SiC ON: Vds low (~?? V) due to Vds,sat  - When OFF: Vds high (~DC supply voltage, ~30 V) | |
| Results | Switching speed is ffine, very fast as expected from SiC), clean edges visible.  Vds near 0 V when ON (confirming low Rds(on)).  Rises to ~30 V (our HV supply).  HS & LS alternation - Implies correct complementary drive (no shoot-through).  Show crisp transitions — SiC responding well to gate drive  A screen shot of a graph  AI-generated content may be incorrect.  HS turns OFF Overshoot ~+3.3 V  A screen shot of a computer  AI-generated content may be incorrect.  HS turns ON Undershoot ~−1.8 V  A screen shot of a graph  AI-generated content may be incorrect.  LS turns OFF Overshoot ~+2.4 V  A screen shot of a graph  AI-generated content may be incorrect.  LS turns ON Undershoot ~−0.4 V  Overshoot and undershoot in switching circuits (especially with SiC MOSFETs) is expected due to:  Fast switching edges (high di/dt)  Parasitic inductance in gate and power loops  Lack of snubbers or insufficient layout decoupling  Overshoot/ Undershoot in acceptable range ≤ ~10%  Frequency is fine - only appears at transitions, not persistent ringing. | |
| Test 3: Phase Node (PHASE) Behavior Test | | |
| Purpose | | Check the switching waveform at the output (PHASE node). |
| Why Important | | ~~PHASE node shows the final combined switching quality; critical for half-bridge operation.~~ The PHASE node is the midpoint between the high-side and low-side switches, and its voltage waveform reflects the half-bridge switching behavior. |
| What to Measure | | Voltage between PHASE and HV−. |
| How to Measure | | Probe across PHASE pin and HV− ground (differential or careful probing). |
| What to Expect | | Clean square wave toggling between near 0 V and near 30 V.  Fast transitions.  Small acceptable ringing. |
| Results | | Full waveform - shows clean transitions between ~0 V and ~30 V, confirming proper half-bridge operation.    Rising edge (LS OFF, HS ON) - shows sharp rising edge from 0 V to 30 V, with very small overshoot ~2 V.  Falling edge (HS OFF, LS ON) - shows fast fall from 30 V to 0 V with mild undershoot ~−1.5 V.  Voltage swing - Full swing from 0 V to 30 V confirms proper complementary drive.  Rise/fall time - Very fast — expected for SiC, indicating excellent switching performance.  Overshoot/Undershoot – Minor, within safe range given our supply voltage and layout.  No abnormal ringing - Suggests good gate drive control and reasonable parasitic inductance. |

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| Test 4: Dead Time Observation | |
| Purpose | Ensure there is a gap between HS turn-OFF and LS turn-ON (and vice versa) — avoid shoot-through. |
| Why Important | Shoot-through can destroy devices instantly. Dead time prevents that. |
| What to Measure | Phase node voltage and/or Vgs of HS/LS together. |
| How to Measure | Two-channel scope: one on HS Vgs, one on LS Vgs. We use 4 channel scope, and Math option..  CH1: Tip to TP10 (HS Gate), Clip to HV− (Vg HS) CH2: Tip to PHASE, Clip to HV−  CH3: Tip to TP20 (LS Gate), Clip to HV− (Vg LS) Math: CH1 minus CH2 = Vg HS minus Vs (PHASE) = Vgs HS Math: CH3 = Vg LS |
| What to Expect | - There must be a short "both OFF" period before switching.  - PHASE should remain floating during dead-time.  (tiny dead-time ~500 ns visible.) |
| Results | Shows the overall PWM behavior for both Vgs\_HS and Vgs\_LS.  Complementary pattern is visible.  Confirms both channels are active and switching.    (HS → LS) Transition  Clear dead time (~800 ns) between HS falling and LS rising  HS turns OFF first, then LS turns ON cleanly, ensures no cross-conduction.    (LS → HS) Transition  No visible dead time between LS turning OFF and HS turning ON, as expected since the hardware limitation of ATmega328P (Uno R3). HS rises too early, before LS finishes falling. Could cause shoot-through at high switching speeds or voltage. |

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| Test 5: Gate Drive Timing Stability | |
| Purpose | Confirm that PWM signals remain consistent, and switching happens at correct times repeatedly. |
| Why Important | Drift or instability can cause switching errors, excessive losses, or shoot-through over time. |
| What to Measure | Vgs waveform stability over multiple periods. |
| How to Measure | Observe Vgs over milliseconds timescale (long timescale). Probes setup is the same as Test 4.. |
| What to Expect | Consistent ON and OFF pulse widths matching PWM setup (?? kHz switching frequency, 50% duty cycle by default).  No drift or glitches. |
| Results | Period stability - PWM waveform is consistently 1 ms (1 kHz) across cycles.  Vgs +15 V (ON), −2 V (OFF), almost clearly reached and maintained.  Switching symmetry - Transitions are symmetrical in shape and spacing.    Overshoot at turn-on (HS & LS) –  ~+6 V above +15 V → peaks at ~21 V, Significant — must be checked against Vgs(max) = ±25 V for CoolSiC devices    Undershoot at turn-off (HS & LS) -  Dips below ~−5 V, Getting close to or slightly exceeding safe negative gate threshold.  We shell consider reducing overshoot via snubber / gate resistor tuning. |

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| Test 6: Soft Turn-Off Behavior (Optional for Now)  Note:  This test is a bit risky if not prepared properly.  You can skip it initially and revisit once the basic switching behavior is confirmed. | |
| Purpose | Confirm soft turn-off feature of gate driver when a desaturation event occurs. |
| Why Important | Soft-off limits Vce overshoot during short-circuit faults; important for device protection. |
| What to Measure | Gate voltage falling slope during a fault. |
| How to Measure | Intentionally simulate a fault (short HV+ to PHASE temporarily) under controlled conditions. ?? |
| What to Expect | During DESAT detection, Vge falls gradually (softly), not immediately.  Scope shows a sloped fall instead of an instant drop. |

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| Test 7: Short-Circuit Turn-Off ??? Later | |
| Purpose |  |
| Why Important |  |
| What to Measure |  |
| How to Measure |  |
| What to Expect |  |

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| Test ??: | |
| Purpose |  |
| Why Important |  |
| What to Measure |  |
| How to Measure |  |
| What to Expect |  |