**Tests IGBT**

סדר בבדיקות שיש לעשות לכל טרנזיסטור:

Core Set of Tests for IGBTs

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| Test 1: Gate-Emitter Voltage (Vge) Switching Test | |
| Purpose | Verify correct gate drive voltages and switching behavior. |
| Why Important | Ensures proper ON/OFF control of the IGBT; prevents damage if wrong voltages are applied. |
| What to Measure | Vge (Gate–Emitter voltage) using oscilloscope |
| How to Measure | Probe between Gate and Emitter ~~(use TP10–PHASE or TP20–PHASE depending on HS or LS).~~**Not simultaneously** (TP10 to PHASE for HS and TP20 to HV- for LS) OR Safer (use TP10 to GP10 for HS and TP20 to GP20 for LS) |
| What to Expect | Clear square waveform toggling between:  - ON-state: ~+15 V  - OFF-state: ~−7.5 V  Sharp rising and falling edges. Note: for the HS +15 to -5.4 V (2V go somewhere, or the way of measuring isn’t accurate. But at least persistence..) |
| Results | A screen shot of a graph  AI-generated content may be incorrect.  HS: Observations:  Clear square waveform.  Levels toggle between +15 V and −7.5 V.  Sharp transitions.  Duty cycle and timing look consistent with PWM setup. Conclusion:  High-Side gate drive is working correctly.  Floating gate drive across PHASE works properly.  -----------  A screen shot of a computer  AI-generated content may be incorrect.  A screen shot of a computer  AI-generated content may be incorrect.  LS: Observations:  Clear square waveform.  Levels toggle between approximately +15 V and −7.5 V.  Sharp rising and falling edges — no visible glitches.  Pulse width matches expected 1 kHz frequency (~500 µs ON, ~500 µs OFF at 50% duty cycle). Conclusion:  Low-Side gate drive is working correctly.  No signal integrity problems. |
| PWM update | יש תמונות מעודכנות אבל הן מאוד דומות להנ"ל. |

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| Test 2: Collector-Emitter Voltage (Vce) Switching Test | |
| Purpose | Confirm that the transistor properly switches high voltage side. |
| Why Important | Vce behavior directly shows if the IGBT is conducting or blocking correctly. |
| What to Measure | Vce (Collector–Emitter voltage) using oscilloscope. |
| How to Measure | Probe between Collector (HV+ node) and Emitter (PHASE) for HS, Collector (PHASE node) and Emitter (HV-) for LS. |
| What to Expect | - When IGBT ON: Vce low (~2–4 V) due to Vce,sat  - When OFF: Vce high (~DC supply voltage, ~30 V) |
| Results | A screen shot of a computer  AI-generated content may be incorrect.  HS:  Observations:  Clear switching waveform.  Voltage toggles between:  ~2–4 V (ON state) → when HS conducts, small Vce,sat.  ~30 V (OFF state) → when HS blocks, full HV across it.  Clean rising and falling edges.  Tiny overshoot or ringing — normal.  Vge and Vce together:  A screenshot of a computer  AI-generated content may be incorrect.  ------  A screen shot of a computer  AI-generated content may be incorrect.  A screen shot of a computer  AI-generated content may be incorrect.  A screen shot of a graph  AI-generated content may be incorrect.  A screen shot of a computer  AI-generated content may be incorrect.  LS: Observations:  Clear square waveform.  Voltage toggles between:  ~2–4 V (ON state) as expected Vce,sat for LS IGBT.  ~30 V (OFF state) → matches HV bus voltage.  Sharp, clean switching edges.  Some tiny overshoot during transitions — normal and acceptable.  Vge and Vce together:  A screen shot of a computer  AI-generated content may be incorrect. |
| PWM updatde | יש תמונות מעודכנות אבל הן מאוד דומות להנ"ל. |

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| Test 3: Phase Node (PHASE) Behavior Test | |
| Purpose | Check the switching waveform at the output (PHASE node). |
| Why Important | PHASE node shows the final combined switching quality; critical for half-bridge operation. |
| What to Measure | Voltage between PHASE and HV−. |
| How to Measure | Probe across PHASE pin and HV− ground (differential or careful probing). |
| What to Expect | Clean square wave toggling between near 0 V and near 30 V.  Fast transitions.  Small acceptable ringing. |
| Results | Observations:  Cclean square waveform.  Voltage toggles cleanly between:  Near 0 V (Low state)  Near 30 V (High state)  Very sharp rising and falling edges.  A very small flat time between transitions — indicating presence of dead-time.  PHASE node shows healthy switching.  No evidence of shoot-through or abnormal distortion.  Minor overshoot (small bumps) during transitions — acceptable at this voltage level.  A screen shot of a computer  AI-generated content may be incorrect.  A tiny "plateau" where PHASE stays floating — this is the dead-time.  Then a sharp transition to High or Low.  No large voltage spikes or oscillations visible.  The transition edges are steep, confirming good driver control.  Conclusion:  Dead-time is clearly visible and working properly.  Transitions are well-controlled.  No excessive ringing or abnormal behavior. |

Before test No.4:  
- Switch to SIGLENT SDS1104CFL — a 4-channel digital scope  
- Probes x10  
- CH on scope x10

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| Test 4: Dead Time Observation | |
| Purpose | Ensure there is a gap between HS turn-OFF and LS turn-ON (and vice versa) — avoid shoot-through. |
| Why Important | Shoot-through can destroy devices instantly. Dead time prevents that. |
| What to Measure | Phase node voltage and/or Vge of HS/LS together. |
| How to Measure | Two-channel scope: one on HS Vge, one on LS Vge. ? We can do it with our setup scope? We switched to 4 channel scope, and used Math..  CH1: Tip to TP10 (HS Gate), Clip to HV− (Vg HS) CH2: Tip to PHASE, Clip to HV−  CH3: Tip to TP20 (LS Gate), Clip to HV− (Vg LS) Math: CH1 minus CH2 = Vg HS minus Ve (PHASE) = Vge HS Math: CH3 = Vg LS |
| What to Expect | - There must be a short "both OFF" period before switching.  - PHASE should remain floating during dead-time.  (tiny dead-time ~100–200 ns visible.) |
| Results | A screen shot of a graph  AI-generated content may be incorrect.  Repeated PWM switching cycles.  MATH (Pink, Vge\_HS) and CH3 (Green, Vge\_LS) are complementary.  The general timing looks mostly correct at first glance.  A screen shot of a graph  AI-generated content may be incorrect.  Left side looks suspicious, right side looks fine.  A screen shot of a graph  AI-generated content may be incorrect.  Observations:  Vge\_HS (Pink) falls sharply from ~ +15 V to -7.5 V.  After about 6.25 µs delay (measured and planned), Vge\_LS (Green) starts rising.  No overlap between HS OFF and LS ON — there is a proper dead-time.  Conclusion:  Dead-time between HS OFF and LS ON is good (~6.25 µs).  A screen shot of a graph  AI-generated content may be incorrect.  Observations:  Vge\_LS (Green) is still HIGH (ON) when Vge\_HS (Pink) starts rising back from ~ -7.5 V to +15 V 🡪 HS starts to turn ON before LS is fully OFF 🡪 This is wrong — it creates a potential overlap, risking shoot-through…  Problem detected:  There is no dead-time (or too small dead-time) between LS turning OFF and HS turning ON.  Or worse: HS starts ON before LS fully turns OFF.  Shoot-through risk exists under this condition!!! The problem is in the Arduino PWM code, we only "push" dead-time by adjusting OCR1A and OCR1B with an offset around 50%.  This introduces dead-time correctly on one edge (HS OFF → LS ON),  but **not** symmetrically on the other edge (LS OFF → HS ON).  גם כאשר מגידילם את הזמן המת או מכניסים אותו בצורה אסימטרית, זה לא פותר את הבעיה, רק מגדיל את הזמן המת במעבר HS אל LS והמעבר LS אל HS נישאר בעייתי.. יש פירוט על הבעיה בדוקומנטציה ... שורה תחתונה קוד PWM חדש מנוון.. תכלס צריך לעשות את כל הבדיקות מחדש \: ברדק.. אולי נמשיך.. אולי זו הזדמנות לשגע את מאור עם זה..  אחרי תיקון של PWM – דרך מנוונת  (switched from hardware PWM to manual (bit-banged) PWM)  A screen shot of a computer  AI-generated content may be incorrect.  Clean complementary waveforms  Dead-time visible  Good spacing between transitions  A screen shot of a graph  AI-generated content may be incorrect.  Vge\_HS (MATH-Pink) falling  Dead-Time (~11 µs)  Vge\_LS (CH3-Green) rising  Confirmed clean HS → LS transition  A screen shot of a graph  AI-generated content may be incorrect.  Vge\_LS (CH3-Green) falling  Gap (~11 µs)  Vge\_HS (MATH-Pink) rising  Confirmed clean LS → HS transition  Perfect symmetric dead-time in both directions. |

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| Test 5: Gate Drive Timing Stability | |
| Purpose | Confirm that PWM signals remain consistent, and switching happens at correct times repeatedly. |
| Why Important | Drift or instability can cause switching errors, excessive losses, or shoot-through over time. |
| What to Measure | Vge waveform stability over multiple periods. |
| How to Measure | Observe Vge over milliseconds timescale (long timescale). Probes setup is the same as Test 4.. |
| What to Expect | Consistent ON and OFF pulse widths matching PWM setup (1 kHz switching frequency, 50% duty cycle by default).  No drift or glitches. |
| Results | ~4 full PWM cycles, Vge levels look clean and stable, Period is consistent (1 ms per cycle, as expected at 1 kHz).    Hold stable at expected ~+15 V (ON) and ~−7.5 V (OFF) Pulse width visually consistent (≈487 µs) Symmetric and steady (~11 µs), unchanged over cycles All waveforms are virtually identical No significant ringing, no shift, no drift    Noticeable overshoot (~4V) above +15 V before settling, for both gates **turn on**. (Classic gate ringing — due to parasitics (inductance + gate loop impedance).)  Undershoot below −7.5 V.  LS stronger than HS turn-off.  (Suggests more inductive kickback or ground bounce in LS loop.) |

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| Test 6: Soft Turn-Off Behavior (Optional for Now)  Note:  This test is a bit risky if not prepared properly.  You can skip it initially and revisit once the basic switching behavior is confirmed. | |
| Purpose | Confirm soft turn-off feature of gate driver when a desaturation event occurs. |
| Why Important | Soft-off limits Vce overshoot during short-circuit faults; important for device protection. |
| What to Measure | Gate voltage falling slope during a fault. |
| How to Measure | Intentionally simulate a fault (short HV+ to PHASE temporarily) under controlled conditions. ?? |
| What to Expect | During DESAT detection, Vge falls gradually (softly), not immediately.  Scope shows a sloped fall instead of an instant drop. |

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| Test 7: Short-Circuit Turn-Off ??? Later | |
| Purpose |  |
| Why Important |  |
| What to Measure |  |
| How to Measure |  |
| What to Expect |  |

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| Test ??: | |
| Purpose |  |
| Why Important |  |
| What to Measure |  |
| How to Measure |  |
| What to Expect |  |