**Test USiC**

סדר בבדיקות שיש לעשות לכל טרנזיסטור:

Core Set of Tests for USiC  
PWM\_1kHz\_Arduino\_UNO\_R3\_for\_USiC\_V2\_basic\_code\_both\_sides\_micro\_dead-time  
Practically ~4us and ~8us dead-time

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| Test 0: Arduino signals | |
| Purpose | Verify correct switching behavior and dead time. |
| Why Important | Because |
| What to Measure | D9 (INP\_H) and D10 (INP\_L) w.r.t SGND |
| How to Measure | At first check the Arduino signals flow – D9 to GND and D10 to GND. TP1 to GP1 (INPH to SGND) and TP11 to GP1 (INPL to SGND). (INP\_H flow : TP6 to GP6 and TP7 to GP6 and TP10 to GP6) (INP\_L flow : TP16 to GP16 and TP17 to GP16 and TP20 to GP16) |
| What to Expect | Clear square waveform toggling between:  - ON-state: +5 V  - OFF-state: 0 V  Sharp rising and falling edges, and dead time. |
| Results | 4.6us dead-time    8.4us dead-time  While the frequency and duty cycle are within expected ranges, the dead time measurements indicate asymmetry and longer durations than configured. This discrepancy is attributed to the software-based PWM generation's limitations on the Arduino Uno R3, which lacks precise timing control for such short intervals. |

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| Test 1: Gate-Source Voltage (Vgs) Switching Test | |
| Purpose | Verify correct gate drive voltages and switching behavior. |
| Why Important | Ensures proper ON/OFF control of the SiC; prevents damage if wrong voltages are applied. |
| What to Measure | Vgs (Gate–Source voltage) using oscilloscope |
| How to Measure | Probe between Gate and Source. **Not simultaneously** (TP10 to PHASE for HS and TP20 to HV- for LS) |
| What to Expect | Clear square waveform toggling between:  - ON-state: ~+15 V  - OFF-state: ~−2 V  Sharp rising and falling edges. |
| Results | HS With the high voltage **off** - Not getting to -2V, gate clamping? Zener diode?    D    D    D    D    D    LS does go to -2 even while high voltage is off..    D    D    d    d    d  With high voltage ON, the values confirm that both the high-side and low-side gate drivers deliver:  Proper positive Vgs turn-on voltages (>+15 V)  Proper negative Vgs turn-off voltages (<−2 V)  The slight difference in peak voltages is likely due to:  Different parasitics (loop inductance, gate trace layout)  Small offset or calibration mismatch in differential probe/scope  Overall: The gate drive performance is robust and symmetric |

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| Test 2: Drain-Source Voltage (Vds) Switching Test | |
| Purpose | Confirm that the transistor properly switches high voltage side. |
| Why Important | Vds behavior directly shows if the SiC is conducting or blocking correctly. |
| What to Measure | Vds (Drain–Source voltage) using oscilloscope. |
| How to Measure | Probe between Drain (HV+ node) and Source (PHASE) for HS, Drain (PHASE node) and Source (HV-) for LS. |
| What to Expect | - When SiC ON: Vds low (~2 V) due to Vds,sat  - When OFF: Vds high (~DC supply voltage, ~30 V) |
| Results | HS  LS For both: Transition Range is good: ~30 V (OFF) → ~-0.5 V (ON)  Fall/Rise Time: Appears sharp and clean.  Saturation Voltage: ON-state Vds settles around ~-0.5 V — good for a SiC MOSFET at 1.5 A load.  There are more results and zoom for this test (Vgs-Vds) etc. Maybe add |

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| Test 3: Phase Node (PHASE) Behavior Test | |
| Purpose | Check the switching waveform at the output (PHASE node). |
| Why Important | PHASE node shows the final combined switching quality; critical for half-bridge operation. |
| What to Measure | Voltage between PHASE and HV−. |
| How to Measure | Probe across PHASE pin and HV− ground (differential or careful probing). |
| What to Expect | Clean square wave toggling between near 0 V and near 30 V.  Fast transitions.  Small acceptable ringing. |
| Results | Clean Switching Behavior - confirms proper alternation of high-side and low-side conduction. A screen shot of a computer  AI-generated content may be incorrect.  zoom    The transition from ~0 V to ~30 V appears clean, fast, and low in ringing. There's a slight overshoot above ≈2 V, typical for hard switching, but well within expected behavior for SiC devices.  A screen shot of a graph  AI-generated content may be incorrect.  The transition from 30 V to 0 V is clean, though it may show slightly more ringing than the rising edge. This asymmetry is often due to layout parasitics or diode reverse recovery effects.  The clean PHASE waveform is strong evidence that:  The complementary PWM and dead time settings (even if imperfectly symmetric) safely avoid shoot-through.  The gate drive strength is sufficient for switching USiC devices at this frequency and voltage.  PCB layout and decoupling are doing a decent job suppressing excessive ringing. |

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| Test 4: Dead Time Observation | |
| Purpose | Ensure there is a gap between HS turn-OFF and LS turn-ON (and vice versa) — avoid shoot-through. |
| Why Important | Shoot-through can destroy devices instantly. Dead time prevents that. |
| What to Measure | Phase node voltage and/or Vgs of HS/LS together. |
| How to Measure | Two-channel scope: one on HS Vgs, one on LS Vgs. We use 4 channel scope, and Math option..  CH1: Tip to TP10 (HS Gate), Clip to HV− (Vg HS) CH2: Tip to PHASE, Clip to HV−  CH3: Tip to TP20 (LS Gate), Clip to HV− (Vg LS) Math: CH1 minus CH2 = Vg HS minus Vs (PHASE) = Vgs HS Math: CH3 = Vg LS |
| What to Expect | - There must be a short "both OFF" period before switching.  - PHASE should remain floating during dead-time.  (tiny dead-time ~?? ns visible.) |
| Results | Only pink(Vgs\_HS) and green(Vgs\_LS)    This confirms enforced dead time on HS → LS transition ~4.4us.  Timing is clean, no overlap, avoiding shoot-through.    Dead time is visible, but longer than the opposite direction ~8.4us.  Likely caused by the asymmetry of software-based delays or timing resolution limitations in the micros() loop-based PWM implementation. |

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| Test 5: Gate Drive Timing Stability | |
| Purpose | Confirm that PWM signals remain consistent, and switching happens at correct times repeatedly. |
| Why Important | Drift or instability can cause switching errors, excessive losses, or shoot-through over time. |
| What to Measure | Vgs waveform stability over multiple periods. |
| How to Measure | Observe Vgs over milliseconds timescale (long timescale). Probes setup is the same as Test 4.. |
| What to Expect | Consistent ON and OFF pulse widths matching PWM setup (?? kHz switching frequency, 50% duty cycle by default).  No drift or glitches. |
| Results | Both exceeds the typical +15 V/−2 V range, possibly stressing the gate oxide — should be clamped or limited if this isn't intentional.    zoom    No visible dead time…    Apparent overlap - Most likely a triggering or sampling artifact (STOP is pressed before zoom in the scope) |

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| Test 6: Soft Turn-Off Behavior (Optional for Now)  Note:  This test is a bit risky if not prepared properly.  You can skip it initially and revisit once the basic switching behavior is confirmed. | |
| Purpose | Confirm soft turn-off feature of gate driver when a desaturation event occurs. |
| Why Important | Soft-off limits Vce overshoot during short-circuit faults; important for device protection. |
| What to Measure | Gate voltage falling slope during a fault. |
| How to Measure | Intentionally simulate a fault (short HV+ to PHASE temporarily) under controlled conditions. ?? |
| What to Expect | During DESAT detection, Vge falls gradually (softly), not immediately.  Scope shows a sloped fall instead of an instant drop. |

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| Test 7: Short-Circuit Turn-Off ??? Later | |
| Purpose |  |
| Why Important |  |
| What to Measure |  |
| How to Measure |  |
| What to Expect |  |

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| Test ??: | |
| Purpose |  |
| Why Important |  |
| What to Measure |  |
| How to Measure |  |
| What to Expect |  |