Department of Computer Science and Engineering
Pandit Deendayal Energy University
Digital Electronics and Computer Organization Lab – **20CP203P**

Lab 6: Designing of Multiplexer, Demultiplexer, Decoder, Encoder

Question 1: Write a Verilog code to design a 4:1 Multiplexer and verify the same.

Question 2: Write a Verilog code to design an 8:1 Multiplexer and verify the same.

Question 3: Write a Verilog code to design a 1:4 Demultiplexer and verify the same.

Question 4: Write a Verilog code to design a 1:8 Demultiplexer and verify the same.

Question 5: Write a Verilog code to design a 3:8 Decoder and verify the same.

Question 6: Write a Verilog code to design a 8:3 Encoder and verify the same.

- Multiplexer is a data selector which takes several inputs and gives a single output. In multiplexer we have 2^n input lines and 1 output lines where n is the number of selection lines.

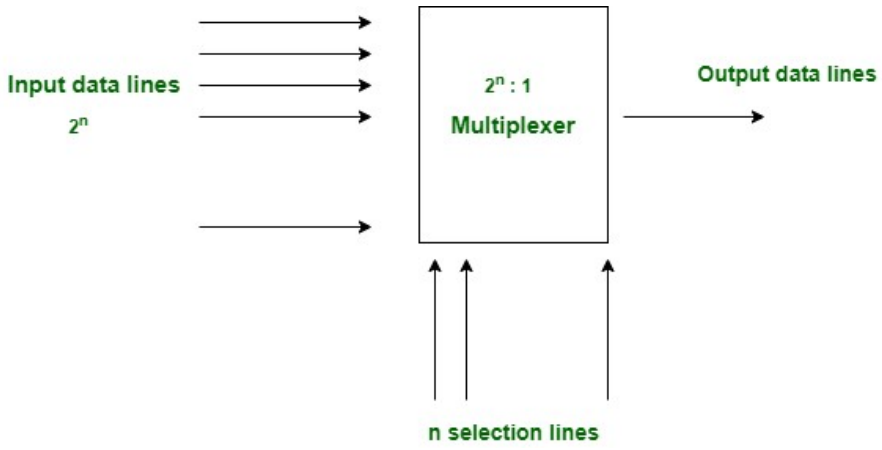

Figure 1: The Block Diagram of Multiplexer.

- Demultiplexer is a data distributor which takes a single input and gives several outputs. In demultiplexer we have 1 input and 2^n output lines where n is the selection line.

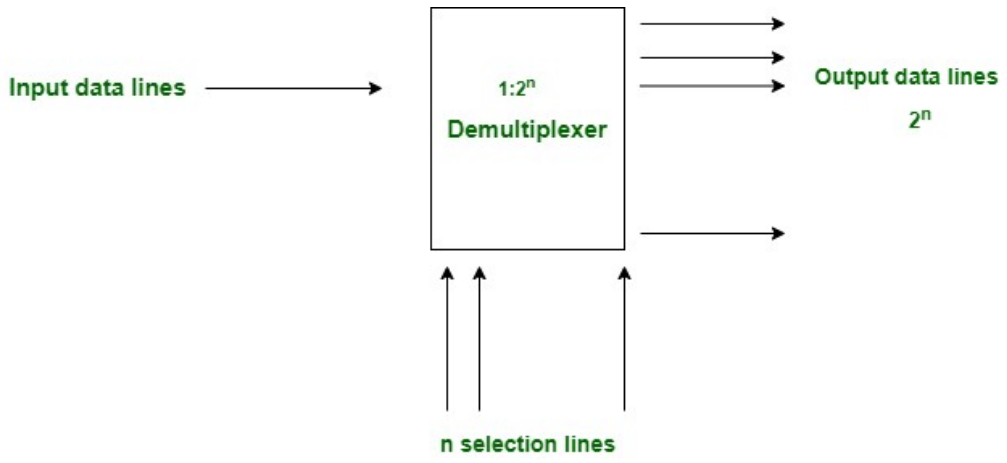

Figure 2: The Block Diagram of Multiplexer.

- A decoder does the opposite job of an encoder. It is a combinational circuit that converts n lines of input into 2^n lines of output.

X	Y	Z	D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	0	0	0	0	0	0
0	1	0	0	0	1	0	0	0	0	0
0	1	1	0	0	0	1	0	0	0	0
1	0	0	0	0	0	0	1	0	0	0
1	0	1	0	0	0	0	0	1	0	0
1	1	0	0	0	0	0	0	0	1	0
1	1	1	0	0	0	0	0	0	0	1

Figure 3: Truth Table of Decoder.

- An encoder is a combinational circuit that converts binary information in the form of a 2N input lines into N output lines, which represent N bit code for the input. For simple encoders, it is assumed that only one input line is active at a time.

D7	D6	D5	D4	D3	D2	D1	D0	X	Y	Z
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

Submission Instructions:

- Prepare the submission file according to the following process:
    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.
    4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.

Convert it into pdf file, Print it and prepare a file for the verification in the next lab.