Department of Computer Science and Engineering
Pandit Deendayal Energy University
Digital Electronics and Computer Organization Lab – **20CP203P**

Lab Assignment – 9: Flip flops (JK, D, T)

Q 1. Write a Verilog code to implement J-K flip flop and validate the code via a suitable Test bench code.

Q 2. Design a J-K flip flop in Logisim and validate the circuit.

Q 3. Write a Verilog code to implement D flip flop and validate the code via a suitable Test bench code.

Q 4. Design a D flip flop in Logisim and validate the circuit.

Q 5. Write a Verilog code to implement T flip flop and validate the code via a suitable Test bench code.

Q 6. Design a T flip flop in Logisim and validate the circuit.

Submission Instructions:

- Prepare the submission file according to the following process:
    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.
    4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.

Convert it into pdf file, print it and prepare a file for the verification in the next lab.