Department of CSE
Pandit Deendayal Energy University (PDEU)
Digital Electronics and Computer Organization Lab (DECO)
20CP203P

Lab 7: Application of Decoder, Recap of Logisim

In this Lab, we shall check about some of the application of Decoder. The design using Logisim will also be checked.

1. Write a Verilog code to implement BCD to seven segment display Decoder. Prepare the Truth Table and circuits and verify the same using Test Bench.
2. Design a 3:8 Decoder using Logisim.
3. Design a 3:8 Decoder using two 2:4 Decoder using Logisim.
4. Design an 8:3 Priority Encoder using Logisim.
5. Design a 4:1 Multiplexer using Logisim.
6. Design a 1:8 Demultiplexer using Logisim.

Submission Instructions:
Prepare the submission file according to the following steps.

1. Copy (Snip/snapshot) the Design circuit and past into the word file.
2. Prepare a corresponding Truth table.
3. Repeat step 1 and 2 for all the problems.
4. For each problem the corresponding circuit design figure must be number accordingly. For example (Fig 1.1 The Circuit Design of XOR using NAND Only).
5. Convert it into pdf file, name it as **RollNo_Assignment# (Example: 20BCP001_ Assignment1.pdf)**.

- Print the corresponding PDF file and prepare a file (Hard copy).
- **The assignment of the previous lab will be verified in the very next lab. Therefore, it is mandatory to bring the file in each lab.**
- Late submission will lead to penalty.
- Any form of plagiarism/copying from peer or internet sources will lead penalty.
- Following of all instructions at submission time is mandatory. Missing of any instructions at submission time will lead to penalty of marks.