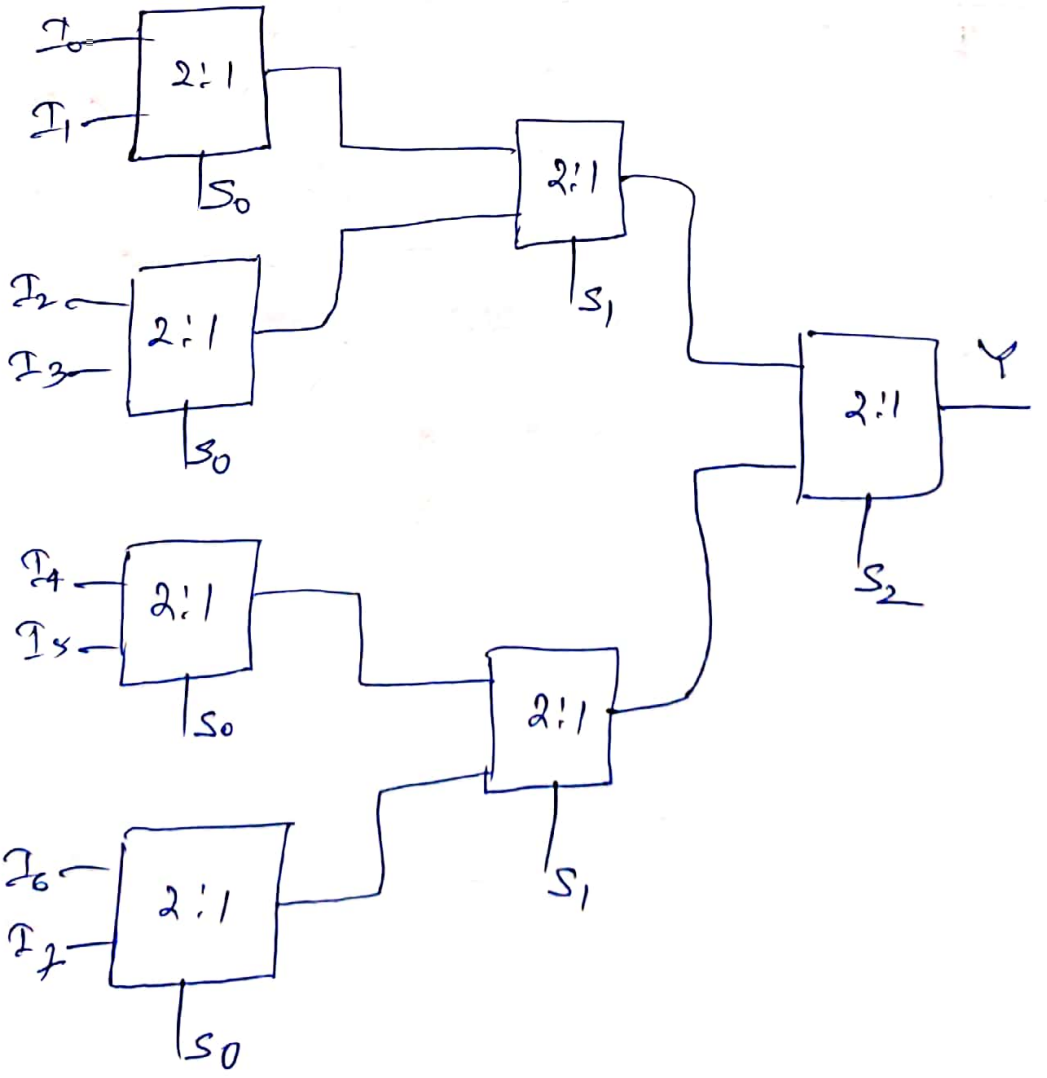
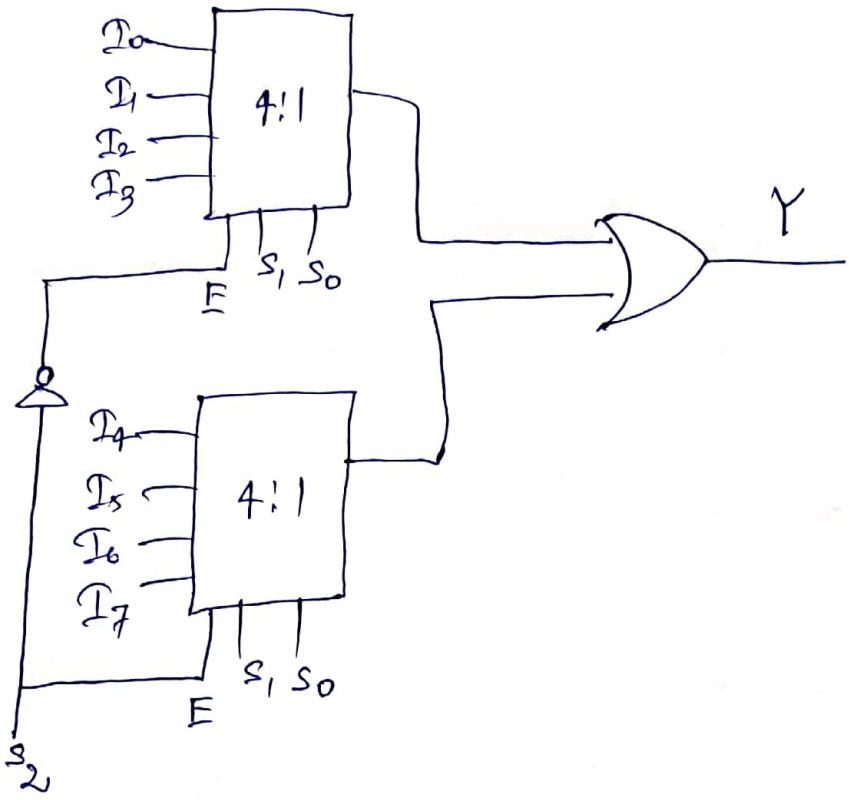
Tutorial - 10 (Solutions)

(1)

S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

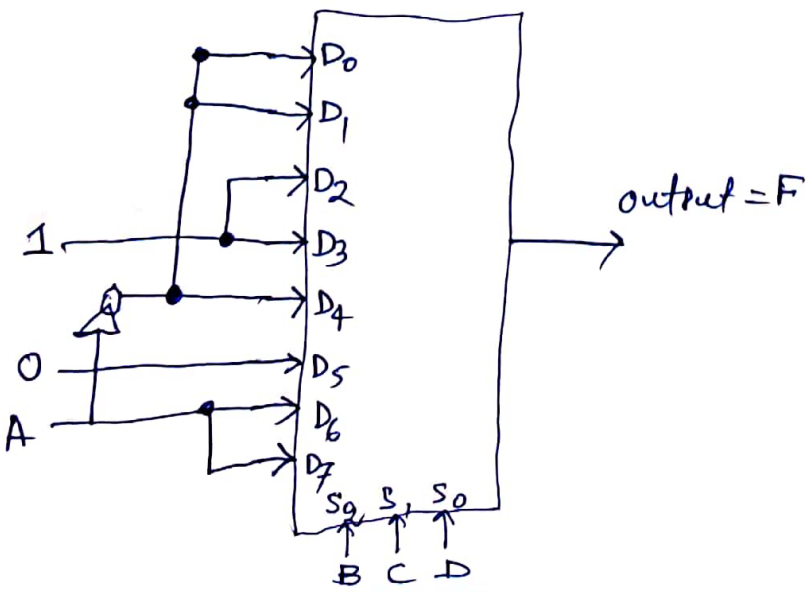


(2) Using enable input we have to implement it.



(3)

S_2	S_1	S_0			Value	For both
A	B	C	D	F	of F	occurances of
0	0	0	0	1	$\overline{A}$	BCD = 000
0	0	0	1	1	$\overline{A}$	BCD = 001
0	0	1	0	1	1	BCD = 010
0	0	1	1	1	1	BCD = 011
0	1	0	0	1	$\overline{A}$	BCD = 100
0	1	0	1	0	0	BCD = 101
0	1	1	0	0	A	BCD = 110
0	1	1	1	0	A	BCD = 111
1	0	0	0	0	$\overline{A}$	BCD = 000
1	0	0	1	0	$\overline{A}$	BCD = 001
1	0	1	0	1	1	BCD = 010
1	0	1	1	1	1	BCD = 011
1	1	0	0	0	$\overline{A}$	BCD = 100
1	1	0	1	0	0	BCD = 101
1	1	1	0	1	A	BCD = 110
1	1	1	1	1	A	BCD = 111



The truth table for the given function is shown above. Since the given function is of 4 variables, we can use a multiplexer with three data inputs. This is shown in the figure above.

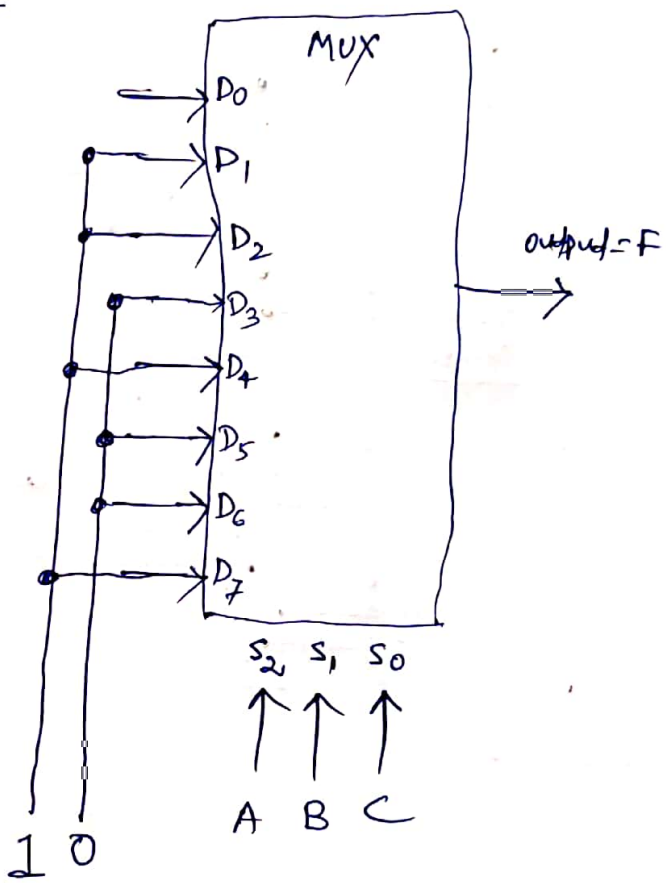
As seen from the table, since F is different for each of the two occurances of BCD = 000, BCD = 001, and BCD = 100, and since $F = \bar{A}$ in each such case, $\bar{A}$ is connected to the data inputs of D_0, D_1, and D_4.

Since F is different for each of the two occurances of BCD = 110 and BCD = 111, and since F = A in both cases, A is connected to D_6 and D_7. Since F is the same for each of the two occurances of BCD = 010 and BCD = 011, and F = 1 in both cases, 1 is connected to D_2 and D_3. and

Since F is same for both the occurances of BCD = 101, and since F = 0 in both the cases, 0 is connected to D_5. The corresponding logic diagram is given above.

④

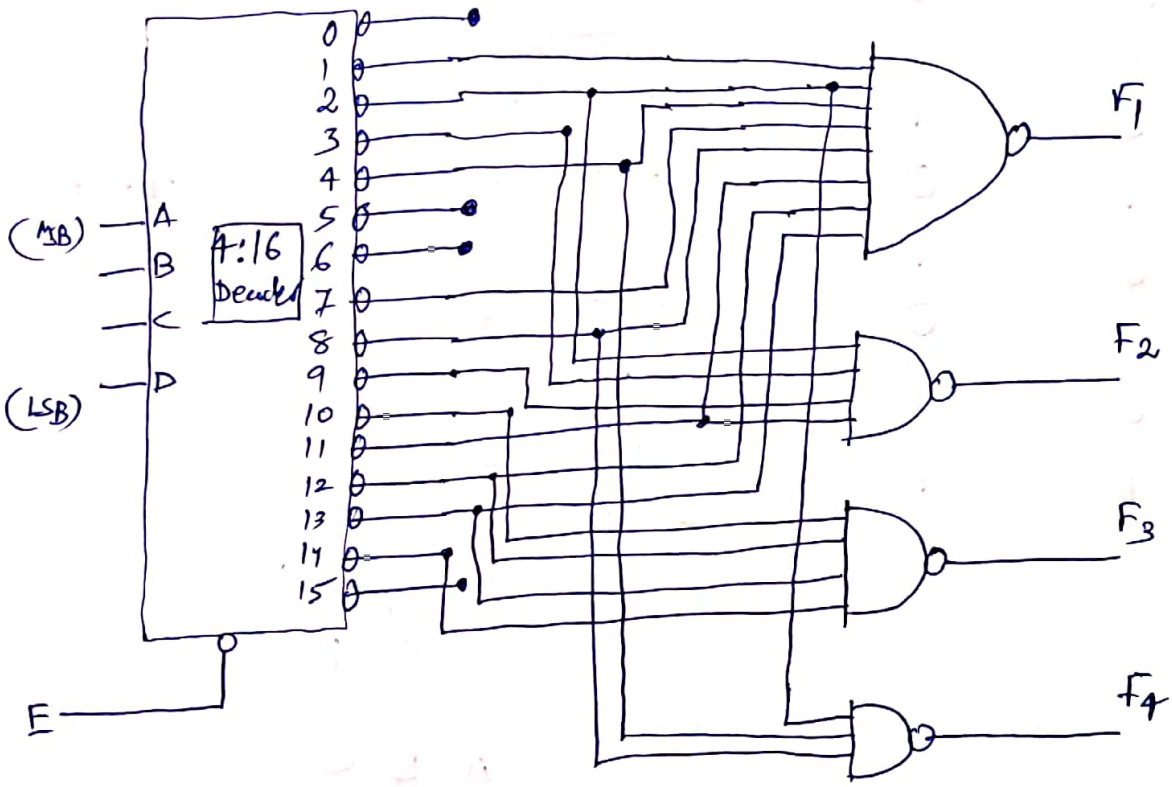
S_2 A	S_1 B	S_0 C	$F = A \oplus B \oplus C$
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1



The truth table for F and the logic diagram to implement F are shown above. Since there are three input variables, we can use a multiplexer with three data select inputs (8 to 1 MUX). The truth table shows the use of data select inputs S_2, S_1, and S_0 for input variables A, B and C respectively.

Since F = 1 when ABC = 001, 010, 100 and 111, we connect logical 1 to data inputs D_1, D_2, D_4, and D_7.
Logical 0 is connected to other data inputs D_0, D_3, D_5, and D_6

(5)



The realization is shown in figure above. The decoder's outputs are active LOW; therefore, a NAND gate is required for every output of the combinational circuit.