Tutorial – 1

1. Compute the value of 'b' for the following case:

   $(16)_b = (100)_b$

2. Determine the base value of the number system in which the following expressions will hold:

   (a) 23 + 44 + 14 + 32 = 223

   (b) $\frac{41}{3} = 13$

   (c) $\sqrt{41} = 5$

3. Find the diminished radix complement for the following:

   (a) $(135)_8$ and $(135)_{16}$

   (b) $(671)_{16}$ and $(ACD)_{16}$

4. Calculate the radix complement of the following:

   (a) $(135)_8$ and $(135)_{16}$

   (b) $(671)_{16}$ and $(ACD)_{16}$

5. Compute the (a) signed magnitude, (b) 1's Complement and (c) 2's Complement for the following:

   (i) 11011

   (ii) 0101

   (iii) 1111111

   (iv) 1111

6. Subtract $(3250)_{10}$ from $(72532)_{10}$ using 10's complement.

7. (a) A person in Saturn possessing 18 fingers has a property worth $(100000)_{18}$. He has 3 daughters and 2 sons. He wants to distribute half the money equally to his sons and the remaining half to his daughters equally. How much will each son and daughter get in Indian Currency?

(b) An Indian started an expedition to Saturn with Rs. 100,000. The expenditure on Saturn will be in the ratio of 1:2:7 for food, clothing and travelling. How much will he be spending on each item in the currency of Saturn.

8. Express -73.75 in 12-bit 2's Complement form.

9. Determine the following:

   (a) 9's complement of $(782.54)_{10}$ and $(5473.924)_{10}$.

   (b) 15's complement of $(ACD.\ 35)_{16}$.

   (c) 7's complement of $(670.13)_8$.

Tutorial – 3 (Questions)

1. Perform the following arithmetic operation using 12-bit 1's complement arithmetic.
    a. 68.75 – 27.50
    b. 43.25 – 89.75
2. Perform the following arithmetic operation using 12-bit 2's complement arithmetic.
    a. 87.5 – 45.75
    b. 27.125 – 79.625
3. Perform the following subtraction operation using (i) diminished radix complement and (ii) radix complement method in base - 3.
    a. 212-121
    b. 121-212
4. Subtract the following numbers using 10's complement method.
    a. 2928.54 – 416.73
    b. 416.73 – 2928.54
5. Perform the following numbers using 9's complement method.
    a. 745.81 – 436.62
    b. 436.62 – 745.81
6. Do the following arithmetic operations in base - 2.
    a. 110101.11 / 101
    b. 1011.101 * 101.01
    c. 1010.010 – 111.111
    d. 1101.101 + 111.011
7. Write the following binary numbers in sign magnitude form, in sign 1's complement form, and in sign 2's complement form using 16-bit register.
    a. +1001010
    b. -11110000
8. Consider n – bit 1's complement representation of integer numbers. Find the range of integer values N that can be represented?
9. Consider n – bit 2's complement representation of integer numbers. What is the range of integer values that can be represented in this system?

Tutorial – 4

Q1. Determine the dual of the following expressions:

(a) $A.B + \overline{A.C} + A.\bar{B}.C$

(b) $\bar{X}.Z + \bar{X}.Y + X.\bar{Y}.Z + Y.Z$

(c) $(A + B + E + F)\,.\,(A + B + \bar{E} + \bar{F})\,.\,(\bar{A} + \bar{B} + E + F)$

(d) $(\bar{X} + Y + Z)\,.\,(X + \bar{Y} + \bar{Z})\,.\,(X + Y + Z).\,(X + Y + \bar{Z})$

Q2. Reduce the following expressions using the Laws of Boolean Algebra:

(a) $f_1 = A[B + \bar{C}\,.\,\overline{(A.B + A.\bar{C})}]$

(b) $f_2 = \overline{(A + \overline{B.C})}\,.\,(A.\bar{B} + A.B.C)$

Q3. Prove the following:

(a) $A\bar{B}C + B + B\bar{D} + AB\bar{D} + \bar{A}C = B + C$

(b) $AB + A\bar{B}C + B\bar{C} = AC + B\bar{C}$

Q4. Prove the following using truth table:

(a) $A + BC = (A + B)(A + C)$

(b) $(A + B)\,.\,\overline{AB} = A \oplus B$

Q5. Design the logic circuit for the following Boolean expression (**use only basic gates – AOI logic**):

$$\overline{AB} + A + \overline{B + C}$$

Q6. Covert the following logic diagram (Fig. 1) to its equivalent Boolean expression (X):

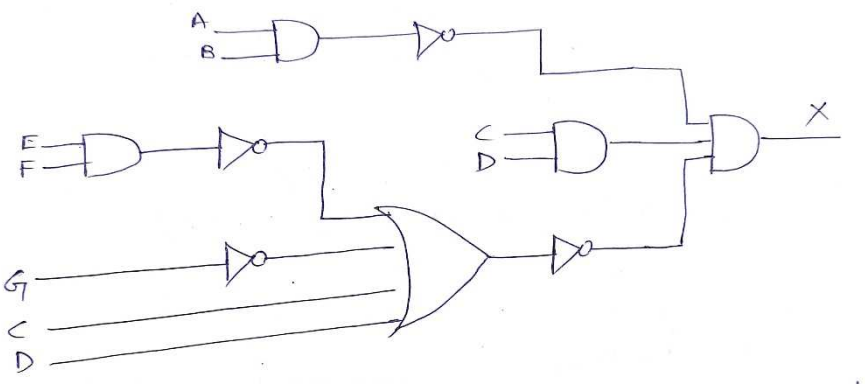


Fig. 1: Logic Diagram with output X

Q7. Reconstruct the following logic diagram (Fig. 2) using universal gates:

(a) Only NAND Gates.

(b) Only NOR Gates.

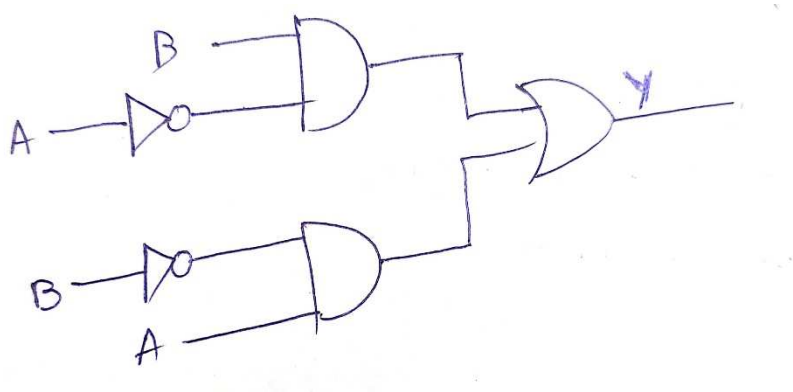


Fig. 2: Logic Diagram with output Y

Q8. Realize the X-OR function for the following scenarios:

(a) Only NAND logic.

(b) Only NOR logic.

Q9. Calculate the number of gate inputs required to realize the following expressions:

(a) $f_1 = ABC + A\bar{B}CD + E\bar{F} + AD$

(b) $f_2 = A(B + C + \bar{D})\,.\,(\bar{B} + C + \bar{E})\,.\,(A + \bar{B} + C + E)$

Also, compute the number of two-input **AND** and **OR** gates required to implement the same.

Tutorial – 5

Q1. Express the Boolean function $F = AB + \bar{A}C$ in a product of maxterm form.

Q2. Find a product of maxterms expression for $F(x, y, z) = \Sigma\,(1, 2, 3, 5, 7)$.

Q3. Compute the sum of minterms expression for $F(x, y, z) = \Pi\,(1, 3, 4, 6)$.

Q4. Express the following function in the POS form:

$$F(A, B, C, D) = \bar{B}D + \bar{A}D + BD$$

Q5. Represent the following function in the SOP form:

$$F(x, y, z) = (xy + z)(xz + y)$$

Q6. Minimize the following expression using mapping and implement using universal logic:

$$F = \Sigma\,(0, 2, 4, 6, 7, 8, 10, 12, 13, 15)$$

Q7. Minimize the following expression using mapping and implement using universal logic:

$$F = \Sigma\,(0, 1, 2, 3, 5, 7, 8, 9, 10, 12, 13)$$

Q8. Determine the prime implicants for the following Boolean function:

$$F(w, x, y, z) = \Sigma\,(0, 2, 4, 5, 6, 7, 8, 10, 13, 14, 15)$$

Q9. Obtain the simplified expression of the following in the POS form:

$$F(A, B, C, D) = \Sigma\,(0, 1, 2, 3, 4, 5) + d(10, 11, 12, 13, 14, 15)$$

Q10. Construct the minimized form of the following expression using K-Map:

$$F(A, B, C, D) = \Sigma\,(4, 5, 7, 12, 14, 15) + d(3, 8, 10)$$

Tutorial - 6

1. Convert the following in the 8,4, -2, -1 and excess-3 coding.
    a. 19
    b. 26
    c. 45
2. Encode the decimal digits 0, 1, 2, ... ,9 by means of weighted codes 3321, 4221, 731-2, 631-1.
3. Perform the following decimal additions in the 8421 code.
    a. 679.6 + 536.8
4. Express the following decimal numbers in (i) 8421 BCD code, (ii) XS-3 code, (iii) 2421 code, (iv) 5211 code, (v) 642-3 code, (vi) 84-2-1 code.
    a. 807
    b. 429.5
5. Convert the following numbers into gray code.
    a. $(1011)_2$ in base - 2
    b. $(110110010)_2$ in base - 2
    c. $(45)_{16}$
    d. $(8512)_{12}$
6. Convert the following gray code into binary.
    a. 1111
    b. 101110
7. In an even-parity scheme, which of the following words contain an error?
    a. 10101010
    b. 11110110
    c. 101110001
8. In an odd-parity scheme, which of the following words contain an error?
    a. 10110111
    b. 10011010
    c. 11101010

Tutorial - 7

Q1 Consider a 3-variable function $f(x, y, z) = \sum(3, 5, 6)$. It is minimized as $x + yz$. What are the don't cares used in this minimization.

Q2 Consider the following K-MAP.

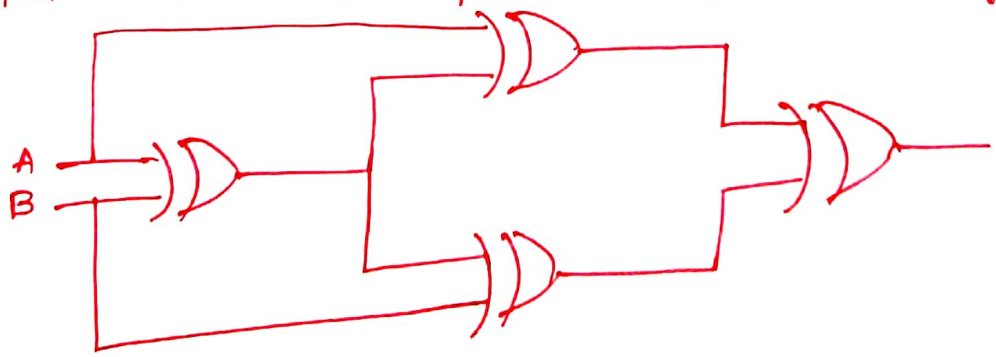
wx \ yz	00	01	11	10
00	1			1
01	1	1	1	1
11	1			1
10	1	1	1	1

Find all the minimal expression denoted by the above K-MAP.

Q3 Let α, β, ν denotes don't cares. What will be their values in the minimization of sum of product expression.

wx \ yz	00	01	11	10
00	0	0	α	0
01	0	0	1	1
11	1	1	1	1
10	β	ν	0	0

Q4 What is the expression represented by following combination.



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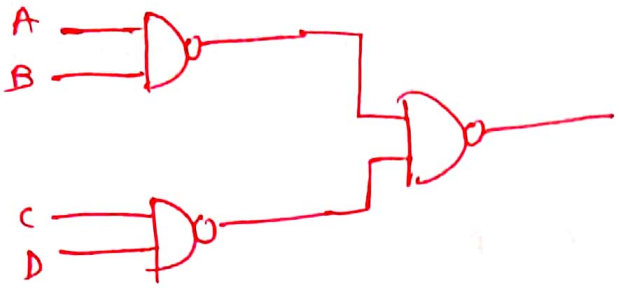
Q5/ What is the function represented by the following realization. (2)



Q6/ What is the value of α and β if the following expression is solved.

$$\begin{array}{r} (\alpha 567)_8 \\ +\ (2\beta\alpha 5)_8 \\ \hline (71\beta\alpha)_8 \end{array}$$

Q7/ Implement half adder using universal logic (i.e. NAND and NOR).

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Tutorial – 9 (Questions)

1. Design and Implement a 4-bit binary-to-gray code converter.

2. Design and Implement a 4-bit gray-to-binary code converter.

3. A safe has 5 locks v, w, x, y and z; all of which must be unlocked for the safe to open. The keys to the locks are distributed among 5 executives in the following manner.

   Mr. A has keys for locks v and x.
   Mr. B has keys for locks v and y.
   Mr. C has keys for locks w and y.
   Mr. D has keys for locks x and z.
   Mr. E has keys for locks v and z.
   Mr. A has keys for locks v and x.

   a. Determine the minimal number of executives required to open the safe.
   b. Find all the combinations of executives that can open the safe; write an expression f(A, B, C, D, E) which specifies when the safe can be opened as a function of what executives are present?
   c. Who is essential executive?

4. The input to computer circuit are the 4-bits of the binary number $A_3A_2A_1A_0$. The circuit is required to produce a 1 if and only if all of the following conditions hold.
   a. The MSB is a 1 or any of the other bits are a 0.
   b. A_2 is a 1 or any of the other bits are a 0.
   c. Any of the 4 bits are a 0.

   Obtain a minimal expression.

5. You are presented with a set of requirements under which an insurance policy can be issued. The applicant must be:
   a. A married female 25 years old or over, or
   b. A female under 25, or
   c. A married male under 25 who has not been involved in a car accident, or
   d. A married male who has been involved in a car accident, or
   e. A married male 25 years or above who has not been involved in a car accident.

   Find the algebraic expression which assumes a value 1 whenever the policy is issued. Simplify the expression obtained.

Tutorial – 10 (Questions)

1. Design an 8×1 multiplexer using 2×1 multiplexer.

2. Design an 8×1 multiplexer using 4×1 multiplexer. Note: You may use enable input of the multiplexers.

3. Use a multiplexer having three data select inputs to implement the logic for the function $F = \Sigma m (0, 1, 2, 3, 4, 10, 11, 14, 15)$.

4. Use a multiplexer to implement the logic function $F = A \oplus B \oplus C$.

5. Implement the following multiple output combinational logic circuit using a 4-line to 16-line decoder.

   $F = \Sigma m (1, 2, 4, 7, 8, 11, 12, 13)$
   $F = \Sigma m (2, 3, 9, 11)$
   $F = \Sigma m (10, 12, 13, 14)$
   $F = \Sigma m (2, 4, 8)$

Tutorial – 12 (Questions)

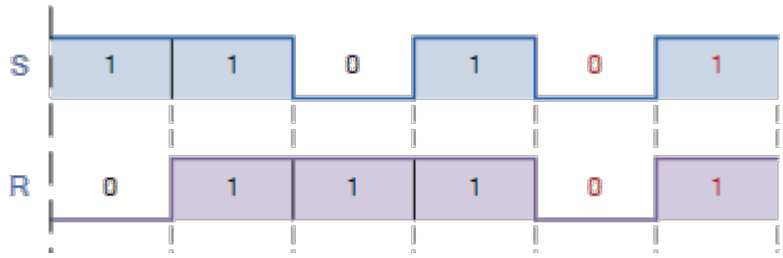
1. Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter.

2. A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.

    a. Tabulate the characteristic table.
    b. Tabulate the excitation table.
    c. Derive the characteristic equation.
    d. Show how the PN flip-flop can be converted to a D flip-flop.

3. Show that the characteristic equation for the complement output of a JK flip-flop is
    $Q'(t + 1) = J'Q' + KQ$

4. Draw the wave form for Q and Q' for the SR flip flop assuming clock is high.



5. Implement SR latch using NAND gates and realize it for the following cases. Finally, write the truth table.
    a. S=0 and R=0
    b. S=0 and R=1
    c. S=1 and R=0
    d. S=1 and R=1

Tutorial – 13 (Questions)

1. Convert T Flip Flop into D Flip Flop.
2. Explain the realization of T Flip Flop from JK Flip Flop.
3. Design and Implement a MOD-6 asynchronous counter using T Flip Flop.
4. A Binary Ripple Counter is required to count up to $(16383)_{10}$.
    1. How many Flip Flops are required?
    2. If the clock Frequency is 8.192 MHz, what is the frequency at the output of MSB?
5. Design a MOD-5 synchronous counter using JK flip-flop.
6. Design and Implement 4-bit Ring Counter using
    1. D Flip Flop
    2. JK Flip Flop

    Also, Draw the Timing Diagram and State Diagram.