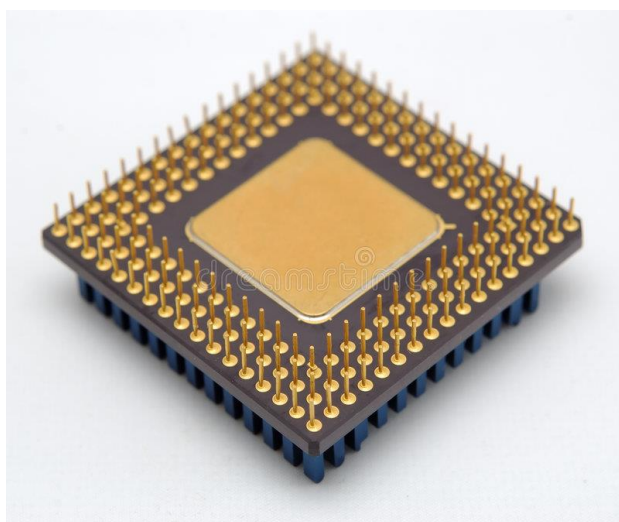


**SCHOOL OF TECHNOLOGY
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GANDHINAGAR, GUJARAT, INDIA**

Computer Science & Engineering

LAB MANUAL (2022-23)

**Digital Electronics and Computer Organization Lab
(20CP203P)**



Student Name: Harsh Shah

Enrollment No.: 21BCP359 Course with Semester: B.Tech (3rd) CSE

Division: 6

Group: G11

**Course Coordinator: Dr. Hiren Thakkar
Course Instructor: Dr. Tanmay Bhowmik**



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CERTIFICATE

This is to certify that Mr. /Miss **Harsh Shah** Enrolment no. **21BCP359** of **3rd Semester** degree course in **Computer Science and Engineering** has satisfactorily prepared and presented his Term Work in **Digital Electronics and Computer Organization Lab (20CP203P)** within four walls of the laboratory of this Institute during **July-2022** to **November-2022**.

Date of Submission: 20-11-2022

Dr. Tanmay Bhowmik
Assistant Professor
Dept. of CSE



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