Department of Computer Science and Engineering
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Digital Electronics and Computer Organization Lab – **20CP203P**

Lab Assignment – 8: Sequential Circuits: Latch and flip flop (SR)

In this lab we will learn about the sequential logic circuits. These circuits can act as a memory unit.

Q 1. Design an SR flip-flop using Logisim.

Q 2. An SR latch (Set/Reset) is an asynchronous device: it works independently of control signals and relies only on the state of the S and R inputs. The symbol, the circuit using NOR gates, and the truth table are shown below.

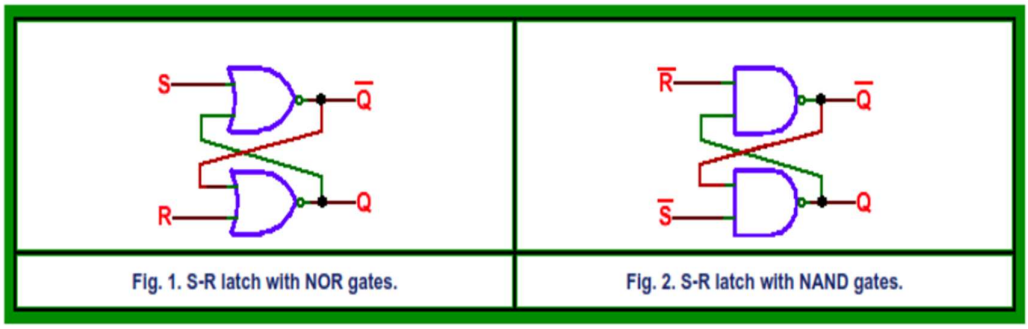

Fig. 1. S-R latch with NOR gates.

Fig. 2. S-R latch with NAND gates.

S	R	Q	Q'	
0	0	NC	NC	No change. Latch remained in present state.
1	0	1	0	Latch SET.
0	1	0	1	Latch RESET.
1	1	0	0	Invalid condition.

Table 1: S-R latch truth table

Based on the above figure and truth table, complete following tasks.

1) Generate the Boolean expression for the S-R latch from the truth table given in Table-1.

2) Write a module for NOR gate and develop a structural Verilog code for the S-R latch using the NOR gate module.

3) Validate the code via a suitable Testbench code.

Q 3. In S-R latch we do not use a clock. Now if we add an additional clock at input so that the S and R inputs are active only when the clock is high. When the clock goes low, the state of flip-flop is latched and cannot change until the clock goes high again. This clocked addition in S-R latch is also called the S-R flip flop. Use the below given figure and truth table for S-R flip flop.

We can add a clock in put in NAND latch in Figure 2, and can convert in S-R flip flop using NAND gates as: (similar results can be achieved via NOR Latch)

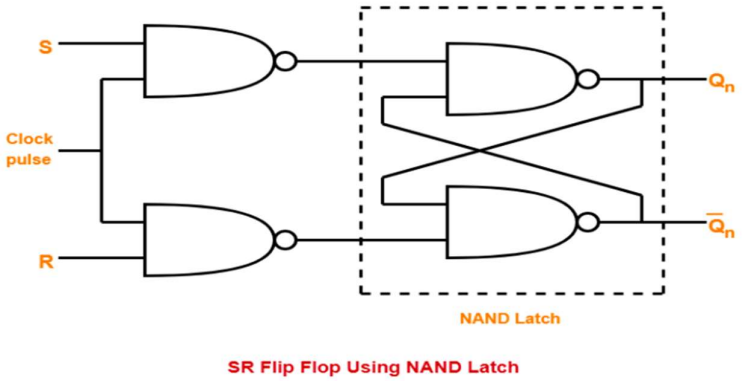

Figure 3: S-R Flip flop using NAND latch

CLOCK EDGE	S	R	Q	Q'	State
Positive/Negative	0	0	Q	Q'	No change
Positive/Negative	0	1	0	1	Reset State
Positive/Negative	1	0	1	0	Set State
Positive/Negative	1	1	X	X	Invalid

Table 2: S-R flip flop truth table

1) Generate the Boolean expression for the S-R flipflop using K-map and truth table given in Table 2.

2) Write a verilog module for NAND gate and utlize it to develop a structural verilog module for S-R flip flop as per figure 3.

3) Validate it using suitable Test bench.

Q 4. We can also develop a behavioral modeling based verilog code for the S-R latch. Here we can use the if-else logic to assign values for output based on the input conditions.

For example, the condition S = 1 or H, R = 0 or L then Q = 1 and Q' = 0 can be expressed under a begin block using if condition as:

```
If (S == 1 & R == 0)
begin
        Q <= 1;
        Q_bar <= 0;
end
```

Similar code can be developed for rest of the conditions.

1) Develop a behavioral verilog code using if-else slatemets for S-R latch.

2) Varify it with a suitable testbench code.

Q 5. Develop a similar behavioral code and test bench for S-R flip flop using if-else condition as per question 3.

Submission Instructions:

- Prepare the submission file according to the following process:
    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.
    4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.

Convert it into pdf file, print it and prepare a file for the verification in the next lab.