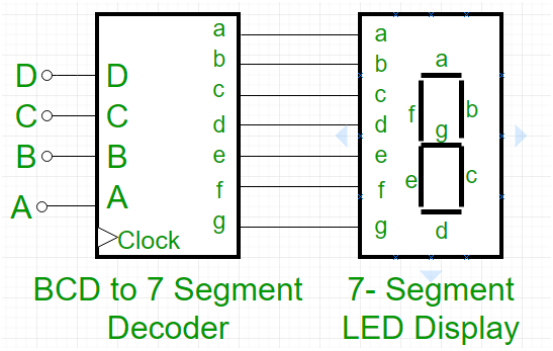
LAB 7: Application of Decoder, Recap of Logisim

Question 1: Write a Verilog code to implement BCD to seven segment display Decoder. Prepare the Truth Table and circuits and verify the same using Test Bench.

Decimal Number	INPUT Lines				OUTPUT Lines						
	A	B	C	D	a	b	c	d	e	f	g
0	0	0	0	0	1	1	1	1	1	1	0
1	0	0	0	1	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	1	1	0	1
3	0	0	1	1	1	1	1	1	0	0	1
4	0	1	0	0	0	1	1	0	0	1	1
5	0	1	0	1	1	0	1	1	0	1	1
6	0	1	1	0	1	0	1	1	1	1	1
7	0	1	1	1	1	1	1	0	0	0	0
8	1	0	0	0	1	1	1	1	1	1	1
9	1	0	0	1	1	1	1	1	0	1	1

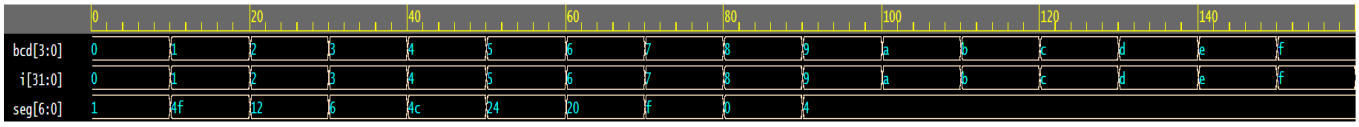


testbench.sv

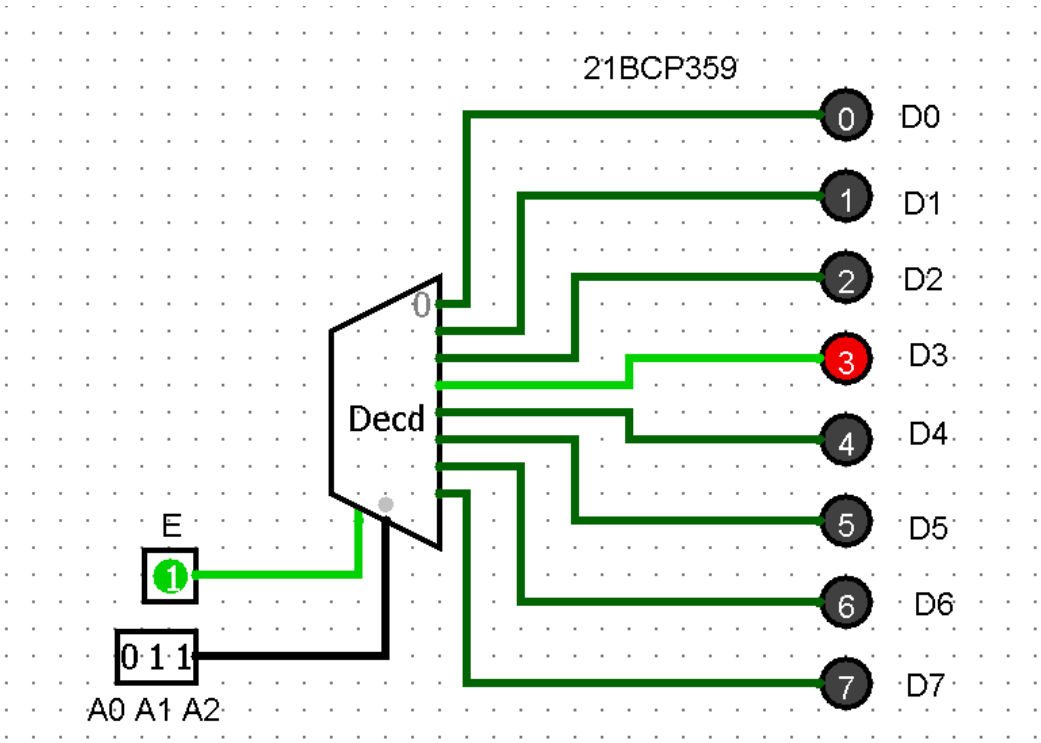
```
module tb_segment7;

    reg [3:0] bcd;
    wire [6:0] seg;
    integer i;

    segment7 uut (
        .bcd(bcd),
        .seg(seg)
    );

    initial begin
        for(i = 0;i < 16;i = i+1)
        begin
            bcd = i;
            #10;
        end
    end
  initial
    begin
      $dumpfile("dump.vcd");
      $dumpvars(1);
    end

endmodule
```

design.sv

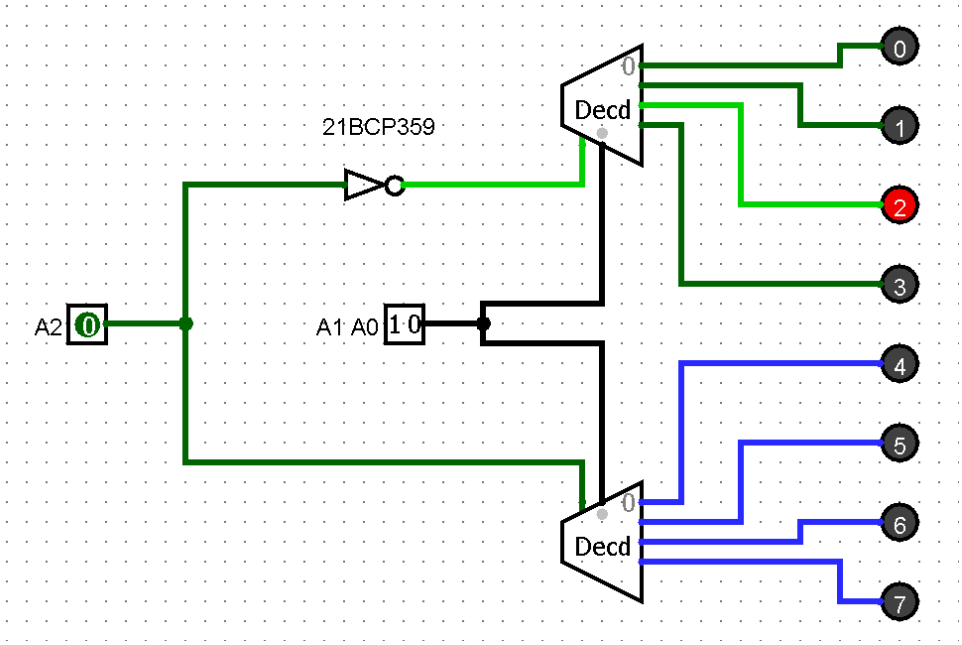
```
module segment7(
     bcd,
     seg
    );

     input [3:0] bcd;
     output [6:0] seg;
     reg [6:0] seg;

    always @(bcd)
    begin
        case (bcd)
            0 : seg = 7'b0000001;
            1 : seg = 7'b1001111;
            2 : seg = 7'b0010010;
            3 : seg = 7'b0000110;
            4 : seg = 7'b1001100;
            5 : seg = 7'b0100100;
            6 : seg = 7'b0100000;
            7 : seg = 7'b0001111;
            8 : seg = 7'b0000000;
            9 : seg = 7'b0000100;
        endcase
    end

endmodule
```



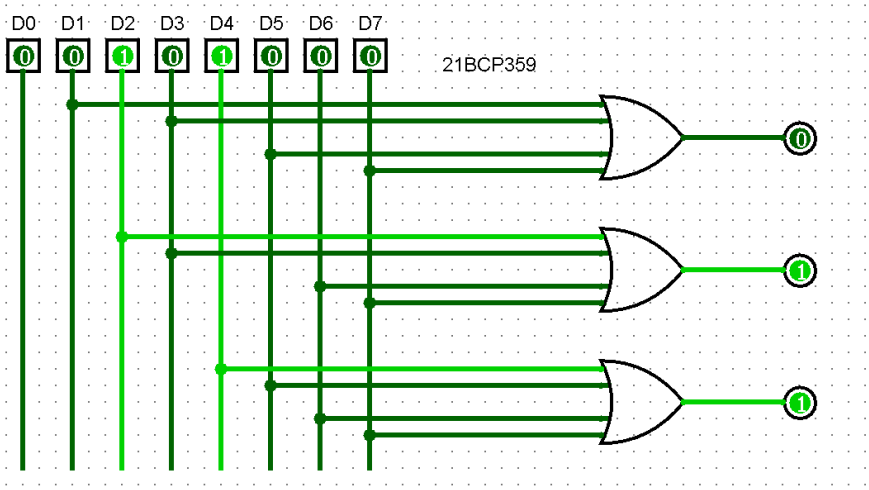
Question 2: Design a 3:8 Decoder using Logisim.



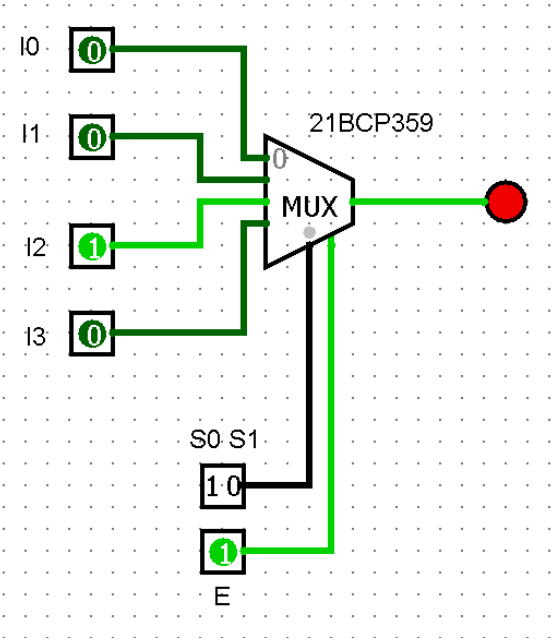
Question 3. Design a 3:8 Decoder using two 2:4 Decoder using Logisim.



Question 4. Design an 8:3 Priority Encoder using Logisim.



Question 5. Design a 4:1 Multiplexer using Logisim.



Question 6. Design a 1:8 Demultiplexer using Logisim