# Lab 4: Design Half Adder & Full Adder Using Half Adder

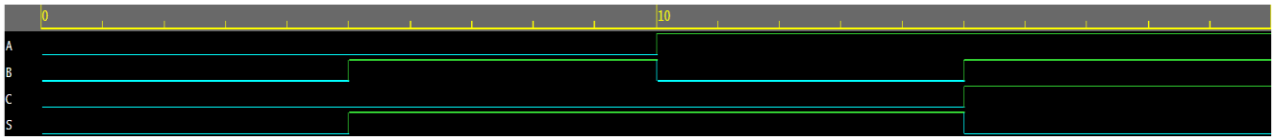
## Question 1: Write Verilog code for half adder. Test using waveform

design.sv

```
module xorgate(
  input a,b,
  output sum, carry);
    assign sum = ~a & b || a & ~b;
    assign carry = a & b;
endmodule
```

testbench.sv

```
module tbxorgate;
  reg A, B;
  wire S, C;
  xorgate a1 (.a(A),.b(B),.sum(S),.carry(C));
  initial
    begin
      A=0;B=0;#5;
      A=0;B=1;#5;
      A=1;B=0;#5;
      A=1;B=1;#5;
    end
  initial
    begin
      $dumpfile("dump.vcd");
      $dumpvars(1);
    end
endmodule
```




## Question 3. Write Verilog code for full adder. Test using waveform.

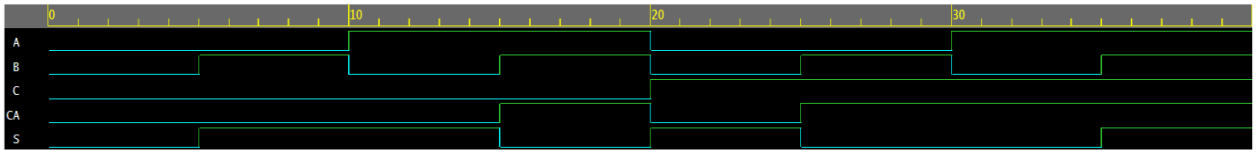
testbench.sv

```
module tbxorgate;
  reg A, B, C;
  wire S, CA;
  xorgate a1 (.a(A),.b(B),.c(C),.sum(S),.carry(CA));
  initial
    begin
      A=0;B=0;C=0;#5;
      A=0;B=1;C=0;#5;
      A=1;B=0;C=0;#5;
      A=1;B=1;C=0;#5;
      A=0;B=0;C=1;#5;
      A=0;B=1;C=1;#5;
      A=1;B=0;C=1;#5;
      A=1;B=1;C=1;#5;
    end
  initial
    begin
      $dumpfile("dump.vcd");
      $dumpvars(1);
    end
endmodule
```

design.sv

SV/Verilog Design

```
module xorgate(
  input a,b,c,
  output sum, carry);
  assign sum = (~(~a & b || a & ~b) & c) | ((~a & b || a & ~b) & ~c);
  assign carry = (a & b) | (b & c) | (c & a);
endmodule
```



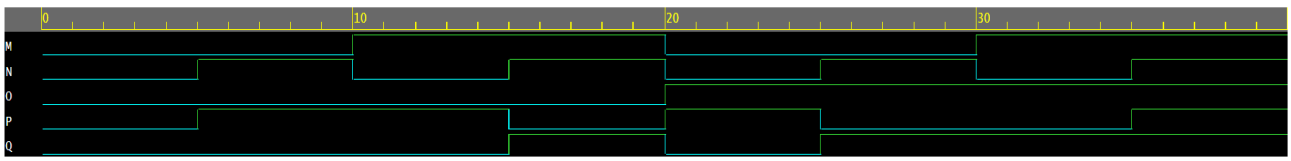
**Question 4. Write Verilog code for full adder using module instantiation of half adder. Test using waveform.**

design.sv

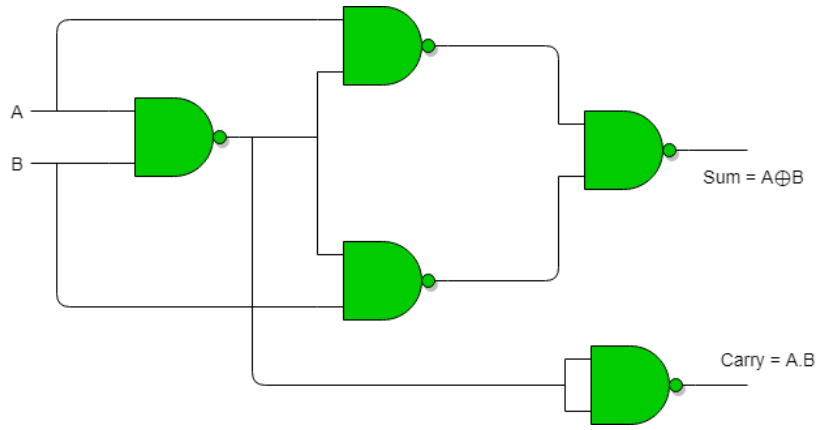
```
module halfadder (input a, b, output c, s);
  assign c = a & b;
  assign s = (~a & b) | (a & ~b);
endmodule

module orgate (input i, j, output k);
  assign k = i | j;
endmodule

module fulladder(input m, n, o, output p , q);
  wire sum1, carry1, carry2;
  halfadder h1 (.a(m),.b(n),.s(sum1));
  halfadder h2 (.a(m),.b(n),.c(carry1));
  halfadder h3 (.a(sum1),.b(o),.s(p));
  halfadder h4 (.a(sum1),.b(o),.c(carry2));
  orgate or1 (.i(carry1),.j(carry2),.k(q));

endmodule

```

testbench.sv

```
module fulladder_tb;
  reg M, N, O;
  wire P, Q;
  fulladder x1 (.m(M), .n(N), .o(O), .p(P), .q(Q));
  initial
    begin
      M = 0; N = 0; O = 0; #5;
      M = 0; N = 1; O = 0; #5;
      M = 1; N = 0; O = 0; #5;
      M = 1; N = 1; O = 0; #5;
      M = 0; N = 0; O = 1; #5;
      M = 0; N = 1; O = 1; #5;
      M = 1; N = 0; O = 1; #5;
      M = 1; N = 1; O = 1; #5;
    end
  initial
    begin
      $dumpfile("dump.vcd");
      $dumpvars(1);
    end
endmodule

```



**Question 5. Write Verilog code for half adder using only NAND gate. Test using waveform**




testbench.sv

```
module tb_ha_nand;
  reg a,b;
  wire sum,carry;

  ha_nand ha1(a,b,sum,carry);


  initial
    begin
      a = 0; b = 0; #5;
      a = 0; b = 1; #5;
      a = 1; b = 0; #5;
      a = 1; b = 1; #5;
    end
initial
  begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end
endmodule

```

design.sv

```
module ha_nand(input a,b, output sum,carry);
  wire temp1,temp2,temp3assign ;
  assign temp1 = ~(a & b);

  assign temp2 = ~(a & temp1);
  assign temp3 = ~(b & temp1);

  assign sum = ~(temp2 & temp3);

  assign carry = ~(temp1 & temp1);
endmodule
```