Pandit Deendayal Energy University
School of Technology
Department of Computer Science and Engineering
Odd Semester 2022-2023

Course file

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Name of the course: Digital Electronics & Computer Organization Lab	**Course Code: 20CP203P**
Program: B.Tech **Branch: Computer Science and Engineering**	**Semester: 3rd** **Academic Year: 2022-2023**
Name of Course Coordinator: Dr. Hiren Kumar Thakkar	
Subject Teachers (Division wise/Batch wise): **Tanmay Bhowmik (G6, G11, G12), Hiren Thakkar (G1, G2, G5, G7, G8, G9, G10)** **Rashmi Bhattad (G3, G4)**	

Date: 25-July-2022

Signature of Subject Teachers **Signature of Department Coordinator (IQAC)** **Signature of Head of the Department**

1. Departmental Vision and Mission

Vision of Department

"To contribute to the society by imparting transformative education and producing globally competent professionals having multidisciplinary skills and core values to do futuristic research & innovations."

Mission of Department

1. To accord high quality education in the continually evolving domain of Computer Engineering by offering state-of-the-art undergraduate, postgraduate, doctoral programmes.
2. To address the problems of societal importance by contributing through the talent we nurture and research we do:
3. To collaborate with industry and academia around the world to strengthen the education and multidisciplinary research ecosystem.
4. To develop human talent to its fullest extent so that intellectually competent and imaginatively exceptional leaders can emerge in a range of computer professions.

2. Program Educational Objectives (PEOs) of Department

The Program Educational Objectives of B. Tech. (Computer Engineering) program are:

PEO-1. To prepare graduates who will be successful professionals in industry, government, academia, research, entrepreneurial pursuit and consulting firms.

PEO-2. To prepare graduates who will make technical contribution to the design, development and production of computing systems.

PEO-3. To prepare graduates who will get engage in lifelong learning with leadership qualities, professional ethics and soft skills to fulfill their goals.

PEO-4. To prepare graduates who will adapt state of the art development in the field of computer engineering

3. Program Outcomes (POs)

Undergraduate engineering program are designed to prepare graduates to attain the following program outcomes:

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. Design / development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

4. Program Specific Outcomes (PSOs)

The graduates of CSE department will be able to:

1. Develop computer engineering solutions for specific needs in different domains applying the knowledge in the areas of programming, algorithms, hardware-interface, system software, computer graphics, web design, networking and advanced computing.
2. Analyze and test computer software designed for diverse needs.
3. Pursue higher education.

5. Academic Calendar

Dear Colleagues,

The new Academic session for all **even semesters** of UG & PG of SLS and B. Tech. Sem. 3/5/7 + M. Tech. Sem. 3 of SPT & SOT shall begin from July 25, 2022 (Monday) as per the following schedule:

ACADEMIC CALENDAR 2022-23 (ODD SEMESTER)

		11	12	13	14	15	16	17	FACULTY DEVELOPMENT PROGRAMME WEEK
		18	19	20	21	22	23	24	FACULTY DEVELOPMENT PROGRAMME WEEK
1	JULY 2022	25	26	27	28	29	30	31	COMMENCEMENT OF ODD SEMESTER: July 25
2	AUGUST	1	2	3	4	5	6	7	
3		8	9	10	11	12	13	14	RAKSHA BANDHAN
4		15	16	17	18	19	20	21	INDEPENDENCE DAY, JANMASHTAMI
5		22	23	24	25	26	27	28	
6	SEP	29	30	31	1	2	3	4	SAMVATSSARI
7		5	6	7	8	9	10	11	
8		12	13	14	15	16	17	18	**MID-SEM EXAMINATIONS**
9		19	20	21	22	23	24	25	
10	OCT	26	27	28	29	30	1	2	COURSE FEEDBACK WEEK
11		3	4	5	6	7	8	9	DUSSHERA
12		10	11	12	13	14	15	16	
13		17	18	19	20	21	22	23	
14		24	25	26	27	28	29	30	DIWALI WEEK
15	NOV	31	1	2	3	4	5	6	
16		7	8	9	10	11	12	13	GURU NANAK JAYANTI
17		14	15	16	17	18	19	20	COMPLETION OF ODD SEMESTER: Nov. 18
		21	22	23	24	25	26	27	**FOET Practical Exams : Nov.21 Onwards** **FOLS Sem. End Examination : Nov. 21 Onwards**
	DEC	28	29	30	1	2	3	4	**FOET Sem. End Examination : Nov.28 Onwards**
		5	6	7	8	9	10	11	
		12	13	14	15	16	17	18	Rural Internship for FOLS Students: Dec. 17, 2022 to Jan. 10, 2023
		19	20	21	22	23	24	25	
		26	27	28	29	30	31	1	**WINTER BREAK**

Completion of Odd Semester: November 18, 2022 (Friday)

Semester End Examination: November 21, 2022 (Monday) Onwards

Even semester starts: January 02, 2023 (Monday)

Ends on: 28th April 2023

6. Class Time-Table and Faculty Time-Table with Office Hours

Tanmay Bhowmik
Computer Science &Engineering

Autumn Semester 2022 — w.e.f : 1st July 2022

Day	08:00-09:00	09:00-10:00	10:00-11:00	11:00-12:00	12:00-13:00	13:00-14:00	14:00-15:00	15:00-16:00	16:00-17:00	17:00-18:00	18:00-19:00
Monday	G12 (20CP203P) E214, CP(3) - P						G11G12 (20CP203T) Y5, CP(3) - L	G9G10 (20CP203T) D005, CP(3) - L			
Tuesday			G9G10 (20CP203T) E104, CP(3) - L				G11 (20CP203P) E115, CP(3) - P			G7G8 (20CP203T) E105, CP(3) - L	
Wednesday				G11G12 (20CP203T) Y6, CP(3) - L				G11G12 (20CP203T) Y6, CP(3) - L		G7G8 (20CP203T) E105, CP(3) - L	
Thursday							G9G10 (20CP203T) Y6, CP(3) - L			G7G8 (20CP203T) E105, CP(3) - L	
Friday	G6 (20CP203P) F-103, CP(3) - P										
Saturday											

Location Abbr.	Location Name
D005	D, Lecture Hall
E104	E, Lecture Hall
E105	E, Lecture Hall
E115	E, ICT Lab1
E214	E, ICTLAB2
F-103	F, HPC LAB
Y5	F, Lecture Hall
Y6	F, Lecture Hall

Subject Abbr.	Subject Name
20CP203P	Digital Electronics &Computer Organization Lab
20CP203T	Digital Electronics &Computer Organization

Office Hours: 16:00 – 17:00 (Students are requested to drop a prior mail before contacting on office hours)

7. Course Outcomes (COs), Course Syllabus, Pre requisites for Course

Pandit Deendayal Energy University — School of Technology

20CP203P					Digital Electronics & Computer Organization LAB					
Teaching Scheme					Examination Scheme					
					Theory			Practical		Total
L	T	P	C	Hrs/Week	MS	ES	IA	LW	LE/Viva	Marks
0	0	2	1	2	-	-	-	50	50	100

COURSE OBJECTIVES

- To simulate elementary GATE operations
- To simulate basic combinational circuits (Adder, subtractor, multiplier etc.)
- To simulate different algorithms required memory mapping
- To simulate an ALU comprising addition, subtraction and multiplication capability

LIST OF EXPERIMENTS

1. Implement basic GATE (AND, OR, NOT, NAND, NOR) operations
2. Design of adder
3. Design of carry-look-ahead adder
4. Design of Flip-flops (any two)
5. Design of Registers and counters
6. Design of Combinational multiplier
7. Design of Booth's multiplier
8. Design of ALU
9. Design of Memory (4*4 RAM)
10. Design of K-map Design
11. Design of Quine - Mc Clusky Algorithm

COURSE OUTCOMES

On completion of the course, student will be able to
CO1- Explain various GATE operations.
CO2- Analyse different combinational circuits for different inputs.
CO3- Compare different sequential circuits.
CO4- Construct basic building blocks such as memory and ALU.
CO5- Use different algorithms for multiplication and division.
CO6- Demonstrate circuit minimization.

TEXT/REFERENCE BOOKS:

1. Linda Null, Julia Lobur, The essentials of computer organization and architecture. Jones & Bartlett Publishers. p. 121. ISBN 978-0-7637-3769-6.
2. Donald P Leach, Albert Paul Malvino,Goutam Saha, Digital Principles and Applications, McGraw-Hill publications.
3. Ronald J.Tocci,Neal S Widmer,Gregory L.Moss, Digital Systems Principles and Applications, Pearson Publication.

END SEMESTER EXAMINATION QUESTION PAPER PATTERN

Max. Marks: 100 — **Exam Duration: 2Hrs**

Part A : Lab Work – Continuous Assessment — 50 Marks
Part B: Lab Exam and Viva — 50 Marks

8. Lesson Plan

Lecture No.	Topic to be covered	Mode of Teaching
1.	Implement Basic Gate Operations	WB+PPT
2.	Design of adders	WB+PPT
3.	Design of carry-look-ahead adder	WB+PPT
4.	Design of Flip Flops (any Two)	WB+PPT
5.	Design of Registers and Counters	WB+PPT
6.	Design of combinational multiplier	WB+PPT
7.	Design of booth's multiplier	WB+PPT
8.	Design of ALU	WB+PPT
9.	Design of memory (4 * 4) RAM	WB+PPT
10	Design of K-map Design	WB+PPT
11	Design of Quine - Mc Clusky Algorithm	WB+PPT

Legends: WB (White Board), PPT (PowerPoint Slides)

9. Program Articulation Matrix and Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	-	1	2	-	3	1	1	-	-	1	1	3	-	-
2	1	1	-	2	-	3	1	1	-	-	1	1	2	-	-
3	2	1	1	-	-	3	1	1	-	-	1	1	2	-	-
4	2	3	3	1	-	2	1	1	-	-	2	1	2	-	-
5	1	2	3	2	-	2	1	1	-	-	1	1	2	-	-
6	1	2	3	1	-	2	1	1	-	-	2	1	2	-	-
	1.6	1.5	1.8	1.3	-	2.5	1	1	-	-	1.3	1	2.1	-	-

CO1- Explain various GATE operations.
CO2- Analyse different combinational circuits for different inputs.
CO3- Compare different sequential circuits.
CO4- Construct basic building blocks such as memory and ALU.
CO5- Use different algorithms for multiplication and division.
CO6- Demonstrate circuit minimization.

10.Evaluation Scheme and Rubrics

Course code: 20CP 203P **Course name:** Digital Electronics & Computer Organization -lab

Course Outcomes (CO's): On completion of the course, students will be able to

CO1- Explain various GATE operations.
CO2- Analyse different combinational circuits for different inputs.
CO3- Compare different sequential circuits.
CO4- Construct basic building blocks such as memory and ALU.
CO5- Use different algorithms for multiplication and division.
CO6- Demonstrate circuit minimization.

Co Assessment Tools (Direct Assessment):
Various assessment tools used to evaluate CO's (Rubrics) and the frequency with which the assessment processes are carried out are listed below.

Assessment Method	Assessment Tool	Description	Marks	Mapping with CO	Contribution to CO's
Direct (Continuous Assessment)	Experiment 1 to Experiment 10	**List of Experiments from syllabus document**	100 (10 for each experiment)	CO1-CO6	It fractionally contributes to 50% weightage of Direct Assessment to CO attainment.
Direct	Lab Exam + Viva	**Topics to be covered:** Whole syllabus	50	CO1 to CO6	It contributes to 50% weightage of Direct Assessment to CO attainment.

11.Lab Experiments.

Sr.No.	Lab Exercise
1.	Implement Basic Gate Operations
2.	Design of adders
3.	Design of carry-look-ahead adder
4.	Design of Flip Flops (any Two)

5.	Design of Registers and Counters
6.	Design of combinational multiplier
7.	Design of booth's multiplier
8.	Design of ALU
9.	Design of memory (4 * 4) RAM
10	Design of K-map Design
11	Design of Quine - Mc Clusky Algorithm

12.Copy of End semester Examination Question Papers (Old and Current), solution of current examination with stage-wise marking scheme

1. Lab experiments from manual
2. Other programs from class notes/presentation
3. Continuous lab assessments and final lab viva

13.Course Covered Beyond Syllabus

Not covered beyond syllabus

14.Actual Engagement of Lab

Teaching Hours/Week: 2 Hour/Week
Term Start to End Date: 25th July 2022 to 18th November 2022
Subject Teacher: Tanmaya Bhowmik, Hiren Kumar Thakkar, Rashmi Bhattad
Division: Combined (Offline)

Sr.No.	Lab Exercise	Date of Experiment
1.	Implement Basic Gate Operations. **Task:** To implement AND, OR, NOT, NAND, NOR, XOR, XNOR using Logisim/Verilog.	25-07-2022
2.	Design of various adders - 1 **Task:** To design a Half adder and Full adder using Logisim/Verilog.	01-08-2022
3.	Design of Various Adders – 2 **Task:** To design a carry-look-ahead adder, parallel adder, ripple-carry adders.	08-08-2022
4.	Design of Flip Flops (any Two) **Task:** To design following flip-flops. SR Flip-Flop D Flip-Flop JK Flip-Flop T Flip-Flop	22-08-2022
5.	Design of Registers and Counters **Task:** To design following registers and counters. 1. Asynchronous UP/Down Counter. 2. Synchronous UP/Down Counter. 3. 04-bit registers. 4. Shift registers.	29-08-2022
6.	Design of combinational multiplier	05-09-2022
7.	Design of booth's multiplier	12-09-2022
8.	Design of ALU	19-09-2022
9.	Design of memory (4 * 4) RAM	26-09-2022
10	Design of K-map Design	03-10-2022
11	Design of Quine - Mc Clusky Algorithm	10-10-2022