**TUTORIAL 3**

1. a. How many 128 × 8 RAM chips are required to provide a memory capacity of 2048 bytes?

   b. How many lines of the address bus must be used to access 2048 bytes of memory? How many of these lines will be common to all chips?

   c. How many lines must be decoded for chip select? Specify the size of the decoders.

2. A set-associative cache consists of 64 lines, or slots, divided into four-line sets. Main memory consists of 4K blocks of 128 words each. Show the main memory address format.

3. Obtain the complement function of the match logic of one word in an associative memory.