Department of CSE
Pandit Deendayal Energy University (PDEU)
Digital Electronics and Computer Organization Lab (DECO)
20CP203P

Lab 1: Basic GATE operations
(Week 01-Aug-2022 to 07-Aug-2022)

In this lab, you will learn how Logisim works and will simulate some sample blocks.
This will help you learn more about digital system design.

Logisim (http://www.cburch.com/logisim/) is a Java application, it can be obtained from http://sourceforge.net/projects/circuit/. Note: JDK installation is prerequisite before using the Logisim. Simply download and run it (tutorial is available help->tutorial).

Learn the interface of the software and learn how basic gates works, how to give input and output signals.

1. Design the following logic functions using basic gates and test the output using truth table.
   - 1.1 Y = ABC + DE + F
   - 1.2 Z = A'B' + AB' + A'B + AB
   - 1.3 K = (A'+B') (A+B') (A'+B) (A+B)
2. Design the verify the functionality using existing library of basic gates in logisim.
   - 2.1 Y = ((A+B).(C+D+E))'
   - 2.2 F = ((A.B')'+((A)'(B)')')'
   - 2.3 K = (((A)'+B)'. ((A)'+(B)')')'
3. For each of the following problem statement, design a circuit, describe a Truth table and verify the outcome using Logisim.
   - 3.1 Implement the functionality of XOR gate using only NAND gates.
   - 3.2 Implement the functionality of XNOR gate using only NOR gates.
   - 3.3 Implement the functionality of AND gate using only NAND gates.
   - 3.4 Implement the functionality of OR gate using only NOR gates.
   - 3.5 Implement the functionality of NOT gate using only NAND gate.

Submission Instructions:
Prepare the submission file according to the following steps.

1. Copy (Snip/snapshot) the Design circuit and past into the word file.
2. Prepare a corresponding Truth table.
3. Repeat step 1 and 2 for all the problems.
4. For each problem the corresponding circuit design figure must be number accordingly. For example (Fig 1.1 The Circuit Design of XOR using NAND Only).
5. Convert it into pdf file, name it as **RollNo_Assignment# (Example: 20BCP001_ Assignment1.pdf)**.

- Print the corresponding PDF file and prepare a file (Hard copy).

- **The assignment of the previous lab will be verified in the very next lab. Therefore, it is mandatory to bring the file in each lab.**
- Late submission will lead to penalty.
- Any form of plagiarism/copying from peer or internet sources will lead penalty.
- Following of all instructions at submission time is mandatory. Missing of any instructions at submission time will lead to penalty of marks.