Department of Computer Science and Engineering
Pandit Deendayal Energy University
Digital Electronics and Computer Organization Lab – **20CP203P**

Lab 5: Design a Half Subtractor, Full Subtractor using Half Subtractors

Question 1: Write a Verilog code to design a Half subtractor and test it using the Waveform.

Question 2: Write a Verilog code to design a Full subtractor using Half subtractors and test it using the Waveform.

Question 3: Write the Verilog code (either structural or behavioral) for a 4-bit ripple carry adder. The block diagram of a 4-bit ripple carry adder has been given in Figure 1 for your reference.

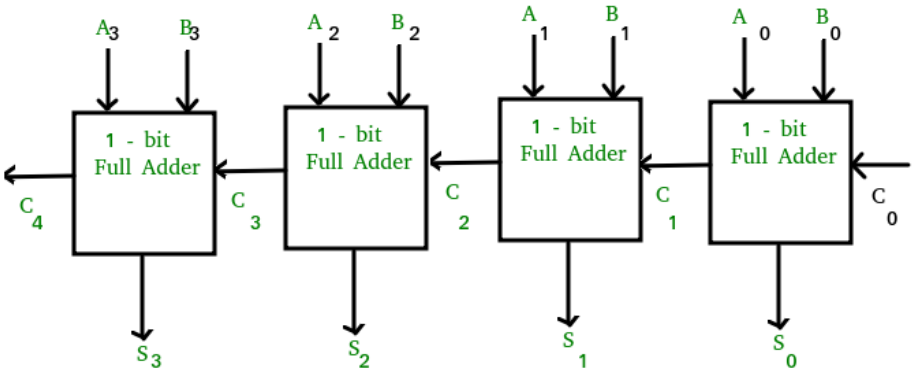

Figure 1: The Block Diagram of four bit ripple carry adder.

Question 4: Write the Verilog code to construct a 4-bit adder-subtractor using. The logic diagram of a 4-bit adder-subtractor using a ripple carry adder has been given in Figure 2 for your reference.

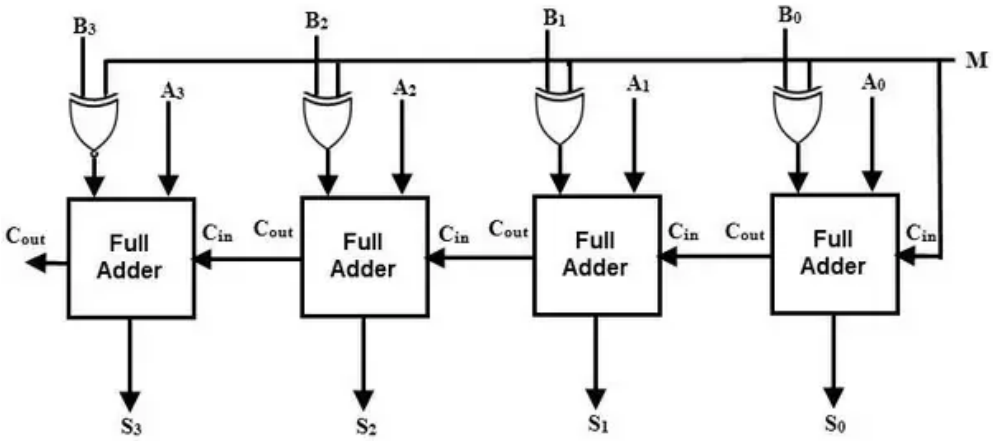

Figure 2: The Block Diagram of four bit adder-cum-subtractor bit.

Question 5: Write the Verilog code for a 4-bit carry look-ahead adder (CLA). The block diagram of the same has been given in Figure 3.

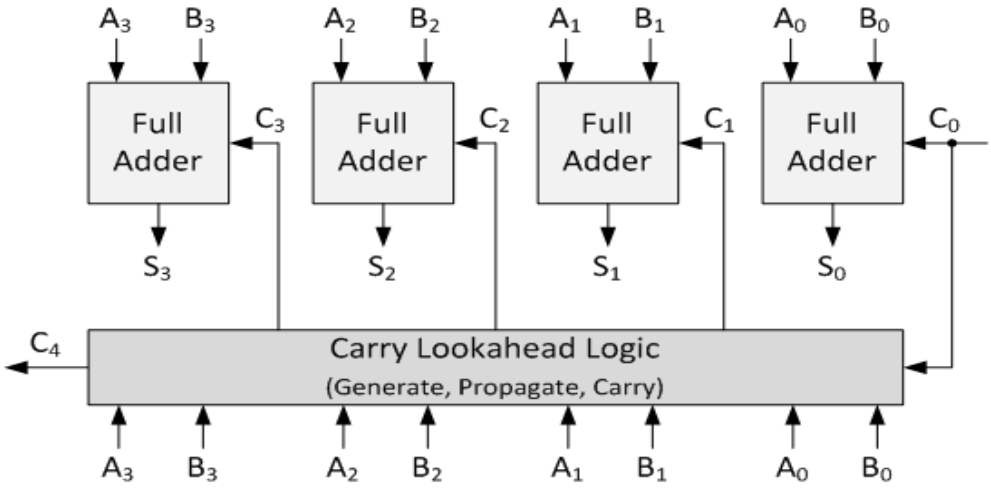

Figure 3: The Block Diagram of four bit carry look-ahead adder (CLA).

Submission Instructions:

- Prepare the submission file according to the following process:
    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.
    4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.

Convert it into pdf file, Print it and prepare a file for the verification in the next lab.