available FF=T Required of = D

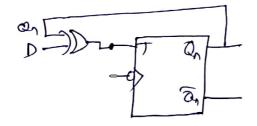
1) Identity available and required off 3) make characteristic table bor required off

(3) Make excitation tech los cevailable F/F

4) Write boolean extremion box available F/F

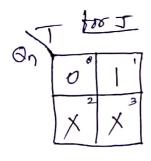
Draw the circuit

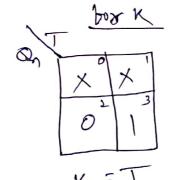
Qn	D	Q_{1+1}	7
0	0	0	0
0	1	1	1
1	0	0	1
1	1	1	0



Qn	T	Qn+1		K
0	O	0	0	X
0	1	1	1	X
1	0	1	X	a
1	1	0	X	j

Q_{2}	Q_{n+1}	I	K
0	0	0	0
0	1 /	1	\times
1	0	\times	1
1	1	X	0





A mod-6 counter has six stades 000,001,010,011, 100, 101. When the sixty slock pulse is applied, the counter should reset to 000. (Though it will temporarily goes + 910 stade) This will happen as we are providing feed back.

It is a divide by 6 counter, in the sense that it divides the input about brequency by 6.

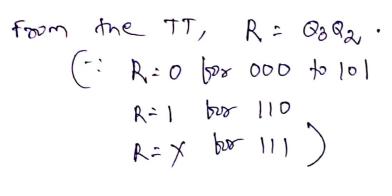
It requires 3 FFs as smallest value satisfying the Cordinan N & 27 is n=3.

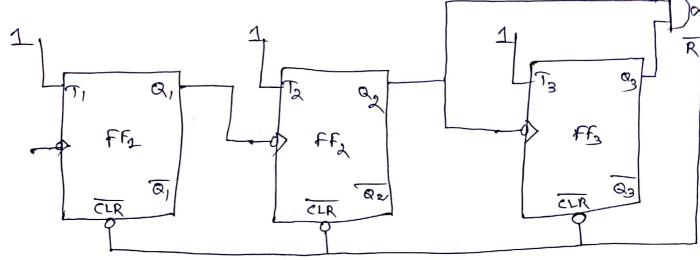
Three FFs can have eight passible stades, out of which only six are utilized and the remaining two stades 110 and 111, are invalid.

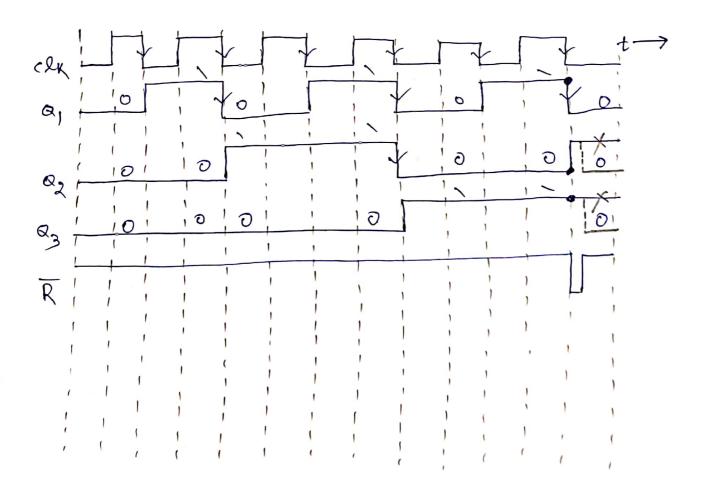
16 initially the counter is in 000 stat, then alter 15 in 1000, above the second 15+ clock pulse it goes to 000, and so on. Abover the sixth chark pulse it goes to 000.

		take	.	R
After pulses	Q3	Qz	QI	
<u></u>	-0	O	0	0
0	-0	0)	0
2	-0	Y	0	\circ
3-	_ ව	1	1	0
4	_1	0	0	O
5 ~	-)	0)	0
6 —	-	1	0	1
	:	'. O	0	0
7	0	0)	0









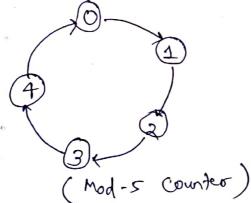
(4) The number of ffs n is to be selected such that the number of states $N \leq 2^n$. With n ffs, the largest count possible is 2^n-1 .

Theselox,

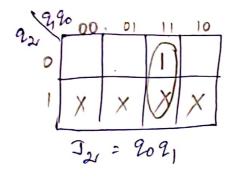
So, the number of FFs regulated is 14.

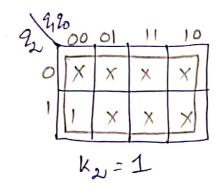
Frequency at the output of last stage is
$$f_{14} = \frac{f_c}{2^{14}} = \frac{8192 \text{ MHz}}{16,384} = 500 \text{Hz}$$

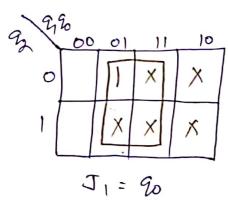
(5) Stale Diagoan:

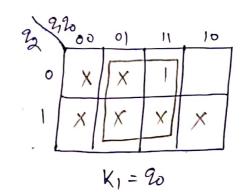


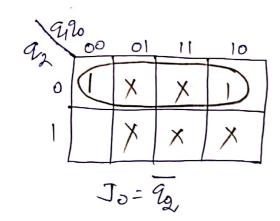
Excitation Inputs Poesent Stark Next Stade Ko J, K, J2 K2 02 Q_0 20 Q₁ 21 921 0 0 OX 0 0 \mathcal{O} \times 0 X 0 0 1 X 0 0 0 X 0 1 0 0 X X O 0 X XX 0 \times X X ١ 0 X X X

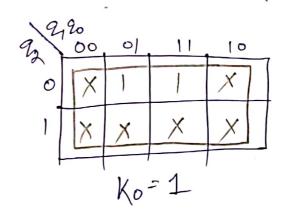


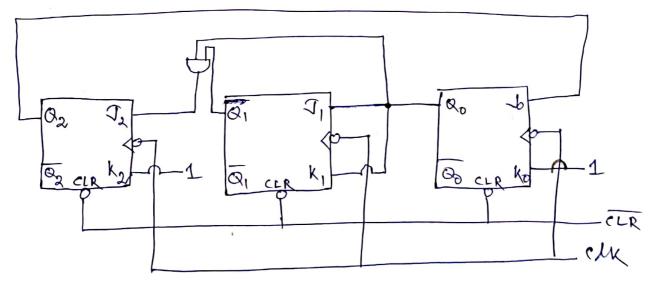


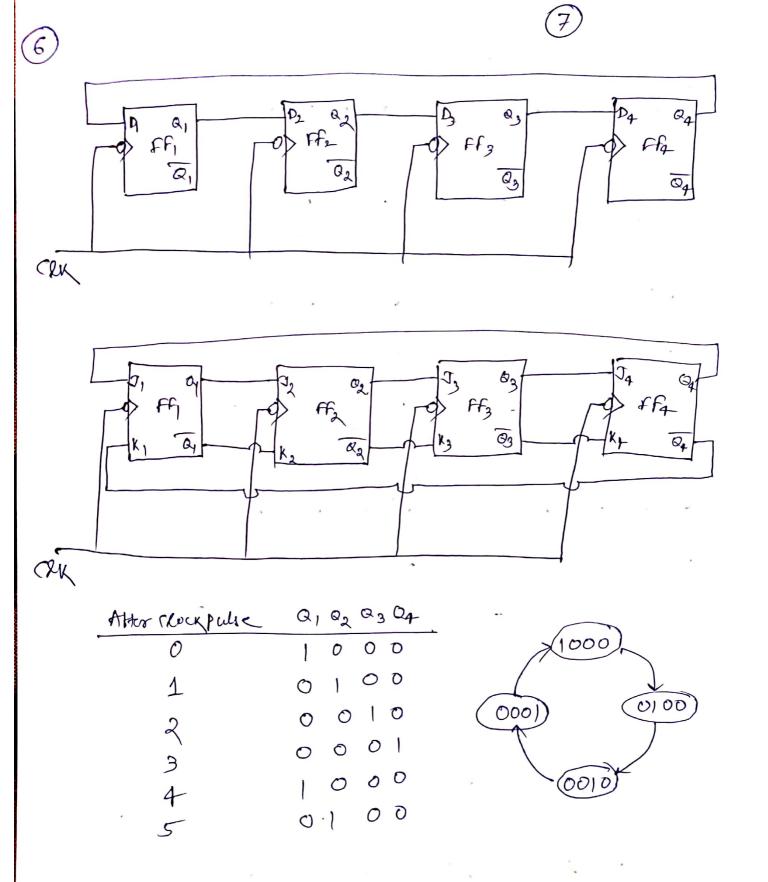


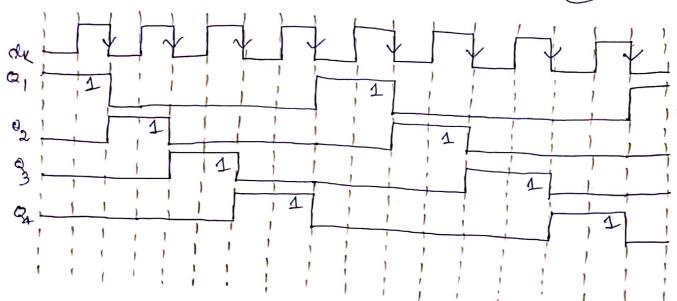












The FFs are arranged as in a normal shift register, i.e. the goutput of each stage is connected to the Dinput of the next stage, but the Quetput of the last FF is connected back to the Dinput of the first FF such that the array of FFs is arranged in a ring and therebox the name ring counter.