Pandit Deendayal Energy University
School of Technology
Department of Computer Science and Engineering
Odd Semester 2022
Course student handout file
INDEX

Name of the course: Digital Electronics & Computer Organization	**Course Code: 20CP203T**
Program: B.Tech. **Branch: CSE**	**Semester: III** **Academic Year: 2022-23**
Name of Course Coordinator: Tanmay Bhowmik	
Subject Teachers (Division wise/Batch wise): **1. Tanmay Bhowmik (G7, G8, G8, G9, G10, G11, G12)** **2. Tushar Kakaiya (G1, G2, G3, G4, G5, G6)**	

Date:

Signature of Subject Teachers **Signature of Department Coordinator (IQAC)** **Signature of Head of the Department**

Departmental Vision & Mission

Vision

"To contribute to the society by imparting transformative education and producing globally competent professionals having multidisciplinary skills and core values to do futuristic research & innovations."

Mission

- To accord high quality education in the continually evolving domain of Computer Engineering by offering state-of-the-art undergraduate, postgraduate, doctoral programmes.
- To address the problems of societal importance by contributing through the talent we nurture and research we do:
- To collaborate with industry and academia around the world to strengthen the education and multidisciplinary research ecosystem.
- To develop human talent to its fullest extent so that intellectually competent and imaginatively exceptional leaders can emerge in a range of computer professions.

Program educational objectives (PEOs) of Department

The Program Educational Objectives of B. Tech. (Computer Engineering) program are:

1. To prepare graduates who will be successful professionals in industry, government, academia, research, entrepreneurial pursuit and consulting firms
2. To prepare graduates who will make technical contribution to the design, development and production of computing systems
3. To prepare graduates who will get engage in lifelong learning with leadership qualities, professional ethics and soft skills to fulfill their goals
4. To prepare graduates who will adapt state of the art development in the field of computer engineering

Program Outcomes (POs)

Undergraduate engineering program are designed to prepare graduates to attain the following program outcomes:

1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. Problem analysis: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. Design / development of solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. Modern tool usage: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
8. Ethics: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. Individual and team work: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. Communication: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. Project management and finance: Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. Life-long learning: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

Program Specific Outcomes (PSOs)

The graduates of CSE department will be able to:

1. Develop computer engineering solutions for specific needs in different domains applying the knowledge in the areas of programming, algorithms, hardware-interface, system software, computer graphics, web design, networking and advanced computing.
2. Analyze and test computer software designed for diverse needs.
3. Pursue higher education.

Academic Calendar

ACADEMIC CALENDAR 2022-23 (ODD SEMESTER)

		11	12	13	14	15	16	17	FACULTY DEVELOPMENT PROGRAMME WEEK
		18	19	20	21	22	23	24	FACULTY DEVELOPMENT PROGRAMME WEEK
1	JULY 2022	25	26	27	28	29	30	31	COMMENCEMENT OF ODD SEMESTER: July 25
2	AUGUST	1	2	3	4	5	6	7	
3		8	9	10	11	12	13	14	RAKSHA BANDHAN
4		15	16	17	18	19	20	21	INDEPENDENCE DAY, JANMASHTAMI
5		22	23	24	25	26	27	28	
6	SEP	29	30	31	1	2	3	4	SAMVATSSARI
7		5	6	7	8	9	10	11	
8		12	13	14	15	16	17	18	**MID-SEM EXAMINATIONS**
9		19	20	21	22	23	24	25	
10	OCT	26	27	28	29	30	1	2	COURSE FEEDBACK WEEK
11		3	4	5	6	7	8	9	DUSSHERA
12		10	11	12	13	14	15	16	
13		17	18	19	20	21	22	23	
14		24	25	26	27	28	29	30	DIWALI WEEK
15	NOV	31	1	2	3	4	5	6	
16		7	8	9	10	11	12	13	GURU NANAK JAYANTI
17		14	15	16	17	18	19	20	COMPLETION OF ODD SEMESTER: Nov. 18
		21	22	23	24	25	26	27	**FOET Practical Exams : Nov.21 Onwards** **FOLS Sem. End Examination : Nov. 21 Onwards**
	DEC	28	29	30	1	2	3	4	**FOET Sem. End Examination : Nov.28 Onwards**
		5	6	7	8	9	10	11	
		12	13	14	15	16	17	18	Rural Internship for FOLS Students: Dec. 17, 2022 to Jan. 10, 2023
		19	20	21	22	23	24	25	
		26	27	28	29	30	31	1	**WINTER BREAK**

Class Time Table and Faculty Time Table with office hours

Tanmay Bhowmik
Computer Science &Engineering

Autumn Semester 2022 — w.e.f : 1st July 2022

Day	08:00-09:00	09:00-10:00	10:00-11:00	11:00-12:00	12:00-13:00	13:00-14:00	14:00-15:00	15:00-16:00	16:00-17:00	17:00-18:00	18:00-19:00
Monday	G12 (20CP203P) E214, CP(3) - P						G11G12 (20CP203T) Y5, CP(3) - L	G9G10 (20CP203T) D005, CP(3) - L			
Tuesday			G9G10 (20CP203T) E104, CP(3) - L				G11 (20CP203P) E115, CP(3) - P			G7G8 (20CP203T) E105, CP(3) - L	
Wednesday				G11G12 (20CP203T) Y6, CP(3) - L				G11G12 (20CP203T) Y6, CP(3) - L		G7G8 (20CP203T) E105, CP(3) - L	
Thursday							G9G10 (20CP203T) Y6, CP(3) - L			G7G8 (20CP203T) E105, CP(3) - L	
Friday	G6 (20CP203P) F-103, CP(3) - P										
Saturday											

Location Abbr.	Location Name
D005	D, Lecture Hall
E104	E, Lecture Hall
E105	E, Lecture Hall
E115	E, ICT Lab1
E214	E, ICTLAB2
F-103	F, HPC LAB
Y5	F, Lecture Hall
Y6	F, Lecture Hall

Subject Abbr.	Subject Name
20CP203P	Digital Electronics &Computer Organization Lab
20CP203T	Digital Electronics &Computer Organization

Office Hours: 16:00 – 17:00 (Students are requested to drop a prior mail before contacting on office hours)

20CP203T					Digital Electronics and Computer Organization					
Teaching Scheme					Examination Scheme					
L	T	P	C	Hrs/Week	Theory			Practical		Total Marks
					CE	MS	ES	LW	LE/Viva	
3	0	0	3	3	25	25	50	-	-	100

COURSE OBJECTIVES

- To introduce the basics involved in data representation and digital logic circuits used in the computer system including logic elements, and their use in combinational and sequential logic circuit design.
- To understand the architecture of processing, memory and I/O organization in a computer system.
- To understand the state transition diagrams to prepare circuits.

UNIT 1 NUMBER SYSTEMS **10 Hrs.**

Introduction to Number Systems, Conversion from one to another, 1's and 2's Complements, Introduction to Boolean Algebra: Addition and Multiplication in Boolean algebra: Binary Logic Functions, Logical Gates and Truth Tables; DEMORGAN's Theorem, Combinational Logic: Forms; Sum of Products Form, Product of Sum Form, K – Map: Plotting a Boolean expression and Logic expression simplification with grouping cells, Quine McClusky Method

UNIT 2: COMBINATIONAL AND SEQUENTIAL CIRCUITS **12 Hrs.**

Analysis and Design of Combinational Logic: Introduction: Binary adders; Half adder, Full adder: Binary Subtractor; Half subtractor, Full subtractor, Decoders; Encoders; Multiplexers, Demultiplexers: Parity Generators and Parity Checkers; Parity, Detecting an Error.

Latches: The S-R Latch (NOR, NAND); Gated Latches; Gated S-R Latches, Gated D-Latch or D-flip-flop: Edge triggered Flip-Flops; Edge triggered S-R Flip-Flop (S-R FF), Edge triggered D-Flip-Flop (D-FF), Edge triggered J-K Flip-Flop (J-K FF), Master-Slave J-K Flip Flop

UNIT 3: CENTRAL PROCESSING UNIT (CPU) **9 Hrs.**

General register organization, the operation of memory stack, variety of addressing modes, instruction format. RISC architecture and CISC architecture. Examples of processors and instruction execution employing RISC and CISC architecture, Introduction to control unit (Hardwired, Microprogrammed).

UNIT 4: INPUT-OUTPUT ORGANIZATION **8 Hrs.**

Computer communication with input and output devices. I/O interface units are presented to show the way that the processor interacts with external peripherals. Memory Organization - The concept of memory hierarchy: cache memory, main memory, auxiliary memory. Virtual memory, Memory Management: physical address and logical address mapping

Max. 39 Hrs

COURSE OUTCOME

CO1: Describe basic gate operations and laws of Boolean algebra.
CO2: Explain basic structure of digital computer, stored program concept and different arithmetic and control unit operations.
CO3: Understand basic structure of different combinational circuits- multiplexer, decoder, encoder.
CO4: Analyze various digital electronic circuits.
CO5: Identify the basic aspects of instruction execution, and examine the sub-operations of computer arithmetic.
CO6: Categorize the organization of memory, and I/O modules.

TEXT/REFERENCE BOOKS

1. V. Rajaraman, T. Radhakrishnan, "Digital Logic and Computer Organization", Prentice Hall India Learning Private Limited; 1 edition (2006)
2. Nikrouz Faroughi, "Digital Logic Design and Computer Organization: With Computer Architecture for Security", 2015 McGraw-Hill Education
3. Yale N. Patt, Sanjay J. Patel, "Introduction to Computing Systems" McGraw Hill
4. C.Hamacher, Z.Vranesic and S.Zaky, Computer Organization, 5th Ed., McGraw-Hill, 2002

END SEMESTER EXAMINATION QUESTION PAPER PATTERN

Max. Marks: 100 **Exam Duration: 3 Hrs**

Part A: 10 Questions of 2 marks each-No choice 20 Marks
Part B: 2 Questions from each unit with internal choice, each carrying 20 marks 80 Marks

Lesson Plan

Lecture No.	Topic to be covered	Teaching Aid to be used	Remarks (Text book/Unit No etc.)
1	Introduction to Number Systems, Conversion from one to another	BW + PPT	Unit 1
2	1's and 2's Complements	BW + PPT	Unit 1
3	Introduction to Boolean Algebra	BW + PPT	Unit 1
4	Addition and Multiplication in Boolean algebra	BW + PPT	Unit 1
5	Logical Gates and Truth Tables	BW + PPT	Unit 1
6	Binary Logic Functions	BW + PPT	Unit 1
7	DEMORGAN's Theorem, Combinational Logic	BW + PPT	Unit 1
8	Forms; Sum of Products Form, Product of Sum Form	BW + PPT	Unit 1
9	K – Map: Plotting a Boolean expression and Logic expression simplification with grouping cells	BW + PPT	Unit 1
10	Quine McClusky Method	BW + PPT	Unit 1
11	Analysis and Design of Combinational Logic circuit	BW + PPT	Unit 2
12	Binary adders; Half adder	BW + PPT	Unit 2
13	Full adder	BW + PPT	Unit 2
14	Binary Subtractor; Half subtractor, Full subtractor	BW + PPT	Unit 2
15	Decoders; Encoders	BW + PPT	Unit 2
16	Multiplexers, Demultiplexers	BW + PPT	Unit 2
17	Parity Generators and Parity Checkers; Detecting an Error.	BW + PPT	Unit 2
18	Latches: The S-R Latch (NOR, NAND)	BW + PPT	Unit 2
19	Gated Latches; Gated S-R Latches, Gated D-Latch or D-flip-flop	BW + PPT	Unit 2
20	Edge triggered Flip-Flops; Edge triggered S-R Flip-Flop (S-R FF)	BW + PPT	Unit 2
21	Edge triggered D-Flip-Flop (D-FF), Edge triggered J-K Flip-Flop (J-K FF)	BW + PPT	Unit 2
22	Master-Slave J-K Flip Flop	BW + PPT	Unit 2
23	General register organization	BW + PPT	Unit 3
24	The operation of memory stack	BW + PPT	Unit 3
25	Variety of addressing modes	BW + PPT	Unit 3
26	Instruction format	BW + PPT	Unit 3
27	RISC architecture and CISC architecture	BW + PPT	Unit 3
28	Examples of processors	BW + PPT	Unit 3
29	instruction execution employing RISC and CISC architecture	BW + PPT	Unit 3
30	Introduction to control unit (Hardwired control)	BW + PPT	Unit 3
31	Introduction to control unit (Microprogrammed control)	BW + PPT	Unit 3
32	Computer communication with input and output devices	BW + PPT	Unit 4
33	I/O interface units are presented to show the way that the processor interacts with external peripherals	BW + PPT	Unit 4

34	Memory Organization	BW + PPT	Unit 4
35	The concept of memory hierarchy	BW + PPT	Unit 4
36	Cache memory	BW + PPT	Unit 4
37	Main memory, Auxiliary memory	BW + PPT	Unit 4
38	Virtual memory	BW + PPT	Unit 4
39	Memory Management: physical address and logical address mapping	BW + PPT	Unit 4

Legends: BW (Board Work), PPT (Power Point Presentation)

Course Articulation Matrix

CO	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PSO1	PSO2	PSO3
1	3	-	1	2	-	3	1	1	-	-	1	1	3	-	-
2	1	1	-	2	-	3	1	1	-	-	1	1	2	-	-
3	2	1	1	-	-	3	1	1	-	-	1	1	2	-	-
4	2	3	3	1	-	2	1	1	-	-	2	1	2	-	-
5	1	2	3	2	-	2	1	1	-	-	1	1	2	-	-
6	1	2	3	1	-	2	1	1	-	-	2	1	2	-	-
	1.6	1.5	1.8	1.3	-	2.5	1	1	-	-	1.3	1	2.1	-	-

Program Articulation Matrix

PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11	PO12	PS01	PSO2	PSO3
3	3	2	1	1	2	1	1	2	2	2	3	3	3	3

Correlation levels 1, 2 or 3 as defined below:

1: Slight (Low) 2: Moderate (Medium) 3: Substantial (High)

Evaluation Scheme and Rubrics

Course code: 20CP203T **Course name:** Digital Electronics & Computer Organization

Course Outcomes (CO's): On completion of the course, students will be able to

CO1. **Understand** the basic gate operations and laws of Boolean algebra, basic aspects of instruction execution, and examine the sub-operations of computer arithmetic.
CO2. **Explain** the basic structure of digital computer, stored program concept and different arithmetic and control unit operations
CO3. **Apply** different combinational circuits- multiplexer, decoder, encoder etc. and Perform different operations with sequential circuits
CO4. **Analyzed** the organization of memory, the basics of I/O modules.
CO5. **Determine** the logic components necessary to design an electronic circuit.
CO6. **Create** or design of digital electronic circuits

Co Assessment Tools (Direct Assessment):
Various assessment tools used to evaluate CO's (Rubrics) and the frequency with which the assessment processes are carried out are listed below.

Assessment Method	Assessment Tool	Description	Marks	Mapping with CO	Contribution to CO's
Direct (Continuous Evaluation)	Internal Assessment -1	Quiz / MCQ Problem Solving / Design Problem / Case Study	15	CO1, CO2, CO3	It fractionally contributes to 25% weightage of Direct Assessment to CO attainment.
	Internal Assessment -2	Quiz / MCQ Problem Solving / Design Problem / Case Study	15	CO4, CO5, CO6	
Direct	Mid-Sem Examination	Problem Solving/ Descriptive Answering	25	CO1, CO2, CO3, CO4, CO5, CO6	It contributes to 25% weightage of Direct Assessment to CO attainment.
Direct	End-Sem Examination	Problem Solving/ Descriptive Answering	50	CO1, CO2, CO3, CO4, CO5, CO6	It contributes to 50% weightage of Direct Assessment to CO attainment.