Department of CSE
Pandit Deendayal Energy University (PDEU)
Digital Electronics and Computer Organization Lab (DECO)
20CP203P

Lab 2: Introduction to Verilog
(Week 02)

In this Lab, we shall start Verilog. To run Verilog, we shall use http://www.edaplayground.com. After opening you will find Design or Testbench window pane. In the Design window you need write the Verilog Code and in the Testbench window, the testbench verification code will be written.

1. Write a Verilog code to implement AND gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of AND Gate:

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

2. Write a Verilog code to implement OR gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of OR Gate:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

3. Write a Verilog code to implement XOR gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of XOR Gate:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

4. Write a Verilog code to implement NOR gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of NOR Gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

5. Write a Verilog code to implement NAND gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of NAND Gate:

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

6. Write a Verilog code to implement XNOR gate. Write the corresponding Testbench code for the verification of your Verilog code.

   Truth Table of XNOR Gate:

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

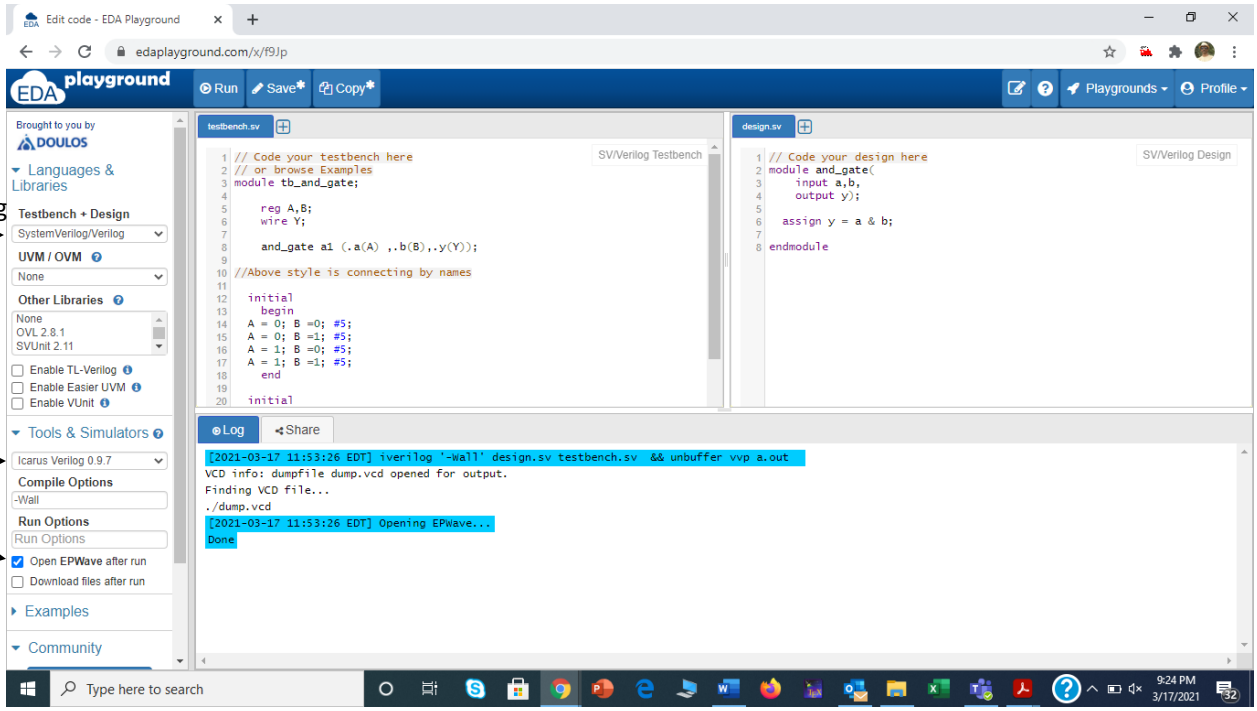
Procedure to run the programs in EDAPlayground:

- **Open** http://www.edaplayground.com
- **Go to Design Window to write the Verilog Code.**
- **Go to Testbench Window to write the Testbench Verification Code.**
- **All the other setup should be done according to the following Screenshot**

(1)
Select SystemVerilog

(2)
Select Icarus Verilog 0.9.7 in Tools and Simulator

(3)
Make it sure the check box has been clicked “Open EPWave after run”



- **Sample Verilog Code for AND Gate:**

```
module and gate(
    input a,b,
    output y);
    assign y = a & b;
endmodule
```

- **Sample Testbench Code for the AND Gate:**

```
module tb_and_gate;

    reg A,B;
    wire Y;
    and_gate a1 (.a(A) ,.b(B),.y(Y));

initial
    begin
        A = 0; B =0; #5;
        A = 0; B =1; #5;
        A = 1; B =0; #5;
        A = 1; B =1; #5;
    end
initial
```

```
  begin
    $dumpfile("dump.vcd");
    $dumpvars(1);
  end

endmodule
```

Submission Instructions:

Prepare the submission file according to the following steps.

1. Copy (Snip/snapshot) the Design circuit and past into the word file.
2. Prepare a corresponding Truth table.
3. Repeat step 1 and 2 for all the problems.
4. For each problem the corresponding circuit design figure must be number accordingly. For example (Fig 1.1 The Circuit Design of XOR using NAND Only).
5. Convert it into pdf file, name it as **RollNo_Assignment# (Example: 20BCP001_ Assignment1.pdf)**.

- Print the corresponding PDF file and prepare a file (Hard copy).
- **The assignment of the previous lab will be verified in the very next lab. Therefore, it is mandatory to bring the file in each lab.**
- Late submission will lead to penalty.
- Any form of plagiarism/copying from peer or internet sources will lead penalty.
- Following of all instructions at submission time is mandatory. Missing of any instructions at submission time will lead to penalty of marks.