Tutorial – 12 (Questions)

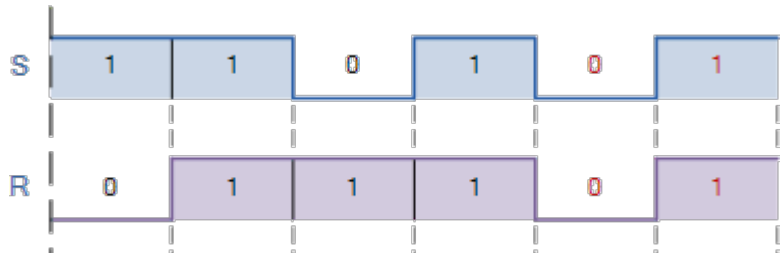
1. Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer, and an inverter.

2. A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11, respectively.

    a. Tabulate the characteristic table.
    b. Tabulate the excitation table.
    c. Derive the characteristic equation.
    d. Show how the PN flip-flop can be converted to a D flip-flop.

3. Show that the characteristic equation for the complement output of a JK flip-flop is
    $Q'(t + 1) = J'Q' + KQ$

4. Draw the wave form for Q and Q' for the SR flip flop assuming clock is high.



5. Implement SR latch using NAND gates and realize it for the following cases. Finally, write the truth table.
    a. S=0 and R=0
    b. S=0 and R=1
    c. S=1 and R=0
    d. S=1 and R=1