Department of Computer Science and Engineering
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Digital Electronics and Computer Organization Lab – **20CP203P**

Lab Assignment – 10 : Flip flops Conversion

In the previous lab we discussed about Sequential circuits. We developed Verilog modules for S-R latch and S-R flip-flops. In today's assignment, we will learn about the conversion of one flip-flop into other.

Please use the table 1, describing the input and output states of various flip-flops for your reference.

Present State	Next State	SR flip-flop inputs		D flip-flop input	JK flip-flop inputs		T flip-flop input
Q t	Q $t+1$	S	R	D	J	K	T
0	0	0	x	0	0	x	0
0	1	1	0	1	1	x	1
1	0	0	1	0	x	1	1
1	1	x	0	1	x	0	0

Table 1: Input and output states of various flip-flops

Q1> The **JK flip flop** is basically a gated SR flip-flop with the addition of a clock input circuitry that prevents the illegal or invalid output condition that can occur when both inputs S and R are equal to logic level “1”.

1) Use the table 1 to develop the conversion table for S-R to J-K flip flop and generate the conversion expression between JK and SR via K map.

2) Use this conversion expression to Modify the S-R flip flop created in last lab into JK flip flop.

3) Verify the functionality of J-K flip flop using suitable Testbench.

Q2> Now lets convert the J-K flip flop created in question 1 into D flip flip. One can use the table 1 to perform similar steps as per previous solution for this conversion.

1) Develop the behavioral verilog module of D flip-flop, converting it from a J-K flip flop. You may utilize **if-else statements** to develop your verilog code.

2) Verify the functionality via a suitable test bench code.

Q3> Develop a characteristic table of T flip-flop along with the excitation inputs of JK flip flop from table 1.

1) Use K map to develop the conversion relation between T and JK flip flop.

2) Develop a behavioral verilog module for JK flip flop using **case** statements. Modify it to act like a T flip flop.

3) Validate the modification via a suitable test bench.

Submission Instructions:

- Prepare the submission file according to the following process:
    1. Copy the Verilog code, the Test Bench Code in a Word File.
    2. Take the ScreenShot of Waveform and paste into the same word file.
    3. Repeat Step 1 and 2 for all the programs.
    4. Copy and Paste all the Verilog code, Testbench Code and Waveform into a single word file as 1_verilog, 1_TestBench, 1_Waveform, 2_verilog, 2_TestBench, 2_Waveform… etc.

Convert it into a pdf file, print it and prepare a file for the verification in the next lab.