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For Odd Roll Number:

Let us assume that Mango Singh is designing a circuit which can produce the bit-wise binary summation and bit-wise binary subtraction. Suppose you are given two four-bit numbers e.g., X_0 X_1 X_2 X_3, and Y_0 Y_1 Y_2 Y_3. Here, X_0 and Y_0 are the least significant bits, and X_3 and Y_3 are most significant bits. Assume the suitable output variables. Write down the Verilog code for the above mentioned problem statement. Display the four-bit output on output screen for sum (S_0 S_1 S_2 S_3) and carry (C_0 C_1 C_2 C_3) for summation mode (m), and difference and borrow for subtraction mode (m). (No need to generate EPWave).

Note: Take X_3 X_2 X_1 X_0, and Y_3 Y_2 Y_1 Y_0 as 0100 and 0001, respectively as inputs.

For Even Roll Number:

Let us assume that Delhi Singh is designing a circuit which can produce the bit-wise binary summation using carry propagator and generator methods. Suppose you are given two four-bit numbers e.g., X_0 X_1 X_2 X_3, and Y_0 Y_1 Y_2 Y_3. Here, X_0 and Y_0 are the least significant bits and X_3 and Y_3 are most significant bits. Assume the suitable output variables. Write down the Verilog code for the above mentioned problem statement with expressions of the outputs. Display the four-bit output on output screen for sum (S_0 S_1 S_2 S_3), carry (C_0 C_1 C_2 C_3), carry generators (G_0 G_1 G_2 G_3), and carry propagators (P_0 P_1 P_2 P_3). (No need to generate EPWave).

Note: Take X_3 X_2 X_1 X_0, and Y_3 Y_2 Y_1 Y_0 as 0101 and 0011, respectively as inputs.