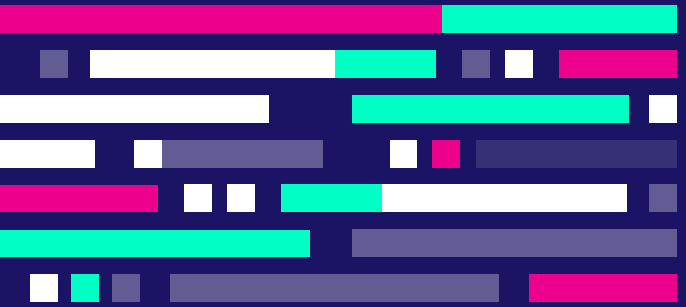
Computer Organization & Architecture



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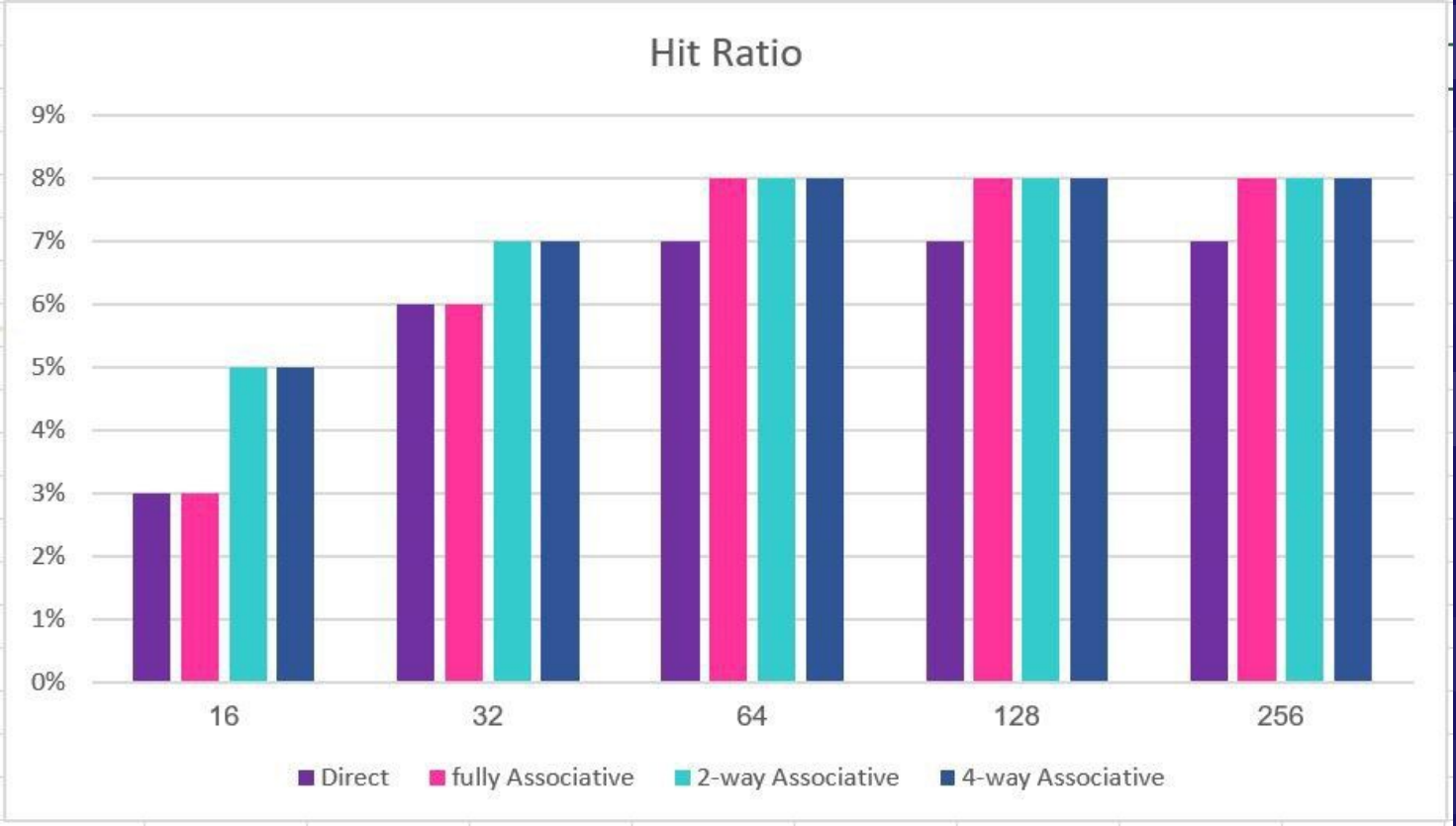
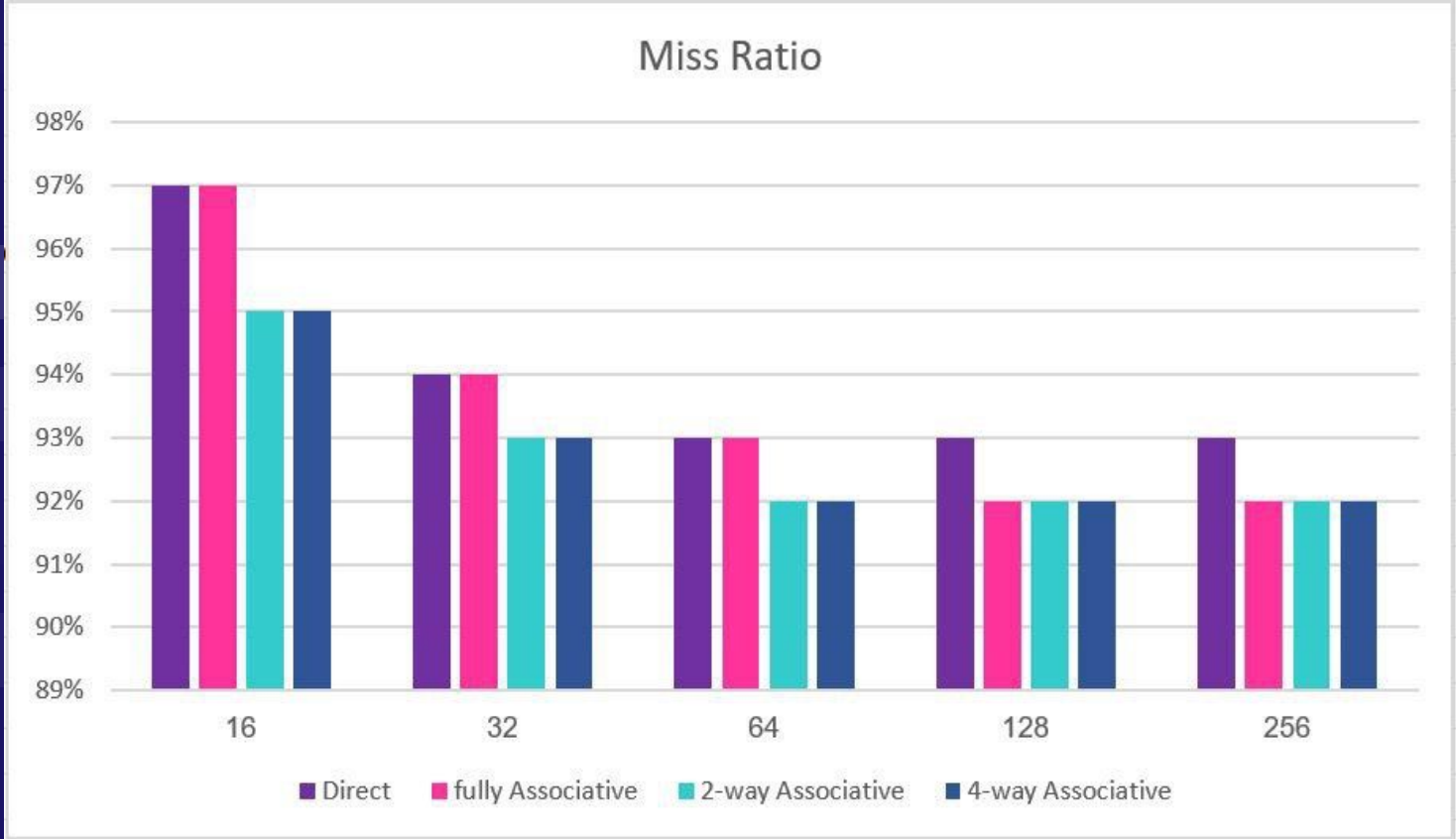
1 Simulation Study of Cache Hit Ratios

Memory Size (power of 2)	512
Offset Bits	0

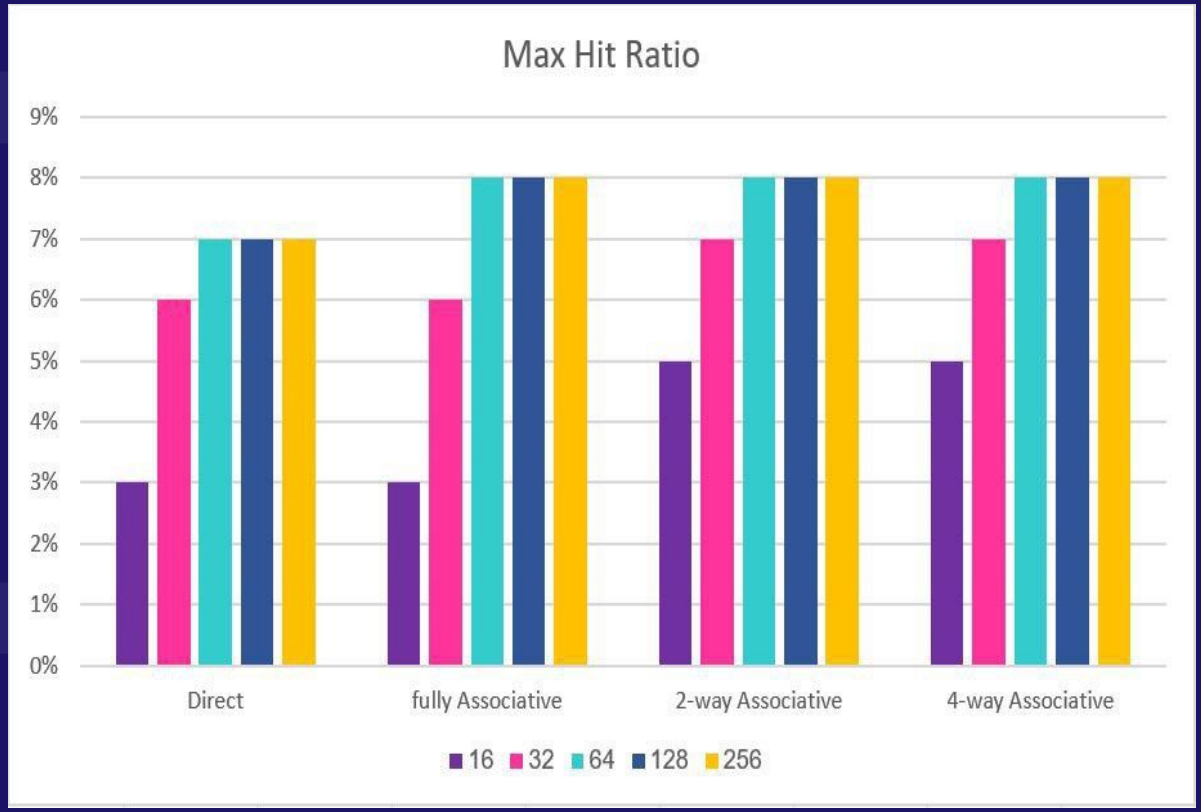


1 Simulation Study of Cache Miss Ratios

Memory Size (power of 2)	512
Offset Bits	0



2 Maximum Hit Ratio



Memory Size (power of 2)	512
Offset Bits	0

3 Mapping Lines

Word (0 bits)	Line (4 bits)	Tag (5 bits)

Direct Mapping

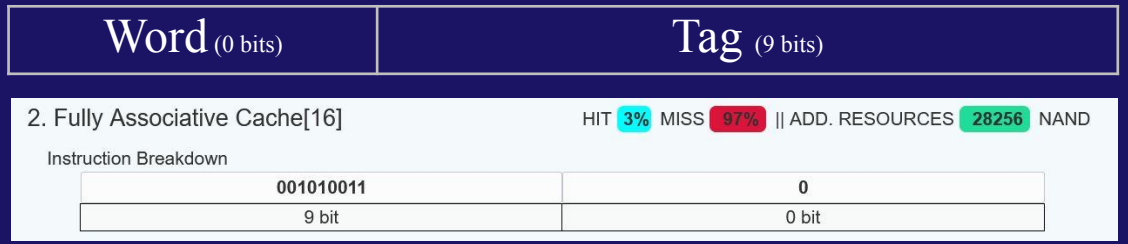
#Number of line
= 2^r = 2^4 = 16

#Size of Tag
= s - r = 9 - 4 = 5 bit

#Number of bits required for RAM address
= s + w ((tag + r) + word) = ((5+4) + 0) = 9 bits

#Size of RAM
= 2^w+s = 2^9 = 512

3 Mapping Lines



Fully Associative Mapping

#Number of line undetermined

#Size of Tag
= 9

#Number of bits required for RAM address
= s + w (tag + word) = (9+0) = 9 bits

#Size of RAM
= 2^w+s = 2^9 = 512

3 Mapping Lines

Word (0 bits)	Set (3 bits)	Tag (6 bits)

3. 2-Way Set Associative Cache[8]

HIT 5% MISS 95% || ADD. RESOURCES 2272 NAND

Instruction Breakdown

001010	011	0
6 bit	3 bit	0 bit

2-way Set Associative Mapping

#Number of line
= k*2^d = 2*2^3 = 16

#Number of sets
= 2^d = 2^3 = 8

#Size of Tag
= s - d = 9 - 3 = 6 bit

#Number of bits required for RAM address
= s + w ((tag + d) + word) = ((6+3) + 0) = 9 bits

#Size of RAM
= 2^w+s = 2^9 = 512

3 Mapping Lines

Word (0 bits)	Set (2 bits)	Tag (7 bits)

4-way Set Associative Mapping

#Number of line
= k*2^d = 4*2^2 = 16

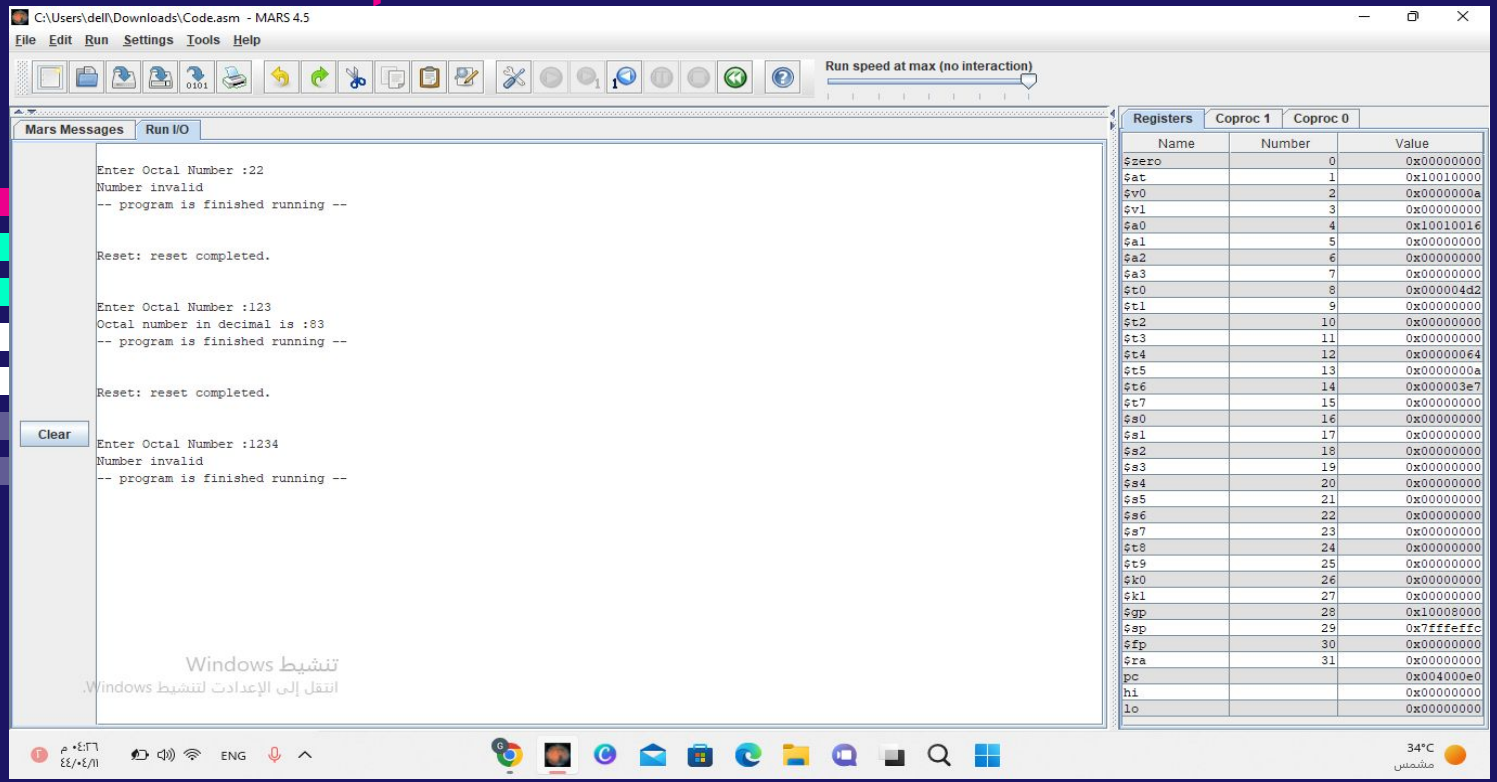
#Number of sets
= 2^d = 2^2 = 4

#Size of Tag
= s - d = 9 - 2 = 7 bit

#Number of bits required for RAM address
= s + w ((tag + d) + word) = ((7+2) + 0) = 9 bits

#Size of RAM
= 2^w+s = 2^9 = 512

4 Assembly Language Program >>output




Thank You!