# Lab<sub>0</sub>

# Lab orientation

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Date: 1/20/2023

CDA 3203 Computer Logic Design
Spring 2023

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#### **Circuit Simulation Results**

Using Altera Quartus II Web Edition 9.1 to simulate a circuit for the equation Y=A\*B'+C'

### **Schematic**

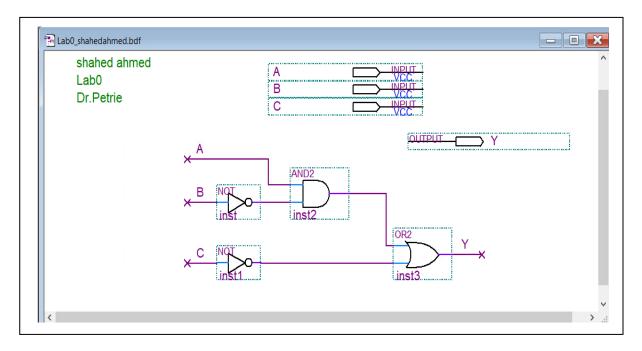


Figure 1: Enter your description HERE

## **Timing Diagram**

