Lab 3

Shahed Ahmed

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CDA 3203 Computer Logic Design

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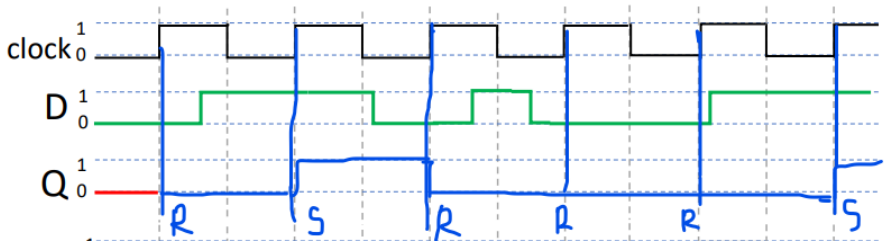
Handwork

1.1 - D Flip Flop

1.1 D Flip Flop

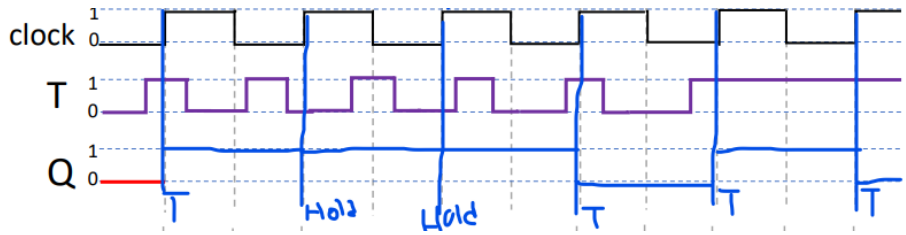
D	Q	Command	Q+
0	0	Make Q=0	0
	1		0
1	0	Make Q =1	1
	1		1



1.2 - T Flip Flop

1.2 T Flip Flop

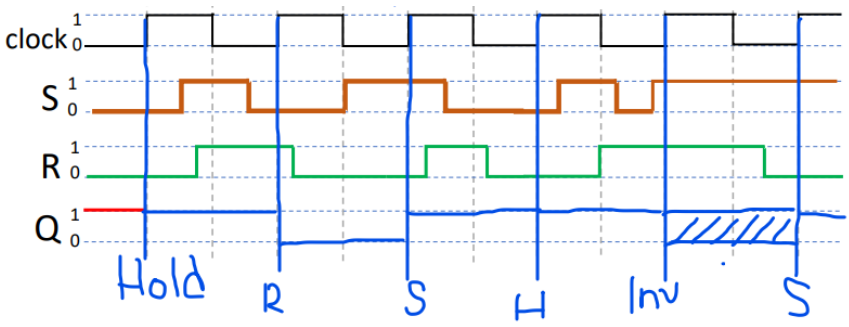
T	Q	Command	Q+
0	0	Hold	0
	1		1
1	0	toggle	1
	1		0



1.3 – S-R Flip Flop

1.3 S-R Flip Flop

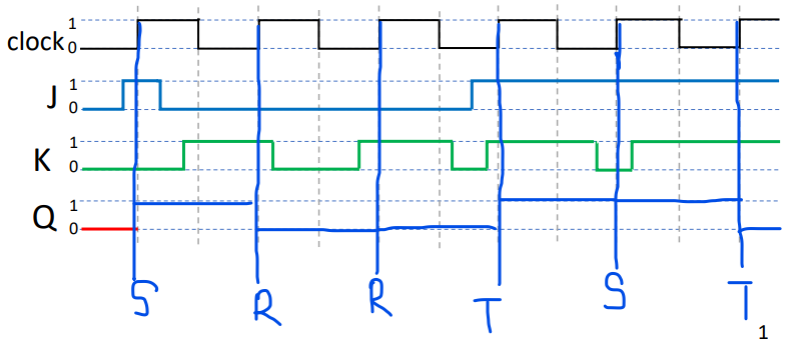
S	R	Q	Command	Q+
0	0	0	HOLD	0
		1		1
0	1	0	RESET	0
		1		0
1	0	0	SET	1
		1		1
1	1	0	INVALID	?
		1		?



1.4 – J-K Flip Flop

1.4 J-K Flip Flop

J	K	Q	Command	Q+
0	0	0	HOLD	0
		1		1
0	1	0	RESET	0
		1		0
1	0	0	SET	1
		1		1
1	1	0	Toggle	1
		1		0



1.5 – Excitation Tables

$Q \rightarrow Q^+$	Command	D
0→0	Make Q=0	0
0→1	Make Q=1	1
1→0	Make Q=0	0
1→1	Make Q=1	1

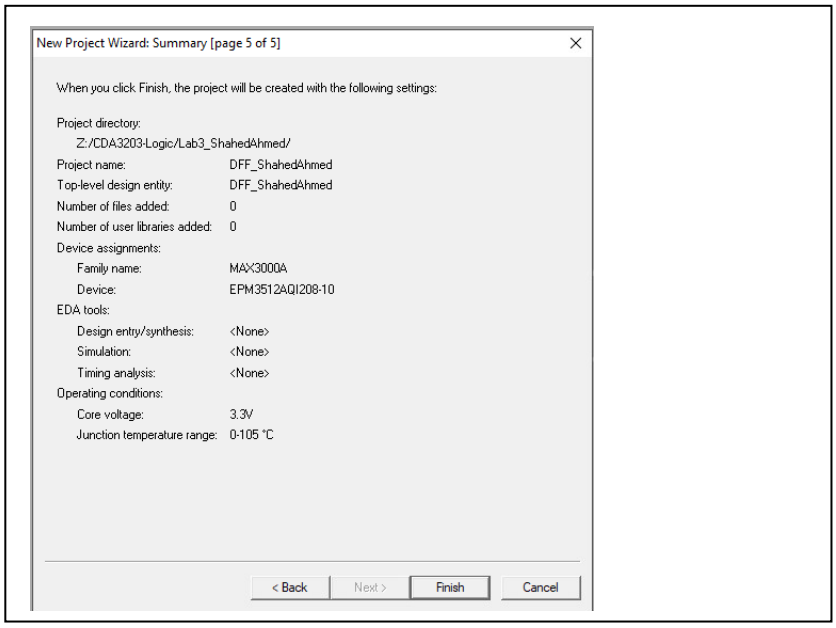
$Q \rightarrow Q^+$	Command	T
0→0	Hold	0
0→1	toggle	1
1→0	toggle	1
1→1	Hold	0

$Q \rightarrow Q^+$	Commands	S R
0→0	Hold reset	0X
0→1	set	10
1→0	reset	01
1→1	Hold set	X0

$Q \rightarrow Q^+$	Commands	J K
0→0	Hold reset	0X
0→1	toggle Set	1X
1→0	toggle reset	X1
1→1	Hold set	X0

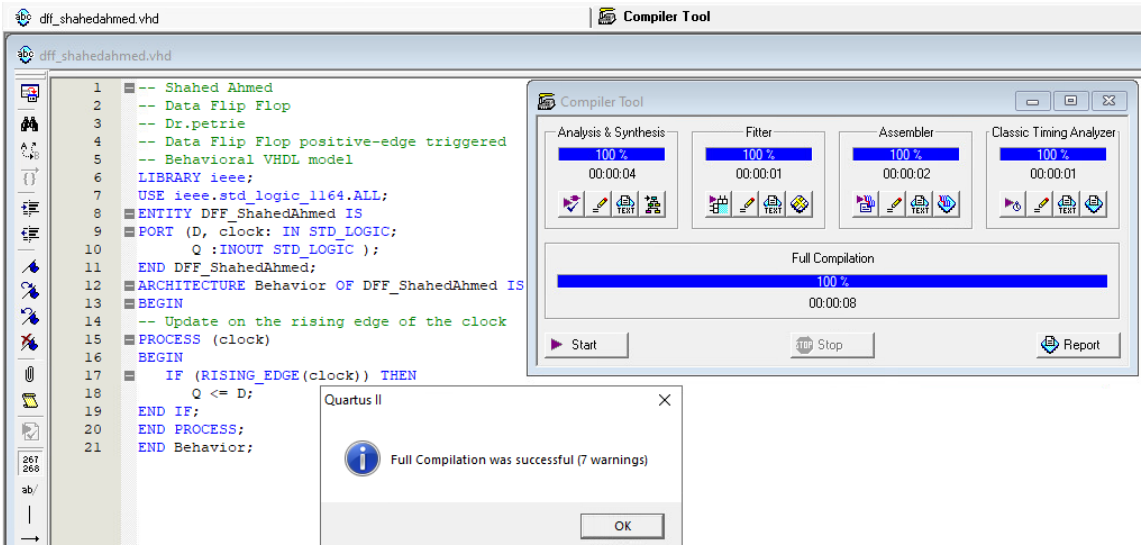
2 – Design and Simulation of Sequential Components in Altera Quartus using VHDL

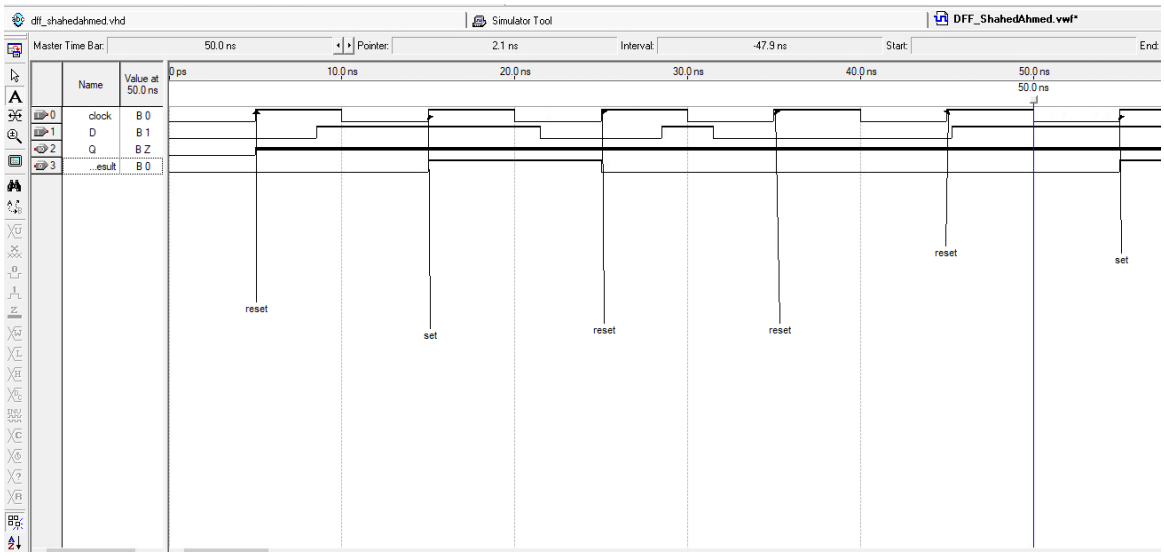
2.1 – Data Flip Flop (DFF)



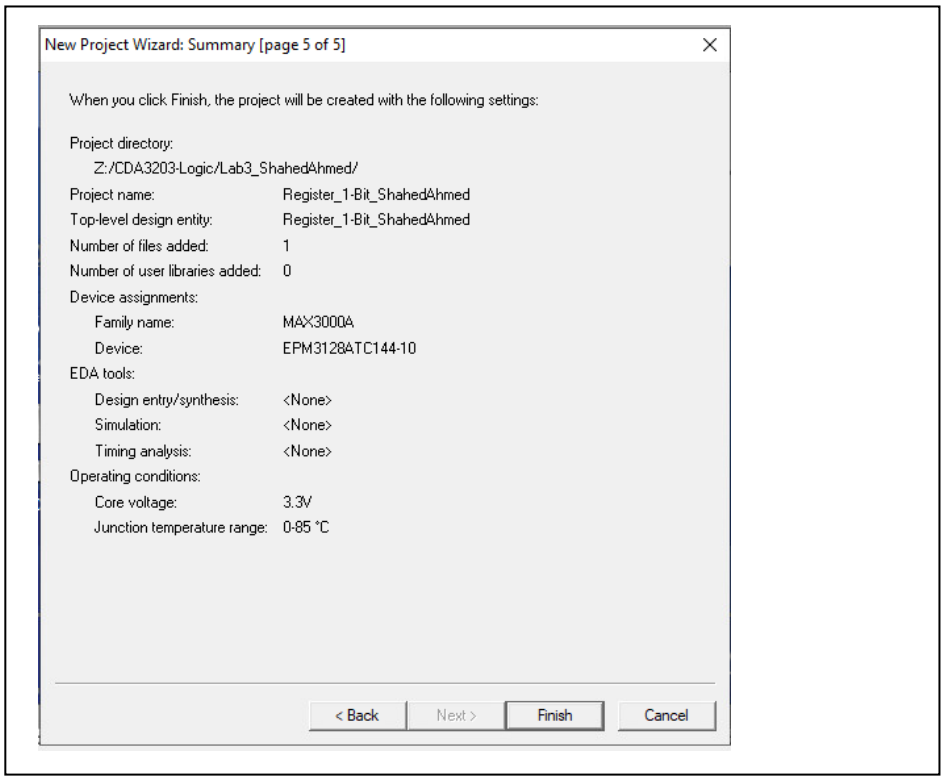
dff_shahedahmed.vhd

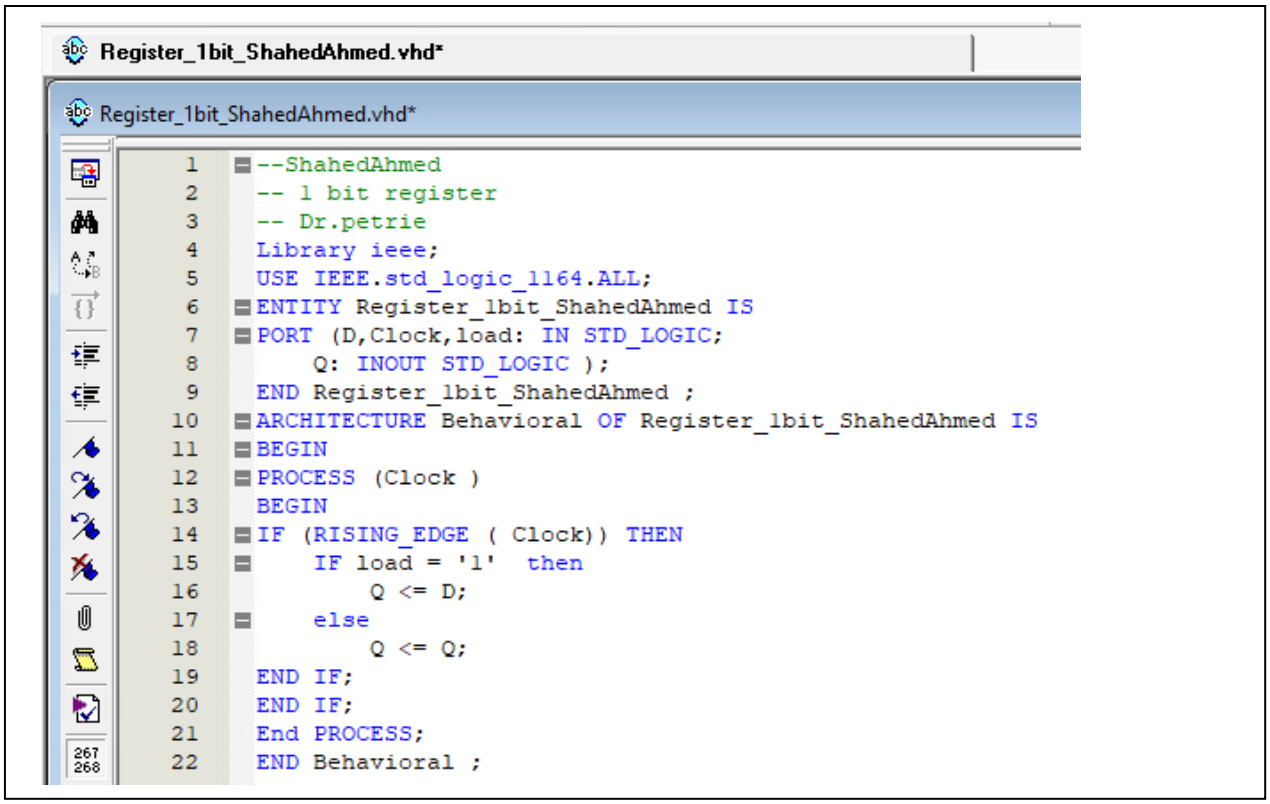
```
1  -- Shahed Ahmed
2  -- Data Flip Flop
3  -- Dr.petrie
4  -- Data Flip Flop positive-edge triggered
5  -- Behavioral VHDL model
6  LIBRARY ieee;
7  USE ieee.std_logic_1164.ALL;
8  ENTITY DFF_ShahedAhmed IS
9  PORT (D, clock: IN STD_LOGIC;
10       Q :INOUT STD_LOGIC );
11 END DFF_ShahedAhmed;
12 ARCHITECTURE Behavior OF DFF_ShahedAhmed IS
13 BEGIN
14 -- Update on the rising edge of the clock
15 PROCESS (clock)
16 BEGIN
17    IF (RISING_EDGE(clock)) THEN
18       Q <= D;
19 END IF;
20 END PROCESS;
21 END Behavior;
```

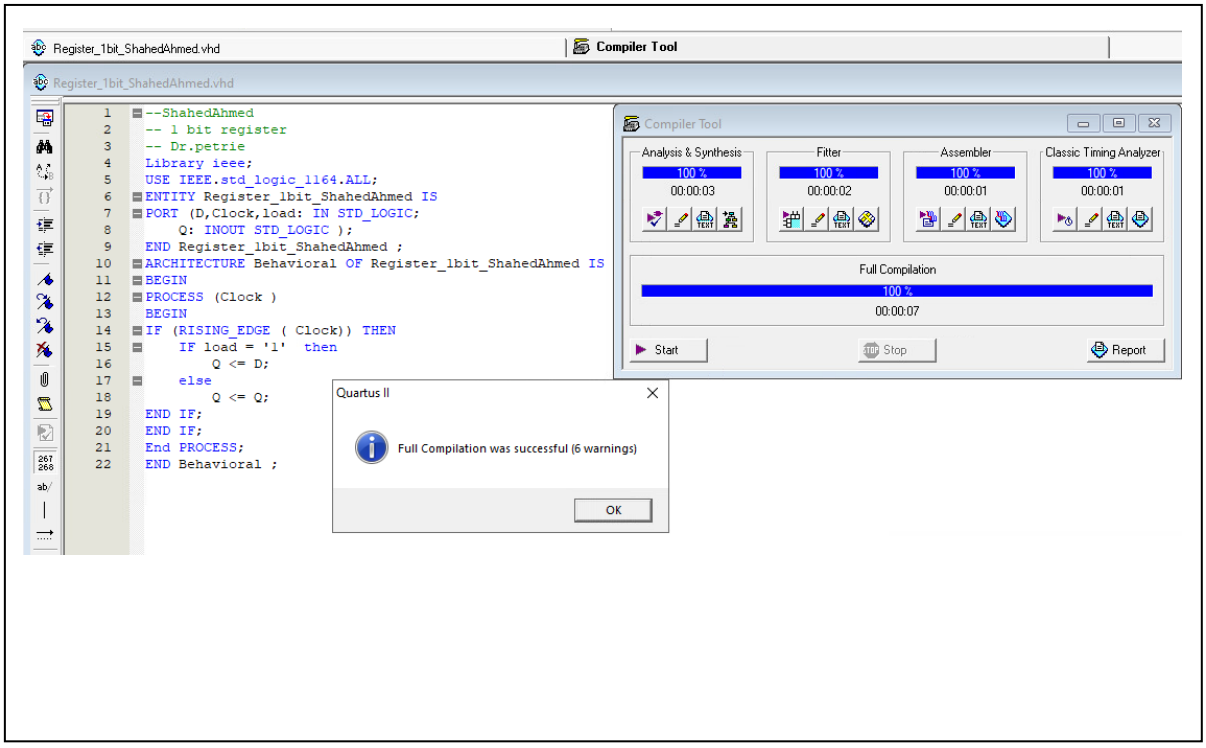

dff_shahedahmed.vhd
Compiler Tool
-- Shahed Ahmed
-- Data Flip Flop
-- Dr.petrie
-- Data Flip Flop positive-edge triggered
-- Behavioral VHDL model
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;
ENTITY DFF_ShahedAhmed IS
PORT (D, clock: IN STD_LOGIC;
Q :INOUT STD_LOGIC);
END DFF_ShahedAhmed;
ARCHITECTURE Behavior OF DFF_ShahedAhmed IS
BEGIN
-- Update on the rising edge of the clock
PROCESS (clock)
BEGIN
IF (RISING_EDGE(clock)) THEN
Q <= D;
END IF;
END PROCESS;
END Behavior;
Analysis & Synthesis
100 %
00:00:04
Fitter
100 %
00:00:01
Assembler
100 %
00:00:02
Classic Timing Analyzer
100 %
00:00:01
Full Compilation
100 %
00:00:08
Start
Stop
Report
Quartus II
Full Compilation was successful (7 warnings)
OK

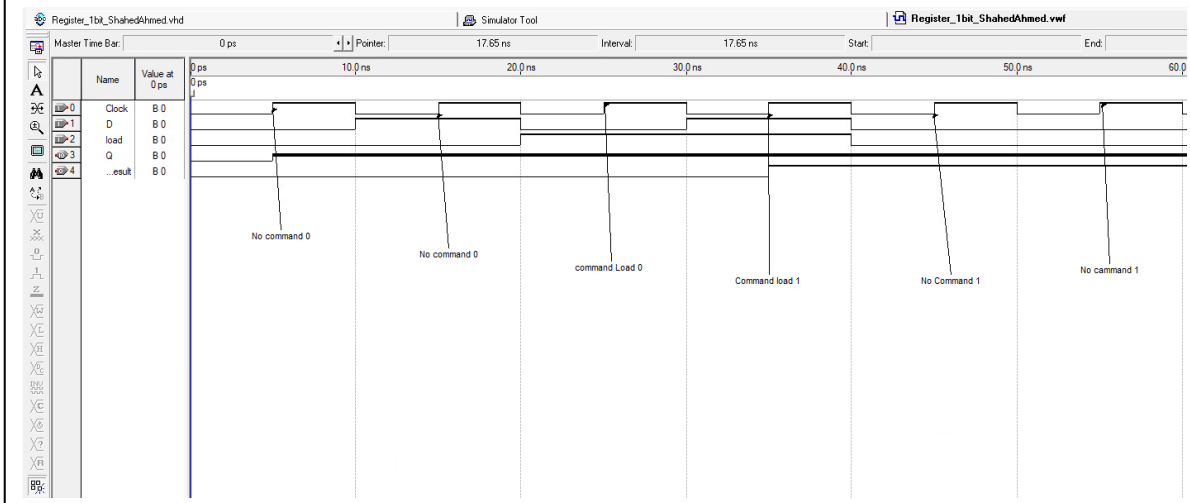

dff_shahedahmed.vhd
Simulator Tool
DFF_ShahedAhmed.vwf*
Master Time Bar:
50.0 ns
Pointer:
2.1 ns
Interval:
-47.9 ns
Start:
End:
Name
Value at 50.0 ns
clock
D
Q
B 0
B 1
B Z
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
reset
set
reset
reset
reset
set

2.2 – 1-Bit Register

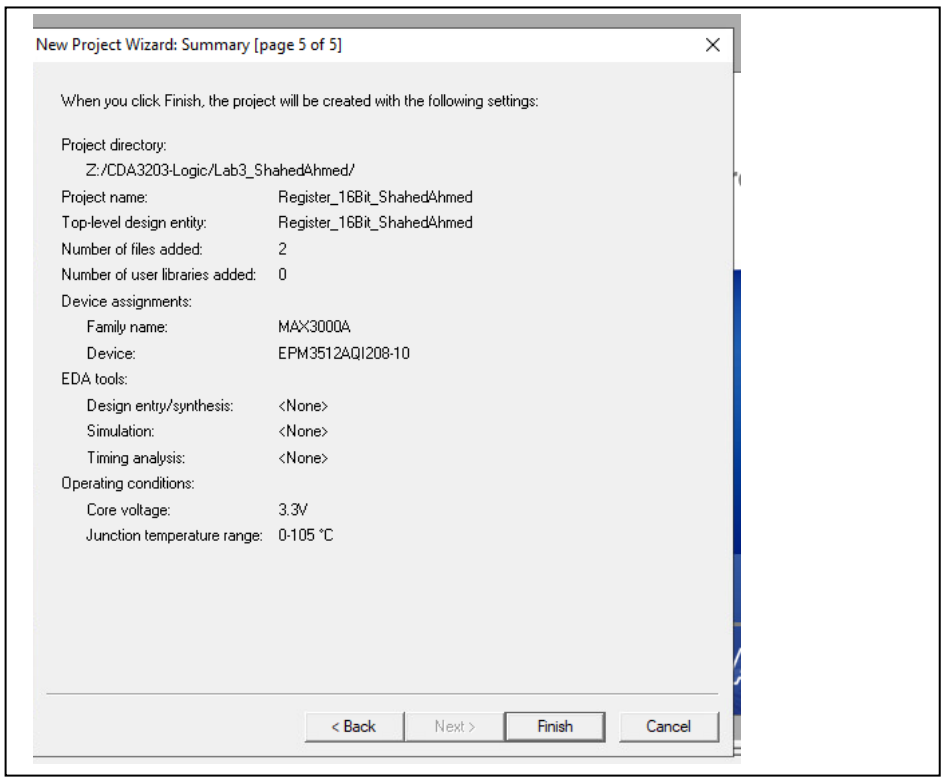





Register_1bit_ShahedAhmed.vhd
Compiler Tool
--ShahedAhmed
-- 1 bit register
-- Dr.petrie
Library ieee;
USE IEEE.std_logic_1164.ALL;
ENTITY Register_1bit_ShahedAhmed IS
PORT (D,Clock,load: IN STD_LOGIC;
Q: INOUT STD_LOGIC);
END Register_1bit_ShahedAhmed ;
ARCHITECTURE Behavioral OF Register_1bit_ShahedAhmed IS
BEGIN
PROCESS (Clock)
BEGIN
IF (RISING_EDGE (Clock)) THEN
IF load = '1' then
Q <= D;
else
Q <= Q;
END IF;
END IF;
End PROCESS;
END Behavioral ;
Compiler Tool
Analysis & Synthesis
100 %
00:00:03
Fitter
100 %
00:00:02
Assembler
100 %
00:00:01
Classic Timing Analyzer
100 %
00:00:01
Full Compilation
100 %
00:00:07
Start
Stop
Report
Quartus II
Full Compilation was successful (6 warnings)
OK

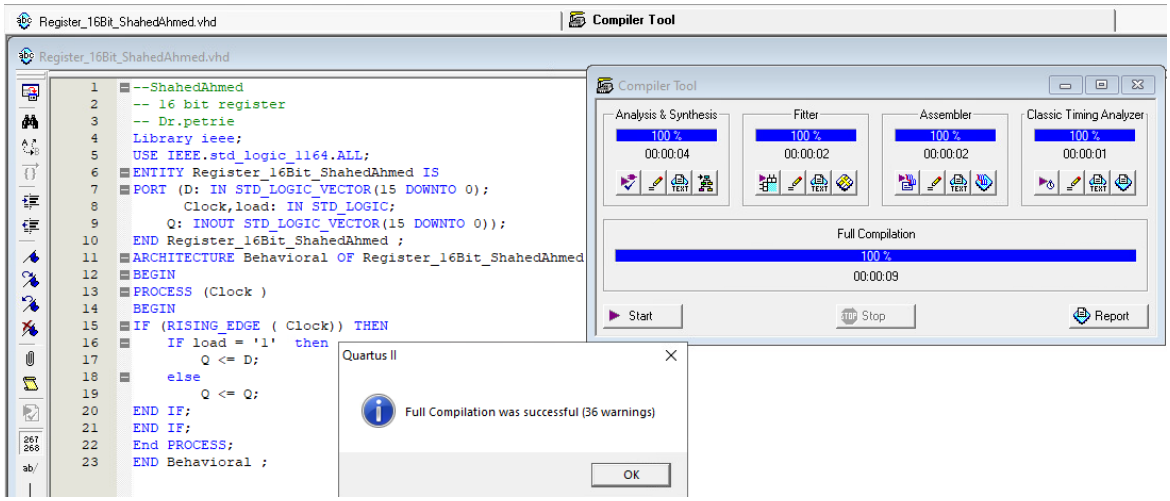

Register_1bit_ShahedAhmed.vhd
Simulator Tool
Register_1bit_ShahedAhmed.vwf
Master Time Bar:
0 ps
Pointer:
17.65 ns
Interval:
17.65 ns
Start:
End:
Name
Value at 0 ps
Clock
D
load
Q
B 0
0 ps
10.0 ns
20.0 ns
30.0 ns
40.0 ns
50.0 ns
60.0
No command 0
No command 0
command Load 0
Command load 1
No Command 1
No command 1

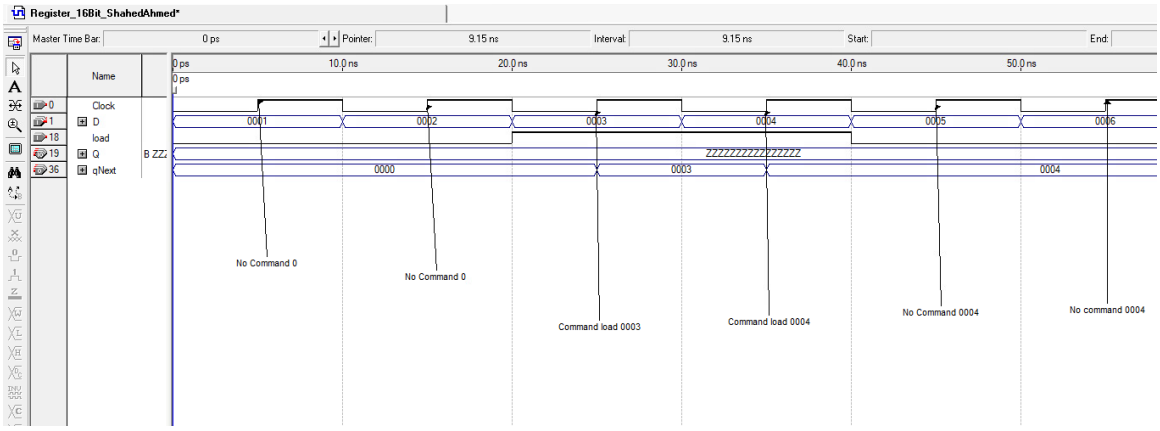
2.3 – 16-Bit Register



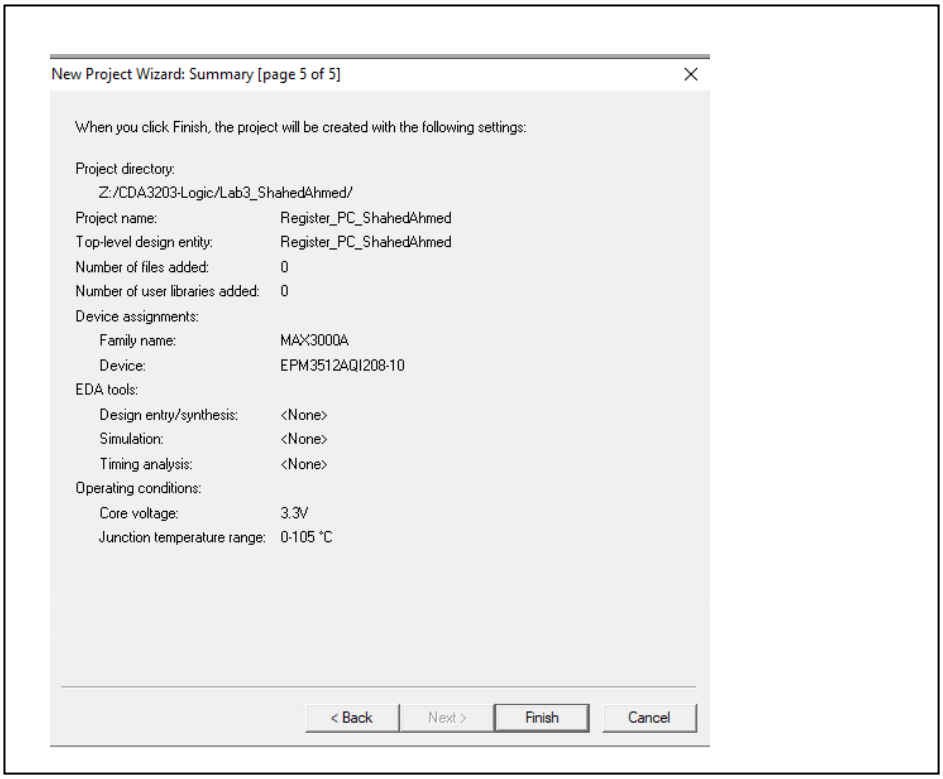
Register_16Bit_ShahedAhmed.vhd*

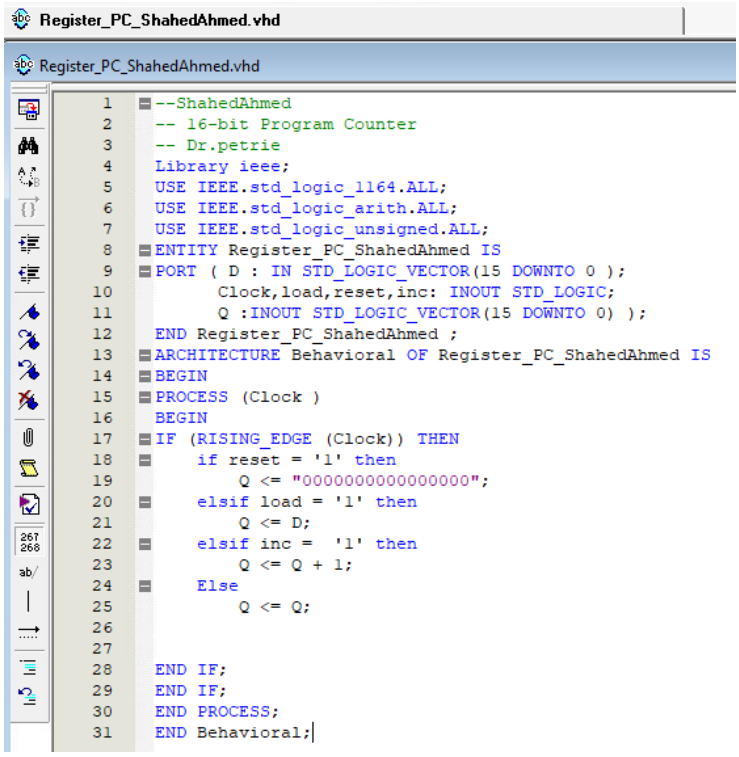
```
1  --ShahedAhmed
2  -- 16 bit register
3  -- Dr.petrie
4  Library ieee;
5  USE IEEE.std_logic_1164.ALL;
6  ENTITY Register_16Bit_ShahedAhmed IS
7  PORT (D: IN STD_LOGIC_VECTOR(15 DOWNTO 0);
8        Clock,load: IN STD_LOGIC;
9      Q: INOUT STD_LOGIC_VECTOR(15 DOWNTO 0));
10 END Register_16Bit_ShahedAhmed ;
11 ARCHITECTURE Behavioral OF Register_16Bit_ShahedAhmed IS
12 BEGIN
13 PROCESS (Clock )
14 BEGIN
15 IF (RISING_EDGE ( Clock)) THEN
16     IF load = '1'  then
17         Q <= D;
18     else
19         Q <= Q;
20 END IF;
21 END IF;
22 End PROCESS;
23 END Behavioral ;
```

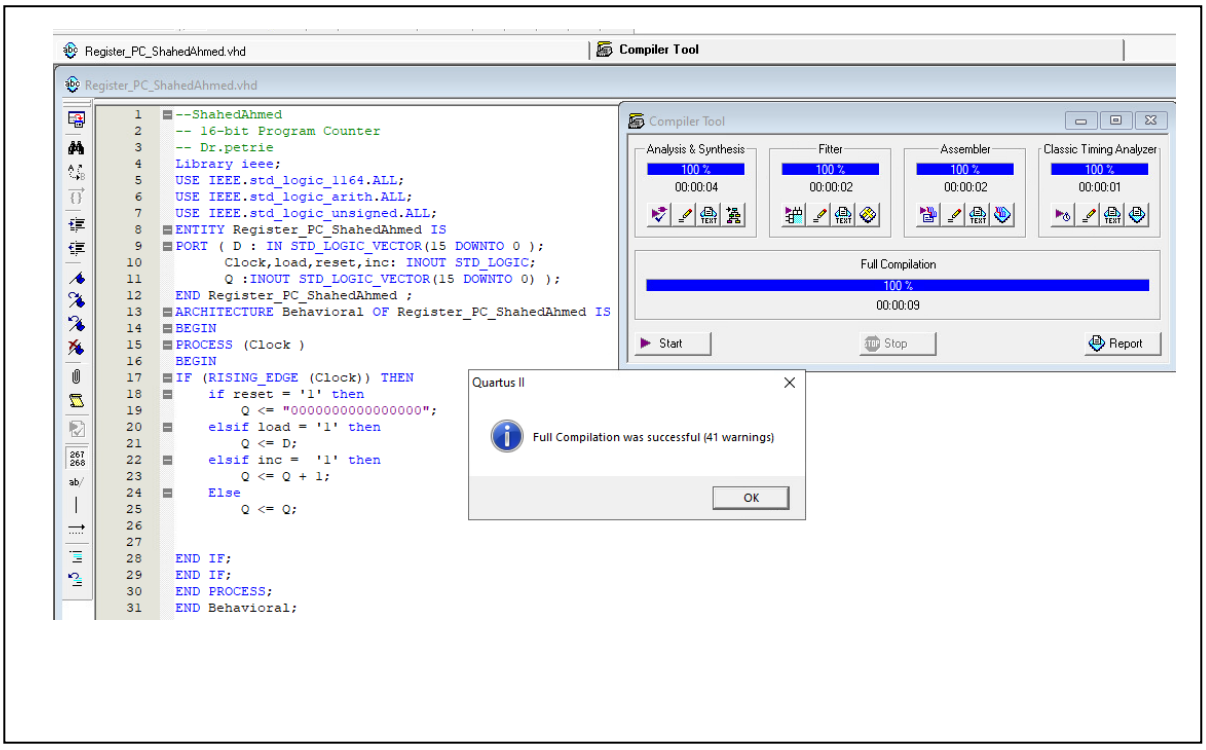

Register_16Bit_ShahedAhmed.vhd
Compiler Tool
--ShahedAhmed
-- 16 bit register
-- Dr.petrie
Library ieee;
USE IEEE.std_logic_1164.ALL;
ENTITY Register_16Bit_ShahedAhmed IS
PORT (D: IN STD_LOGIC_VECTOR(15 DOWNTO 0);
Clock,load: IN STD_LOGIC;
Q: INOUT STD_LOGIC_VECTOR(15 DOWNTO 0));
END Register_16Bit_ShahedAhmed ;
ARCHITECTURE Behavioral OF Register_16Bit_ShahedAhmed
BEGIN
PROCESS (Clock)
BEGIN
IF (RISING_EDGE (Clock)) THEN
IF load = '1' then
Q <= D;
else
Q <= Q;
END IF;
END IF;
End PROCESS;
END Behavioral ;
Analysis & Synthesis
100 %
00:00:04
Fitter
100 %
00:00:02
Assembler
100 %
00:00:02
Classic Timing Analyzer
100 %
00:00:01
Full Compilation
100 %
00:00:09
Start
Stop
Report
Quartus II
Full Compilation was successful (36 warnings)
OK

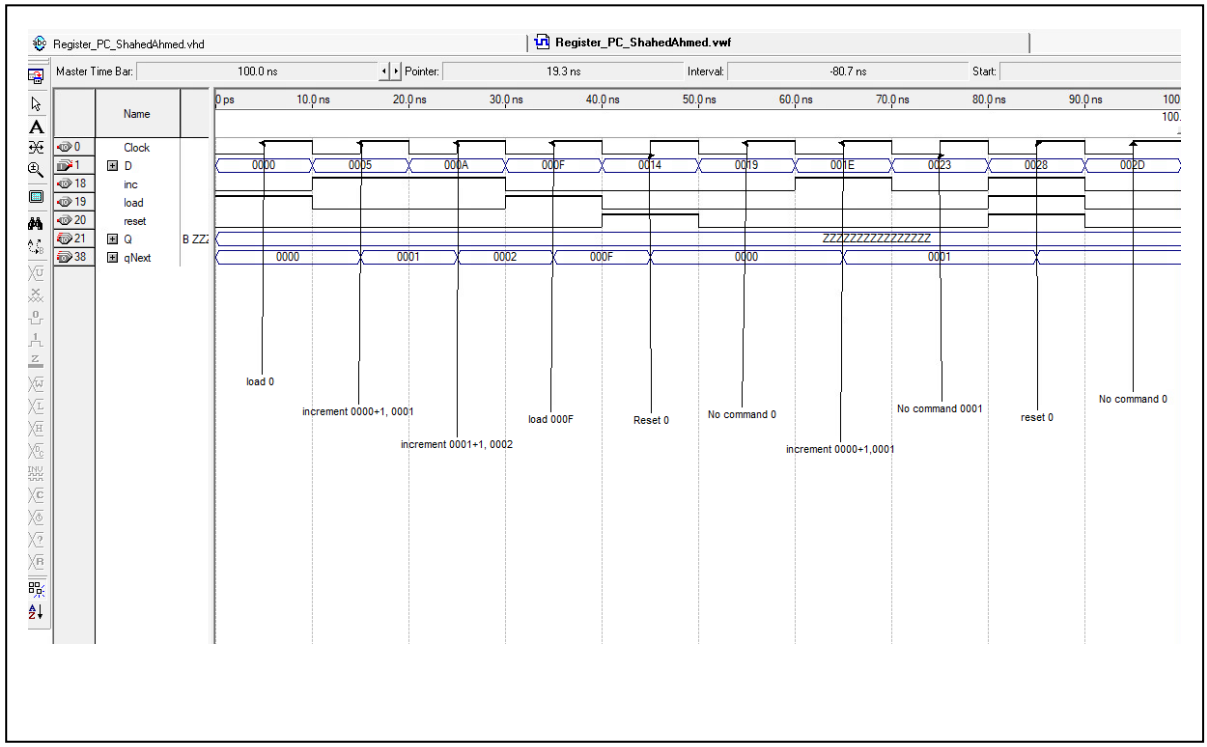

Register_16Bit_ShahedAhmed*
Master Time Bar:
0 ps
Pointer:
9.15 ns
Interval:
9.15 ns
Start:
End:
Name
Clock
D
load
Q
qNext
0001
0002
0003
0004
0005
0006
0000
0003
0004
ZZZZZZZZZZZZZZZ
No Command 0
No Command 0
Command load 0003
Command load 0004
No Command 0004
No command 0004

2.4 – Program Counter Register

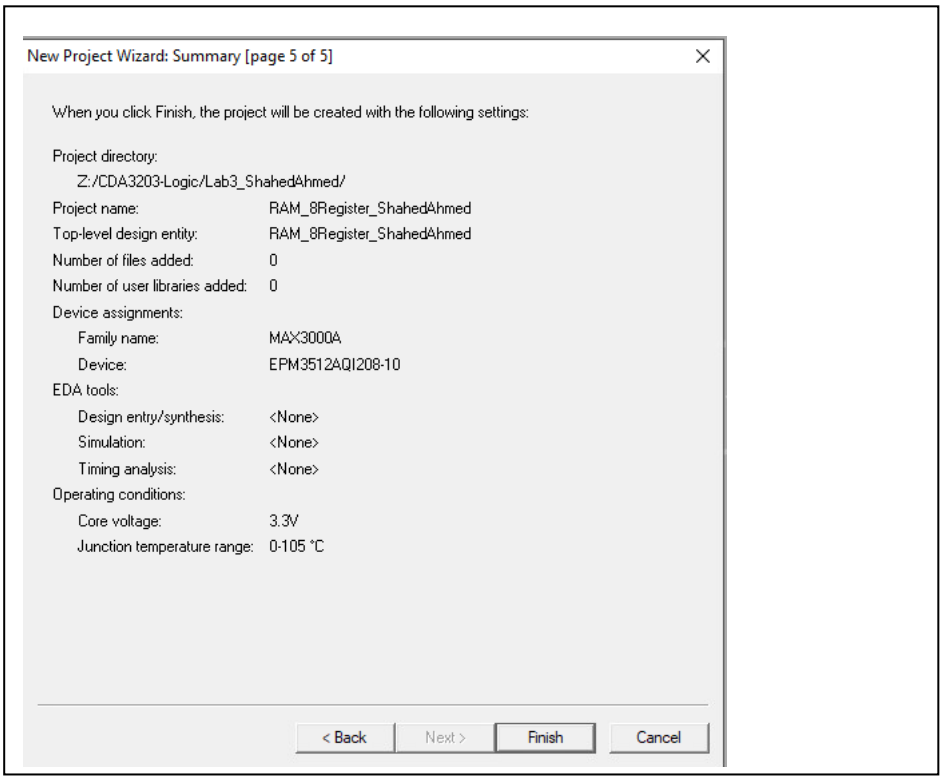





Register_PC_ShahedAhmed.vhd
Compiler Tool
--ShahedAhmed
-- 16-bit Program Counter
-- Dr.petrie
Library ieee;
USE IEEE.std_logic_1164.ALL;
USE IEEE.std_logic_arith.ALL;
USE IEEE.std_logic_unsigned.ALL;
ENTITY Register_PC_ShahedAhmed IS
PORT (D : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
Clock,load,reset,inc: INOUT STD_LOGIC;
Q :INOUT STD_LOGIC_VECTOR(15 DOWNTO 0));
END Register_PC_ShahedAhmed ;
ARCHITECTURE Behavioral OF Register_PC_ShahedAhmed IS
BEGIN
PROCESS (Clock)
BEGIN
IF (RISING_EDGE (Clock)) THEN
if reset = '1' then
Q <= "0000000000000000";
elsif load = '1' then
Q <= D;
elsif inc = '1' then
Q <= Q + 1;
Else
Q <= Q;
END IF;
END IF;
END PROCESS;
END Behavioral;
Analysis & Synthesis
100 %
00:00:04
Fitter
100 %
00:00:02
Assembler
100 %
00:00:02
Classic Timing Analyzer
100 %
00:00:01
Full Compilation
100 %
00:00:09
Start
Stop
Report
Quartus II
Full Compilation was successful (41 warnings)
OK

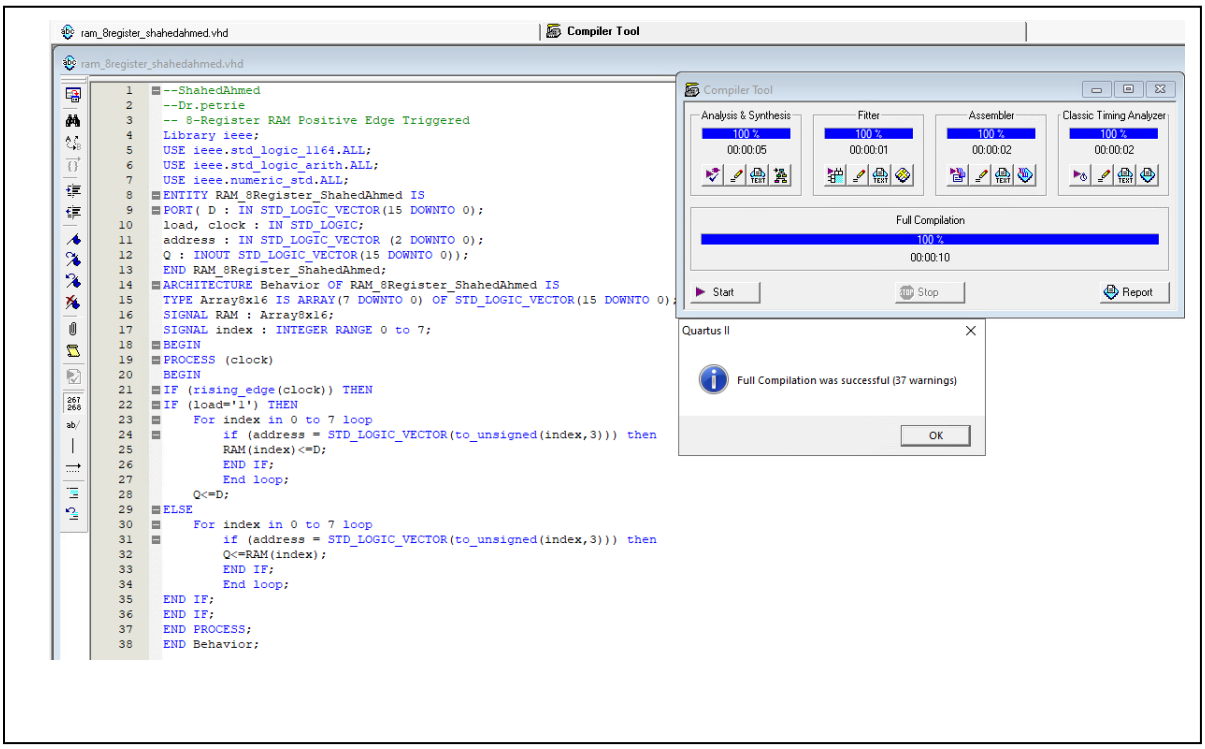

Register_PC_ShahedAhmed.vhd
Register_PC_ShahedAhmed.vwf
Master Time Bar:
100.0 ns
Pointer:
19.3 ns
Interval:
-80.7 ns
Start:
Name
Clock
D
inc
load
reset
Q
qNext
0000
0005
000A
000F
0014
0019
001E
0023
0028
002D
0000
0001
0002
000F
0000
0001
load 0
increment 0000+1, 0001
increment 0001+1, 0002
load 000F
Reset 0
No command 0
increment 0000+1,0001
No command 0001
reset 0
No command 0

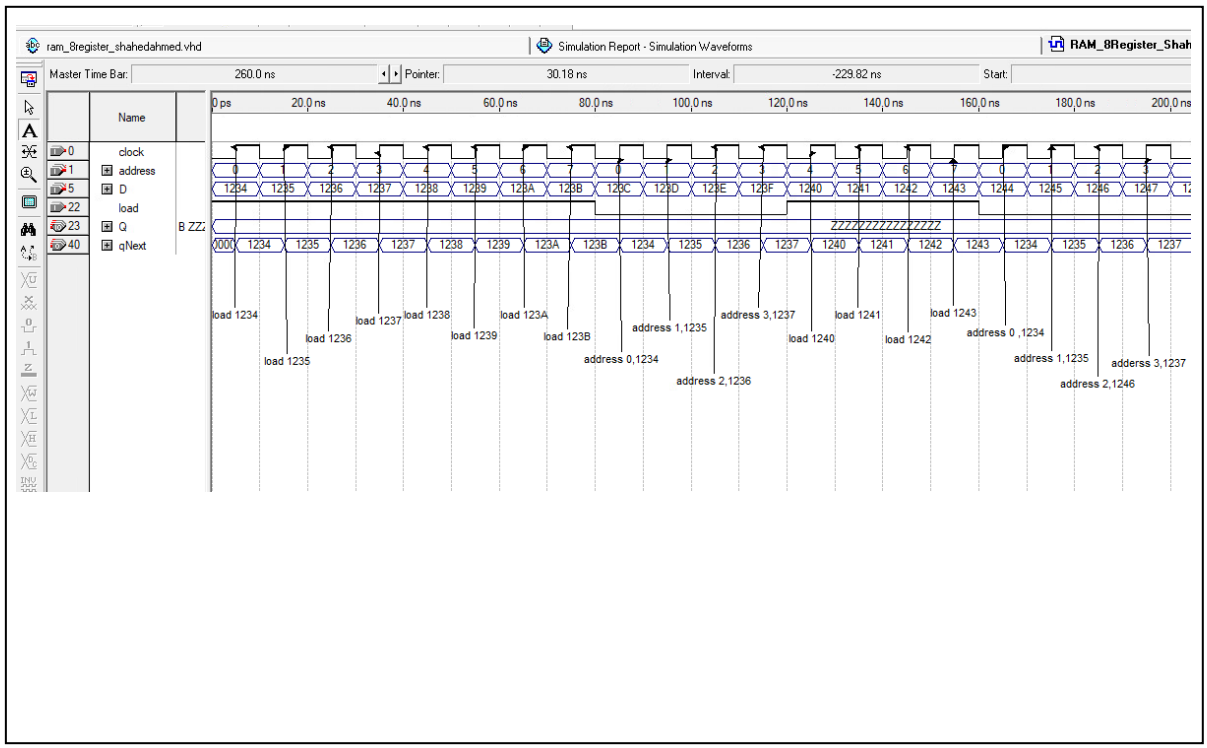
2.5 – 8 Register RAM



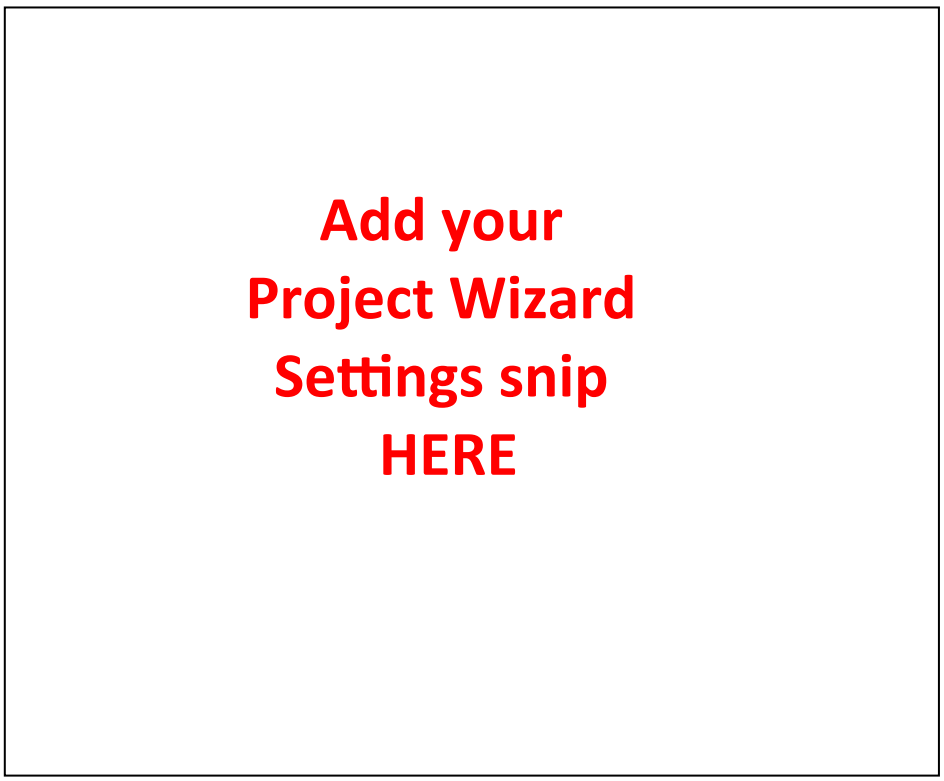
ram_8register_shahedahmed.vhd*

```
1  --ShahedAhmed
2  --Dr.petrie
3  -- 8-Register RAM Positive Edge Triggered
4  Library ieee;
5  USE ieee.std_logic_1164.ALL;
6  USE ieee.std_logic_arith.ALL;
7  USE ieee.numeric_std.ALL;
8  ENTITY RAM_8Register_ShahedAhmed IS
9  PORT( D : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
10 load, clock : IN STD_LOGIC;
11 address : IN STD_LOGIC_VECTOR (2 DOWNTO 0);
12 Q : INOUT STD_LOGIC_VECTOR(15 DOWNTO 0));
13 END RAM_8Register_ShahedAhmed;
14 ARCHITECTURE Behavior OF RAM_8Register_ShahedAhmed IS
15 TYPE Array8x16 IS ARRAY(7 DOWNTO 0) OF STD_LOGIC_VECTOR(15 DOWNTO 0);
16 SIGNAL RAM : Array8x16;
17 SIGNAL index : INTEGER RANGE 0 to 7;
18 BEGIN
19 PROCESS (clock)
20 BEGIN
21 IF (rising_edge(clock)) THEN
22 IF (load='1') THEN
23     For index in 0 to 7 loop
24         if (address = STD_LOGIC_VECTOR(to_unsigned(index,3))) then
25         RAM(index)<=D;
26         END IF;
27         End loop;
28     Q<=D;
29 ELSE
30     For index in 0 to 7 loop
31         if (address = STD_LOGIC_VECTOR(to_unsigned(index,3))) then
32         Q<=RAM(index);
33         END IF;
34         End loop;
35 END IF;
36 END IF;
37 END PROCESS;
38 END Behavior;
```


ram_8register_shahedahmed.vhd
Compiler Tool
--ShahedAhmed
--Dr.petrie
-- 8-Register RAM Positive Edge Triggered
Library ieee;
USE ieee.std_logic_1164.ALL;
USE ieee.std_logic_arith.ALL;
USE ieee.numeric_std.ALL;
ENTITY RAM_8Register_ShahedAhmed IS
PORT(D : IN STD_LOGIC_VECTOR(15 DOWNTO 0);
load, clock : IN STD_LOGIC;
address : IN STD_LOGIC_VECTOR (2 DOWNTO 0);
Q : INOUT STD_LOGIC_VECTOR(15 DOWNTO 0));
END RAM_8Register_ShahedAhmed;
ARCHITECTURE Behavior OF RAM_8Register_ShahedAhmed IS
TYPE Array8x16 IS ARRAY(7 DOWNTO 0) OF STD_LOGIC_VECTOR(15 DOWNTO 0);
SIGNAL RAM : Array8x16;
SIGNAL index : INTEGER RANGE 0 to 7;
BEGIN
PROCESS (clock)
BEGIN
IF (rising_edge(clock)) THEN
IF (load='1') THEN
For index in 0 to 7 loop
if (address = STD_LOGIC_VECTOR(to_unsigned(index,3))) then
RAM(index)<=D;
END IF;
End loop;
Q<=D;
ELSE
For index in 0 to 7 loop
if (address = STD_LOGIC_VECTOR(to_unsigned(index,3))) then
Q<=RAM(index);
END IF;
End loop;
END IF;
END IF;
END PROCESS;
END Behavior;
Compiler Tool
Analysis & Synthesis
100 %
00:00:05
Fitter
100 %
00:00:01
Assembler
100 %
00:00:02
Classic Timing Analyzer
100 %
00:00:02
Full Compilation
100 %
00:00:10
Start
Stop
Report
Quartus II
Full Compilation was successful (37 warnings)
OK


ram_8register_shahedahmed.vhd
Simulation Report - Simulation Waveforms
RAM_8Register_Shah
Master Time Bar:
260.0 ns
Pointer:
30.18 ns
Interval:
-229.82 ns
Start:
Name
clock
address
D
load
Q
qNext
load 1234
load 1235
load 1236
load 1237
load 1238
load 1239
load 123A
load 123B
address 0,1234
address 1,1235
address 2,1236
address 3,1237
load 1240
load 1241
load 1242
load 1243
address 0 ,1234
address 1,1235
address 2,1246
adderss 3,1237

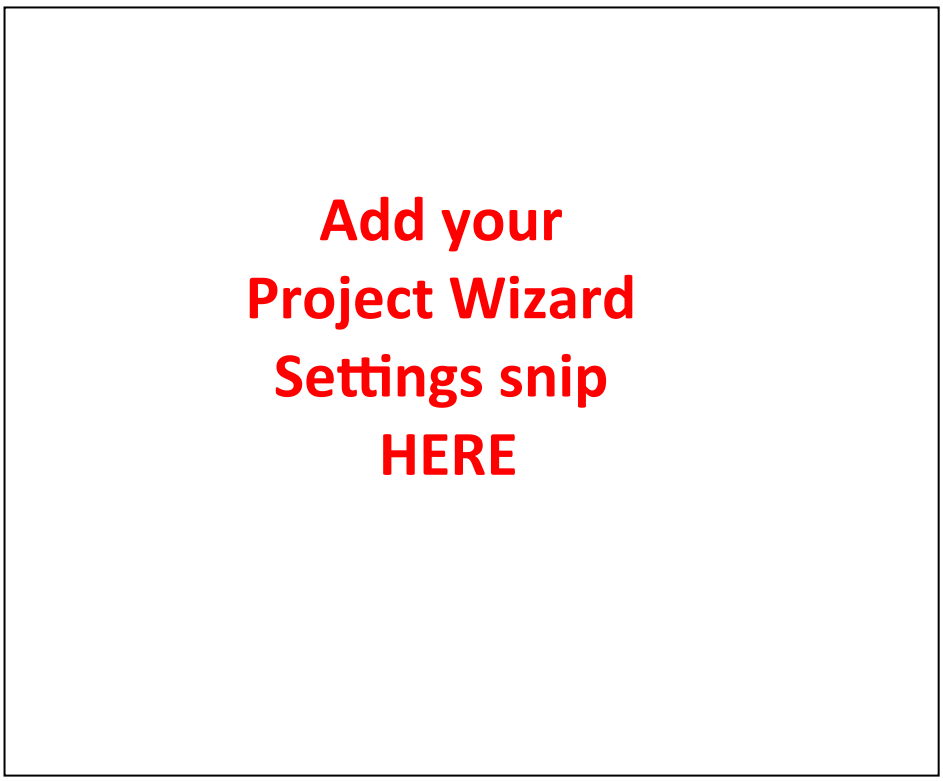
2.6 – Extra Credit – n Register RAM – RAM64



Add Successful Compilation Snip Here

Add Timing Diagram Here

2.7 – Extra Credit – Arithmetic Logic unit -ALU



Add Successful Compilation Snip Here

Add Timing Diagram Here