Lab 1

Shahed Ahmed

2/16/2023

CDA 3203 Computer Logic Design

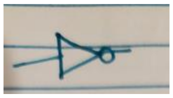
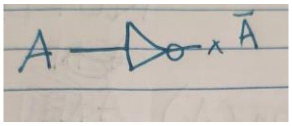
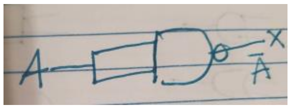
Spring 2023

Dr. Maria Petrie

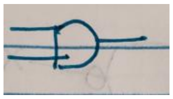
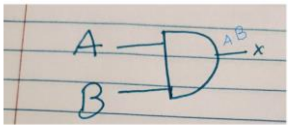
Florida Atlantic University

Part 1: Design 9 circuits by completing below: Draw the symbol for the gate, its Truth Table, its Simplest Sum of Products Expression, draw its NOT-AND-OR Equivalent Circuit, its all-NAND Equivalent Circuit.

1.1 NOT gate.

<table>
<tr><th>Draw NOT gate</th><th>Truth Table and Canonical Sum of Products Equation</th><th>NOT-AND-OR Equivalent Circuit</th><th>all-NAND Equivalent Circuit</th></tr>
<tr>
<td></td>
<td>
<table>
<tr><th>A</th><th>NOT(A)</th></tr>
<tr><td><b>1</b></td><td>1</td></tr>
<tr><td><b>0</b></td><td>0</td></tr>
</table>
Y1=A’
</td>
<td>
</td>
<td>
</td>
</tr>
</table>

1.2- AND gate

<table>
<tr><th>Draw AND gate</th><th>Truth Table and Canonical Sum of Products Equation</th><th>NOT-AND-OR Equivalent Circuit</th><th>all-NAND Equivalent Circuit</th></tr>
<tr>
<td></td>
<td>
<table>
<tr><th>A</th><th>B</th><th>AND(A,B)</th></tr>
<tr><td><b>0</b></td><td>0</td><td>0</td></tr>
<tr><td><b>0</b></td><td>1</td><td>0</td></tr>
<tr><td><b>1</b></td><td>0</td><td>0</td></tr>
<tr><td><b>1</b></td><td>1</td><td>1</td></tr>
</table>
Y2= AB
</td>
<td>
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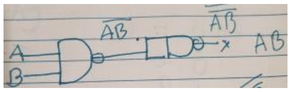
<td>
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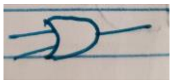
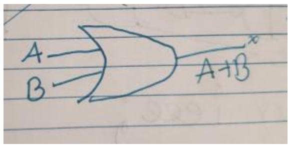
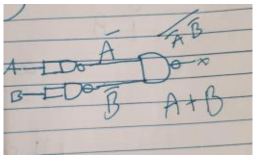
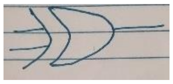
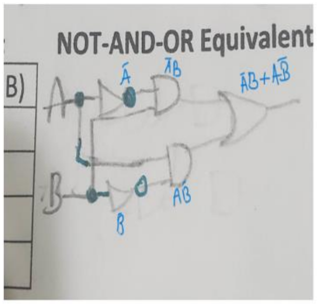
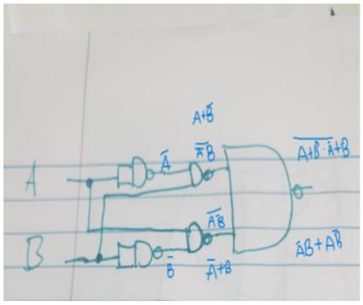
</tr>
</table>

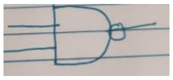
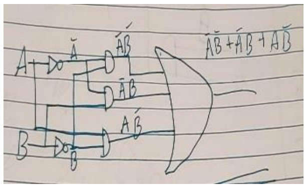
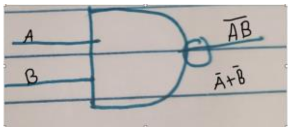
1.3- OR gate

<table>
<tr><th>Draw OR gate</th><th>Truth Table and Canonical Sum of Products Equation</th><th>NOT-AND-OR Equivalent Circuit</th><th>all-NAND Equivalent Circuit</th></tr>
<tr>
<td></td>
<td>
<table>
<tr><th>A</th><th>B</th><th>OR(A,B)</th></tr>
<tr><td><b>0</b></td><td>0</td><td>0</td></tr>
<tr><td><b>0</b></td><td>1</td><td>1</td></tr>
<tr><td><b>1</b></td><td>0</td><td>1</td></tr>
<tr><td><b>1</b></td><td>1</td><td>1</td></tr>
</table>
Y3=A+B
</td>
<td>
</td>
<td>
</td>
</tr>
</table>

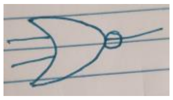
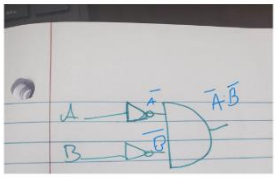
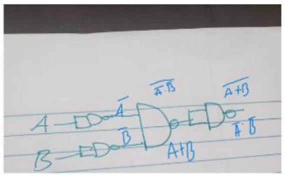
1.4- XOR gate

<table>
<tr><th>Draw XOR gate</th><th>Truth Table and Canonical Sum of Products Equation</th><th>NOT-AND-OR Equivalent Circuit</th><th>all-NAND Equivalent Circuit</th></tr>
<tr><td></td><td><table><tr><th>A</th><th>B</th><th>XOR(A,B)</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>Y4= A’B + AB’</td><td></td><td></td></tr>
</table>

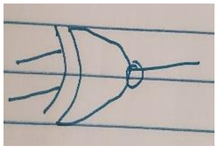
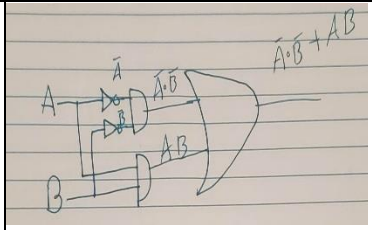
1.5- NAND gate

<table>
<tr><th>Draw NAND gate</th><th>Truth Table and Canonical Sum of Products Equation</th><th>NOT-AND-OR Equivalent Circuit</th><th>all-NAND Equivalent Circuit</th></tr>
<tr><td></td><td><table><tr><th>A</th><th>B</th><th>NAND(A,B)</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>Y5=A’B’+A’B+AB’</td><td></td><td></td></tr>
</table>

1.6- NOR gate

<table>
<tr><th>Draw NOR gate</th><th>Truth Table and Canonical Sum of Products Equation</th><th>NOT-AND-OR Equivalent Circuit</th><th>all-NAND Equivalent Circuit</th></tr>
<tr><td></td><td><table><tr><th>A</th><th>B</th><th>NOR(A,B)</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table>Y6=A’B’</td><td></td><td></td></tr>
</table>

1.7- XNOR gate

<table>
<tr><th>Draw XNOR gate</th><th>Truth Table and Canonical Sum of Products Equation</th><th>NOT-AND-OR Equivalent Circuit</th><th>all-NAND Equivalent Circuit</th></tr>
<tr>
<td></td>
<td>
<table>
<tr><th>A</th><th>B</th><th>XNOR(A,B)</th></tr>
<tr><td><b>0</b></td><td>0</td><td>1</td></tr>
<tr><td><b>0</b></td><td>1</td><td>0</td></tr>
<tr><td><b>1</b></td><td>0</td><td>0</td></tr>
<tr><td><b>1</b></td><td>1</td><td>1</td></tr>
</table>
Y7=A’B’+AB
</td>
<td>
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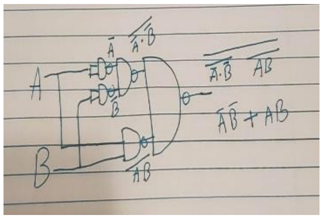
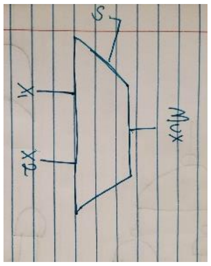
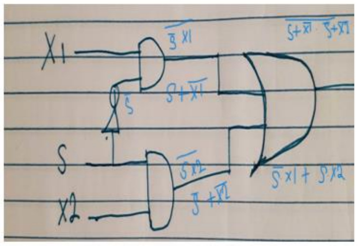
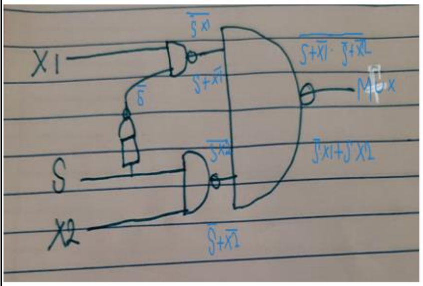
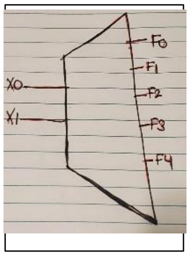
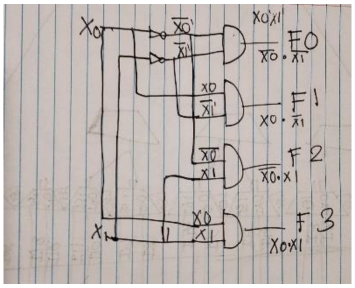
<td>
A
B
$\bar{A}$
$\bar{B}$
$\overline{\bar{A}\cdot\bar{B}}$
$\overline{AB}$
$\overline{\overline{\bar{A}\cdot\bar{B}}\ \overline{AB}}$
$\bar{A}\bar{B}+AB$

</td>
</tr>
</table>

1.8- 2 to 1 Encoder or Multiplexer (Mux)

<table>
<tr><th>Draw 2to1 Mux</th><th>Truth Table and Canonical Sum of Products Equation</th><th>NOT-AND-OR Equivalent Circuit</th><th>all-NAND Equivalent Circuit</th></tr>
<tr>
<td>
</td>
<td>
<table>
<tr><th>s</th><th>X_1</th><th>X_2</th><th>Mux</th></tr>
<tr><td><b>0</b></td><td>0</td><td>0</td><td>0</td></tr>
<tr><td><b>0</b></td><td>0</td><td>1</td><td>0</td></tr>
<tr><td><b>0</b></td><td>1</td><td>0</td><td>1</td></tr>
<tr><td><b>0</b></td><td>1</td><td>1</td><td>1</td></tr>
<tr><td><b>1</b></td><td>0</td><td>0</td><td>0</td></tr>
<tr><td><b>1</b></td><td>0</td><td>1</td><td>1</td></tr>
<tr><td><b>1</b></td><td>1</td><td>0</td><td>0</td></tr>
<tr><td><b>1</b></td><td>1</td><td>1</td><td>1</td></tr>
</table>
Y8= S’X1+SX2
</td>
<td>
</td>
<td>
</td>
</tr>
</table>

1.9- 2 to 4 decoder or Demultiplexer (DMux)

<table>
<tr><th>Draw 2to4 DMux</th><th>Truth Table and Canonical Sum of Products Equation</th><th>NOT-AND-OR Equivalent Circuit</th><th>all-NAND Equivalent Circuit</th></tr>
<tr>
<td>
</td>
<td>
<table>
<tr><th>X_1</th><th>X_0</th><th>F_3</th><th>F_2</th><th>F_1</th><th>F_0</th></tr>
<tr><td><b>0</b></td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td><b>0</b></td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td><b>1</b></td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td><b>1</b></td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
</table>
Y9:
F3=x0x1
F2=x0’x1
F1=x0x1’
F0=x0’x1’
</td>
<td>
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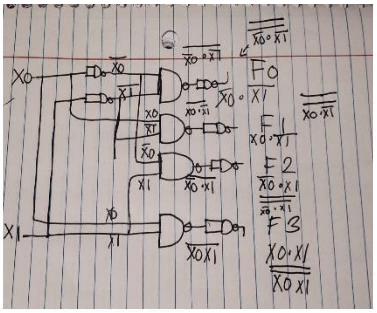
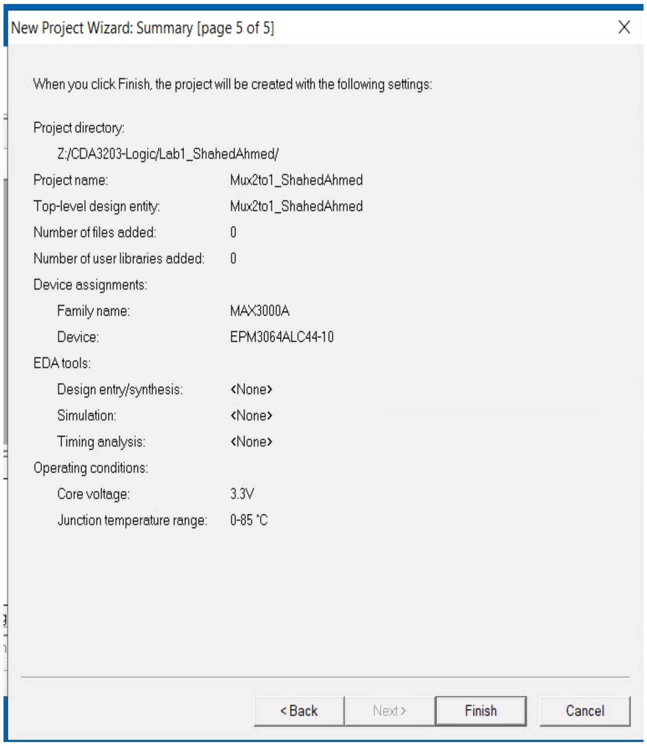
<td>
</td>
</tr>
</table>

Part 2. Create a new project in Altera Quartus using VHDL instead of a schematic simulate the Mux2to1 using all-NAND gates.

Project Wizard

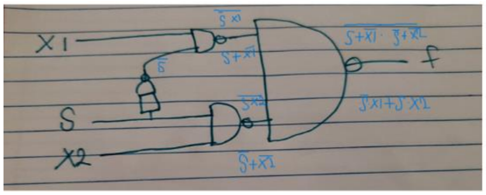


New Project Wizard: Summary [page 5 of 5]

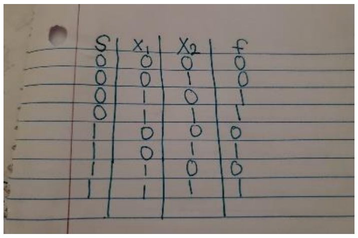
When you click Finish, the project will be created with the following settings:

```
Project directory:
    Z:/CDA3203-Logic/Lab1_ShahedAhmed/
Project name:                     Mux2to1_ShahedAhmed
Top-level design entity:          Mux2to1_ShahedAhmed
Number of files added:            0
Number of user libraries added:   0
Device assignments:
    Family name:                  MAX3000A
    Device:                       EPM3064ALC44-10
EDA tools:
    Design entry/synthesis:       <None>
    Simulation:                   <None>
    Timing analysis:              <None>
Operating conditions:
    Core voltage:                 3.3V
    Junction temperature range:   0-85 °C
```

Mux2to1 Diagram

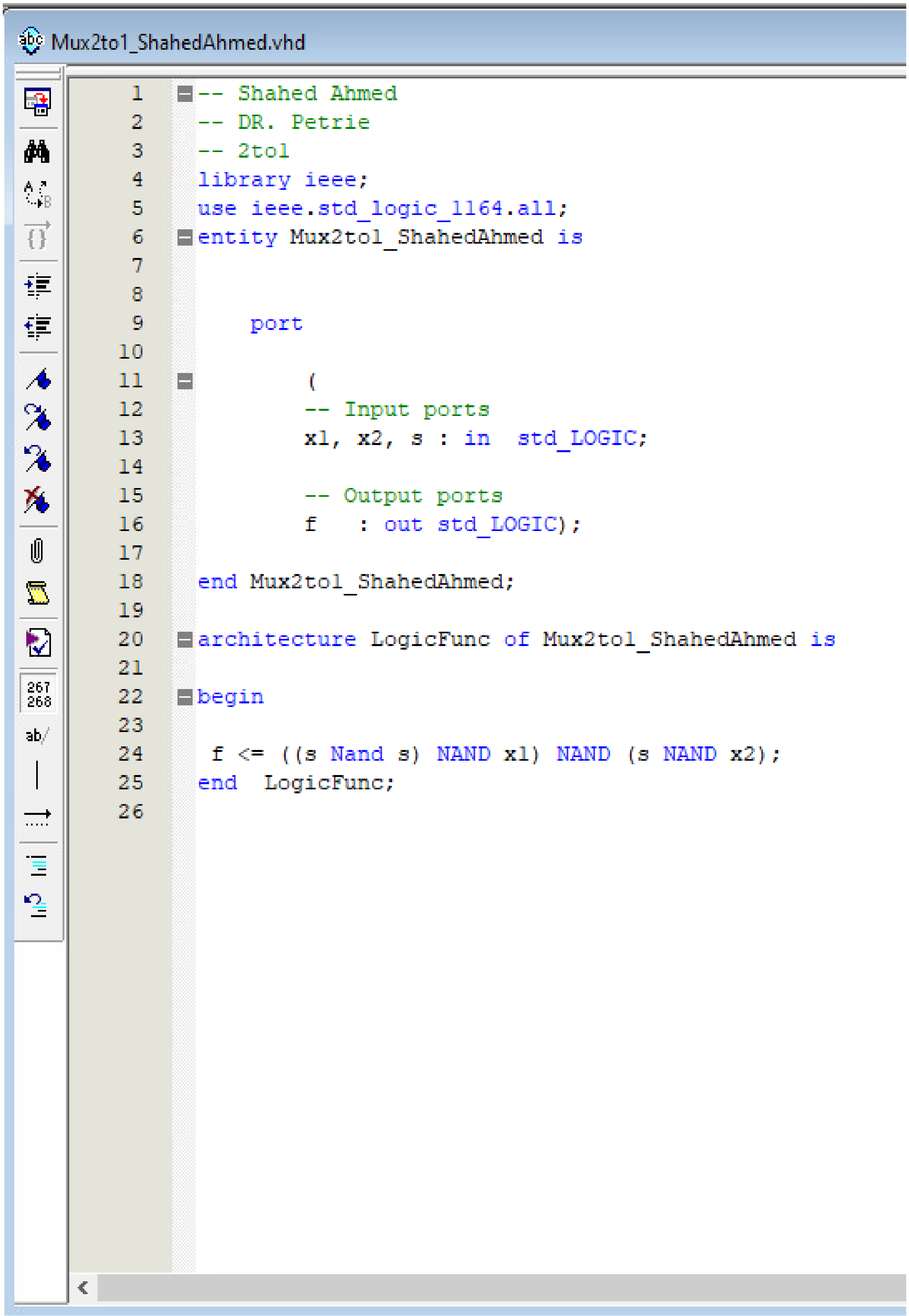


Truth Table



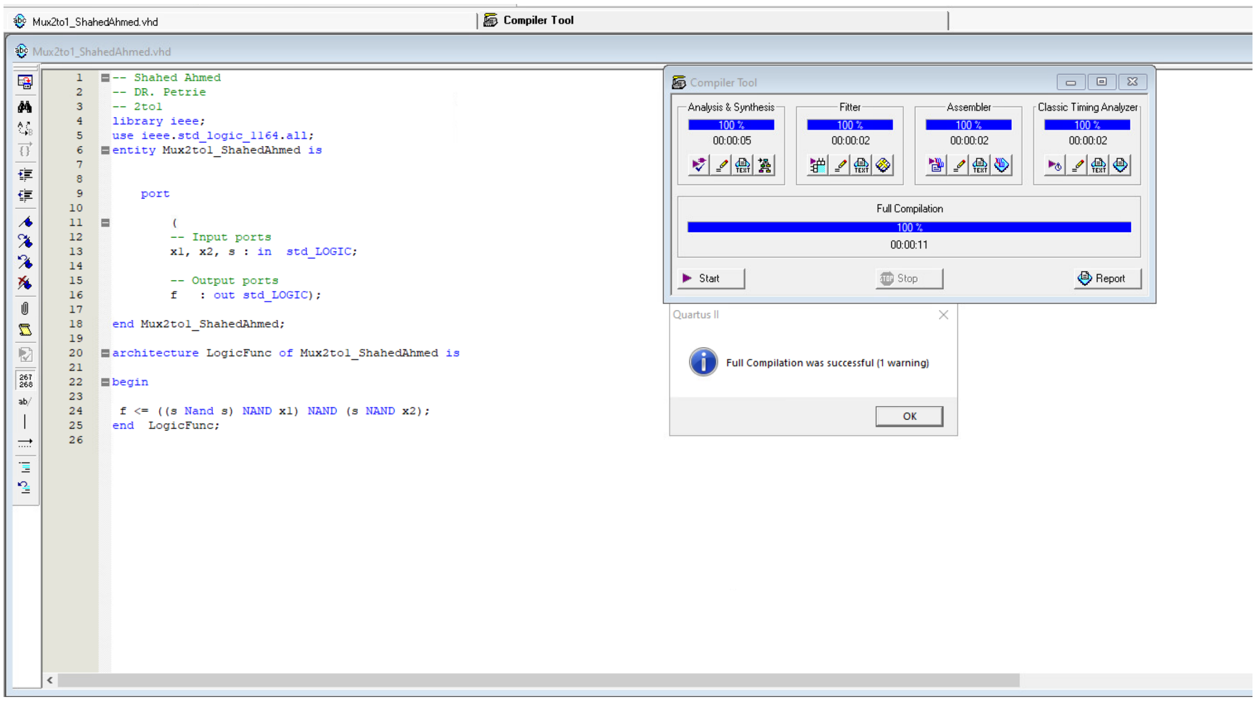
S	X_1	X_2	f
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

VHDL code



```vhdl
-- Shahed Ahmed
-- DR. Petrie
-- 2to1
library ieee;
use ieee.std_logic_1164.all;
entity Mux2to1_ShahedAhmed is


    port

        (
        -- Input ports
        x1, x2, s : in  std_LOGIC;

        -- Output ports
        f   : out std_LOGIC);

end Mux2to1_ShahedAhmed;

architecture LogicFunc of Mux2to1_ShahedAhmed is

begin

 f <= ((s Nand s) NAND x1) NAND (s NAND x2);
end  LogicFunc;

```

Successful Compilation



Mux2to1_ShahedAhmed.vhd

```
-- Shahed Ahmed
-- DR. Petrie
-- 2tol
library ieee;
use ieee.std_logic_1164.all;
entity Mux2tol_ShahedAhmed is


    port

        (
        -- Input ports
        x1, x2, s : in  std_LOGIC;

        -- Output ports
        f    : out std_LOGIC);

end Mux2tol_ShahedAhmed;

architecture LogicFunc of Mux2tol_ShahedAhmed is

begin

 f <= ((s Nand s) NAND x1) NAND (s NAND x2);
end  LogicFunc;
```

Compiler Tool

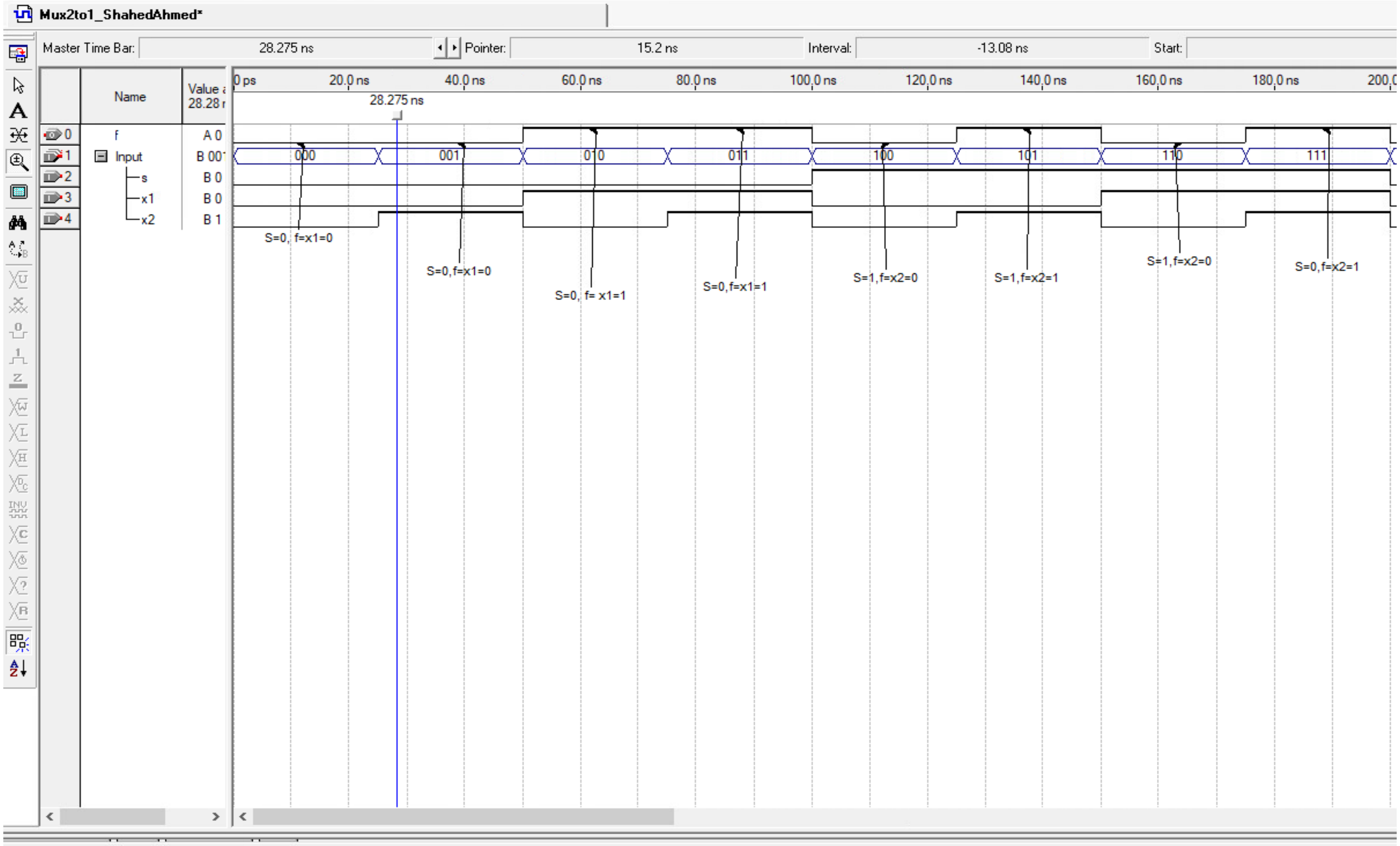
Analysis & Synthesis	Fitter	Assembler	Classic Timing Analyzer
100 %	100 %	100 %	100 %
00:00:05	00:00:02	00:00:02	00:00:02

Full Compilation 100 % 00:00:11

Quartus II

Full Compilation was successful (1 warning)

Timing Diagram



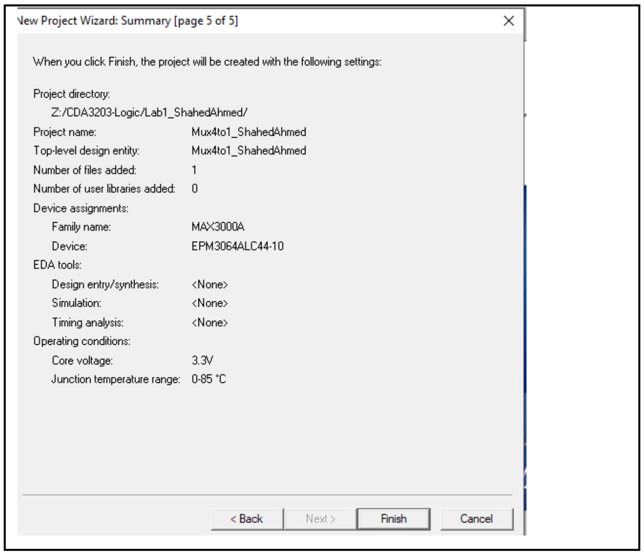
Mux2to1_ShahedAhmed*

Master Time Bar: 28.275 ns   Pointer: 15.2 ns   Interval: -13.08 ns   Start:

	Name	Value at 28.28 ns
0	f	A 0
1	Input	B 001
2	s	B 0
3	x1	B 0
4	x2	B 1

Part 3. Design and simulate a 4-to-1 Multiplexer (Mux) **using only Mux2to1 components**.

Project Wizard

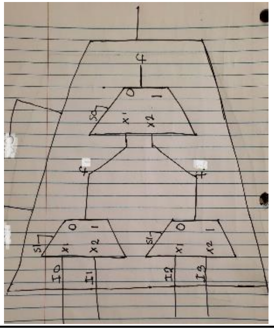


New Project Wizard: Summary [page 5 of 5]

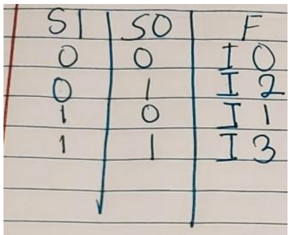
When you click Finish, the project will be created with the following settings:

Project directory:	
Z:/CDA3203-Logic/Lab1_ShahedAhmed/	
Project name:	Mux4to1_ShahedAhmed
Top-level design entity:	Mux4to1_ShahedAhmed
Number of files added:	1
Number of user libraries added:	0
Device assignments:	
Family name:	MAX3000A
Device:	EPM3064ALC44-10
EDA tools:	
Design entry/synthesis:	<None>
Simulation:	<None>
Timing analysis:	<None>
Operating conditions:	
Core voltage:	3.3V
Junction temperature range:	0-85 °C

Mux4to1 Diagram

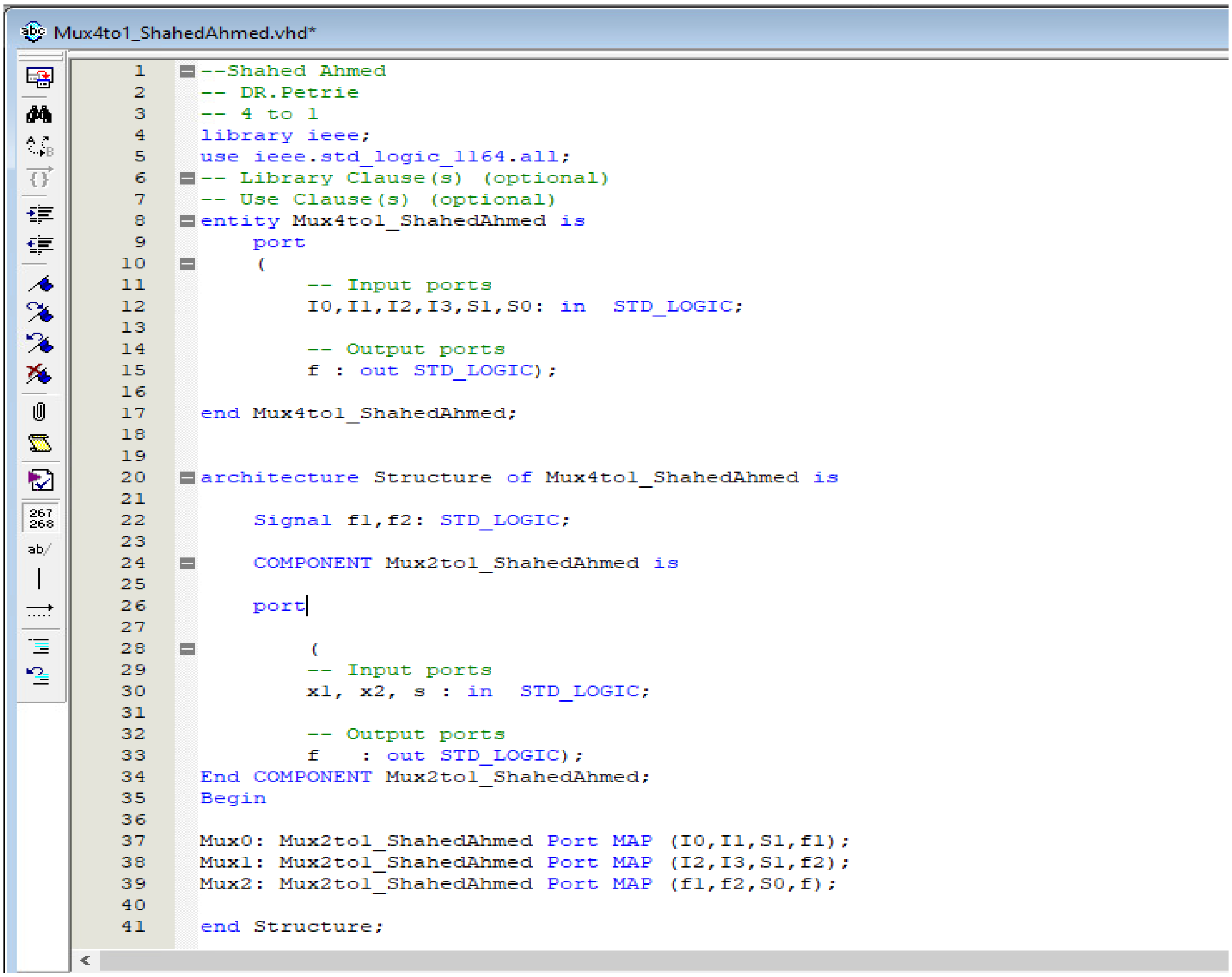


Truth Table



S1	S0	F
0	0	I0
0	1	I2
1	0	I1
1	1	I3

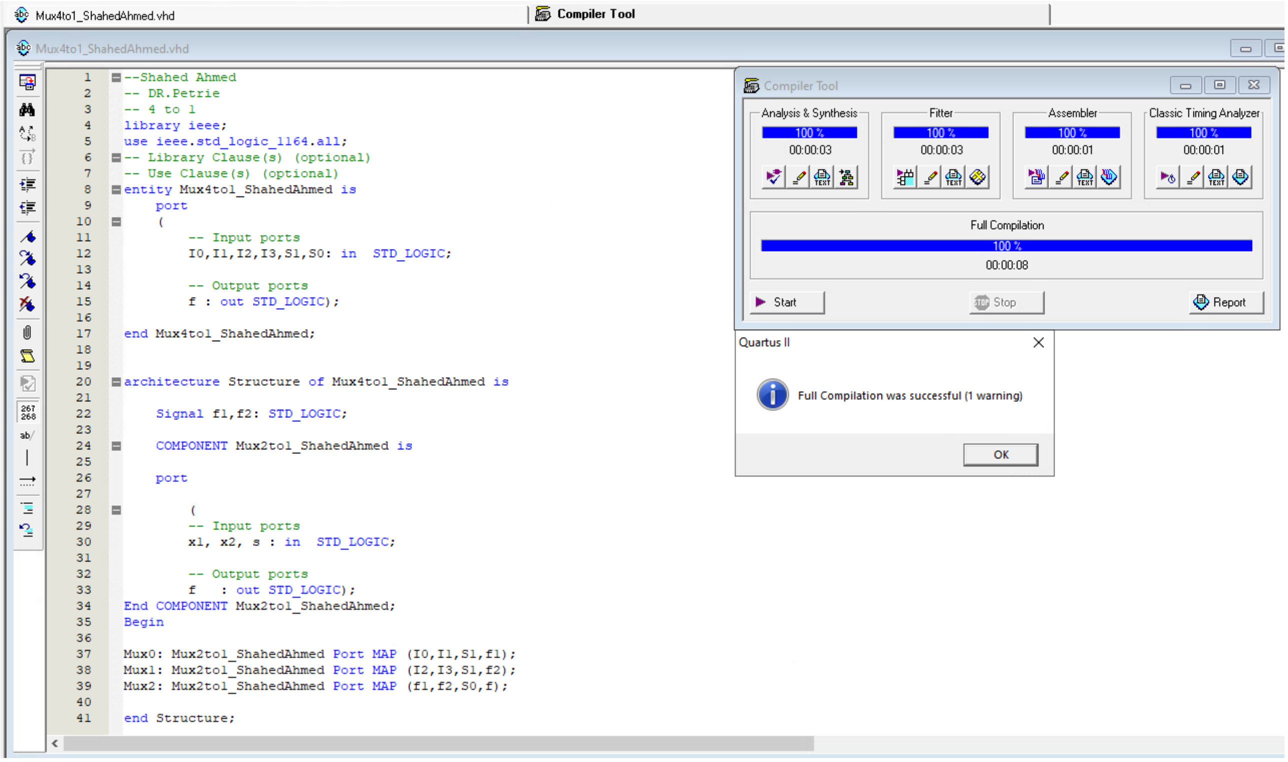
VHDL code



Mux4to1_ShahedAhmed.vhd*

```vhdl
--Shahed Ahmed
-- DR.Petrie
-- 4 to 1
library ieee;
use ieee.std_logic_1164.all;
-- Library Clause(s) (optional)
-- Use Clause(s) (optional)
entity Mux4to1_ShahedAhmed is
    port
    (
        -- Input ports
        I0,I1,I2,I3,S1,S0: in  STD_LOGIC;

        -- Output ports
        f : out STD_LOGIC);

end Mux4to1_ShahedAhmed;


architecture Structure of Mux4to1_ShahedAhmed is

    Signal f1,f2: STD_LOGIC;

    COMPONENT Mux2to1_ShahedAhmed is

    port

        (
        -- Input ports
        x1, x2, s : in  STD_LOGIC;

        -- Output ports
        f   : out STD_LOGIC);
End COMPONENT Mux2to1_ShahedAhmed;
Begin

Mux0: Mux2to1_ShahedAhmed Port MAP (I0,I1,S1,f1);
Mux1: Mux2to1_ShahedAhmed Port MAP (I2,I3,S1,f2);
Mux2: Mux2to1_ShahedAhmed Port MAP (f1,f2,S0,f);

end Structure;
```

Successful Compilation



```
--Shahed Ahmed
-- DR.Petrie
-- 4 to 1
library ieee;
use ieee.std_logic_1164.all;
-- Library Clause(s) (optional)
-- Use Clause(s) (optional)
entity Mux4tol_ShahedAhmed is
    port
    (
        -- Input ports
        I0,I1,I2,I3,S1,S0: in  STD_LOGIC;

        -- Output ports
        f : out STD_LOGIC);

end Mux4tol_ShahedAhmed;


architecture Structure of Mux4tol_ShahedAhmed is

    Signal f1,f2: STD_LOGIC;

    COMPONENT Mux2tol_ShahedAhmed is

    port

        (
        -- Input ports
        x1, x2, s : in  STD_LOGIC;

        -- Output ports
        f   : out STD_LOGIC);
End COMPONENT Mux2tol_ShahedAhmed;
Begin

Mux0: Mux2tol_ShahedAhmed Port MAP (I0,I1,S1,f1);
Mux1: Mux2tol_ShahedAhmed Port MAP (I2,I3,S1,f2);
Mux2: Mux2tol_ShahedAhmed Port MAP (f1,f2,S0,f);

end Structure;
```

Compiler Tool

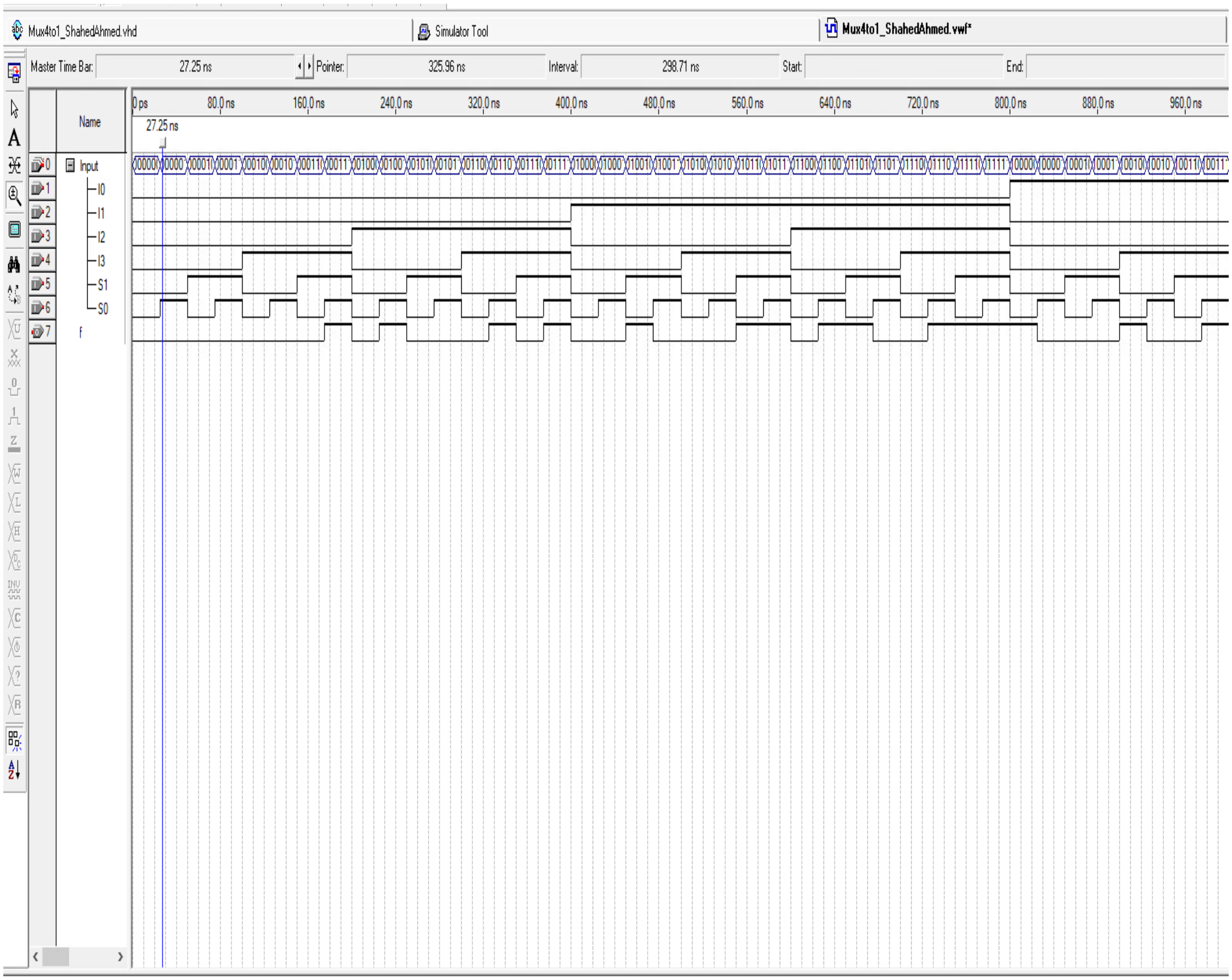
Analysis & Synthesis	Fitter	Assembler	Classic Timing Analyzer
100 %	100 %	100 %	100 %
00:00:03	00:00:03	00:00:01	00:00:01

Full Compilation
100 %
00:00:08

Quartus II

Full Compilation was successful (1 warning)

Timing Diagram



Master Time Bar: 27.25 ns

Pointer: 325.96 ns

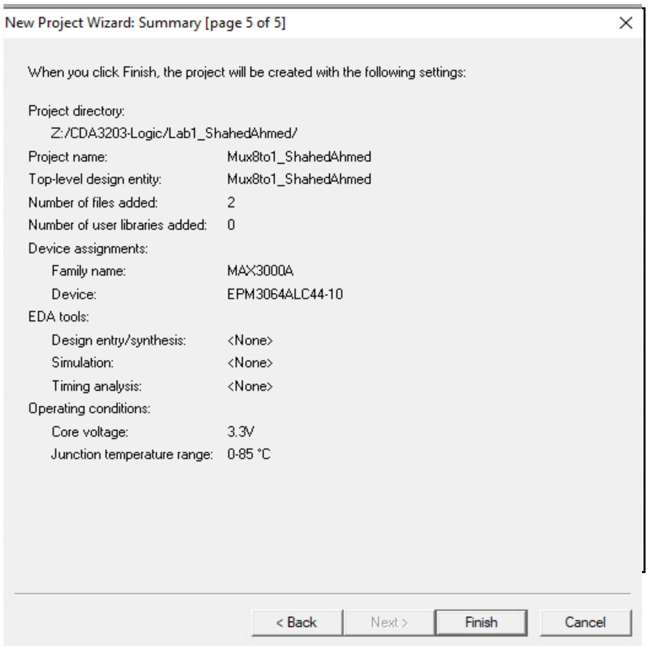
Interval: 298.71 ns

Start:

End:

Part 4. Design and simulate an 8-to-1 Multiplexer (Mux) **using only Mux4to1 and/or Mux2to1 components.**

Project Wizard



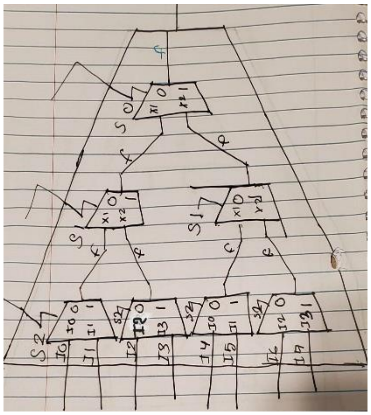
New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

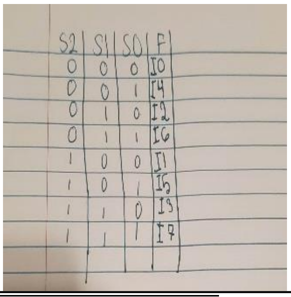
Project directory:
Z:/CDA3203-Logic/Lab1_ShahedAhmed/

Project name: Mux8to1_ShahedAhmed
Top-level design entity: Mux8to1_ShahedAhmed
Number of files added: 2
Number of user libraries added: 0
Device assignments:
Family name: MAX3000A
Device: EPM3064ALC44-10
EDA tools:
Design entry/synthesis: <None>
Simulation: <None>
Timing analysis: <None>
Operating conditions:
Core voltage: 3.3V
Junction temperature range: 0-85 °C

Mux8to1 Diagram

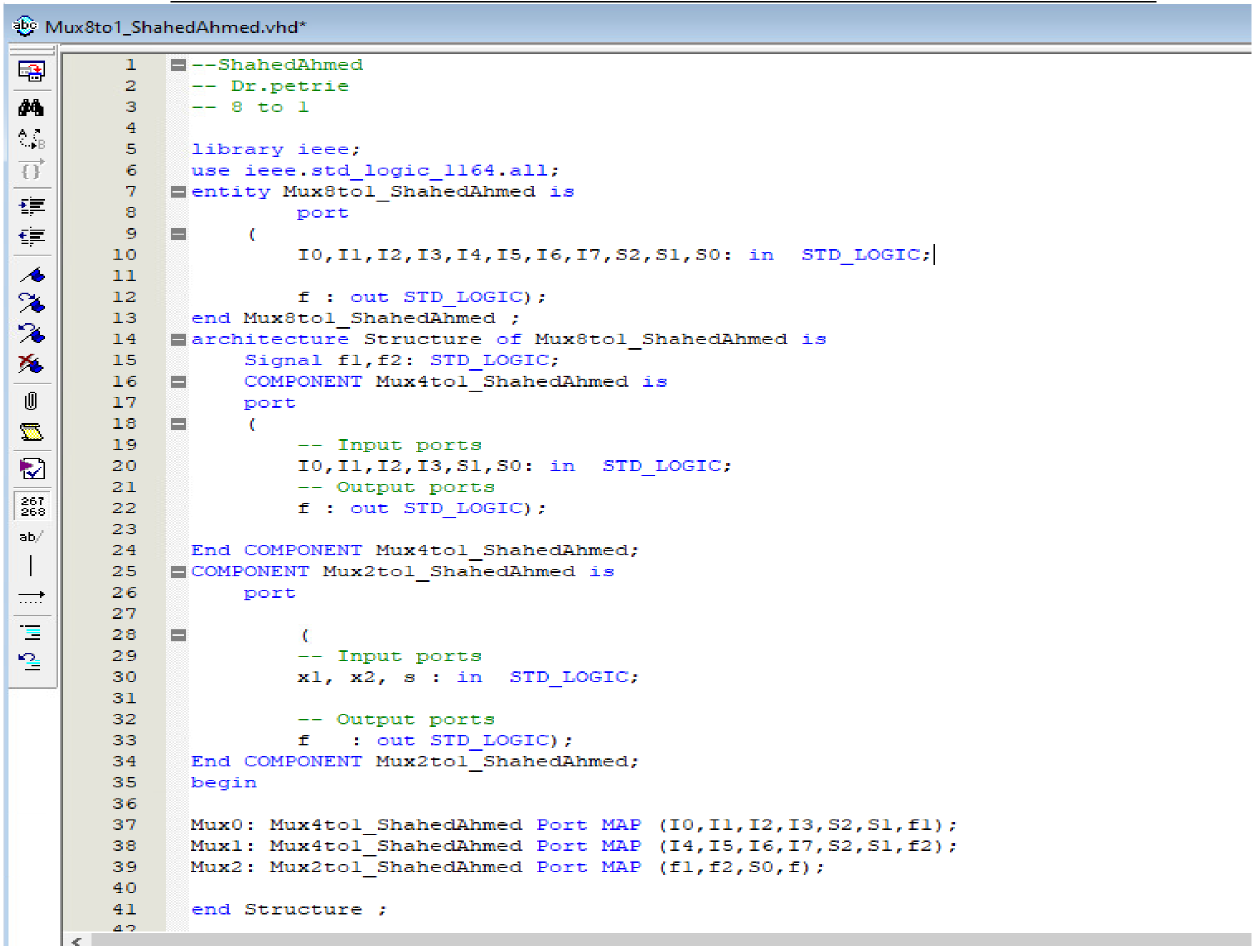


Truth Table



S2	S1	S0	F
0	0	0	I0
0	0	1	I4
0	1	0	I2
0	1	1	I6
1	0	0	I1
1	0	1	I5
1	1	0	I3
1	1	1	I7

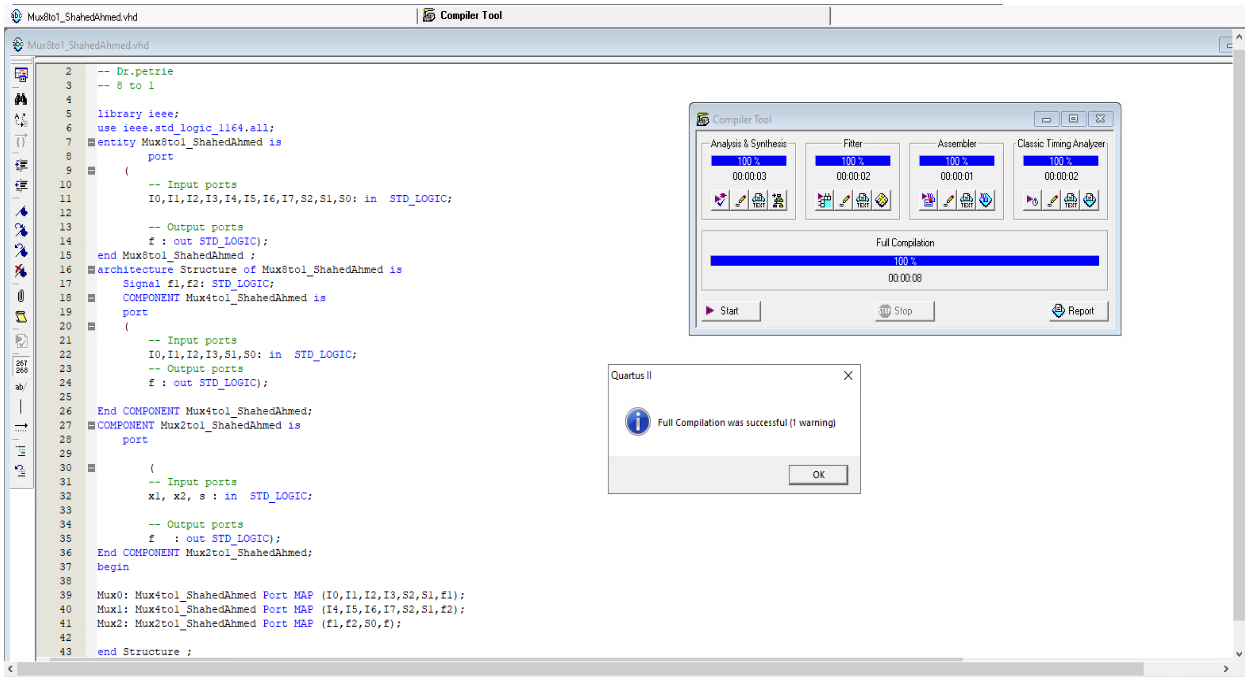
VHDL code



Mux8to1_ShahedAhmed.vhd*

```
--ShahedAhmed
-- Dr.petrie
-- 8 to 1

library ieee;
use ieee.std_logic_1164.all;
entity Mux8to1_ShahedAhmed is
        port
    (
        I0,I1,I2,I3,I4,I5,I6,I7,S2,S1,S0: in  STD_LOGIC;

        f : out STD_LOGIC);
end Mux8to1_ShahedAhmed ;
architecture Structure of Mux8to1_ShahedAhmed is
    Signal f1,f2: STD_LOGIC;
    COMPONENT Mux4to1_ShahedAhmed is
    port
    (
        -- Input ports
        I0,I1,I2,I3,S1,S0: in  STD_LOGIC;
        -- Output ports
        f : out STD_LOGIC);

End COMPONENT Mux4to1_ShahedAhmed;
COMPONENT Mux2to1_ShahedAhmed is
    port

        (
        -- Input ports
        x1, x2, s : in  STD_LOGIC;

        -- Output ports
        f   : out STD_LOGIC);
End COMPONENT Mux2to1_ShahedAhmed;
begin

Mux0: Mux4to1_ShahedAhmed Port MAP (I0,I1,I2,I3,S2,S1,f1);
Mux1: Mux4to1_ShahedAhmed Port MAP (I4,I5,I6,I7,S2,S1,f2);
Mux2: Mux2to1_ShahedAhmed Port MAP (f1,f2,S0,f);

end Structure ;
```

Successful Compilation



Mux8to1_ShahedAhmed.vhd | Compiler Tool

Mux8to1_ShahedAhmed.vhd

```vhdl
-- Dr.petrie
-- 8 to 1

library ieee;
use ieee.std_logic_1164.all;
entity Mux8to1_ShahedAhmed is
        port
    (
        -- Input ports
        I0,I1,I2,I3,I4,I5,I6,I7,S2,S1,S0: in  STD_LOGIC;

        -- Output ports
        f : out STD_LOGIC);
end Mux8to1_ShahedAhmed ;
architecture Structure of Mux8to1_ShahedAhmed is
    Signal f1,f2: STD_LOGIC;
    COMPONENT Mux4to1_ShahedAhmed is
    port
    (
        -- Input ports
        I0,I1,I2,I3,S1,S0: in  STD_LOGIC;
        -- Output ports
        f : out STD_LOGIC);

End COMPONENT Mux4to1_ShahedAhmed;
COMPONENT Mux2to1_ShahedAhmed is
    port

        (
        -- Input ports
        x1, x2, s : in  STD_LOGIC;

        -- Output ports
        f   : out STD_LOGIC);
End COMPONENT Mux2to1_ShahedAhmed;
begin

Mux0: Mux4to1_ShahedAhmed Port MAP (I0,I1,I2,I3,S2,S1,f1);
Mux1: Mux4to1_ShahedAhmed Port MAP (I4,I5,I6,I7,S2,S1,f2);
Mux2: Mux2to1_ShahedAhmed Port MAP (f1,f2,S0,f);

end Structure ;
```

Compiler Tool

Analysis & Synthesis	Fitter	Assembler	Classic Timing Analyzer
100 %	100 %	100 %	100 %
00:00:03	00:00:02	00:00:01	00:00:02

Full Compilation

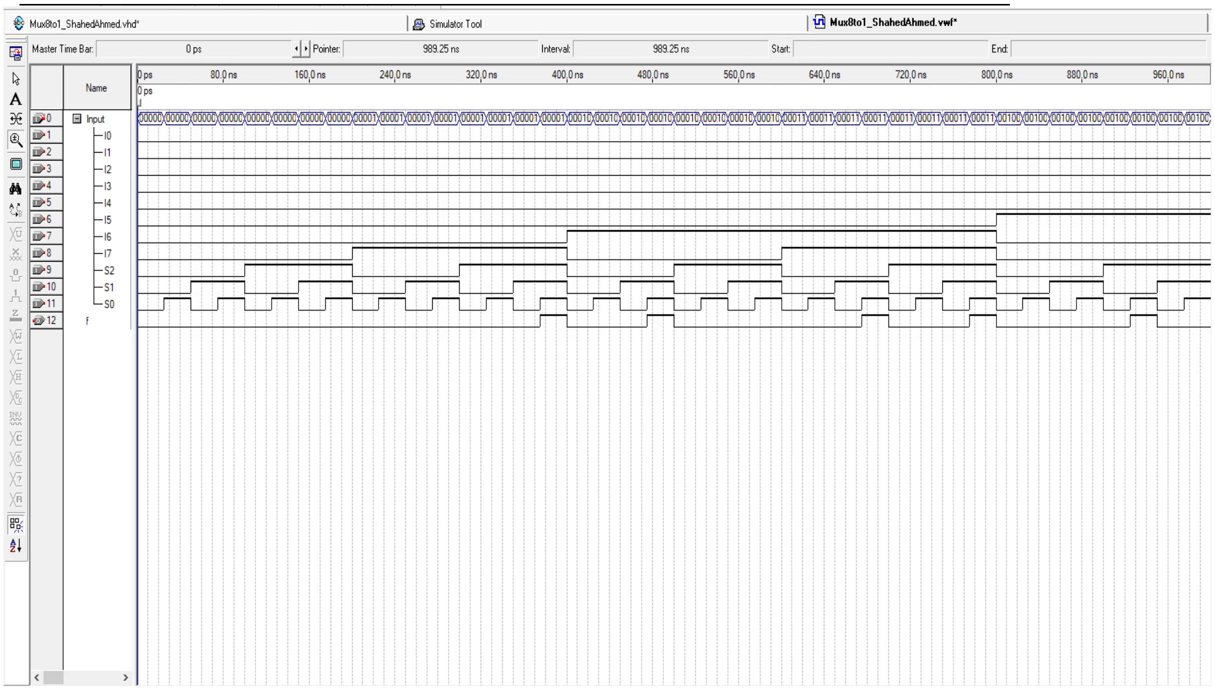
100 %

00:00:08

Quartus II

Full Compilation was successful (1 warning)

Timing Diagram

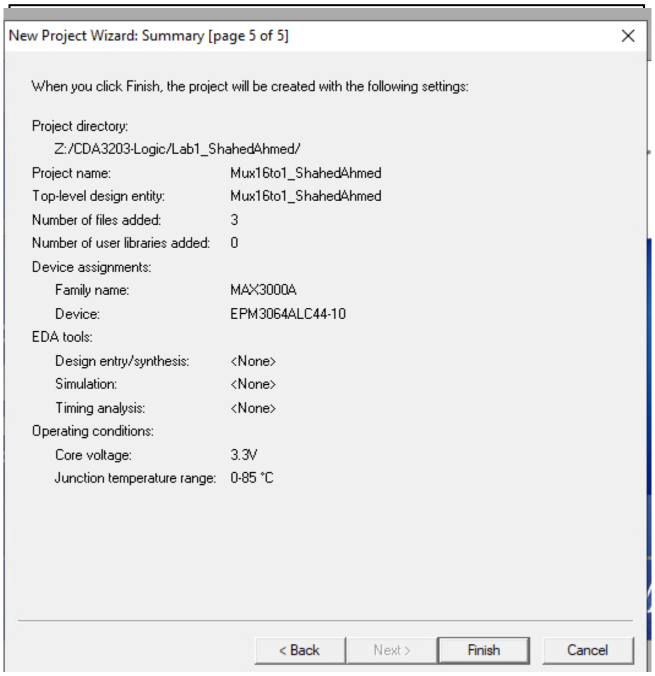


Mux8to1_ShahedAhmed.vhd* | Simulator Tool | Mux8to1_ShahedAhmed.vwf*

Master Time Bar: 0 ps | Pointer: 989.25 ns | Interval: 989.25 ns | Start: | End:

Part 5. Design and simulate a 16-to-1 Multiplexer (Mux) **using only Mux8to1, Mux4to1 and/or Mux2to1**.

Project Wizard



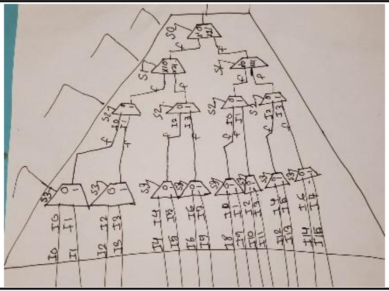
New Project Wizard: Summary [page 5 of 5]

When you click Finish, the project will be created with the following settings:

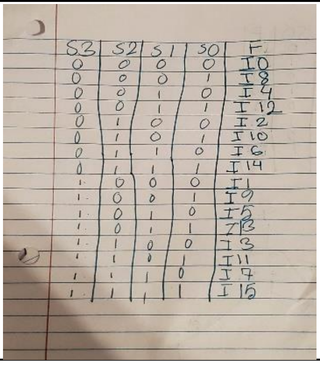
Project directory:
Z:/CDA3203-Logic/Lab1_ShahedAhmed/

Project name:	Mux16to1_ShahedAhmed
Top-level design entity:	Mux16to1_ShahedAhmed
Number of files added:	3
Number of user libraries added:	0
Device assignments:	
Family name:	MAX3000A
Device:	EPM3064ALC44-10
EDA tools:	
Design entry/synthesis:	<None>
Simulation:	<None>
Timing analysis:	<None>
Operating conditions:	
Core voltage:	3.3V
Junction temperature range:	0-85 °C

Mux16to1 Diagram

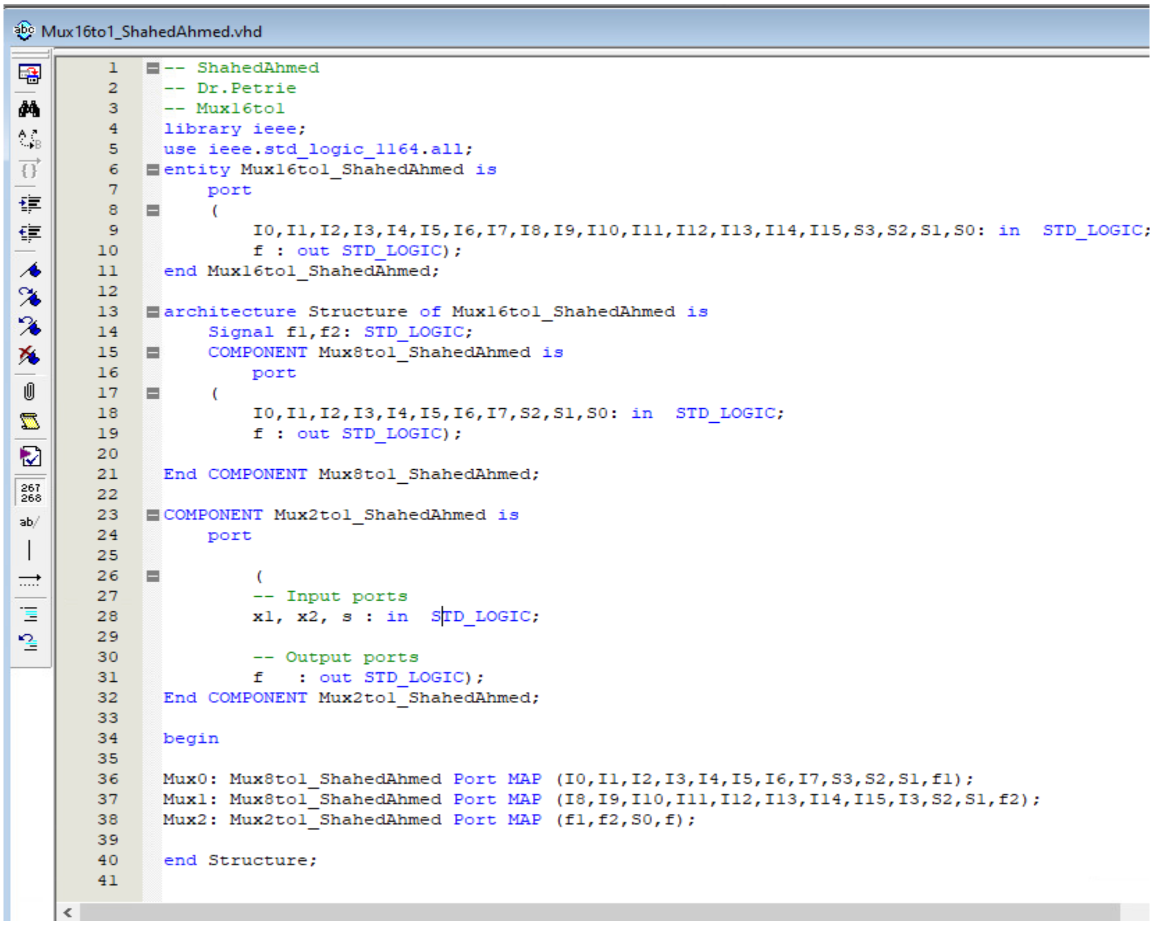


Truth Table



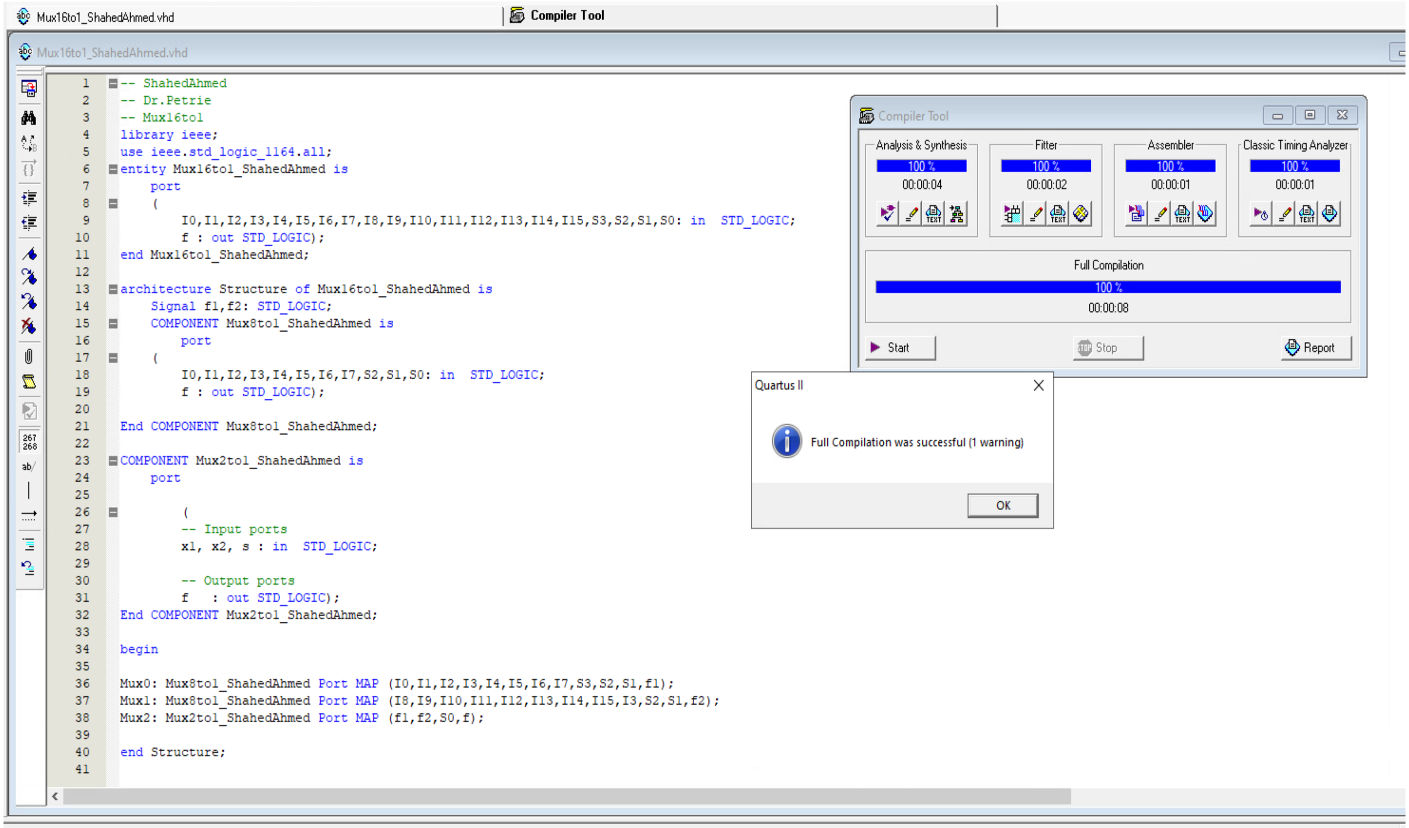
S3	S2	S1	S0	F
0	0	0	0	I0
0	0	0	1	I8
0	0	1	0	I4
0	0	1	1	I 12
0	1	0	0	I 2
0	1	0	1	I 10
0	1	1	0	I 6
0	1	1	1	I 14
1	0	0	0	I1
1	0	0	1	I9
1	0	1	0	I5
1	0	1	1	I13
1	1	0	0	I 3
1	1	0	1	I 11
1	1	1	0	I 7
1	1	1	1	I 15

VHDL code



Mux16to1_ShahedAhmed.vhd

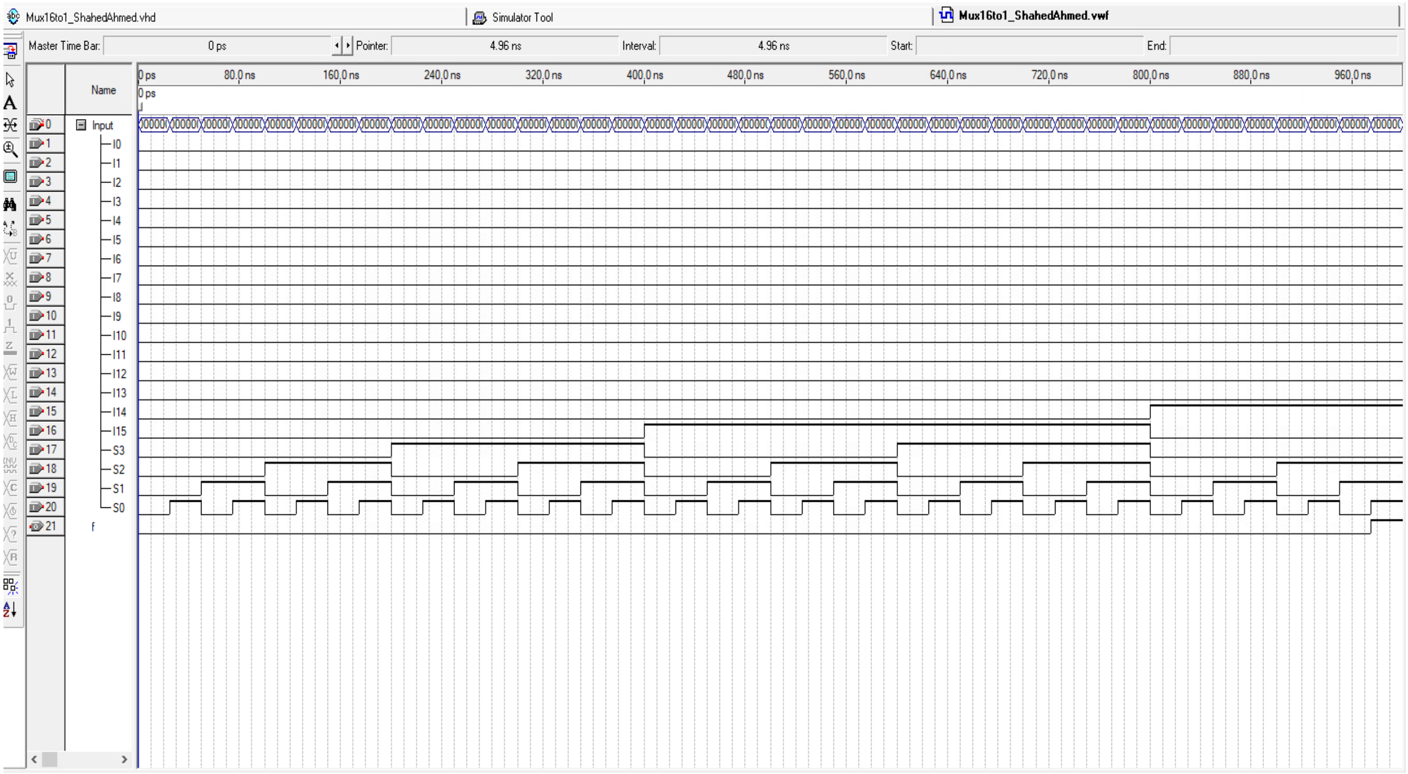
```
-- ShahedAhmed
-- Dr.Petrie
-- Mux16to1
library ieee;
use ieee.std_logic_1164.all;
entity Mux16to1_ShahedAhmed is
    port
    (
        I0,I1,I2,I3,I4,I5,I6,I7,I8,I9,I10,I11,I12,I13,I14,I15,S3,S2,S1,S0: in  STD_LOGIC;
        f : out STD_LOGIC);
end Mux16to1_ShahedAhmed;

architecture Structure of Mux16to1_ShahedAhmed is
    Signal f1,f2: STD_LOGIC;
    COMPONENT Mux8to1_ShahedAhmed is
        port
    (
        I0,I1,I2,I3,I4,I5,I6,I7,S2,S1,S0: in  STD_LOGIC;
        f : out STD_LOGIC);

End COMPONENT Mux8to1_ShahedAhmed;

COMPONENT Mux2to1_ShahedAhmed is
    port

        (
        -- Input ports
        x1, x2, s : in  STD_LOGIC;

        -- Output ports
        f    : out STD_LOGIC);
End COMPONENT Mux2to1_ShahedAhmed;

begin

Mux0: Mux8to1_ShahedAhmed Port MAP (I0,I1,I2,I3,I4,I5,I6,I7,S3,S2,S1,f1);
Mux1: Mux8to1_ShahedAhmed Port MAP (I8,I9,I10,I11,I12,I13,I14,I15,I3,S2,S1,f2);
Mux2: Mux2to1_ShahedAhmed Port MAP (f1,f2,S0,f);

end Structure;
```



```
-- ShahedAhmed
-- Dr.Petrie
-- Mux16to1
library ieee;
use ieee.std_logic_1164.all;
entity Mux16to1_ShahedAhmed is
    port
    (
        I0,I1,I2,I3,I4,I5,I6,I7,I8,I9,I10,I11,I12,I13,I14,I15,S3,S2,S1,S0: in  STD_LOGIC;
        f : out STD_LOGIC);
end Mux16to1_ShahedAhmed;

architecture Structure of Mux16to1_ShahedAhmed is
    Signal f1,f2: STD_LOGIC;
    COMPONENT Mux8to1_ShahedAhmed is
        port
    (
        I0,I1,I2,I3,I4,I5,I6,I7,S2,S1,S0: in  STD_LOGIC;
        f : out STD_LOGIC);

End COMPONENT Mux8to1_ShahedAhmed;

COMPONENT Mux2to1_ShahedAhmed is
    port

        (
        -- Input ports
        x1, x2, s : in  STD_LOGIC;

        -- Output ports
        f   : out STD_LOGIC);
End COMPONENT Mux2to1_ShahedAhmed;

begin

Mux0: Mux8to1_ShahedAhmed Port MAP (I0,I1,I2,I3,I4,I5,I6,I7,S3,S2,S1,f1);
Mux1: Mux8to1_ShahedAhmed Port MAP (I8,I9,I10,I11,I12,I13,I14,I15,I3,S2,S1,f2);
Mux2: Mux2to1_ShahedAhmed Port MAP (f1,f2,S0,f);

end Structure;
```

Full Compilation was successful (1 warning)

Timing Diagram



Master Time Bar: 0 ps   Pointer: 4.96 ns   Interval: 4.96 ns   Start: End: