EXPERIMENT 03

Implementation of Basic Gates using Universal Gates

Objectives:

Using two input NAND and NOR gates, construct the following

1. NOT
2. AND
3. OR

After doing this, implement the given expression on the trainer board.

Equipment /Tool:

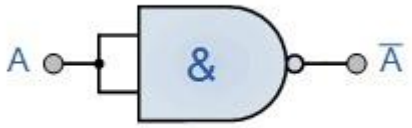
Trainer, IC 74LS00, 74LS02.

Theory:

NAND and NOR gates are called universal gates because we can make any basic gate from them by using the following circuits.

1) **Implementation of Gates using NAND Gate only: i)**

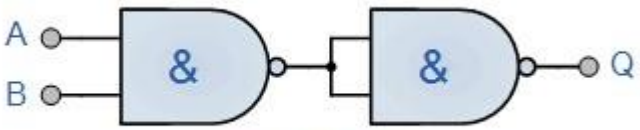
NOT Gate Behavior:



NOT Gate

Input	output
0	1
1	0

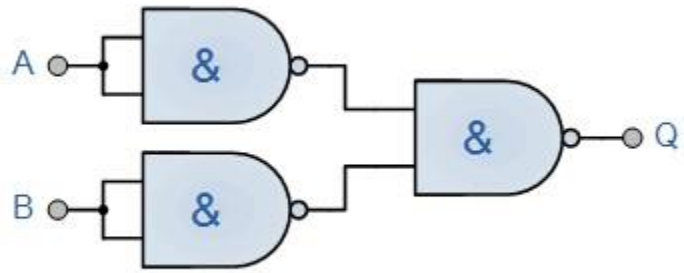
ii) AND Gate Behavior:



2-input AND Gate

Input		Output
A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

iii) OR Gate Behavior:



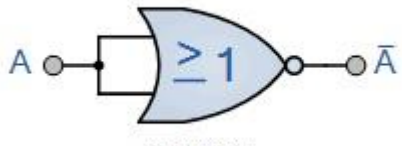
2-input OR Gate

Input		Output
X	Y	F
0	0	0
0	1	1
1	0	1
1	1	1

2) Implementation of Gates using NOR Gate Only:

Verify all the truth tables for all the gates.

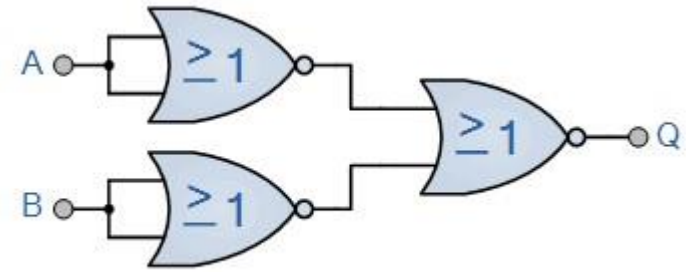
i) NOT Gate Behavior:



NOT Gate

A	A’
0	1
1	0

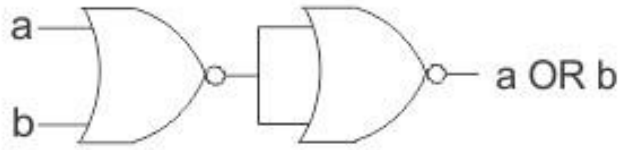
ii) <u>AND Gate Behavior:</u>



2-input AND Gate

A	B	Q
0	0	0
0	1	0
1	0	0
1	1	1

iii) <u>OR Gate Behavior:</u>



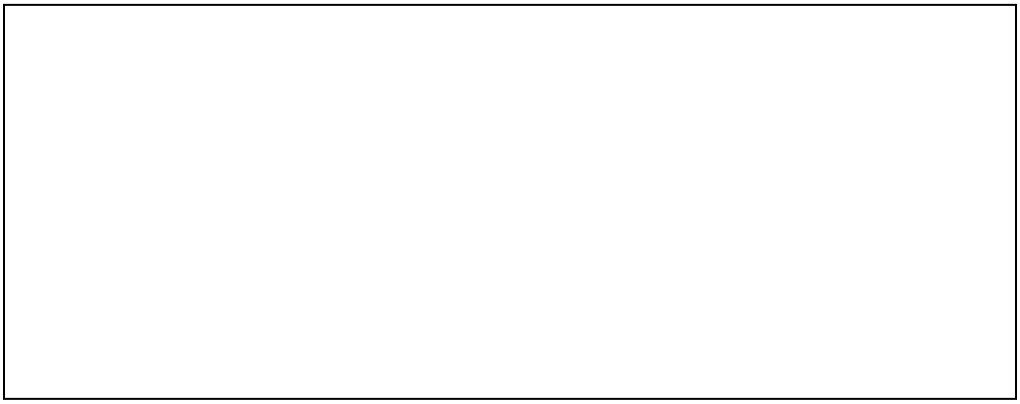
A	B	F
0	0	0
0	0	1
1	0	1
1	1	1

Exercise in Lab:

1) Implement following expression using NOR Gate only.
2) Implement following expression using NAND Gate only.

$$F=X+\overline{Y}.Z$$

Circuit diagram



Truth Table:

Input			Output
X	Y	Z	F
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	