Digital Logic Design (DLD)

(Lab Task No 1)

Session (2022-2026)

Program

BS-Computer Science

Submitted By:

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Lab Task No 1

Implementation of AND, OR, NAND, NOR and NOT Gates

Objectives:

Demonstrate the operations of basic logic gates.

Use the following gates and draw their truth table.

7408 Quad 2-Input AND Gate

7432 Quad 2-Input OR Gate

7400 Quad 2-Input NAND Gate

7402 Quad 2-Input NOR Gate 7404

Hex Single-Input NOT Gate

Equipment /Tool:

Trainer, IC 7404, 7400, 7432, 7408, 7402

Background:

A logic gate is a circuit which has one or more inputs and single output. A logic gate is an elementary building block of a digital circuit. Most logic gates have two inputs and one output. At any given moment, every terminal is in one of the two binary conditions low (0) or high (1), represented by different voltage levels. The logic state of a terminal can, and generally does, change often, as the circuit processes data. In most logic gates, the low state is approximately zero volts (0 V), while the high state is approximately five volts positive (+5 V).

For TTL 0 - 0.8V corresponds to '0' logic level and 2 – 5V corresponds to '1' logic level.

Procedure:

Connect the circuit according to the pin configuration of the ICs as mentioned in the datasheets and check the truth tables.

Symbols:

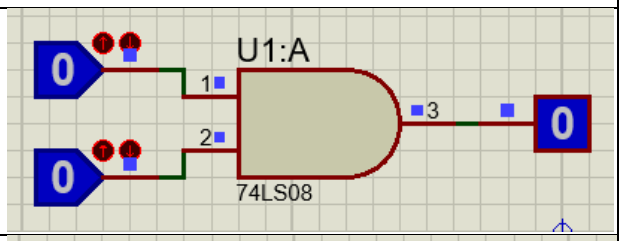
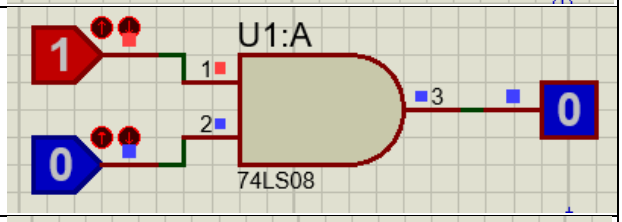
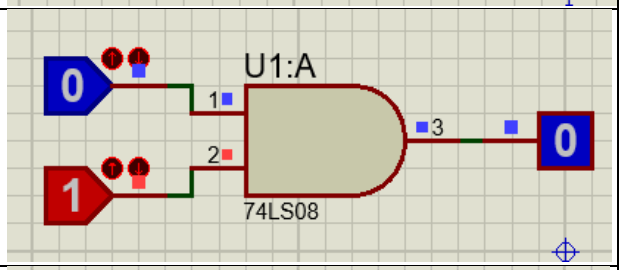
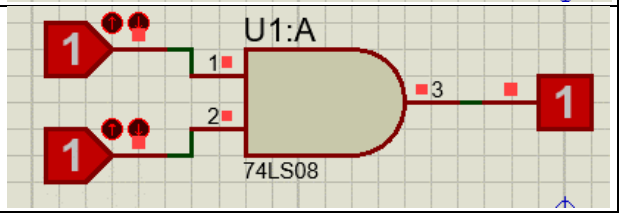
Following are the symbols of the basic logic gates:

Lab Tasks

- Verify the truth tables of all the ICs specified:

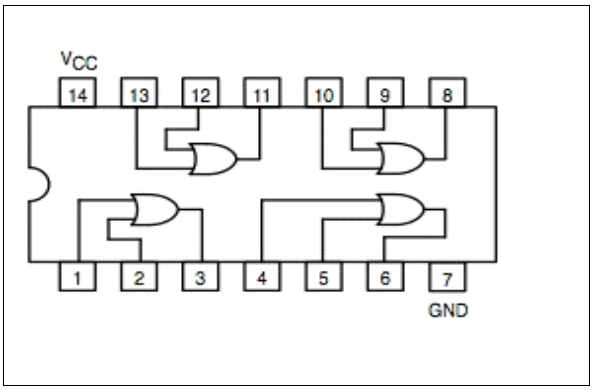
1). 74LS08 (AND Gate):

Truth Table With Proof:

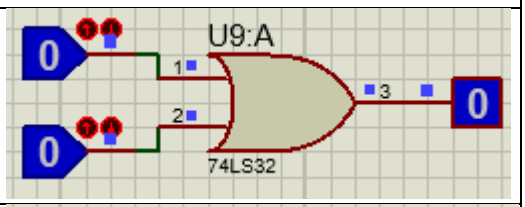
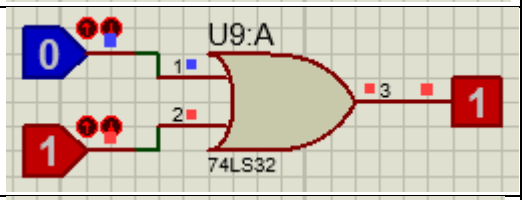
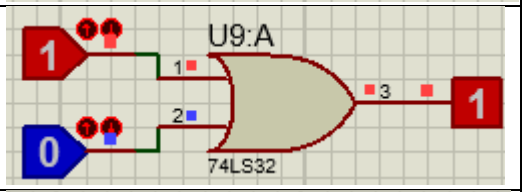
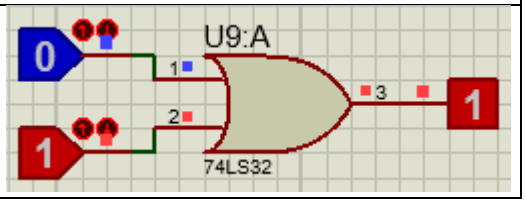
Input		Output	Proof
A	B	Y=A.B	
0	0	0	
0	1	0	
1	0	0	
1	1	1	

2). 74LS32 (OR Gate):

Y=A+B

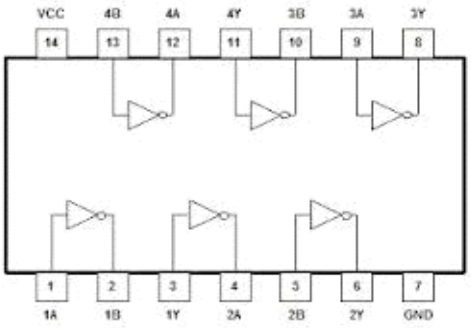


Truth Table With Proof:

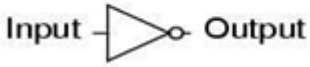
Input		Output	Proof
A	B	Y=A+B	
0	0	0	
0	1	1	
1	0	1	
1	1	1	

3). 74LS04 (NOT Gate):

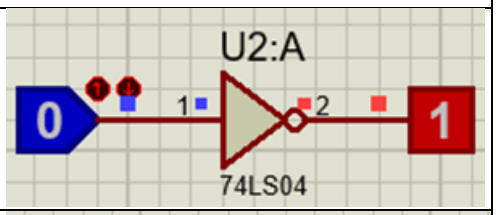
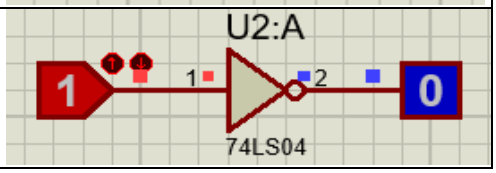
Y=A`



NOT gate truth table

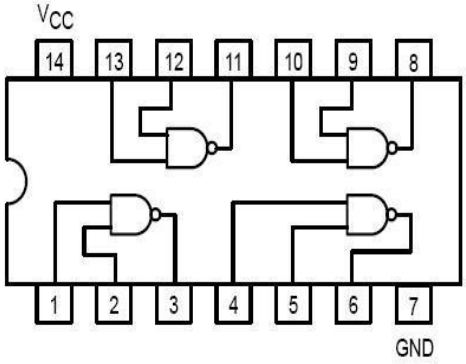


Truth Table With Proof:

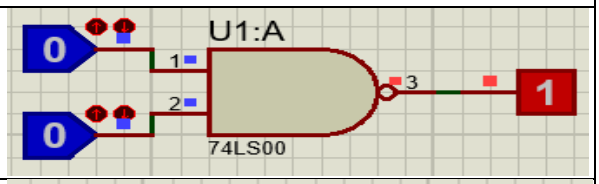
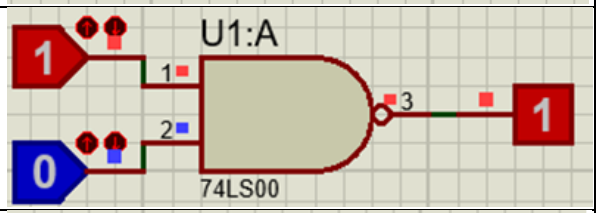
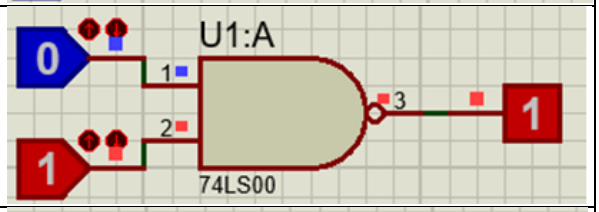
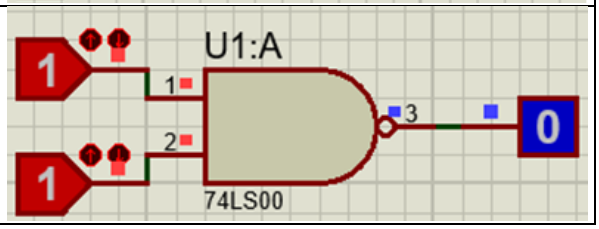
Input	Output	Proof
A	**A`**	**A=A`**
0	**1**	
1	**0**	

4). 74LS00 (NAND Gate):

Y=(A.B)`



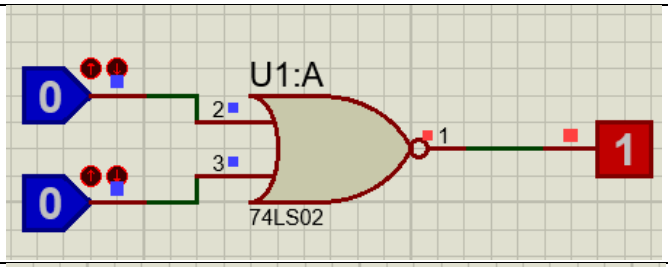
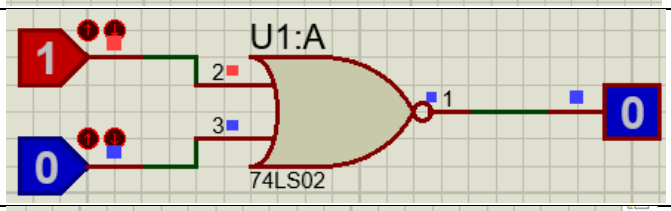
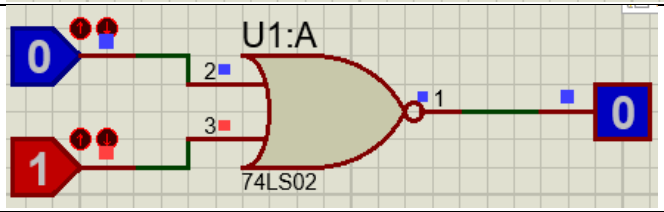
Truth Table With Proof:

Input		Output	Proof
A	**B**	**Y=(A.B)`**	
0	**0**	**1**	
0	**1**	**1**	
1	**0**	**1**	
1	**1**	**0**	

5). 74LS02(NOR Gate):

Y=(A`+B`)`

Truth Table With Proof:

Input		Output	Proof
A	B	Y=(A`+B`)`	
0	0	1	
0	1	0	
1	0	0	
1	1	0