Digital Logic & Design

Hazara University Mansehra
Department of Computer Science & IT

Introduction

- Now we discuss some of the major functions of Combinational Logic including:
  - Adders,
  - Comparators,
  - Decoders,
  - Encoders,
  - Code Converters,
  - Multiplexers (data selectors),
  - Demultiplexers, and
  - Parity generators/checkers

Half and Full Adders

- Adders are important in computers and also in other types of digital systems in which numerical data are processed.
- An understanding of the basic adder operation is fundamental to the study of digital systems.
- In this section, the half-adder and the full-adder are introduced.

The Half-Adder

- A half-adder adds two bits and produces a sum and an output carry.

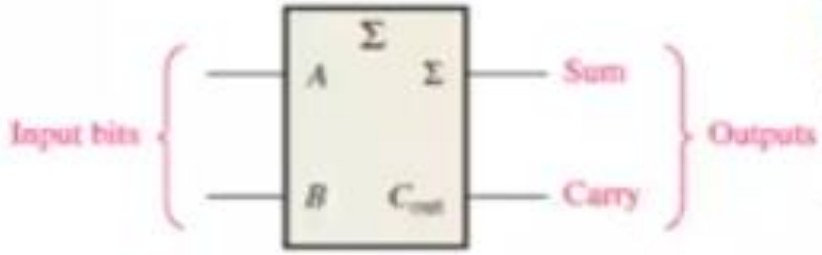

TABLE 6–1

Half-adder truth table

A	B	C_{out}	Σ
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Σ = sum

C_{out} = output carry

A and B = input variables (operands)

0 + 0 = 0
0 + 1 = 1
1 + 0 = 1
1 + 1 = 10

1
1
1 0

The Half-Adder

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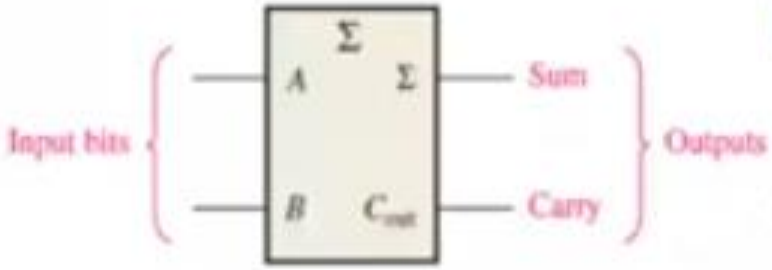

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$\Sigma = \bar{A}B + A\bar{B}$

$= A \oplus B$

$C_o = AB$

The Half-Adder

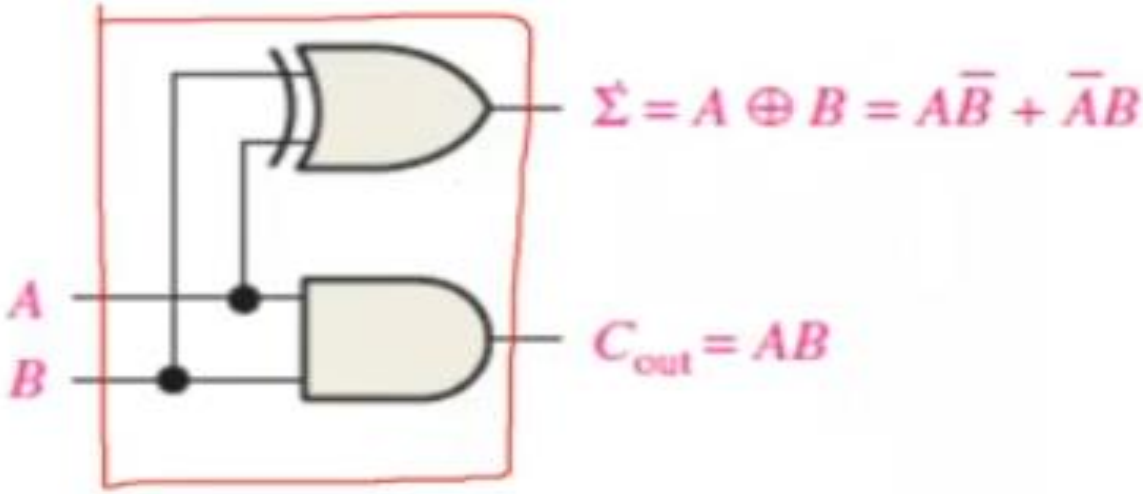
- From the operation of the half-adder as stated in Table 6–1, expressions can be derived for the sum and the output carry as functions of the inputs.
- Notice that the output carry (C_{out}) is a 1 only when both *A* and *B* are 1s; therefore, C_{out} can be expressed as the AND of the input variables.

$$C_{out} = AB$$

- Now observe that the sum output is a 1 only if the input variables, *A* and *B*, are not equal.
- The sum can therefore be expressed as the exclusive-OR of the input variables.

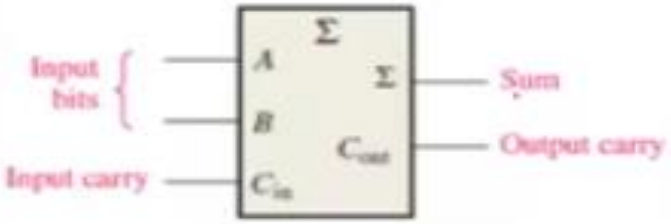
$$\Sigma = A \oplus B$$

Half-Adder Logic Diagram



The Full-Adder

- The second category of adder is the full-adder.
- The full-adder accepts two input bits and an input carry and generates a sum output and an output carry.



$$\Sigma = (A \oplus B) \oplus C_{in}$$

$$C_{out} = AB + (A \oplus B)C_{in}$$

TABLE 6–2

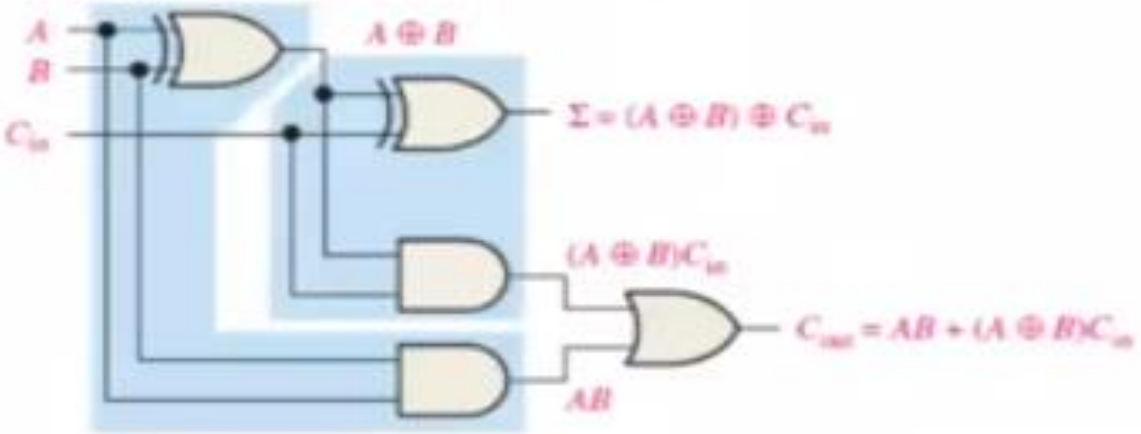
Full-adder truth table.

A	B	C_{in}	C_{out}	Σ
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

C_{in} = input carry, sometimes designated as CI
C_{out} = output carry, sometimes designated as CO
Σ = sum
A and B = input variables (operands)

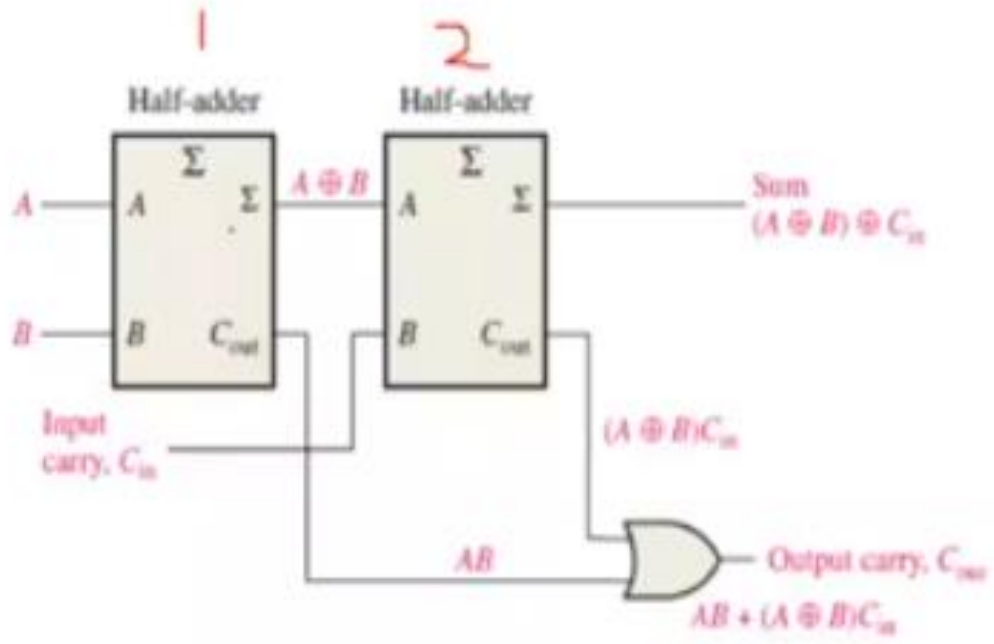
Full-Adder Logic Diagram

(a) Logic required to form the sum of three bits



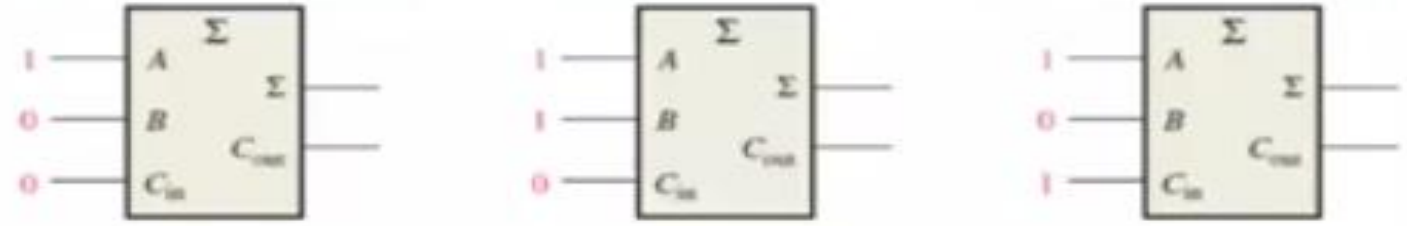
(b) Complete logic circuit for a full-adder (each half-adder is enclosed by a shaded area)

Arrangement of two half-adders to form a full-adder



EXAMPLE 6–1

For each of the three full-adders in Figure 6–6, determine the outputs for the inputs shown.



SECTION 6–1 CHECKUP

Answers are at the end of the chapter.

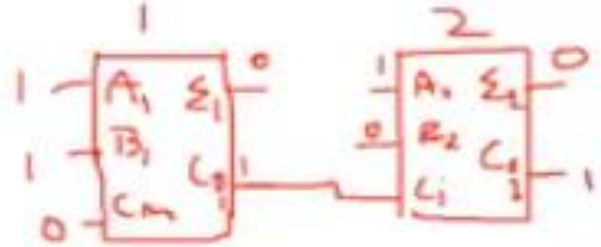
1. Determine the sum (Σ) and the output carry (C_{out}) of a half-adder for each set of input bits:

   (a) 01 (b) 00 (c) 10 (d) 11

2. A full-adder has $C_{in} = 1$. What are the sum (Σ) and the output carry (C_{out}) when $A = 1$ and $B = 1$?

Parallel Binary Adders

- A single full-adder is capable of adding two 1-bit numbers and an input carry.
- To add binary numbers with more than one bit, you must use additional full-adders. When one binary number is added to another, each column generates a sum bit and a 1 or 0 carry bit to the next column to the left, as illustrated here with 2-bit numbers.



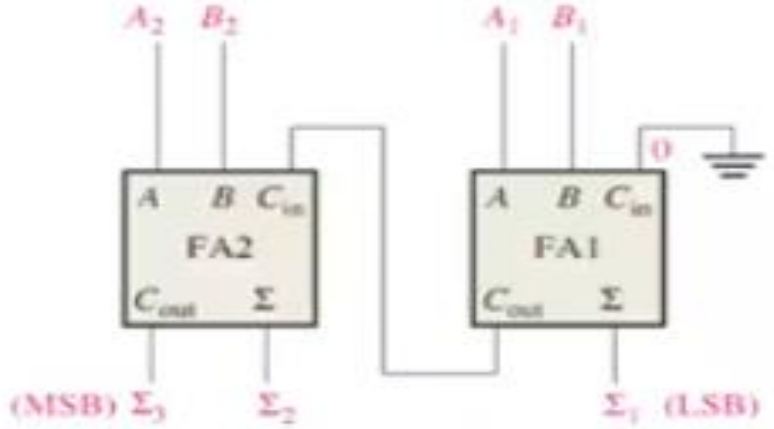
$$\begin{array}{r} {}^{1}C_{0_1} \\ 11 \\ 01 \\ \hline 100 \\ C_0 Z_2 Z_1 \end{array}$$

Parallel Binary Adders

- To add two binary numbers, a full-adder (FA) is required for each bit in the numbers.
- So for 2-bit numbers, two adders are needed; for 4-bit numbers, four adders are used; and so on.
- The carry output of each adder is connected to the carry input of the next higher-order adder

General format, addition of two 2-bit numbers:

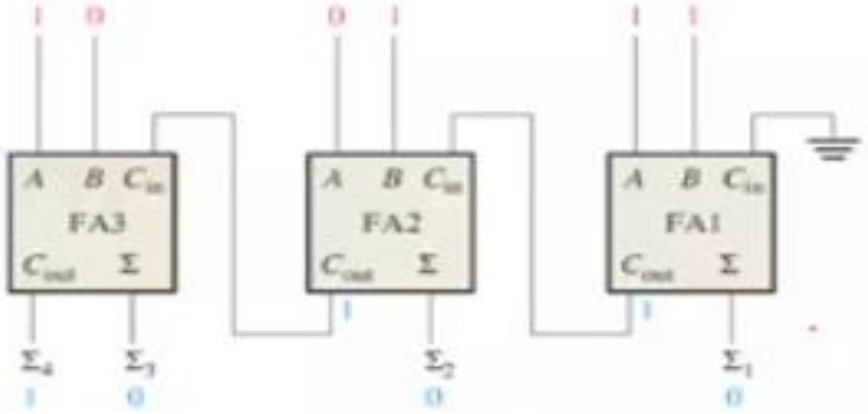
$$\begin{array}{r} A_2A_1 \\ +\ B_2B_1 \\ \hline \Sigma_3\Sigma_2\Sigma_1 \end{array}$$

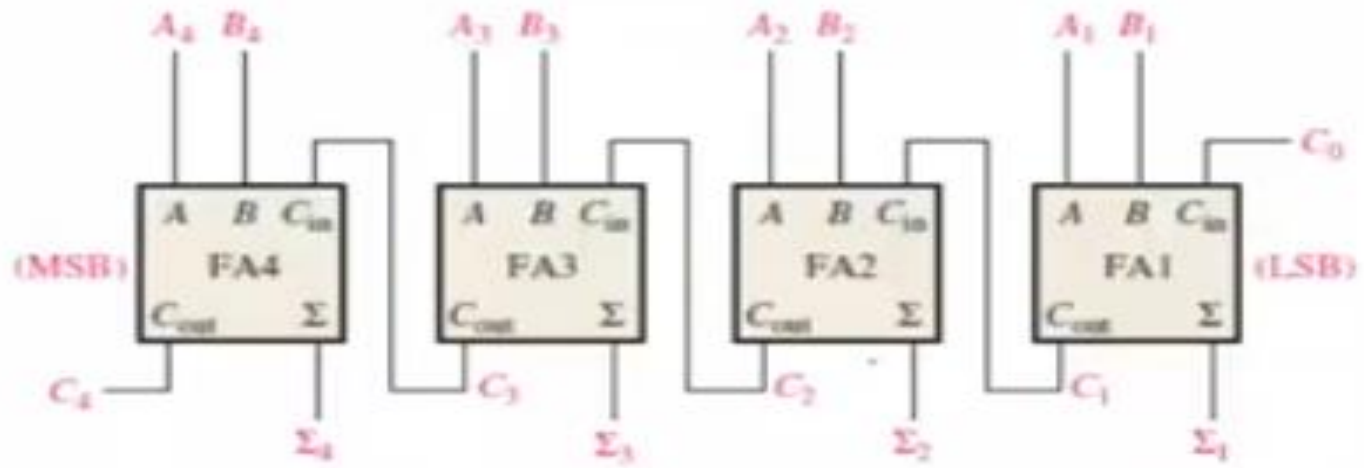


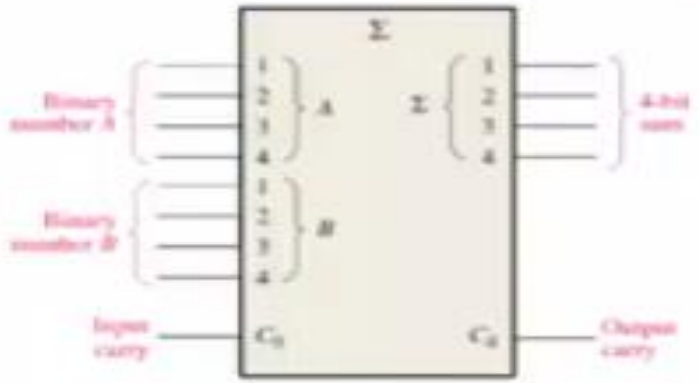
Parallel Binary Adders

EXAMPLE 6–2

Determine the sum generated by the 3-bit parallel adder in Figure 6–8 and show the intermediate carries when the binary numbers 101 and 011 are being added.







Truth table for each stage of a 4-bit parallel adder.

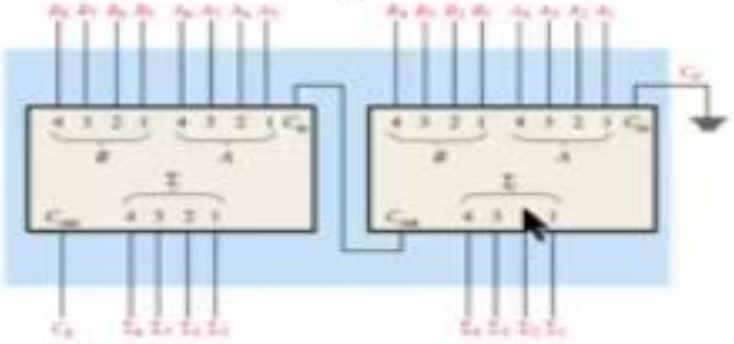
C_{n-1}	A_n	B_n	Σ_n	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Four-Bit Parallel Adders

- A group of four bits is called a **Nibble**.
- A basic 4-bit parallel adder is implemented with four full-adder stages as shown in Figure,
- Again, the LSBs (A1 and B1) in each number being added go into the right-most full-adder; the higher-order bits are applied as shown to the successively higher-order adders, with the MSBs (A4 and B4) in each number being applied to the left-most full-adder.
- The carry output of each adder is connected to the carry input of the next higher-order adder as indicated.
- These are called internal carries.

Adder Expansion

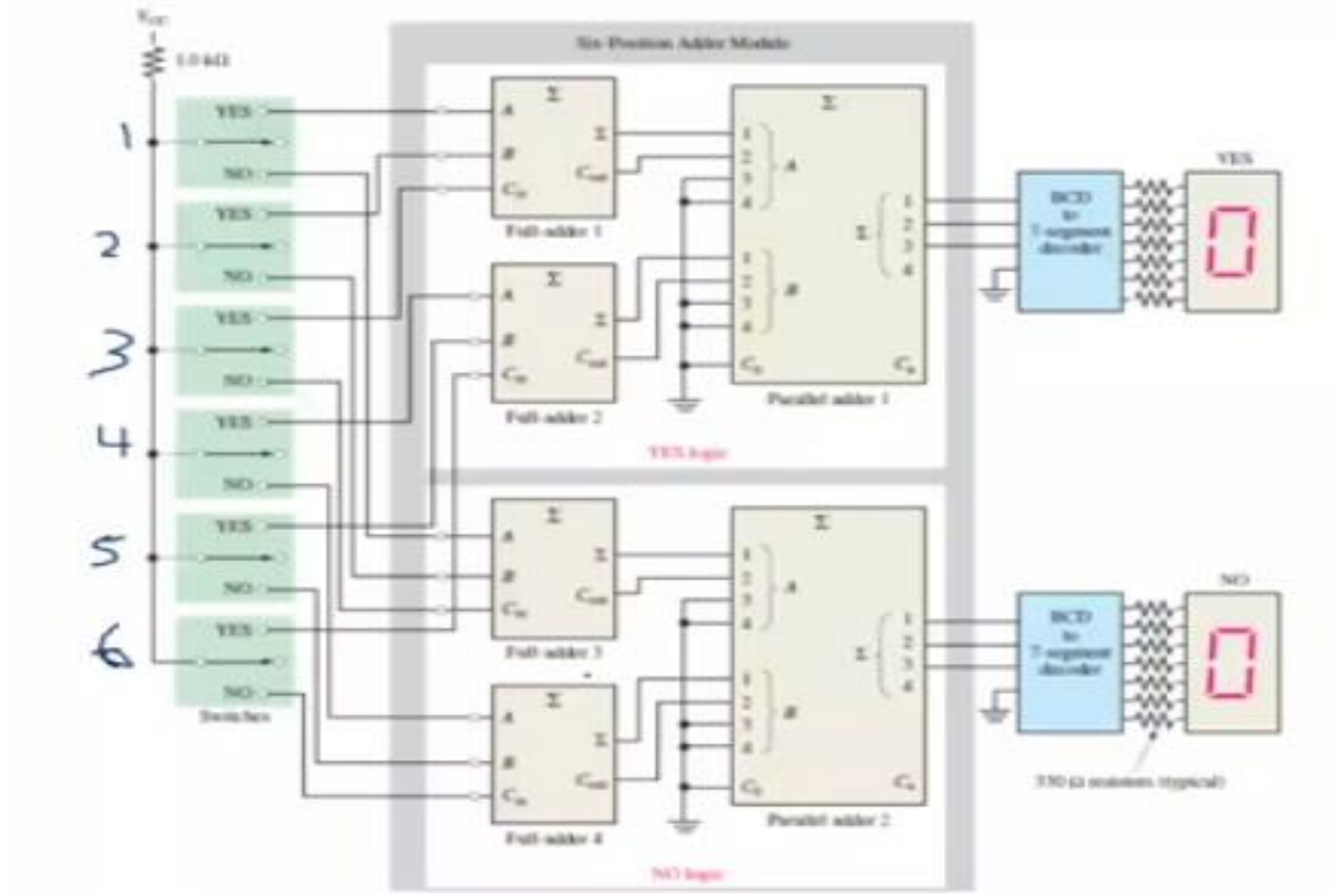
- The 4-bit parallel adder can be expanded to handle the addition of two 8-bit numbers by using two 4-bit adders.
- The carry input of the low-order adder (C_0) is connected to ground because there is no carry into the least significant bit position, and the carry output of the low-order adder is connected to the carry input of the high-order adder, as shown in Figure:



Application

An example of full-adder and parallel adder application is a simple voting system that can be used to simultaneously provide the number of "yes" votes and the number of "no" votes. This type of system can be used where a group of people are assembled and there is a need for immediately determining opinions (for or against), making decisions, or voting on certain issues or other matters.

In its simplest form, the system includes a switch for "yes" or "no" selection at each position in the assembly and a digital display for the number of yes votes and one for the number of no votes. The basic system is shown in Figure 6–13 for a 6-position setup, but it can be expanded to any number of positions with additional 6-position modules and additional parallel adder and display circuits.


1
2
3
4
5
6
YES
NO
Full-adder 1
Full-adder 2
Full-adder 3
Full-adder 4
Parallel adder 1
Parallel adder 2
BCD to 7-segment decoder
BCD to 7-segment decoder
YES
NO