Digital Logic Design (DLD)
(Lab Task No 6)

Session (2022-2026)

Program

BS-Computer Science

Submitted By:

Student Name: Shaheer Ali Roll Number: 301-221044

Supervised By:

Ms. Muneeba Darwaish
Lecturer
CS& IT Department

Hazara University, Mansehra

EXPERIMENT 06

Implementation of a 2 to 4 Decoder

Objectives:

Implementation of a 2 to 4 decoder using basic gates.

Equipment use:

Trainer, IC74LS04 (NOT), 74LS11 (Three input AND gate).

Background Theory:

A decoder is a combinational circuit that converts binary information from "n" codes to "2n" (two raised to the power n) unique outputs. They can be 2 to 4, 3 to 8, 4 to 16 etc. It has a lot of applications. There are many scenarios in which we must use such devices.

Lab Tasks:

- Write truth table for a 2 to 4 decoder with enable bit in it.
- Draw the gate diagram of a 2 to 4 decoder.
- Implementation of a 2 to 4 decoder using three input AND gate with enable bit as active low and verify with truth table.
- For three input AND gate use 74LS11.

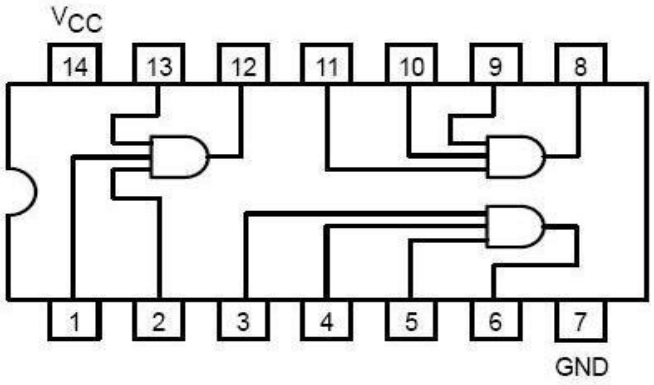
Procedure:

Fill in the truth table for a 2 to 4 decoder with an active low enable bit:

E	S1	S0	D3	D2	D1	D0
0	0	0	0	0	0	1
0	0	1	0	0	1	0
0	1	0	0	1	0	0
0	1	1	1	0	0	0
1	X	X	X	X	X	X

Pin configuration of 74LS11:

Following is the pin diagram of three input AND gate IC:



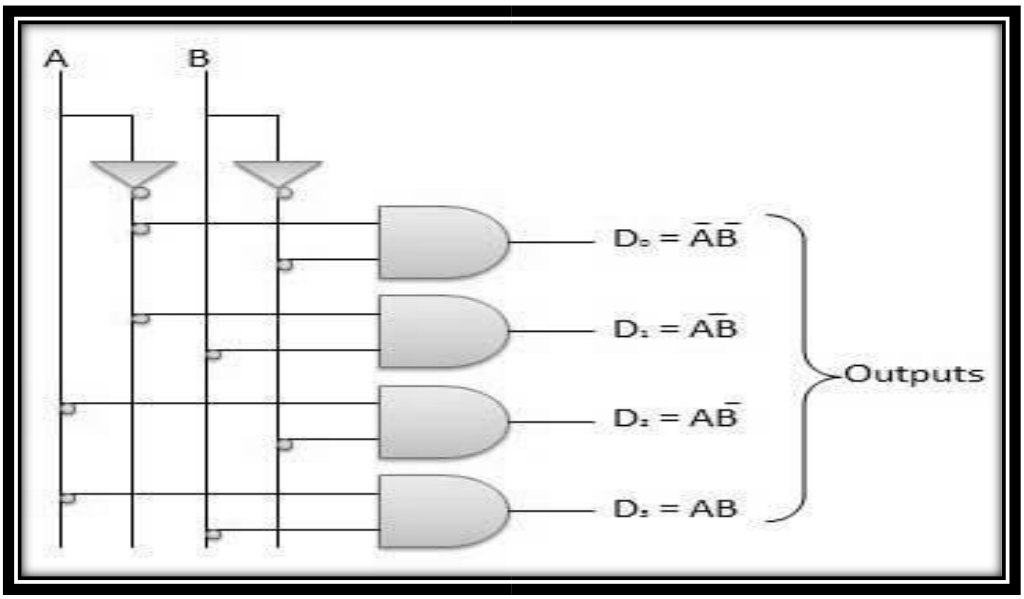
Following is the truth table for three input AND gate IC:

INPUTS		OUTPUTS	
A	**B**	**C**	**Y**
X	X	L	L
X	L	X	L
L	X	X	L
H	H	H	H

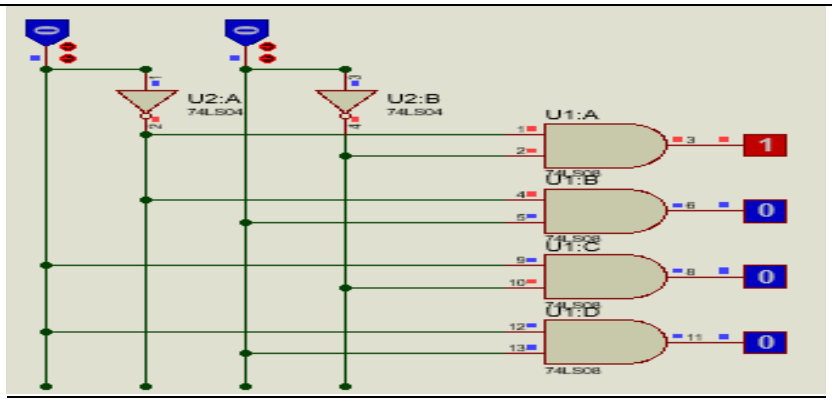
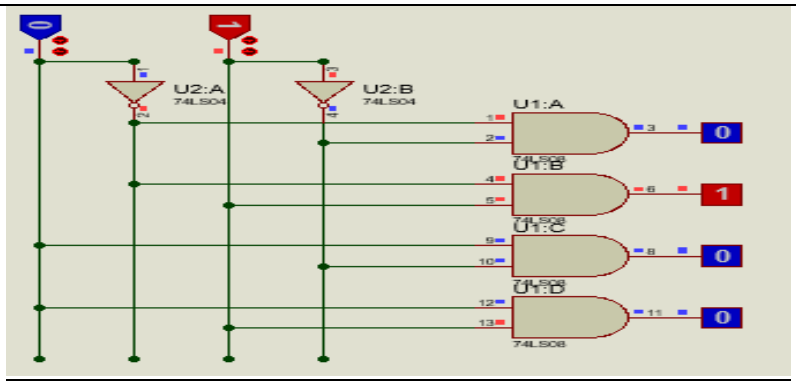
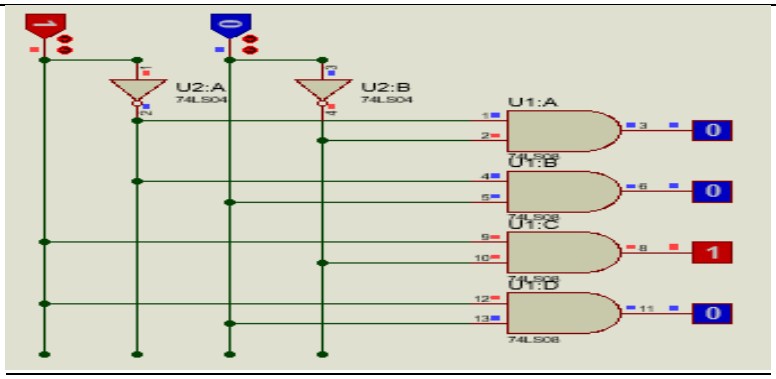
H=HIGH Logic level
L=LOW Logic level
X=Either LOW or HIGH Logic level

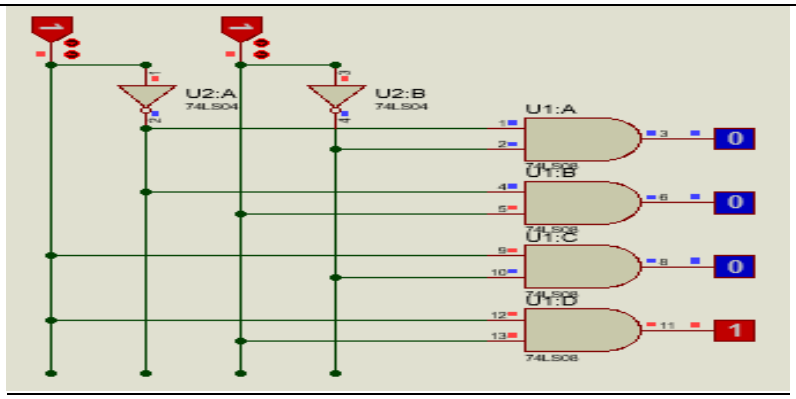
CIRCUIT DIAGRAM:

Draw a 2 to 4 decoder with active low pin:



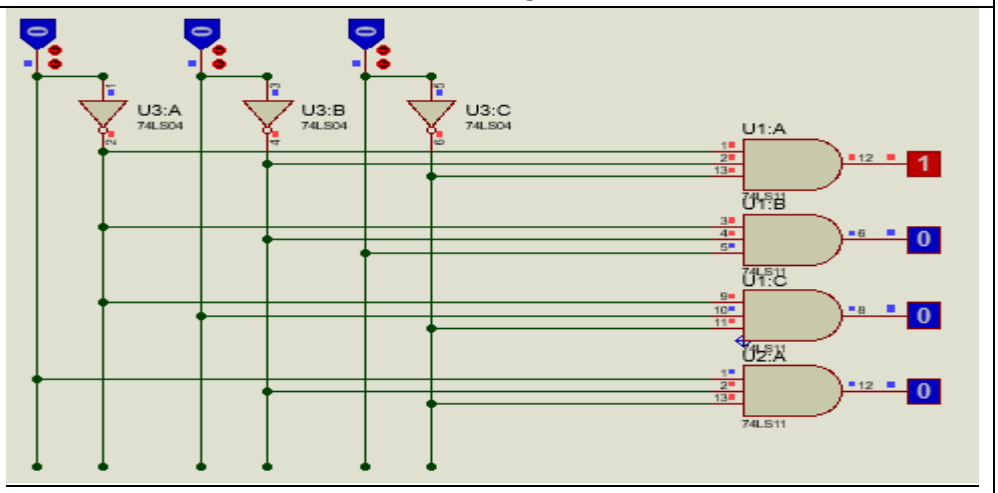
IMPLEMENTATION USING 2-Input Logic Gate:

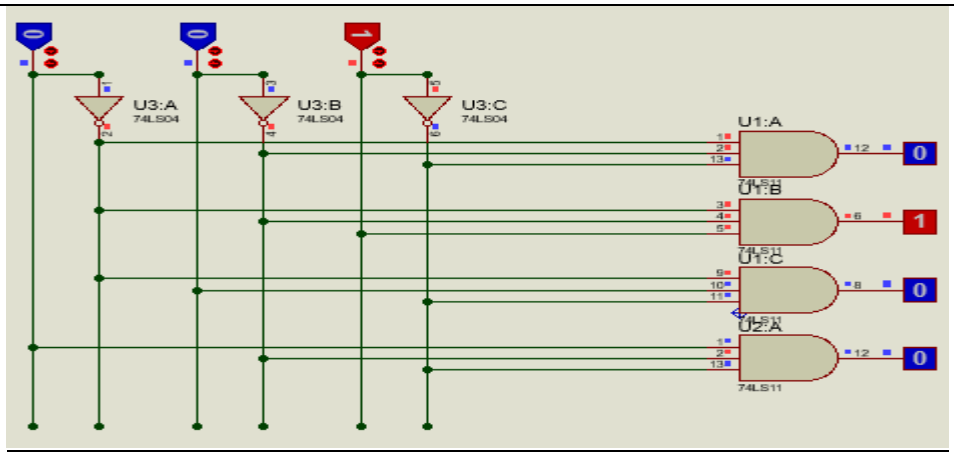
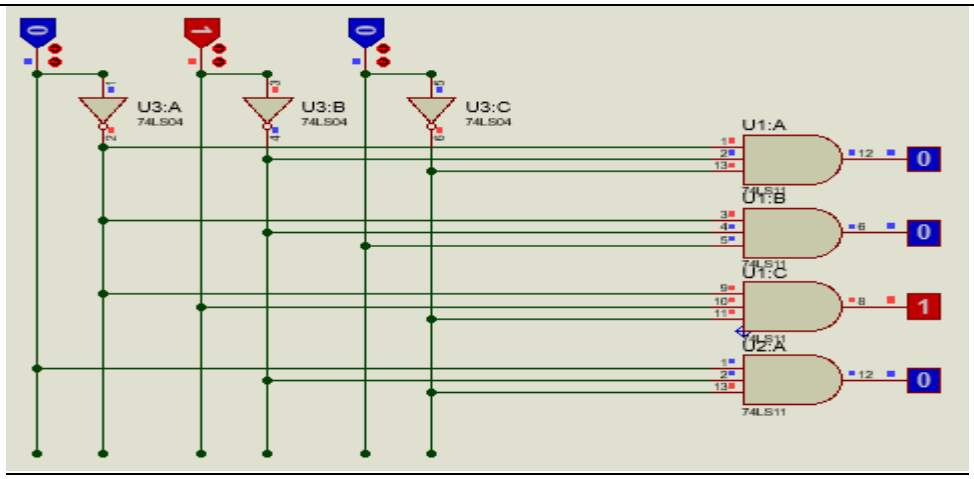
E	S1	S0	D3	D2	D1	D0	Proof With Circuit Diagram
0	0	0	0	0	0	1	
0	0	1	0	0	1	0	
0	1	0	0	1	0	0	

0	1	1	1	0	0	0	

OR

IMPLEMENTATION USING 3-Input Logic Gate:

E	S1	S0	D3	D2	D1	D0	Proof With Circuit Diagram
0	0	0	0	0	0	1	

0	0	1	0	0	1	0	
0	1	0	0	1	0	0	
0	1	1	1	0	0	0