DLD
Sequential Circuits

Latches and Flip Flop

Latches

A **latch** is a temporary storage device

Has two stable states i.e SET or RESET (bistable).

Uses feedback arrangement. (output is fed back to input)

It is a basic form of memory.

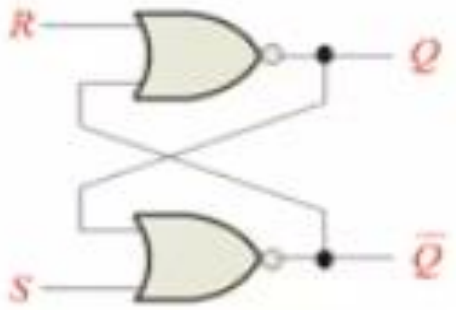
S-R (Set-Reset) Latch

The S-R (Set-Reset) latch is the most basic type.

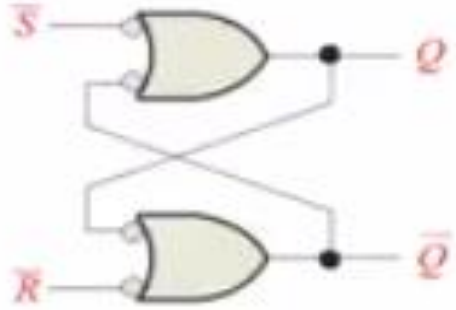
It can be constructed from NOR gates or NAND gates.

With NOR gates, the latch responds to active-HIGH inputs.

With NAND gates, it responds to active-LOW inputs.



NOR Active-HIGH Latch

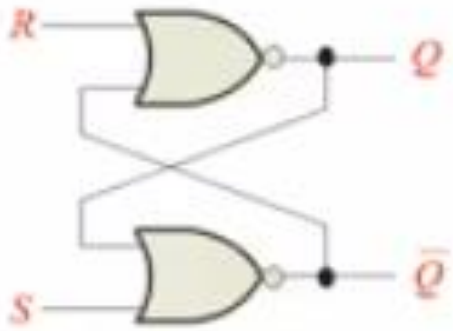


NAND Active-LOW Latch

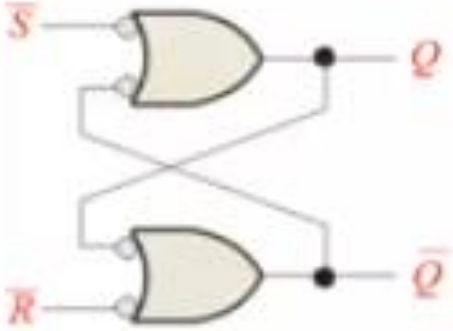
S-R (Set-Reset) Latch

Note that the output of each gate is connected to the input of opposite gate.

This produces a regenerative feedback that is the core characteristic of all latches and flip flops.



NOR Active-HIGH Latch



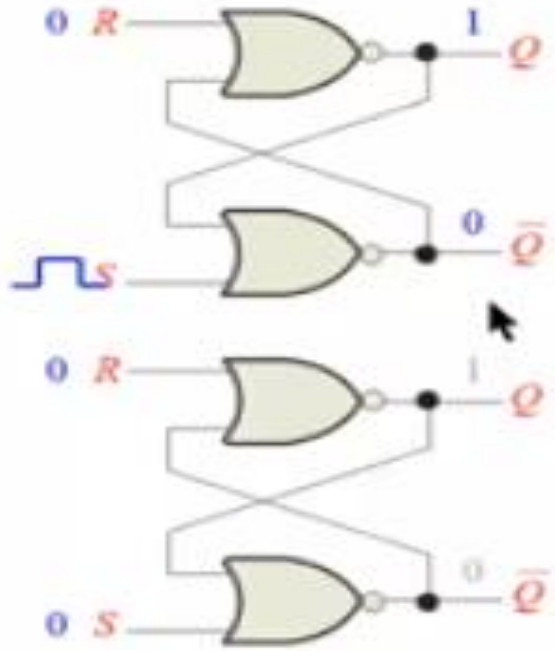
NAND Active-LOW Latch

Active-HIGH S-R Latch

The active-HIGH *S*-*R* latch is in a stable (latched) condition when both inputs are LOW.

Assume the latch is initially RESET ($Q = 0$) and the inputs are at their inactive level (0). To SET the latch ($Q = 1$), a momentary HIGH signal is applied to the *S* input while the *R* remains LOW.

To RESET the latch ($Q = 0$), a momentary HIGH signal is applied to the *R* input while the *S* remains LOW.



Active-HIGH S-R Latch

Truth Table:

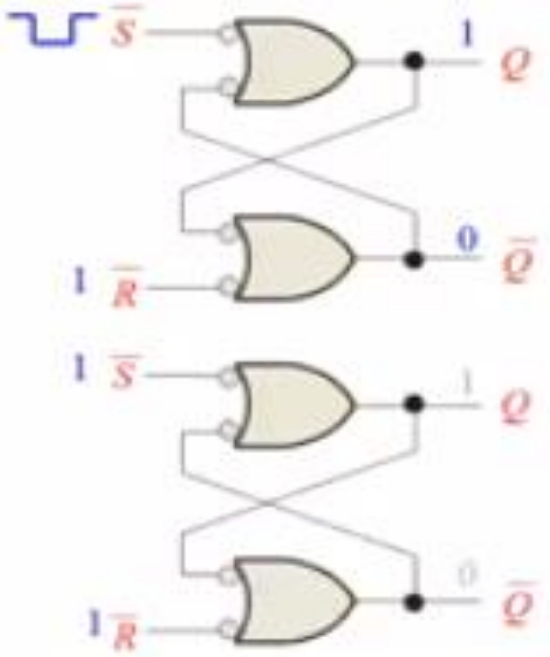
INPUTS		OUTPUTS		COMMENTS
S	R	Q	$\overline{Q}$	
0	0	Qo	$\overline{Qo}$	No change
1	0	1	0	SET
0	1	0	1	RESET
1	1	1	1	Invalid State

Active-LOW S-R Latch

The active-LOW $\overline{S}$-$\overline{R}$ latch is in a stable (latched) condition when both inputs are HIGH.

Assume the latch is initially RESET ($Q = 0$) and the inputs are at their inactive level (1). To SET the latch ($Q = 1$), a momentary LOW signal is applied to the $\overline{S}$ input while the $\overline{R}$ remains HIGH.

To RESET the latch a momentary LOW is applied to the $\overline{R}$ input while $\overline{S}$ is HIGH.



Active-LOW S-R Latch

Truth Table:

INPUTS		OUTPUTS		COMMENTS
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	
1	1	Qo	$\overline{Qo}$	No change
0	1	1	0	SET
1	0	0	1	RESET
0	0	1	1	Invalid State

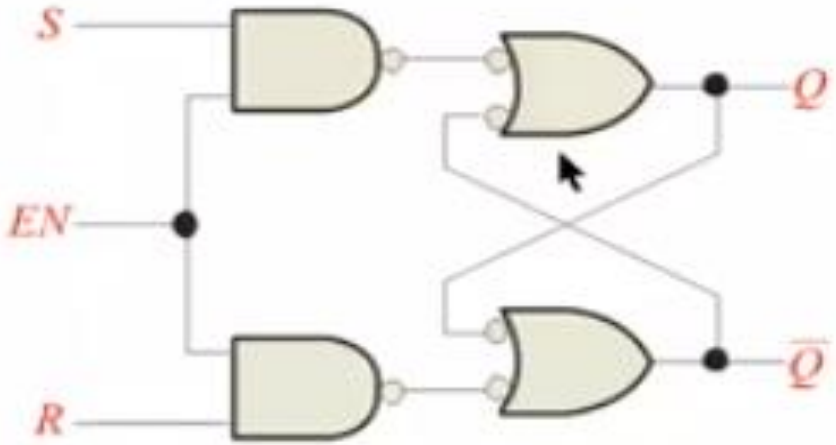
The Gated S-R Latch

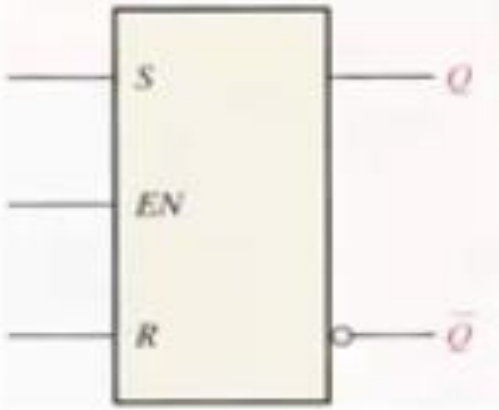
A gated S-R Latch is a variation on the basic S-R Latch.

The S and R inputs control the state to which the latch will go when a HIGH level is applied to the *EN* input.

The latch will not change until *EN* is HIGH

As long as it remains HIGH, the output is controlled by the state of the *S* and *R* inputs.





The Gated S-R Latch

Truth Table:

INPUTS			OUTPUTS		COMMENTS
S	R	EN	Q	$\overline{Q}$	
0	0	1	Qo	$\overline{Qo}$	No change
1	0	1	1	0	SET
0	1	1	0	1	RESET
1	1	1	1	1	Invalid State
X	X	0	Qo	$\overline{Qo}$	No change

The Gated S-R Latch

EXAMPLE 7–2

Determine the *Q* output waveform if the inputs shown in Figure 7–9(a) are applied to a gated S-R latch that is initially RESET.

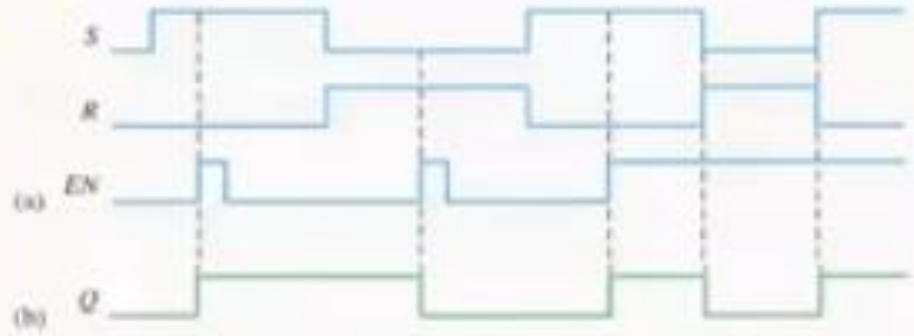
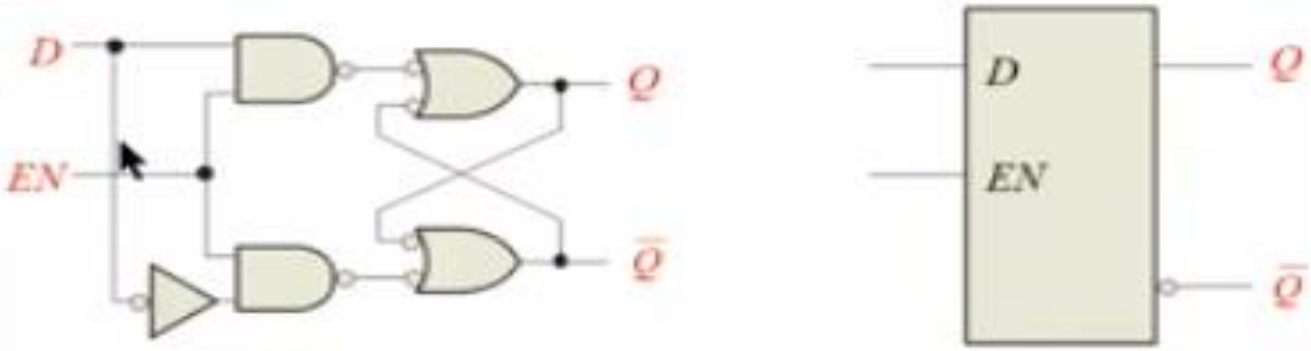


FIGURE 7–9

The *Q* waveform is shown in Figure 7–9(b). When *S* is HIGH and *R* is LOW, a HIGH on the *EN* input sets the latch. When *S* is LOW and *R* is HIGH, a HIGH on the *EN* input resets the latch.

The Gated D-Latch

The D latch is an variation of the S-R latch but combines the S and R inputs into a single D input as shown:



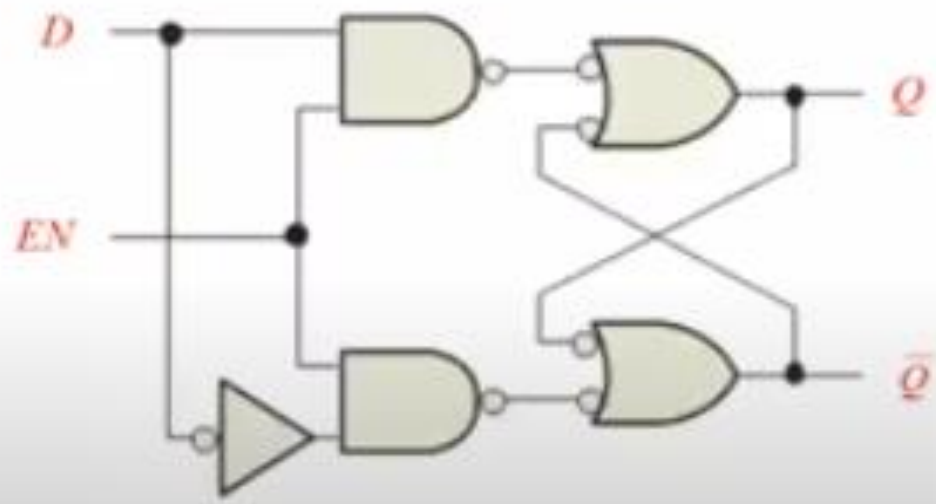
A simple rule for the D latch is:

Q follows D when the Enable is active.

The Gated D-Latch

Operation:

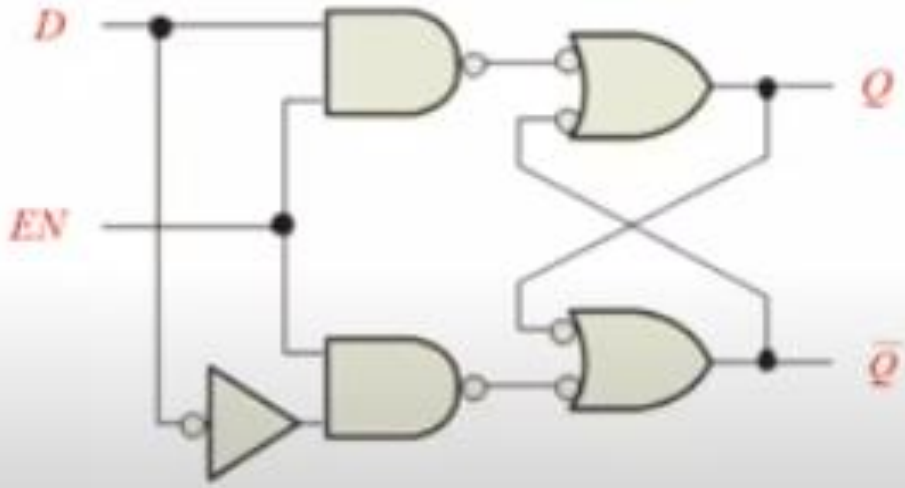
Assume the latch is initially RESET ($Q = 0$) and the inputs are at their inactive level (0). To SET the latch ($Q = 1$), a momentary HIGH signal is applied to the D input.



The Gated D-Latch

Operation:

To RESET the latch ($Q = 0$), a momentary LOW signal is applied to the D input of the latch.



The Gated D-Latch

The truth table for the *D* latch summarizes its operation. If *EN* is LOW, then there is no change in the output and it is latched.

INPUTS		OUTPUTS		COMMENTS
D	EN	Q	$\overline{Q}$	
X	0	Qo	$\overline{Qo}$	No change
1	1	1	0	SET
0	1	0	1	RESET

The Gated D-Latch

EXAMPLE 7–3

Determine the *Q* output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.

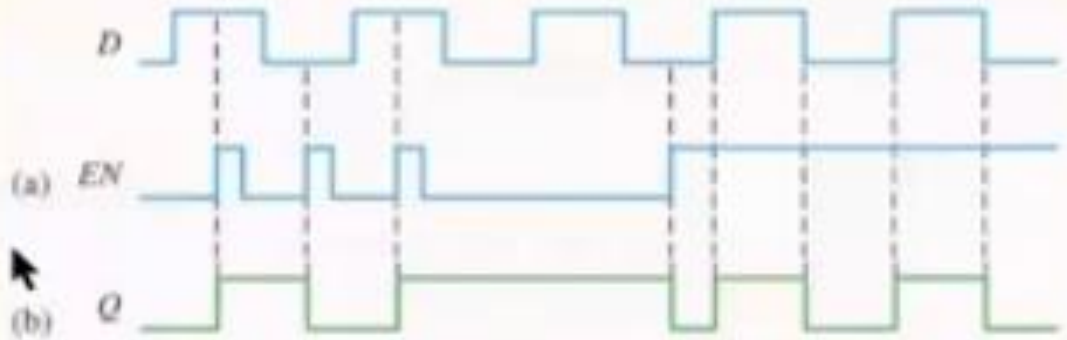


FIGURE 7–11

The *Q* waveform is shown in Figure 7–11(b). When *D* is HIGH and *EN* is HIGH, *Q* goes HIGH. When *D* is LOW and *EN* is HIGH, *Q* goes LOW. When *EN* is LOW, the state of the latch is not affected by the *D* input.

FLIP FLOP

Flip-Flops

Flip-flops are synchronous bistable devices.

The term synchronous means that the output changes state only at specified point on triggering of input called **clock** (CLK).

CLK is designated as a control input **C**.

This means that changes in output occur in synchronization with the clock.

Flip-Flops

Flip-flops are synchronous bistable devices.

The basic difference between latches and flip-flops is in the method used for changing their state.

CLK is designated as a control input **C**.

This means that changes in output occur in synchronization with the clock.

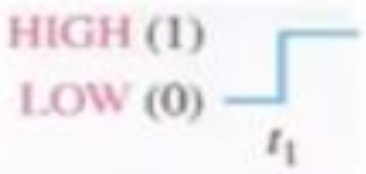
Edge-Triggered Flip-Flop

An edge-triggered FF changes state at active edge.

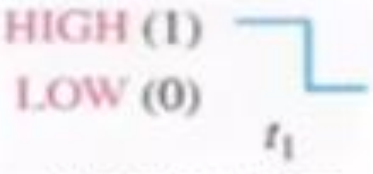
An active edge can be of two types:

Positive edge triggered (rising edge).

Negative edge triggered (falling edge).

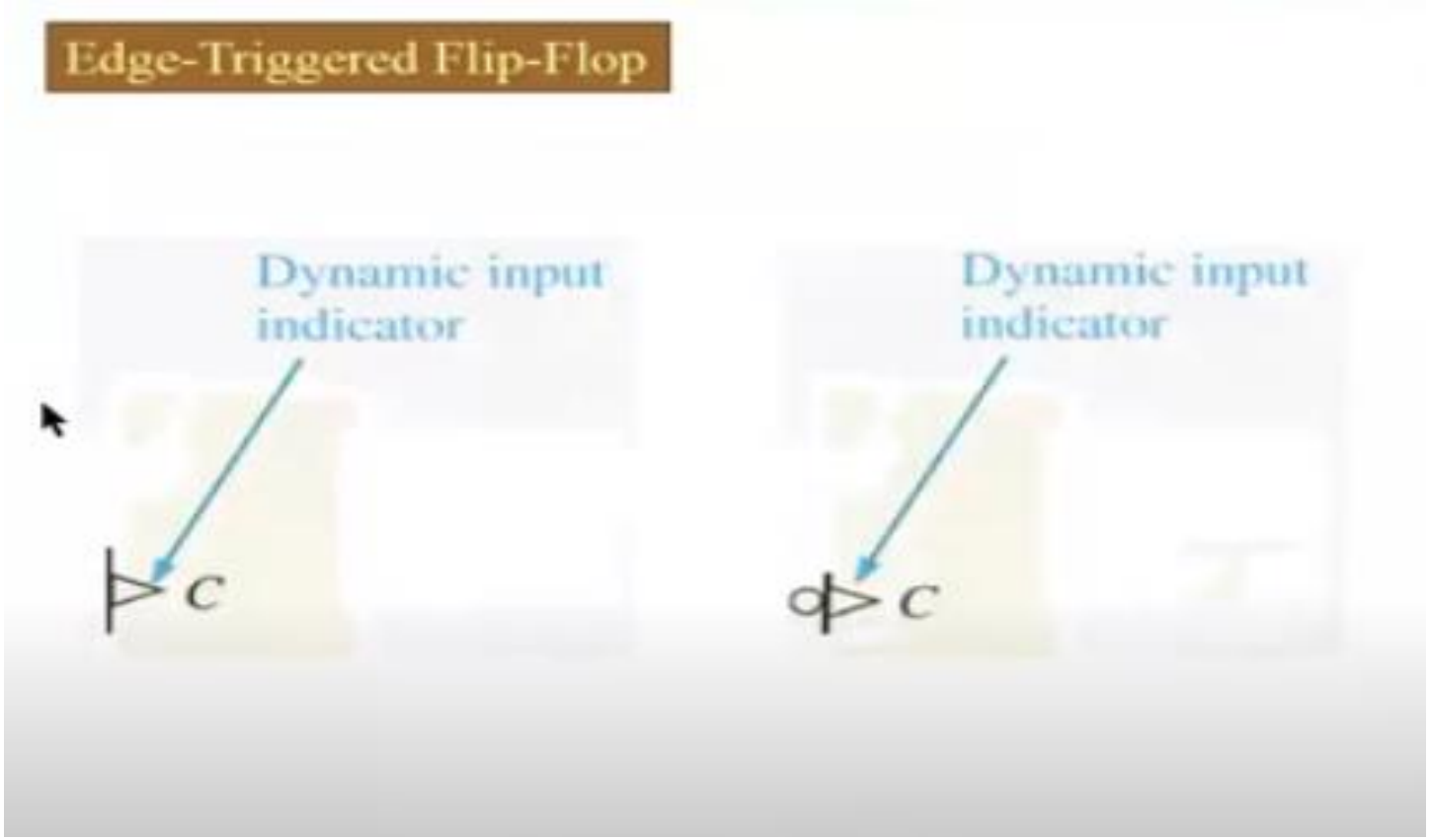


Positive Edge



Negative Edge

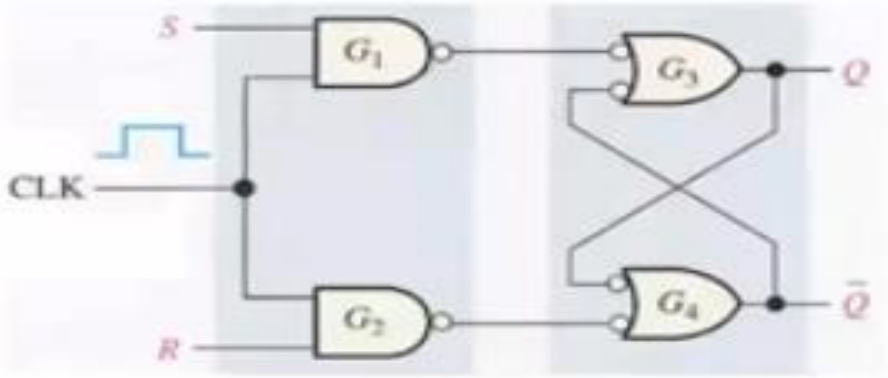
Edge-Triggered Flip-Flop



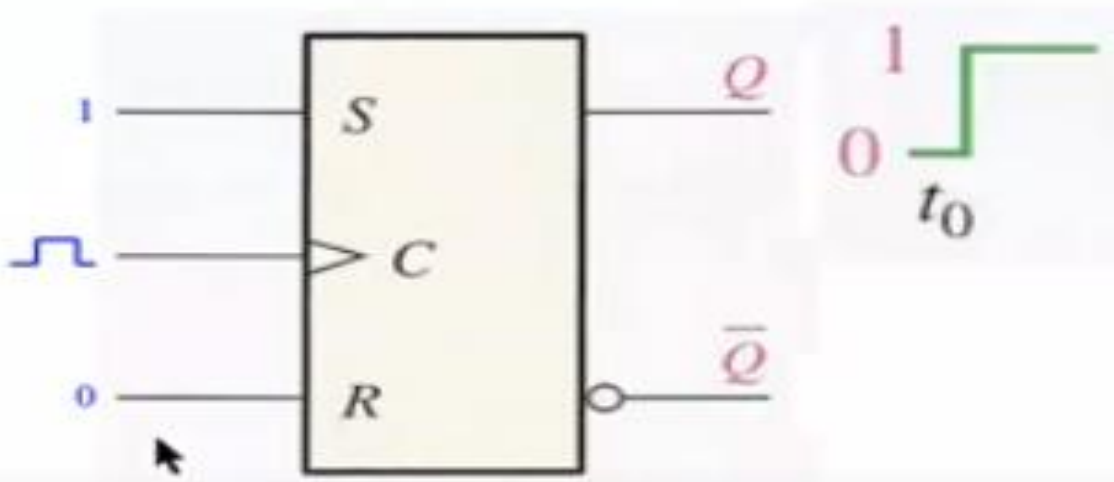
The Edge-Triggered S-R Flip-Flop

The S and R inputs of the **S-R flip-flop** are called **synchronous** inputs

Data on these inputs are transferred to the FF's output only on the triggering edge of the clock pulse

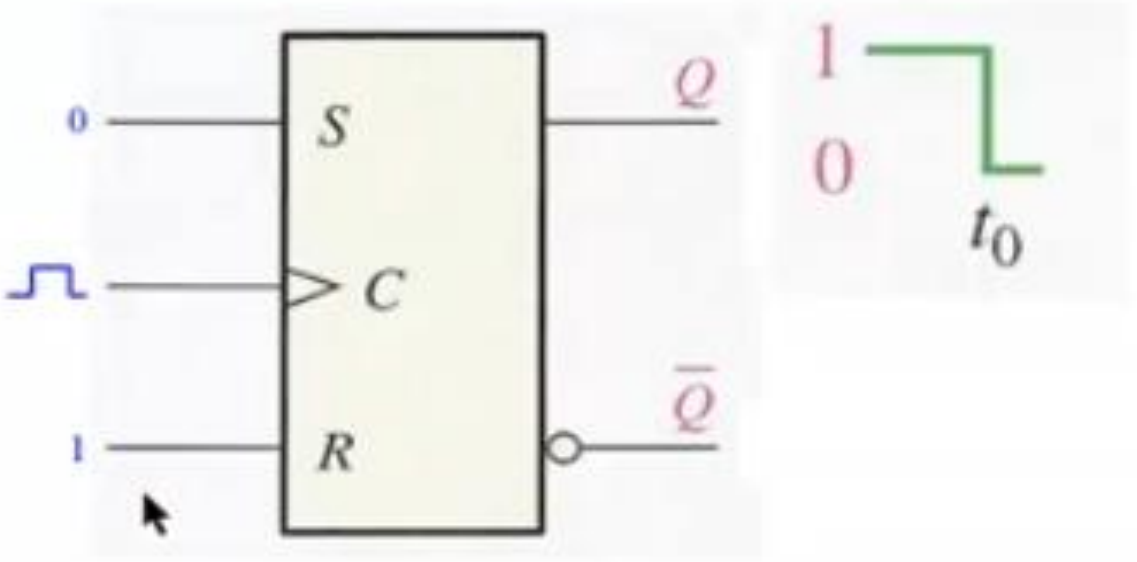


The Edge-Triggered S-R Flip-Flop



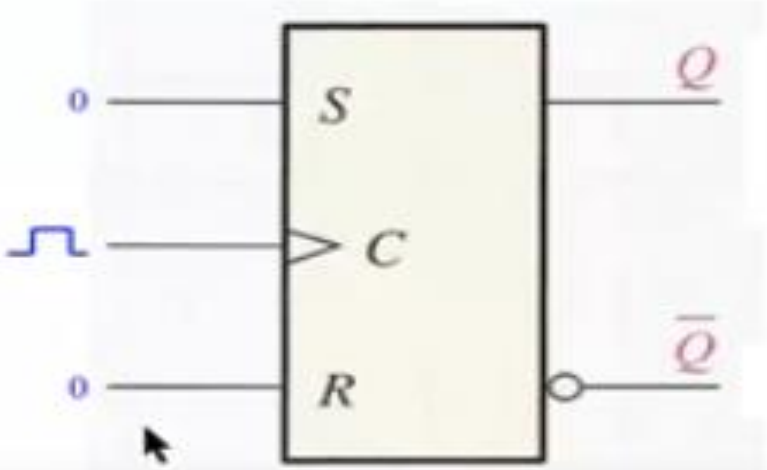
S=1, R=0 flip-flop SETS on positive clock edge.

The Edge-Triggered S-R Flip-Flop



S=0, R=1 flip-flop RESETS on positive clock edge.

The Edge-Triggered S-R Flip-Flop



Q_0 (no change)

S=0, R=0 flip-flop does not change.

The Edge-Triggered S-R Flip-Flop

INPUTS			OUTPUTS		
S	R	CLK	Q	$\overline{Q}$	COMMENTS
0	0	X	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	?	?	Invalid

↑ = clock transition LOW to HIGH

X = irrelevant ("don't care")

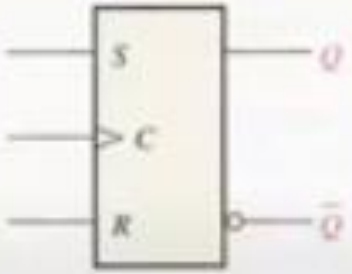
Q_0 = output level prior to clock transition

The Edge-Triggered S-R Flip-Flop

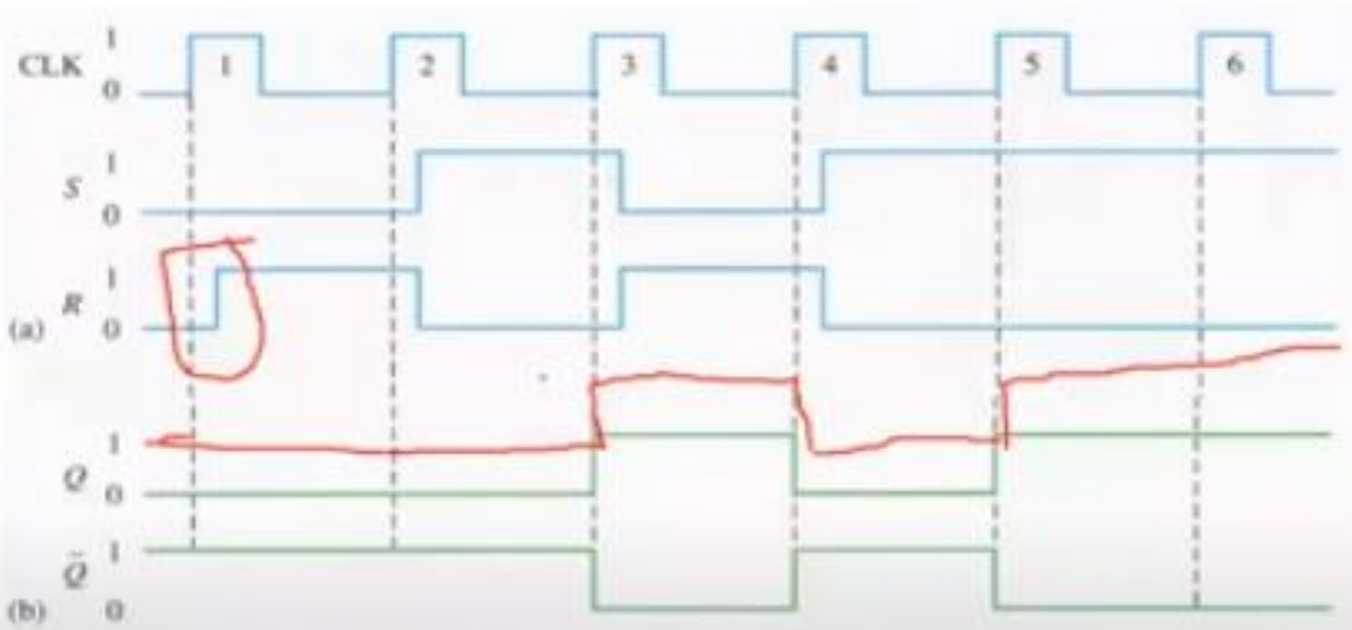
EXAMPLE 7–4

Determine the Q and $\bar{Q}$ output waveforms of the flip-flop in Figure 7–15 for the S, R, and CLK inputs in Figure 7–16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

FIGURE 7–15



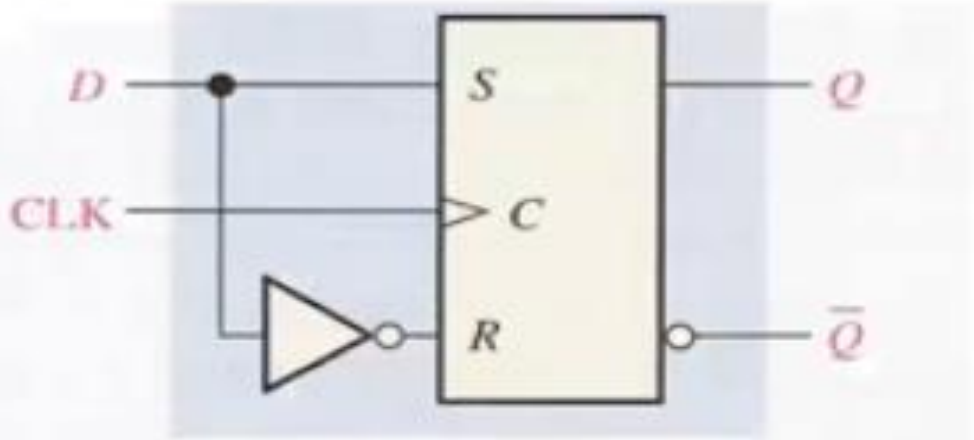
The Edge-Triggered S-R Flip-Flop



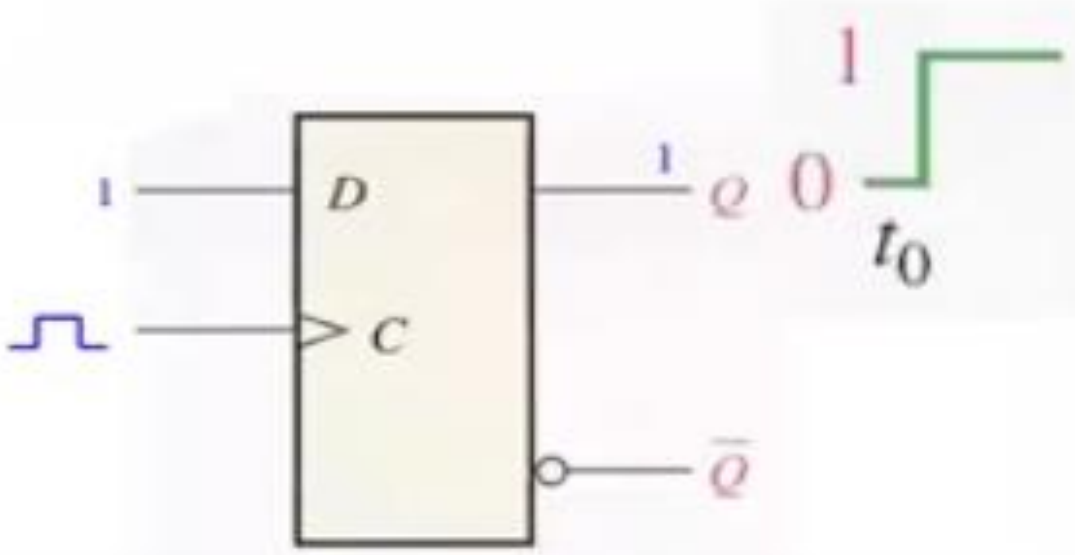
The Edge-Triggered D Flip-Flop

The **D flip-flop** is useful when a single data bit (1 or 0) is to be stored.

The addition of an inverter to an S-R flip-flop creates a basic D flip-flip as shown in figure below.



The Edge-Triggered D Flip-Flop



D=1, flip-flop SETS on positive clock edge.

The Edge-Triggered D Flip-Flop

EXAMPLE 7–5

Given the waveforms in Figure 7–21(a) for the *D* input and the clock, determine the *Q* output waveform if the flip-flop starts out RESET.

The Edge-Triggered J-K Flip-Flop

The **J-K flip-flop** is versatile and is a widely used type of flip-flop.

The functioning of the J-K flip-flop is identical to that of the S-R flip-flop for following conditions:

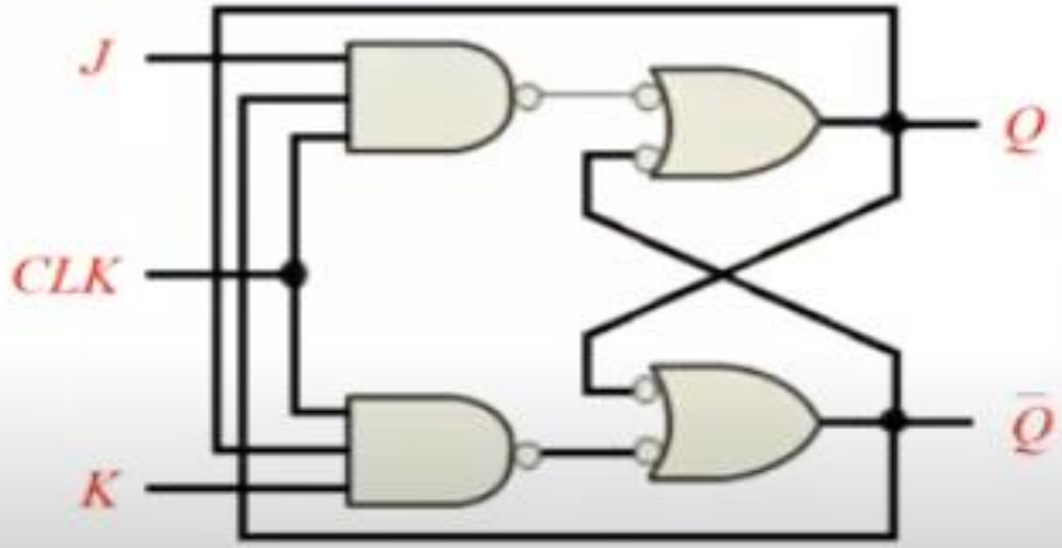
- SET
- RESET
- No-change

The difference is that it has no invalid state as in S-R flip-flop.

The two inputs are labeled ***J*** and ***K*** in honor of Jack Kilby, the person who invented the integrated circuit.

The Edge-Triggered J-K Flip-Flop

Figure below shows the basic internal logic diagram for a positive edge-triggered J-K flip-flip.



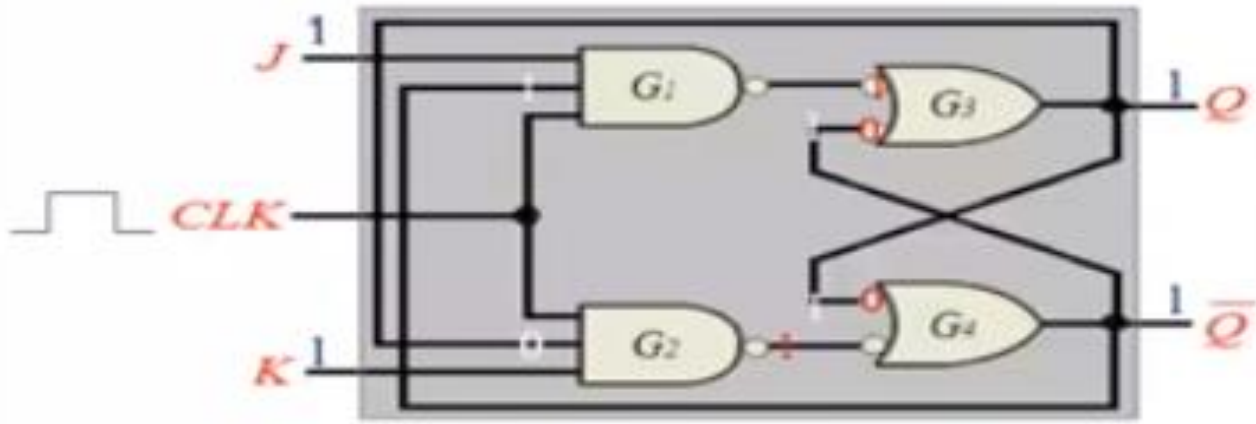
The Edge-Triggered J-K Flip-Flop

OPERATION:

The functioning of SET, RESET and No-change states remains same as of S-R flip-flop.

Lets examine the toggle operation:

Assume that J-K FF is in Reset state.



The Edge-Triggered J-K Flip-Flop

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

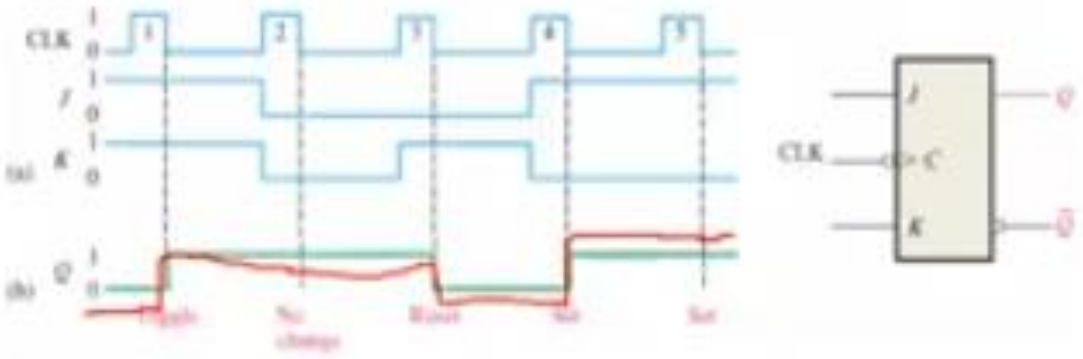
↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

The Edge-Triggered J-K Flip-Flop

EXAMPLE 7–6

The waveforms in Figure below are applied to the *J*, *K*, and clock inputs as indicated. Determine the *Q* output, assuming that the flip-flop is initially RESET.



Asynchronous Preset and Clear Inputs

For the flip-flops just discussed, the S-R, D and J-K inputs are called synchronous inputs.

Data on these inputs is transferred to the flip-flop's output only on the triggering edge of the clock pulse.

In other words, data is transferred synchronously with the clock.

Most integrated circuit flip-flops also have **asynchronous** inputs.

These are inputs that affect the state of the flip-flop *independent of the clock.*

Asynchronous Preset and Clear Inputs

They are normally labeled **preset** (*PRE*) and **clear** (*CLR*), or *direct set* (*SD*) and *direct reset* (*RD*) by some manufacturers.

An active level on the preset (*PRE*) input will set the flip-flop.

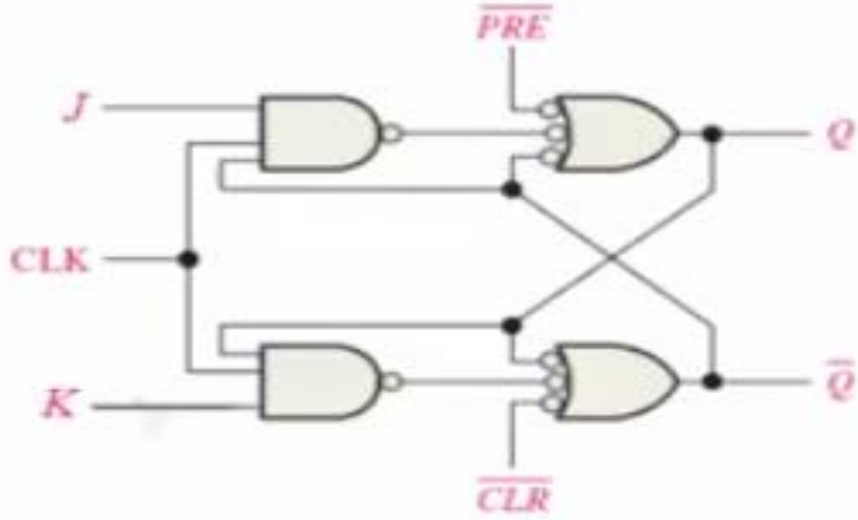
An active level on the clear (*CLR*) input will reset it.

These preset and clear inputs must both be kept HIGH for synchronous operation.

In normal operation, preset and clear would not be LOW at the same time.

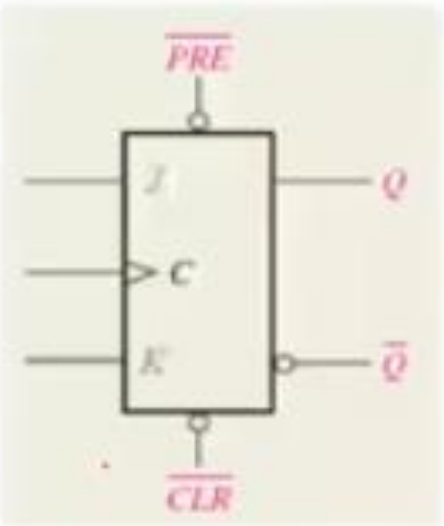
Asynchronous Preset and Clear Inputs

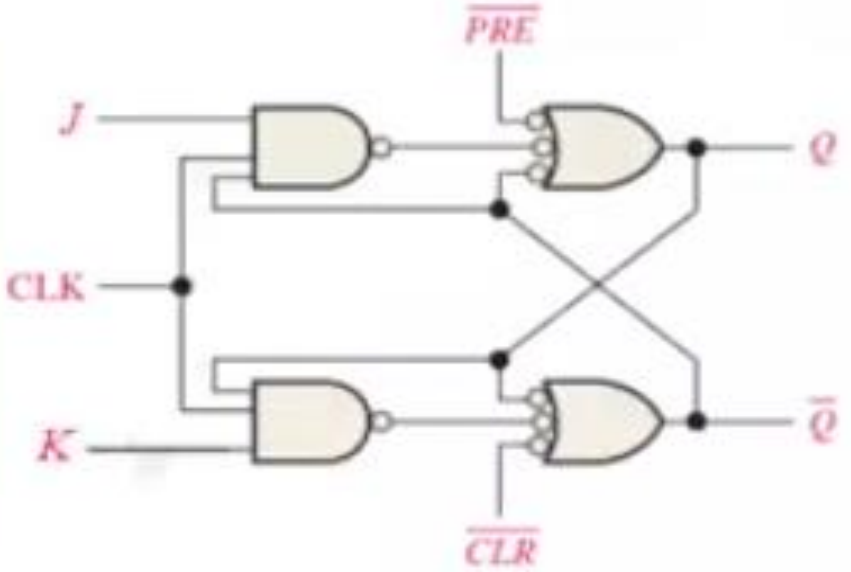
Figure below shows the logic diagram for an edge-triggered J-K Flip-Flop with active LOW preset *(PRE)* and clear *(CLR)* inputs.



Asynchronous Preset and Clear Inputs

Figure below shows the logic diagram for an edge-triggered J-K Flip-Flop with active LOW preset *(PRE)* and clear *(CLR)* inputs.

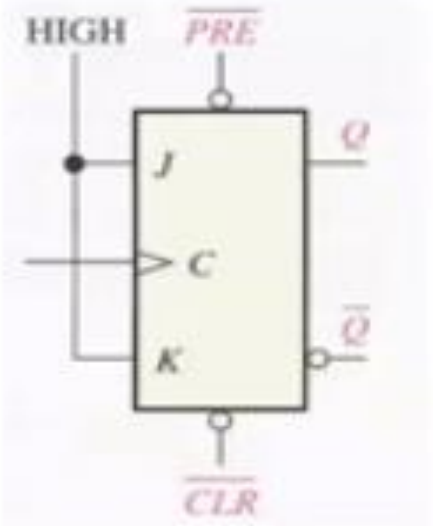




Asynchronous Preset and Clear Inputs

EXAMPLE 7–8

For the positive edge-triggered J-K flip-flop with preset and clear inputs in Figure 7–28, determine the Q output for the inputs shown in the timing diagram in part (a) if Q is initially LOW.



Asynchronous Preset and Clear Inputs

EXAMPLE 7–8

For the positive edge-triggered J-K flip-flop with preset and clear inputs in Figure 7–28, determine the Q output for the inputs shown in the timing diagram in part (a) if Q is initially LOW.