Digital Logic Design (DLD)
(Lab Task No 2)

Session (2022-2026)

Program

BS-Computer Science

Submitted By:

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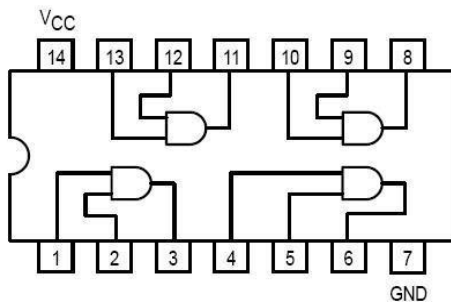
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Hazara University, Mansehra

Lab Task No 02

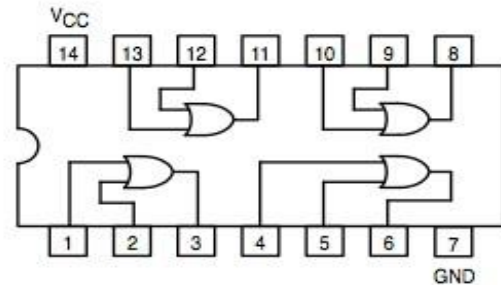### Implementation of a Circuit from Given Expressions

Objective:

To implement a circuit from given expression, make its truth table, find its minterms. Now Implement the circuit from the minterms again and verify the results with the initial given expression.
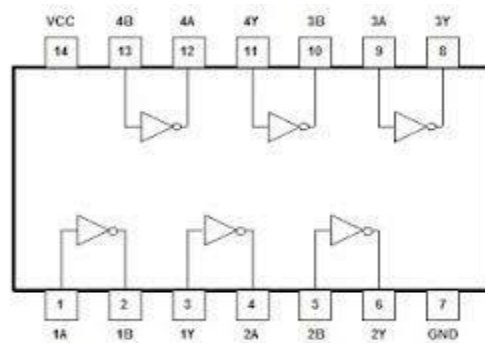
Equipment /Tool:

Trainer, 74LS32 (OR), 74LS08 (AND), 74LS04 (NOT).

Figure 1. AND Gate 7408

Figure 2. OR Gate IC 7432
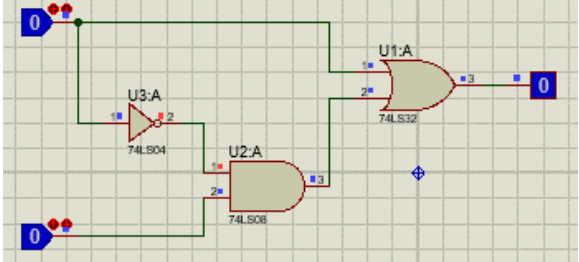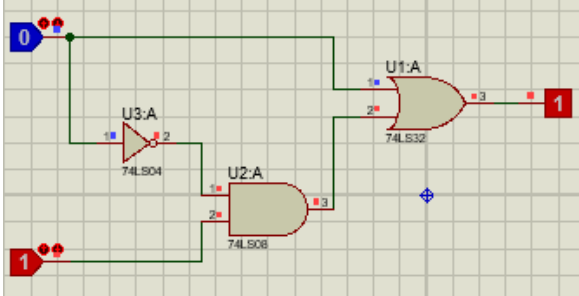

Figure 3. NOT Gate IC 7404
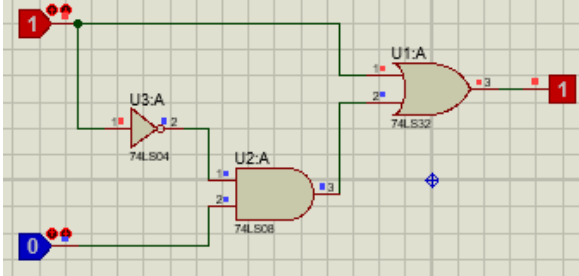
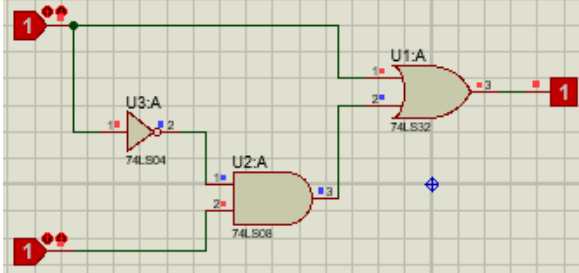# 1). F=X+X`.Y

Procedure:

Q1). From the Expression given make the circuit on the trainer using ICs mentioned and fill in the truth table.
Answer:

Truth Table With Proof:

X	Y	$\overline{X}$	$\overline{X}.Y$	F	Proof
0	0	1	0	0	
0	1	1	1	1	
1	0	0	0	1	
1	1	0	0	1	

Q2). Now find the minterms of this expression and write it on the following blank:
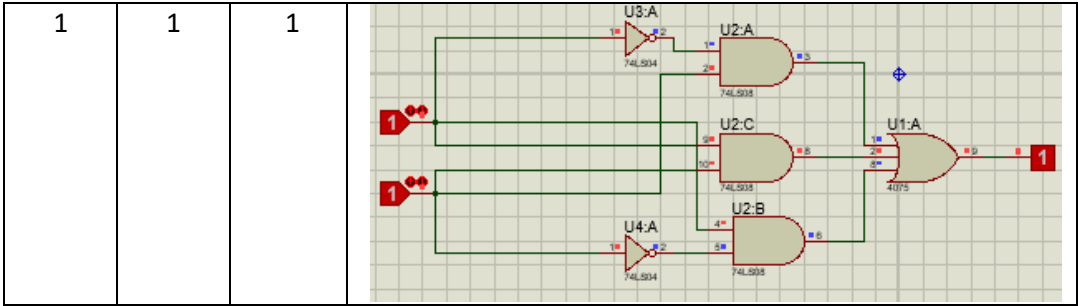
Answer:

$$F = X.Y + X.Y` + X`.Y$$

Q3). Implement the above expression on the trainer and fill the following table:
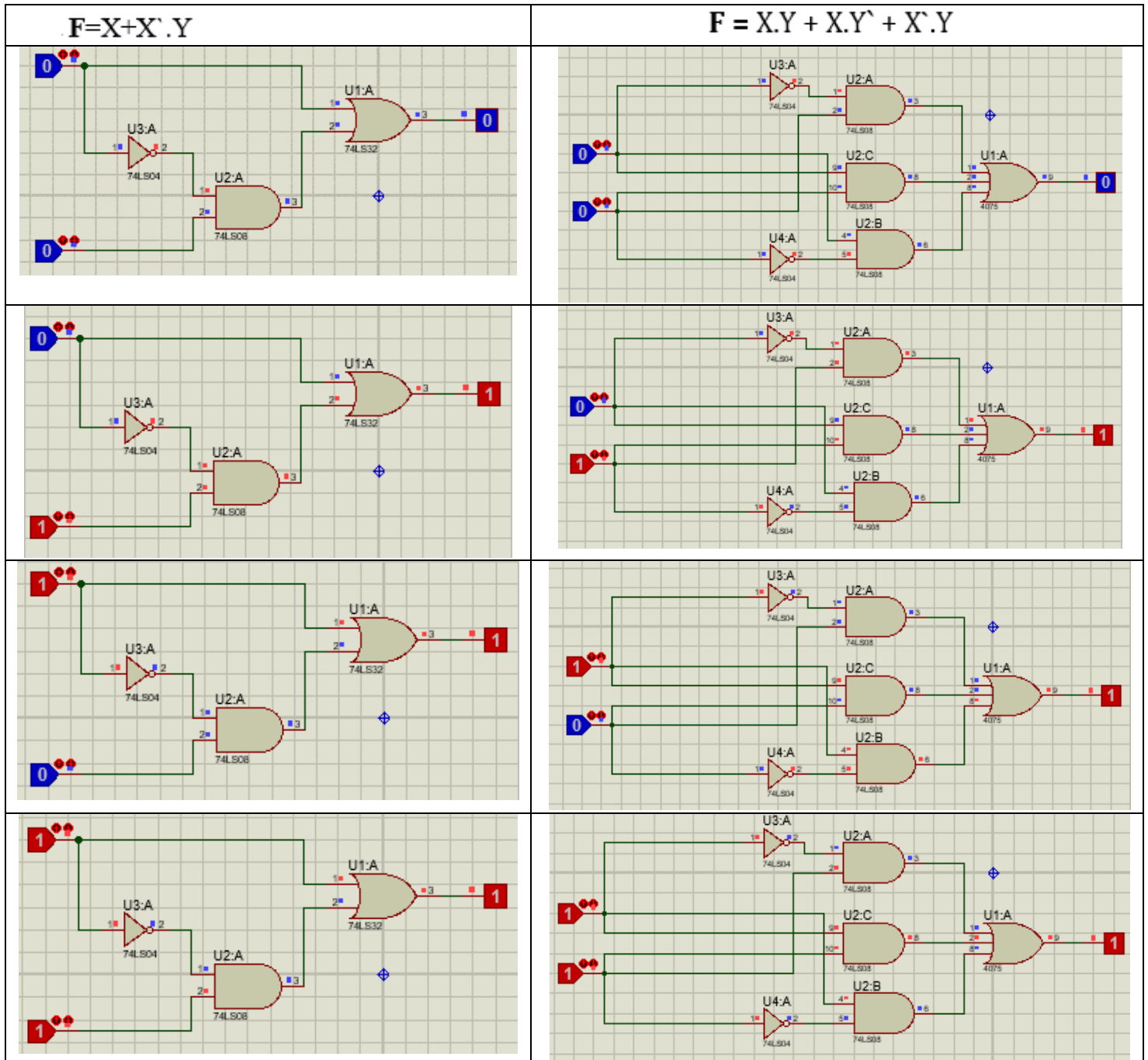
Answer:

Truth Table With Proof:

X	Y	F	Proof
0	0	0	
0	1	1	
1	0	1	

1	1	1	

Q4). Now verify the results of both the tables. Are they both the same or not? And why?

Answer:

Verifying That The Result is Same or not:

$F=X+X`.Y$	$F = X.Y + X.Y` + X`.Y$

Reason Why the Result is same:

The reason the results are the same is because the expression F = X + X'.Y is logically equivalent to the expression F = X.Y + X.Y' + X'.Y. The two expressions represent the same Boolean function, so when these fucntions are implemented on the Proteus Software or implemented on the circuit trainer, they will produce the same truth table outputs. This is because the two expressions are different ways of representing the same underlying logical operation, which is the OR of the AND of X and Y, and the AND of X and the complement of Y. Implementing either of these equivalent expressions on the circuit will yield the same results.