Digital Logic Design (DLD)
(Lab Task No 5)

Session (2022-2026)

Program

BS-Computer Science

Submitted By:

Student Name: Shaheer Ali Roll Number: 301-221044

Supervised By:

Ms. Muneeba Darwaish
Lecturer
CS& IT Department

Hazara University, Mansehra

EXPERIMENT 05:

Implementation of a 4 to 1 MUX using Gates and using IC 74LS153.

Objective:

To familiarize student with basic working of multiplexer and implementation of 4x1 mux.

Equipment / Tool:

Trainer, IC 74LS04 (NOT), 74LS32 (OR), 74LS08 (AND), 74LS153 (4 TO 1 MUX).

Background Theory:

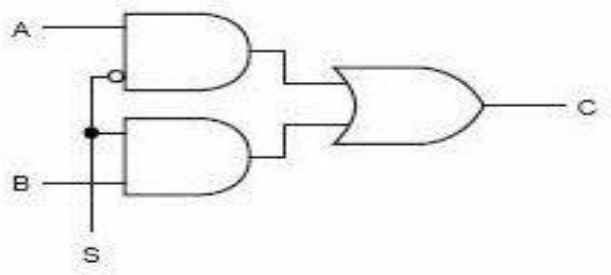
A MUX is a combinational circuit that can be used to select data and produce it at the output. They can be 2 to 1, 4 to 1, 8 to 1, 16 to 1, etc. It has a lot of applications. There are many scenarios in which we have to select a particular data and produce it at the output.

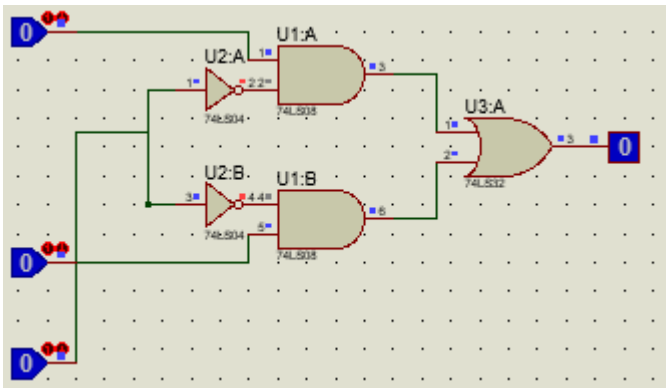
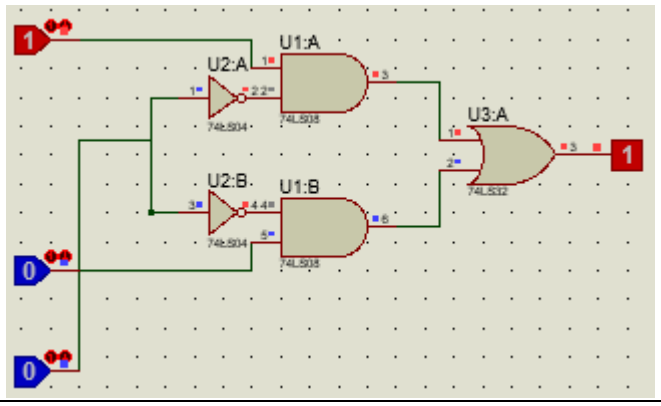
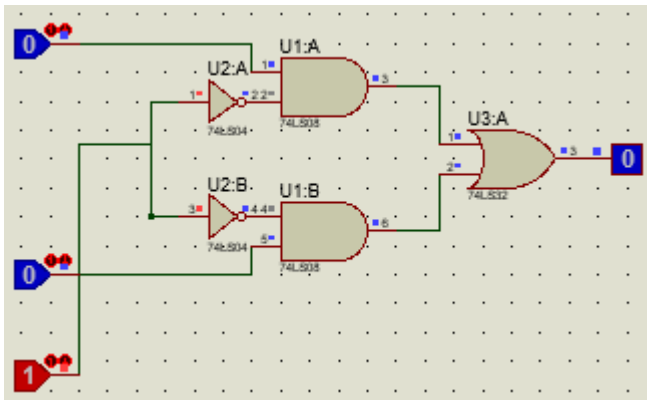
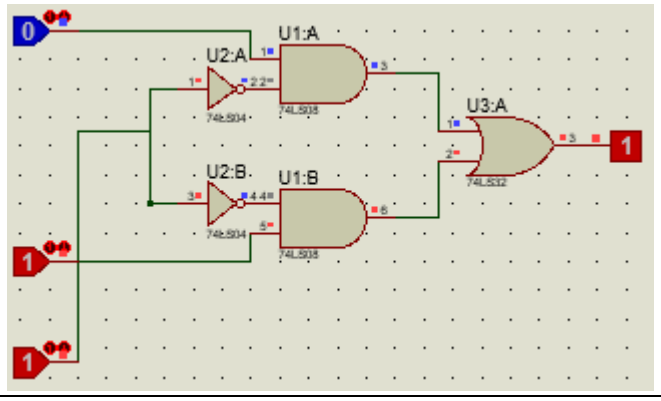
Lab Tasks:

- Write the truth table for a 2 to 1 MUX, design a circuit from it, implement it and verify the results.
- Write down the truth table for a 4 to 1 MUX, draw the circuit, implement it and verify the results.
- Use the IC 74LS153 (4 to 1 MUX) and verify the results.

Procedure

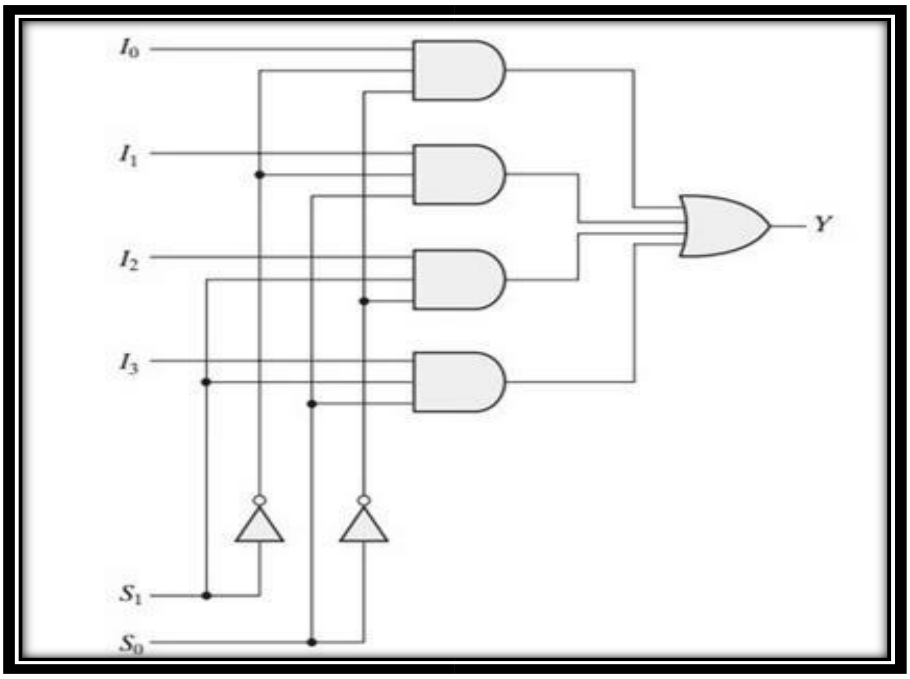
Following is the circuit for 2 to 1 MUX and truth table:



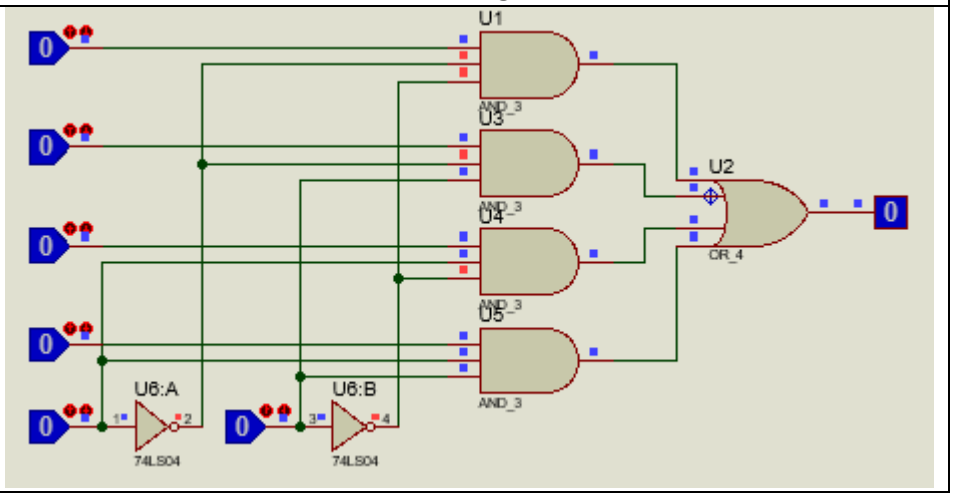
S	B	A	Y	Proof
0	X	0	0	
0	X	1	1	
1	0	X	0	
1	1	X	1	

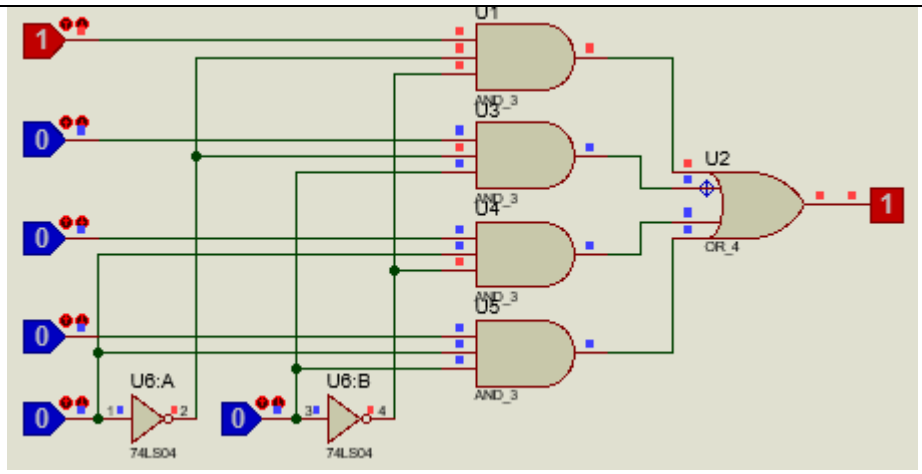
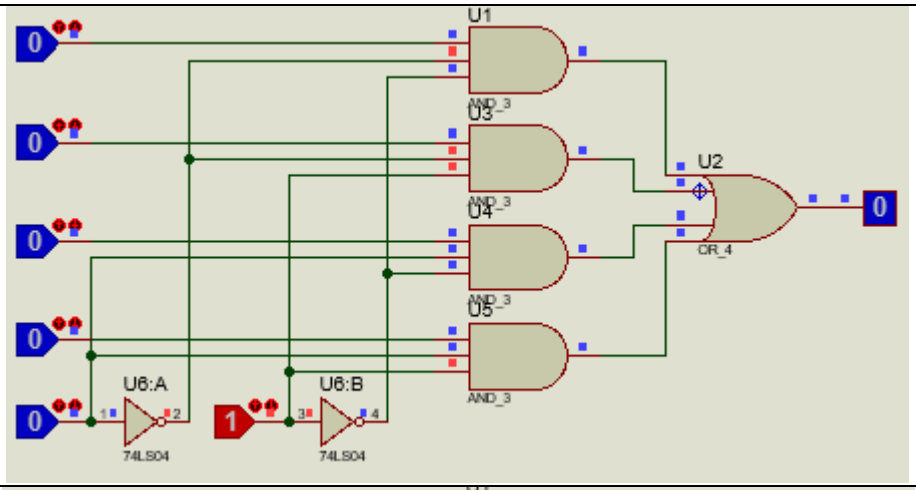
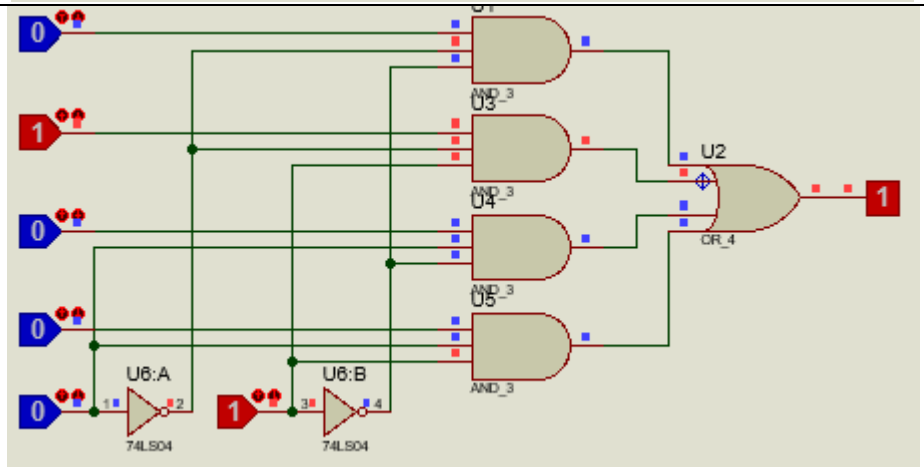
Circuit Diagrams:

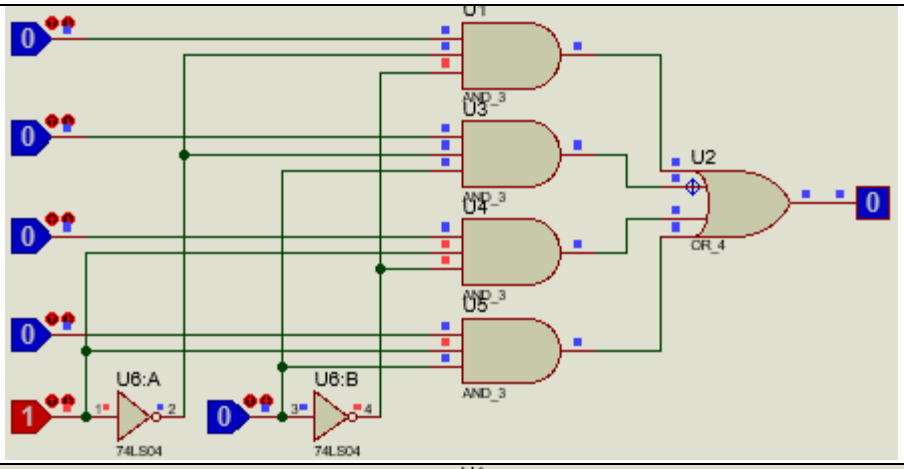
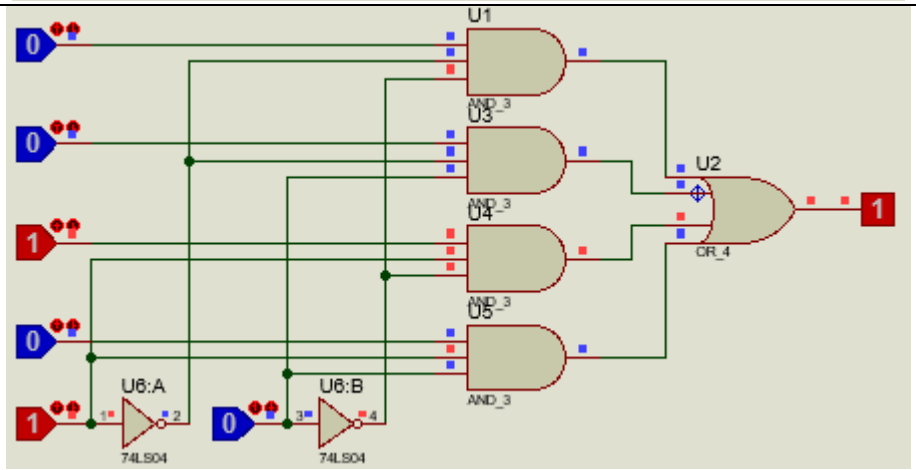
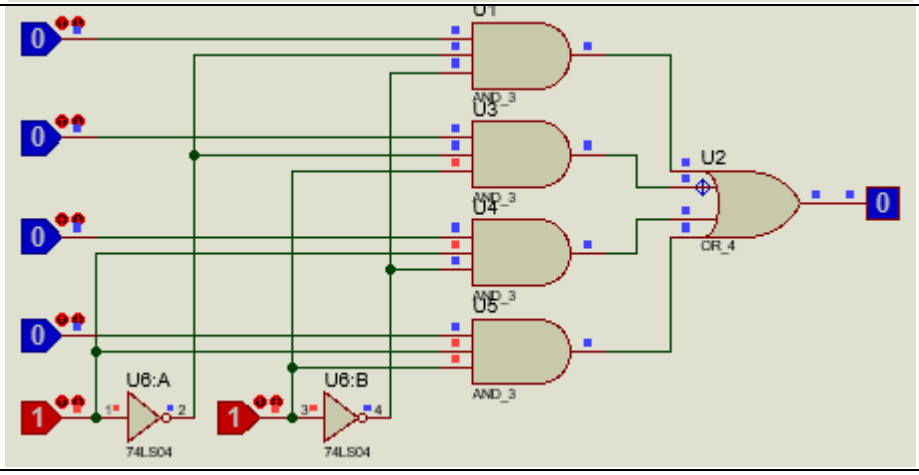
Draw the diagram of 4 to 1 MUX as follow

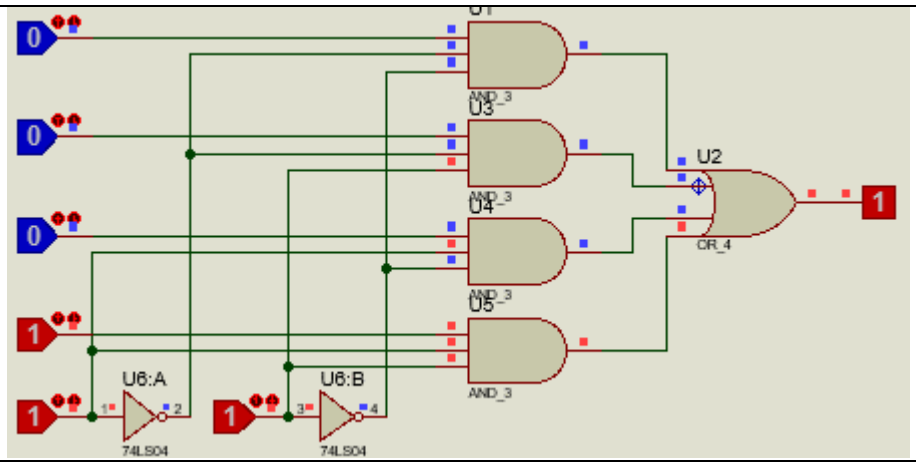


Fill in the following Truth Table:

S1	S0	L3	L2	L1	L0	Y	Proof With Circuit Diagram
0	0	X	X	X	0	0	

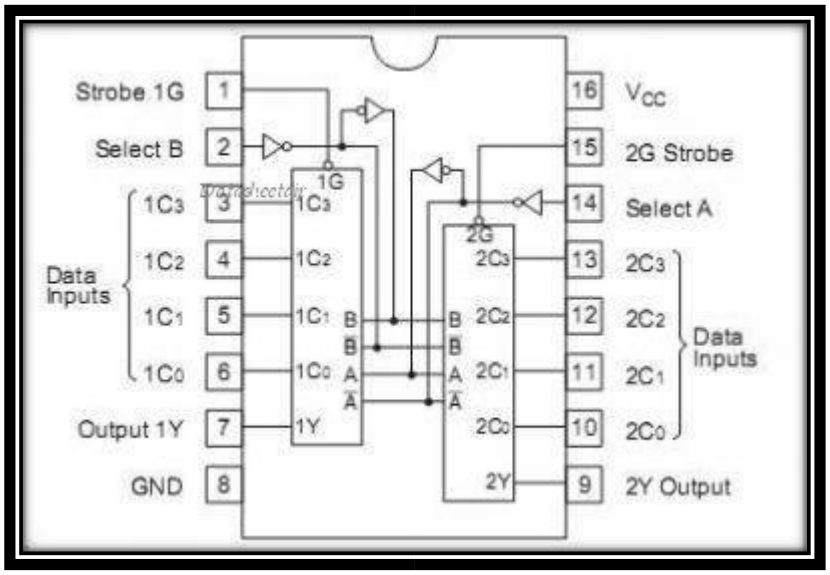
0	0	X	X	X	1	1	
0	1	X	X	0	X	0	
0	1	X	X	1	X	1	

1	0	X	0	X	X	0	
1	0	X	1	X	X	1	
1	1	0	X	X	X	0	

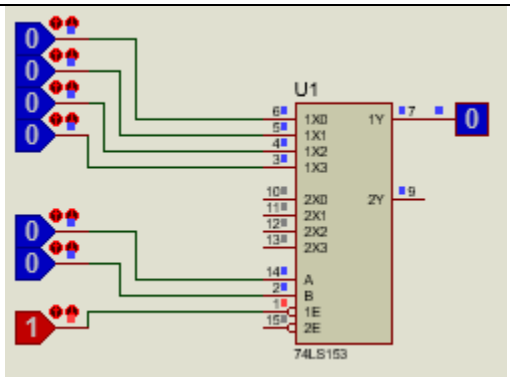
1	1	1	X	X	X	1	

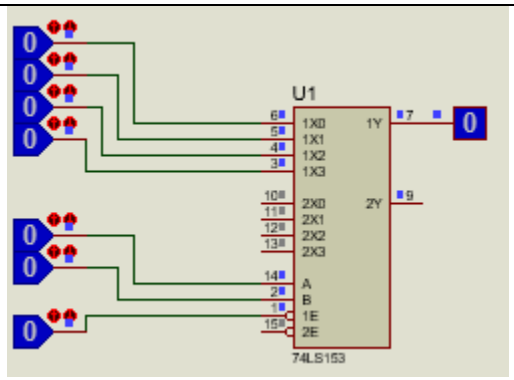
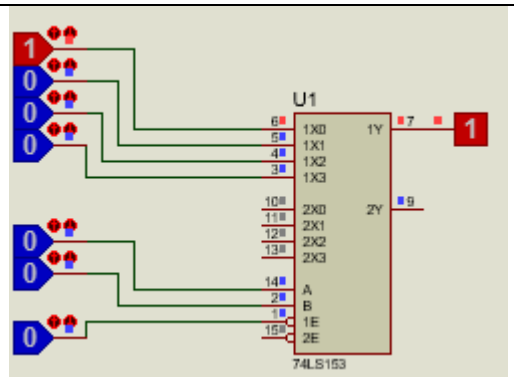
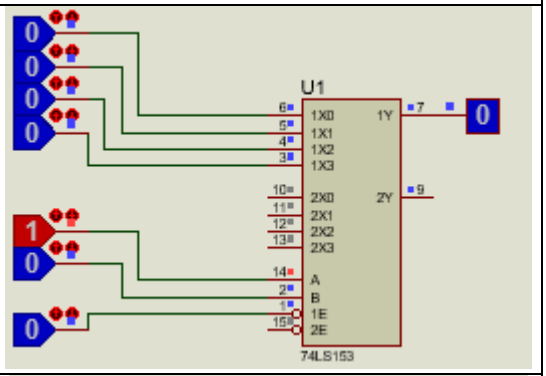
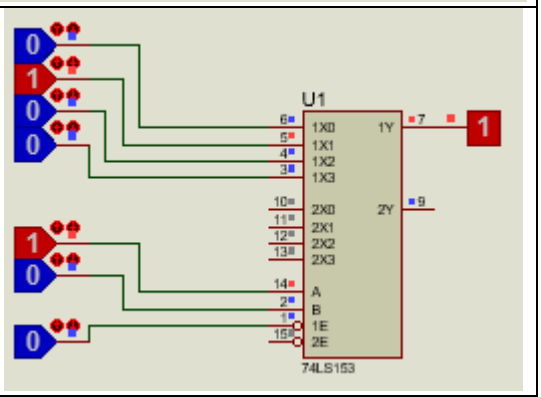
Implementing using 74LS153:

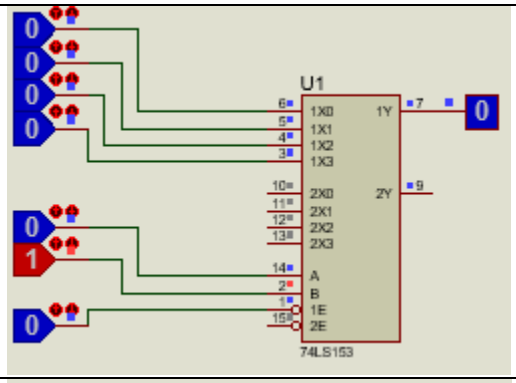
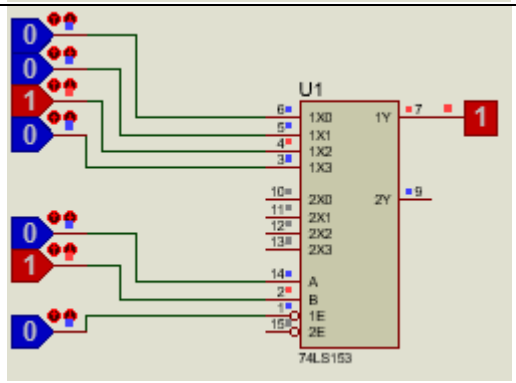
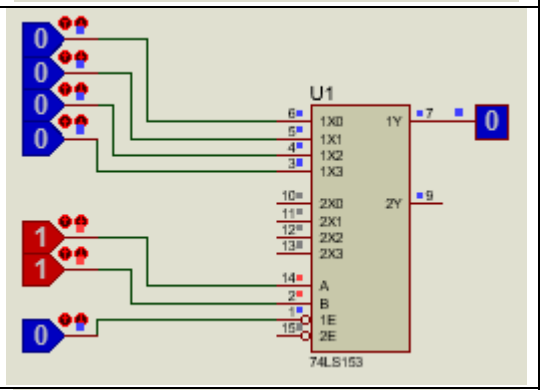
Following is the pin configuration extracted from the datasheet.
DUAL-IN-LINE Package



Function Table:

Select Inputs		Data Inputs				Strobe	Output	Proof With Circuit Diagram
B	A	C0	C1	C2	C3	G (E)	Y	
X	X	X	X	X	X	H	L	

L	L	L	X	X	X	L	L	
L	L	H	X	X	X	L	H	
L	H	X	L	X	X	L	L	
L	H	X	H	X	X	L	H	

H	L	X	X	L	X	L	L	
H	L	X	X	H	X	L	H	
H	H	X	X	X	L	L	L	
H	H	X	X	X	H	L	H