# Digital Logic Design (DLD)
# (Lab Task No 3)


Session (2022-2026)

Program

**BS-Computer Science**

Submitted By:

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**EXPERIMENT 03**

**Implementation of Basic Gates using Universal Gates**

**Objectives:**

Using two input NAND and NOR gates, construct the following

1. NOT
2. AND
3. OR

After doing this, implement the given expression on the trainer board.

**Equipment /Tool:**

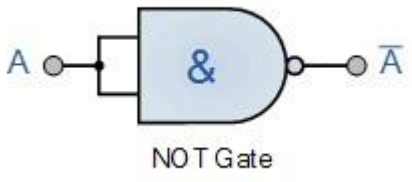
Trainer, IC 74LS00, 74LS02.

**Theory:**

NAND and NOR gates are called universal gates because we can make any basic gate from them by using the following circuits.

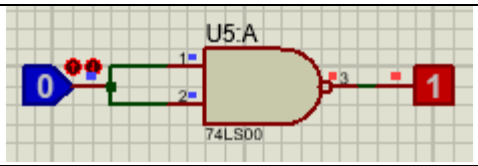
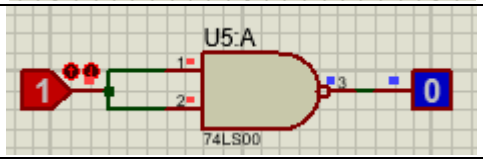
1) **Implementation of Gates using NAND Gate only: i)**

**NOT Gate Behavior:**

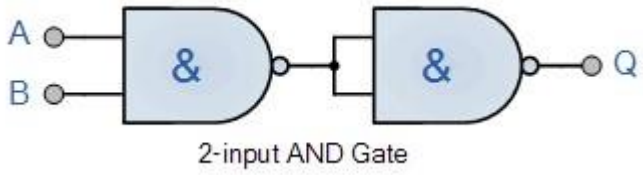


NOT Gate

## Truth Table With Proof:

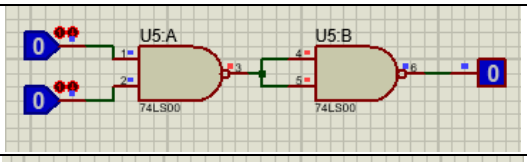
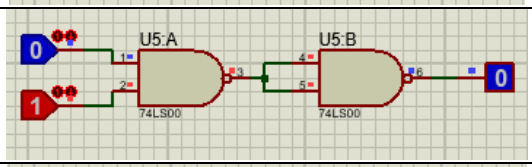
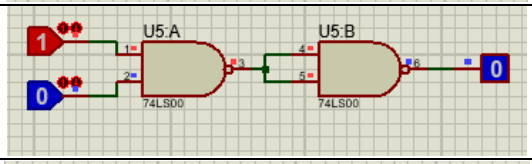
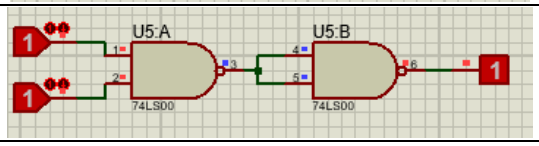
| Input | output | Proof |
|---|---|---|
| 0 | 1 |  |
| 1 | 0 |  |

**ii)** **AND Gate Behavior:**

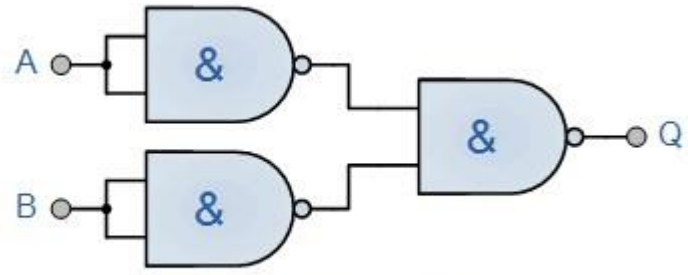


2-input AND Gate

## Truth Table With Proof:

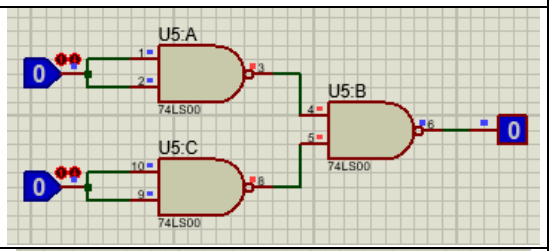
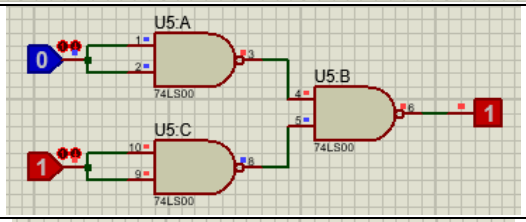
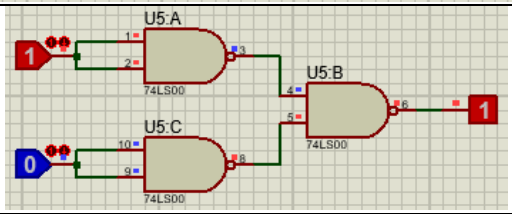
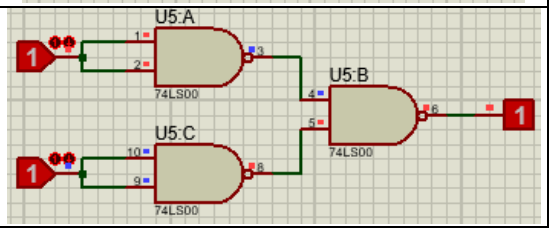
| Input | | Output | Proof |
|---|---|---|---|
| A | B | Q | |
| 0 | 0 | 0 |  |
| 0 | 1 | 0 |  |
| 1 | 0 | 0 |  |
| 1 | 1 | 1 |  |

**iii)** **OR Gate Behavior:**




2-input OR Gate

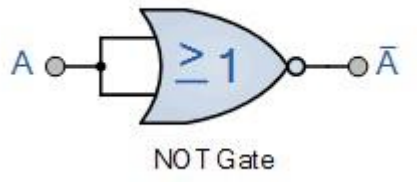
## Truth Table With Proof:

| Input | | Output | Proof |
|---|---|---|---|
| X | Y | F | |
| 0 | 0 | 0 |  |
| 0 | 1 | 1 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 1 |  |

## 2) Implementation of Gates using NOR Gate Only:

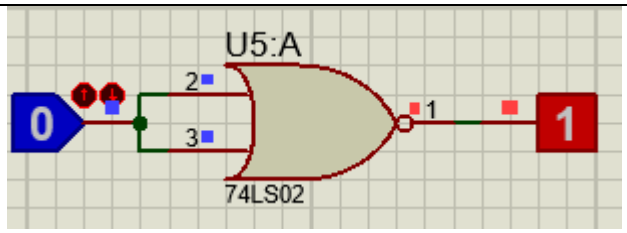
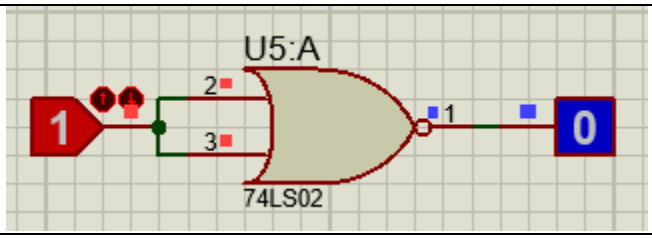
Verify all the truth tables for all the gates.

### i) NOT Gate Behavior:

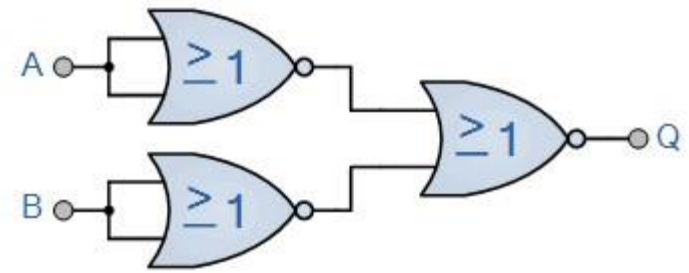


NOT Gate

## Truth Table With Proof:

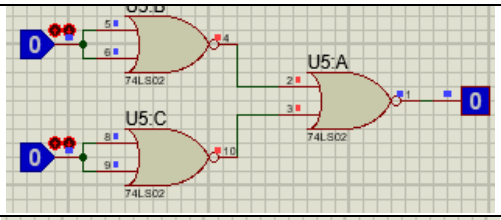
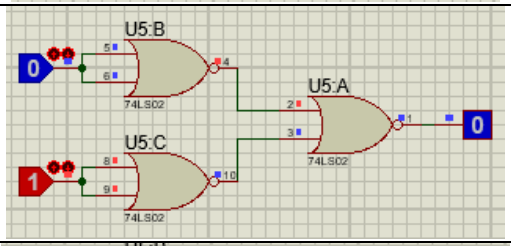
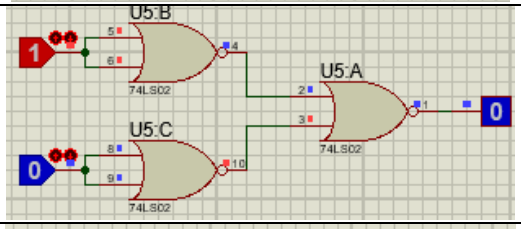
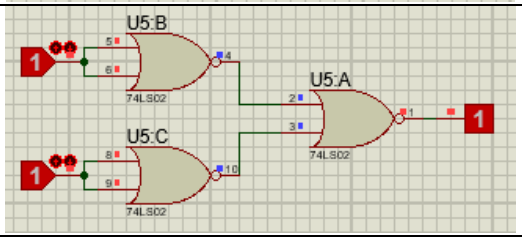
| A | A' | Proof |
|---|---|---|
| 0 | 1 |  |
| 1 | 0 |  |

**ii) <u>AND Gate Behavior:</u>**

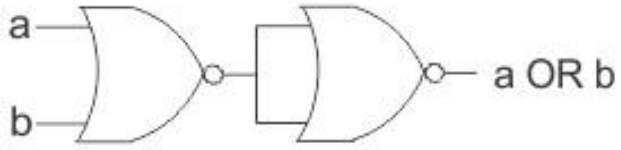



2-input AND Gate

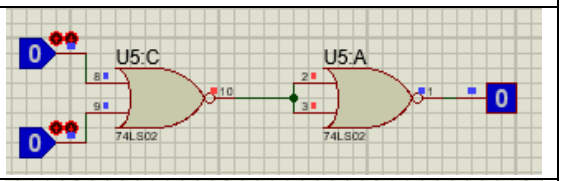
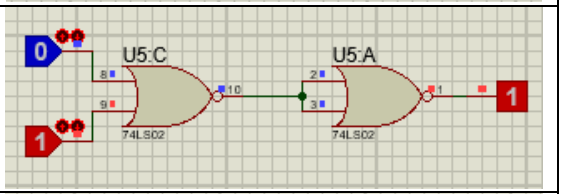
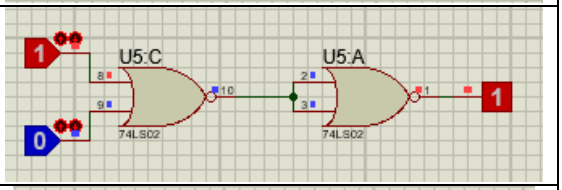
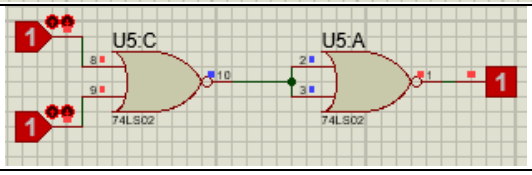
## Truth Table With Proof:

| A | B | Q | Proof |
|---|---|---|---|
| 0 | 0 | 0 |  |
| 0 | 1 | 0 |  |
| 1 | 0 | 0 |  |
| 1 | 1 | 1 |  |

## iii) OR Gate Behavior:




### Truth Table With Proof:

| A | B | F | Proof |
|---|---|---|---|
| 0 | 0 | 0 |  |
| 0 | 0 | 1 |  |
| 1 | 0 | 1 |  |
| 1 | 1 | 1 |  |

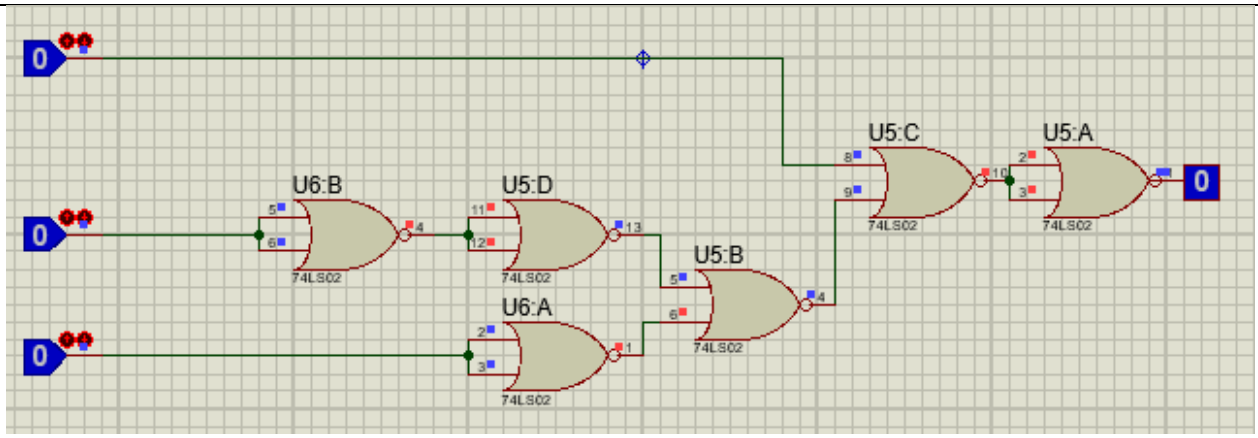
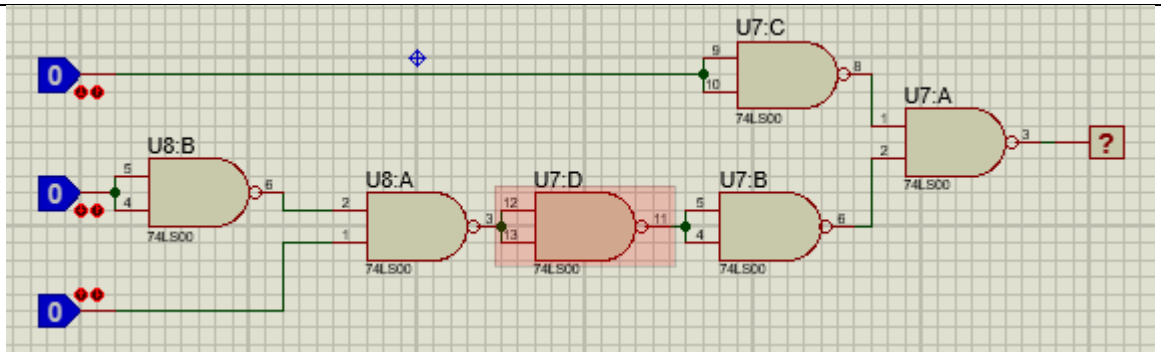
**Exercise in Lab:**

1) Implement following expression using NOR Gate only.
2) Implement following expression using NAND Gate only.

$$F=X+\overline{Y}.Z$$

**Make Circuit Diagram By Implementing Both Methods :**

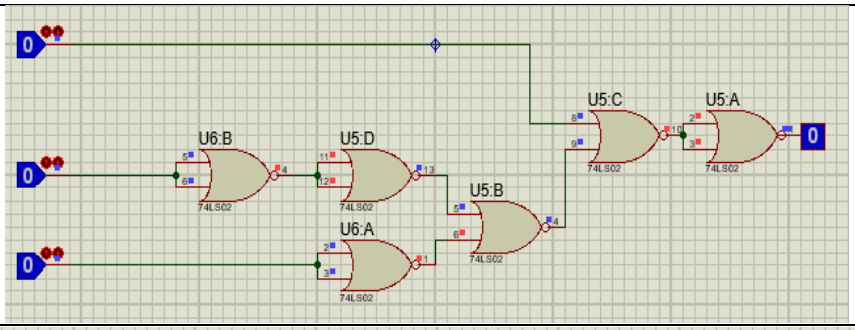
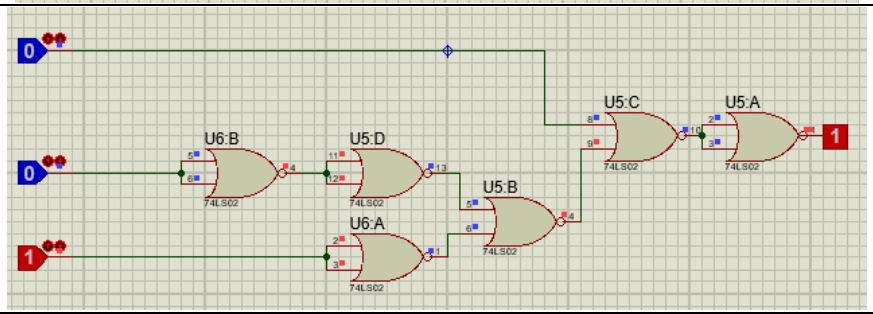
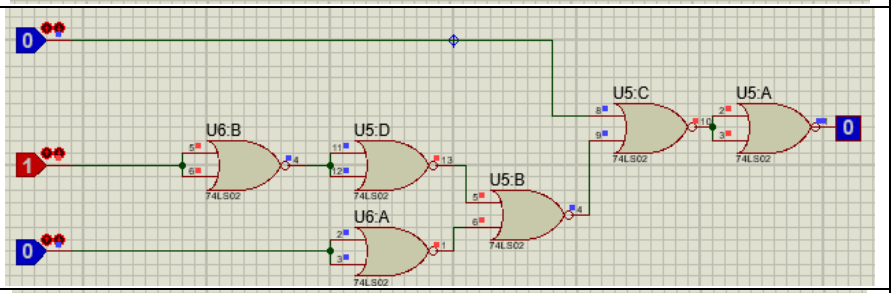
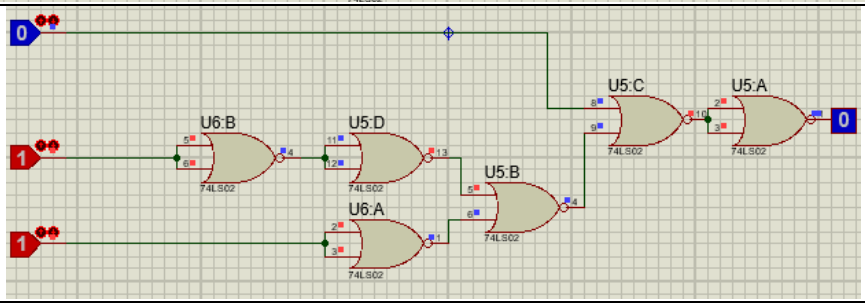
**Answer**:

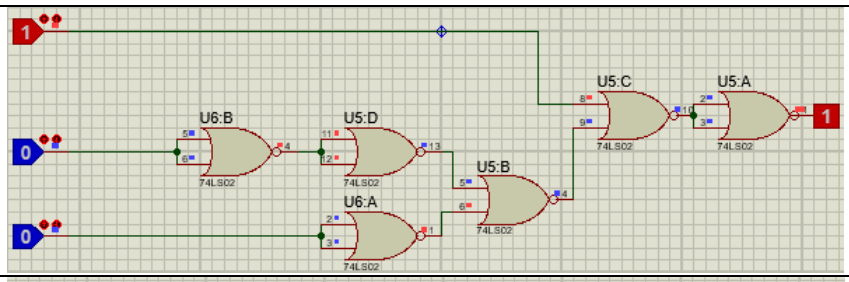
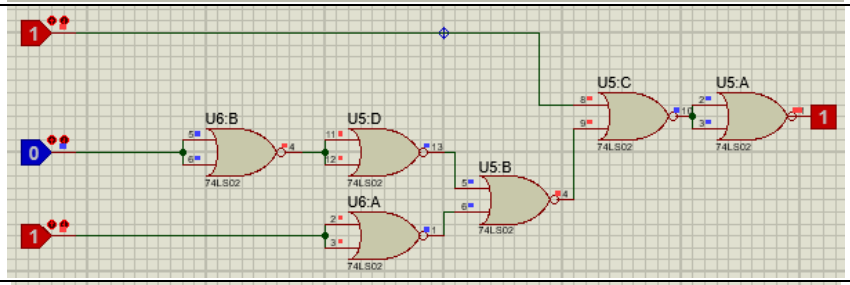
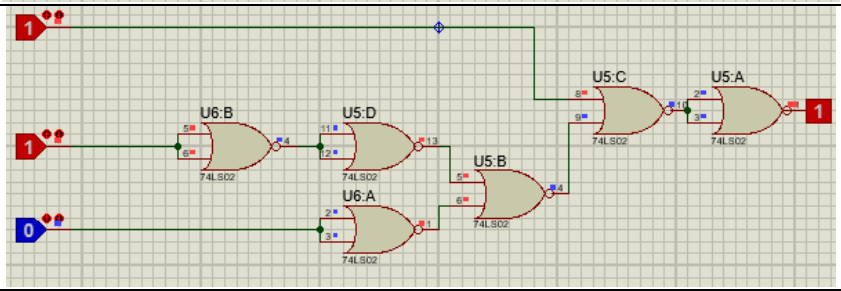
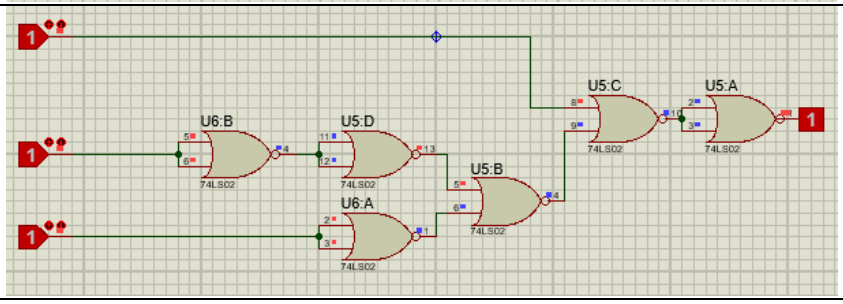
| | |
|---|---|
| **Implementation Using NOR Gate Only:** |   |
| **Implementation Using NAND Gate Only:** |   |

**1) Implement following expression using NOR Gate only:**

**Answer:**

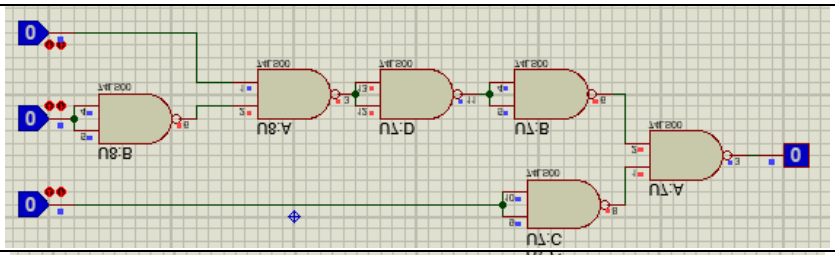
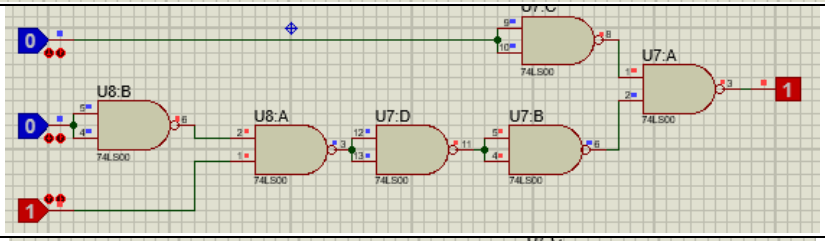
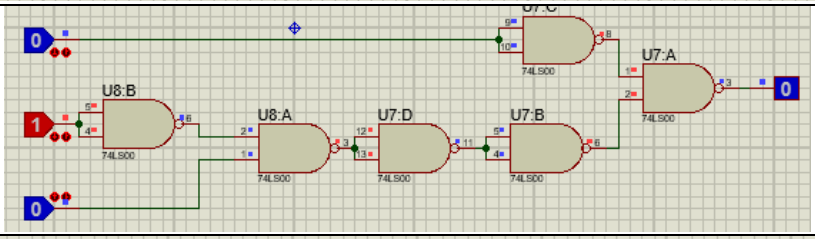
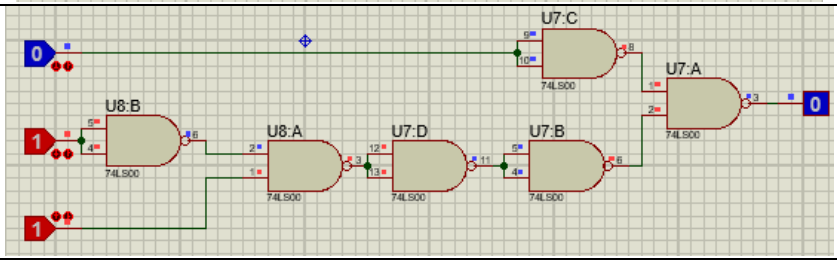
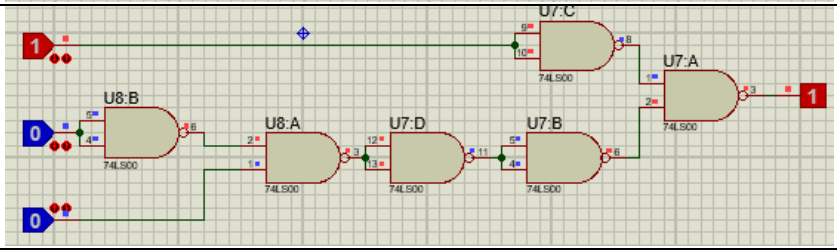
## Truth Table With Proof:

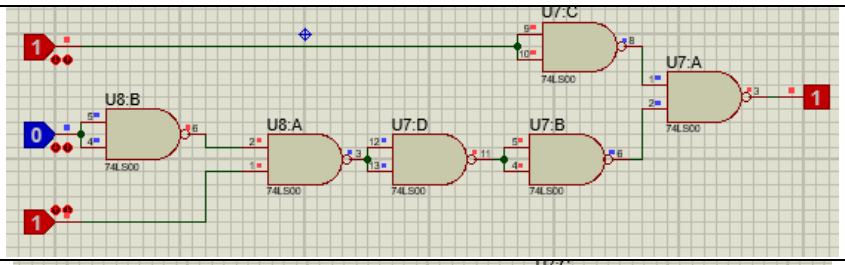
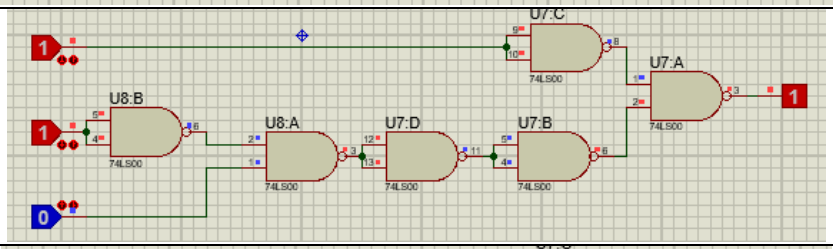
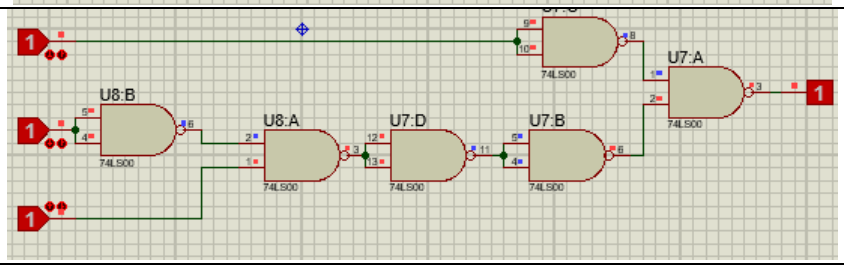
| Input | | | Output | Proof |
|---|---|---|---|---|
| X | Y | Z | F | |
| 0 | 0 | 0 | 0 |  |
| 0 | 0 | 1 | 1 |  |
| 0 | 1 | 0 | 0 |  |
| 0 | 1 | 1 | 0 |  |

| | | | | |
|---|---|---|---|---|
| 1 | 0 | 0 | 1 |  |
| 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 1 |  |

## 2) Implement following expression using NOR Gate only:

### Truth Table With Proof:

| Input | | | Output | Proof |
|---|---|---|---|---|
| X | Y | Z | F | |
| 0 | 0 | 0 | 0 |  |
| 0 | 0 | 1 | 1 |  |
| 0 | 1 | 0 | 0 |  |
| 0 | 1 | 1 | 0 |  |
| 1 | 0 | 0 | 1 |  |

| | | | | |
|---|---|---|---|---|
| 1 | 0 | 1 | 1 |  |
| 1 | 1 | 0 | 1 |  |
| 1 | 1 | 1 | 1 |  |