DSM LAB REPORT-2

Lab 2: Gate Identification and De Morgan's Theorems

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Experiment-1

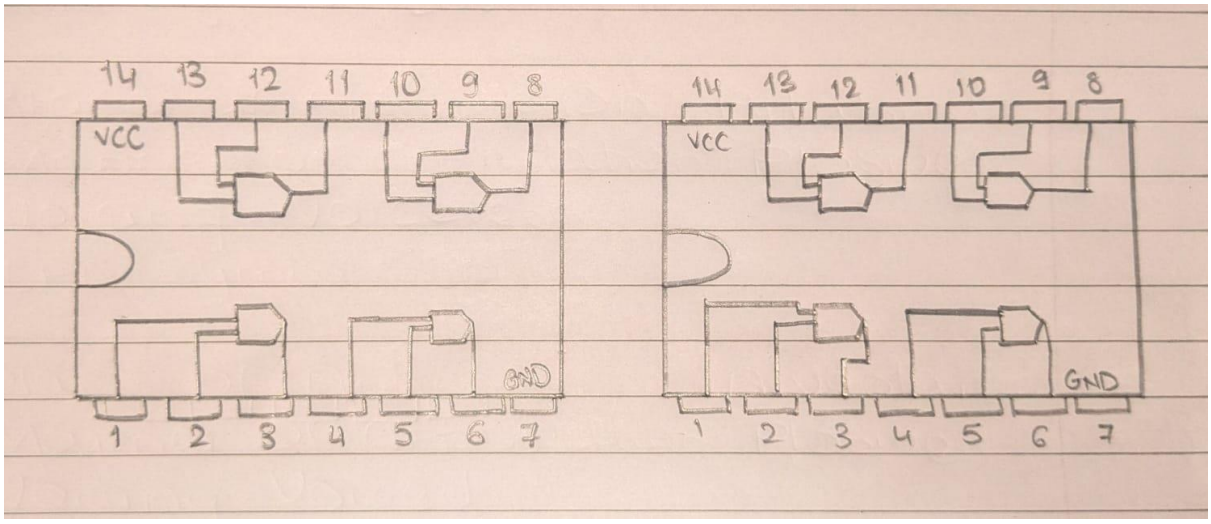
Objective:

To identify the logic gate present in each of the given ICs.

Components Used:

Digital Test Kit, wires, ICs = CPAE0014, CD4001BE, HD74LS86P, MC14001BCP, HD74LS32B, 74F08N

Reference Circuit:

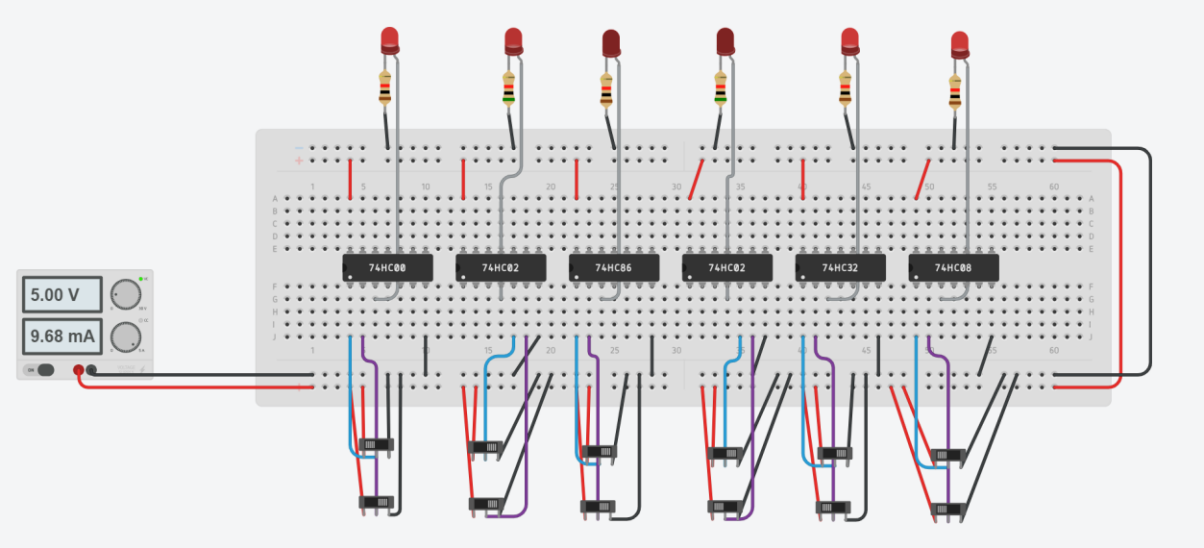


Procedure:

1. Connect the VCC and GND of the Digital Test Kit to the VCC and GND pins of the ICs.
2. Connect the two input pins of each IC to any of the input switches on the Digital Test Kit and their respective output pins to the display points.
3. Now, toggle the input switches of each gate and record the readings in a truth table for each of the ICs.

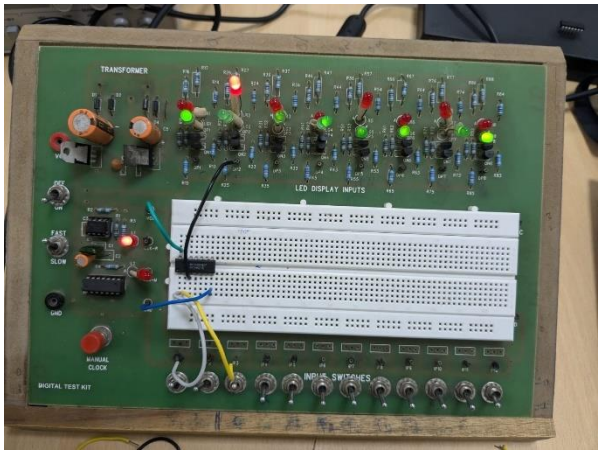
Tinkercad Simulation:

https://www.tinkercad.com/things/6hRjDU00NTk-dsmlab2exp1?sharecode=E_V9b1jKBYWSkEKcW-v8Ed_BTaks-ZafsexHGEd9p8E



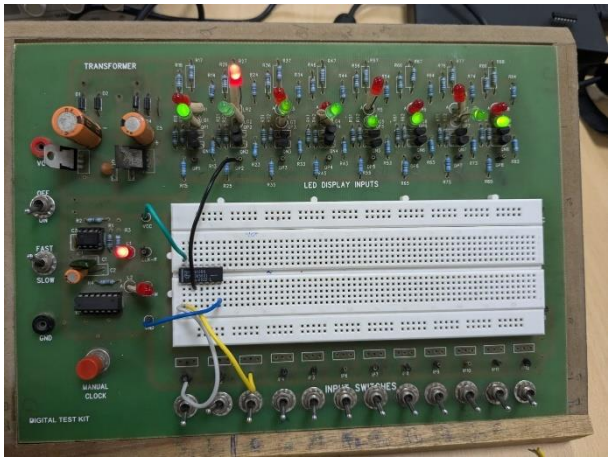
Observation:

1. NOR GATE (MC14001BCP)



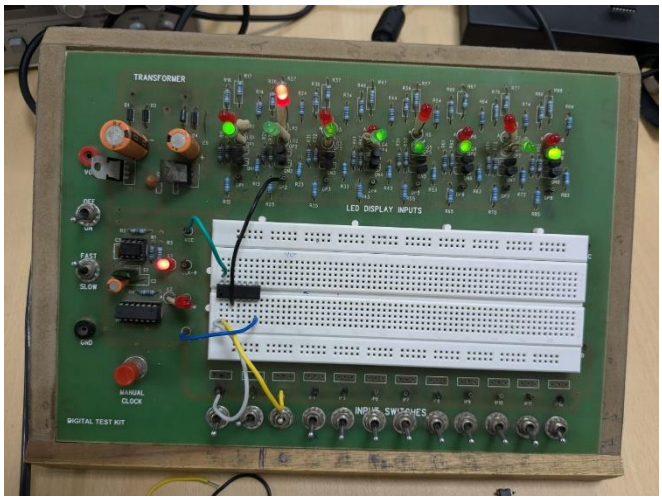
A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

2. AND GATE (74F08N)



A	B	A AND B
0	0	0
0	1	0
1	0	0
1	1	1

3. OR GATE (HD74LS32B)



A	B	A OR B
0	0	0
0	1	1
1	0	1
1	1	1

4. NAND GATE (CPAE0014)

A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

5. NOR GATE (CD4001BE)

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

6. XOR GATE (HD74LS86P)

A	B	A NOR B
0	0	0
0	1	1
1	0	1
1	1	0

Conclusion:

Logic gates present in the ICs identified via truth tables.

Experiment-2

Objective:

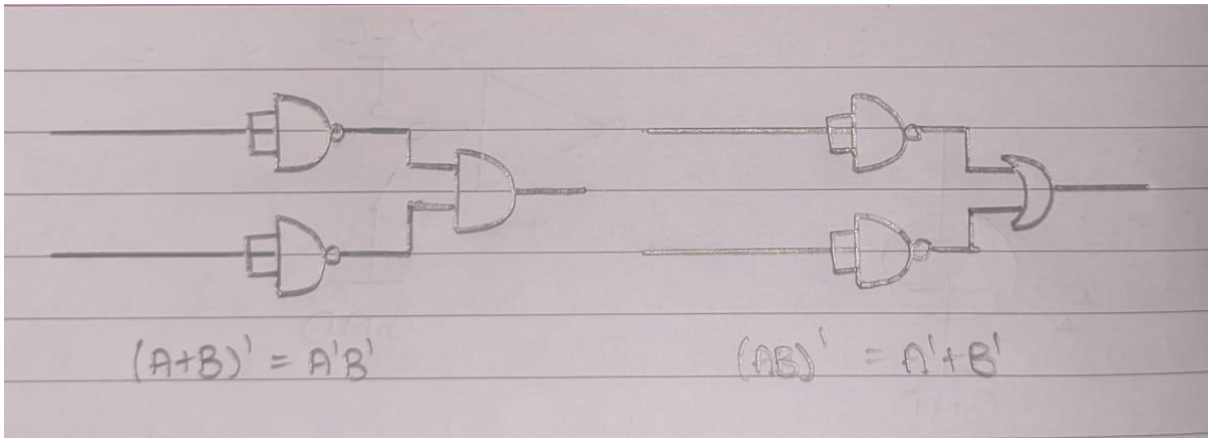
Verifying the De Morgan theorems.

1. (A+B)’ = A’B’
2. (AB)’ = A’ + B’

Components Used:

Digital Test Kit, wires, ICs = CPAE0014, C005601, HD74LS32B

Reference Circuits:



Procedure:

1. For A’B’, create a circuit using two NAND gates and one AND gate. Connect two inputs to the NAND gates to perform the NOT function. ((AA)’ = A’)
2. Now follow steps 1, 2, and 3 from Experiment 1 to verify that A’B’ is logically equivalent to the NOR gate.
3. Similarly using two NAND gates and one OR gate verify that A’ + B’ is logically equivalent to the NAND gate.

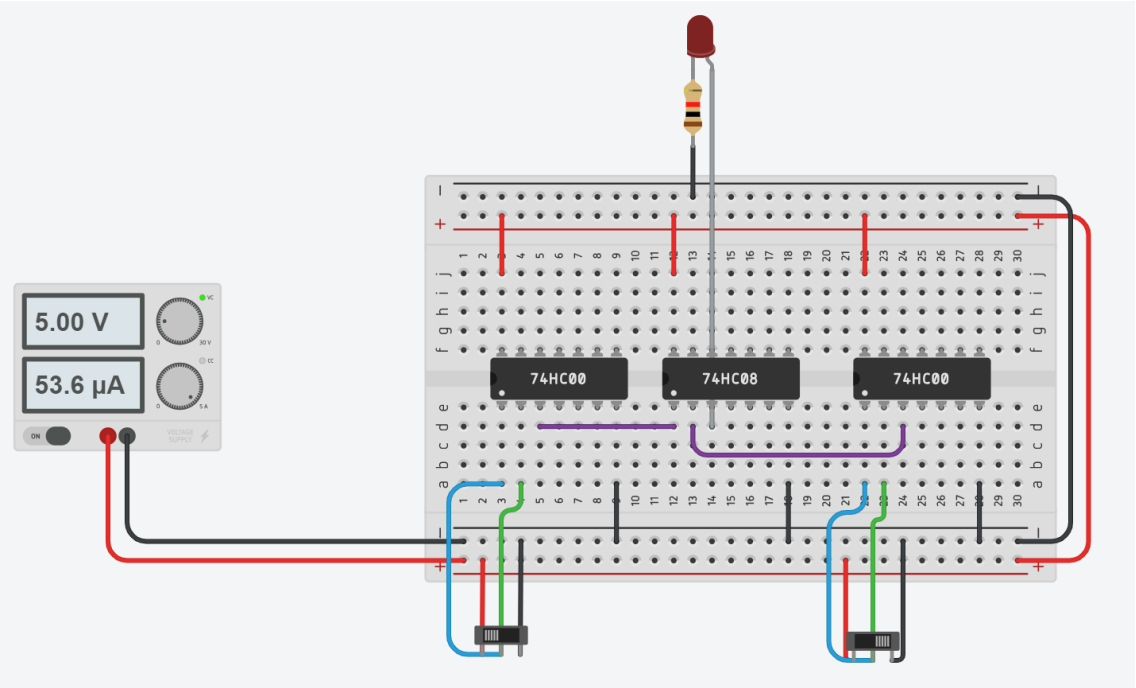
Outputs:

DSM_Lab-2(1).mp4 & DSM_Lab-2(2).mp4

Tinkercad Simulations:

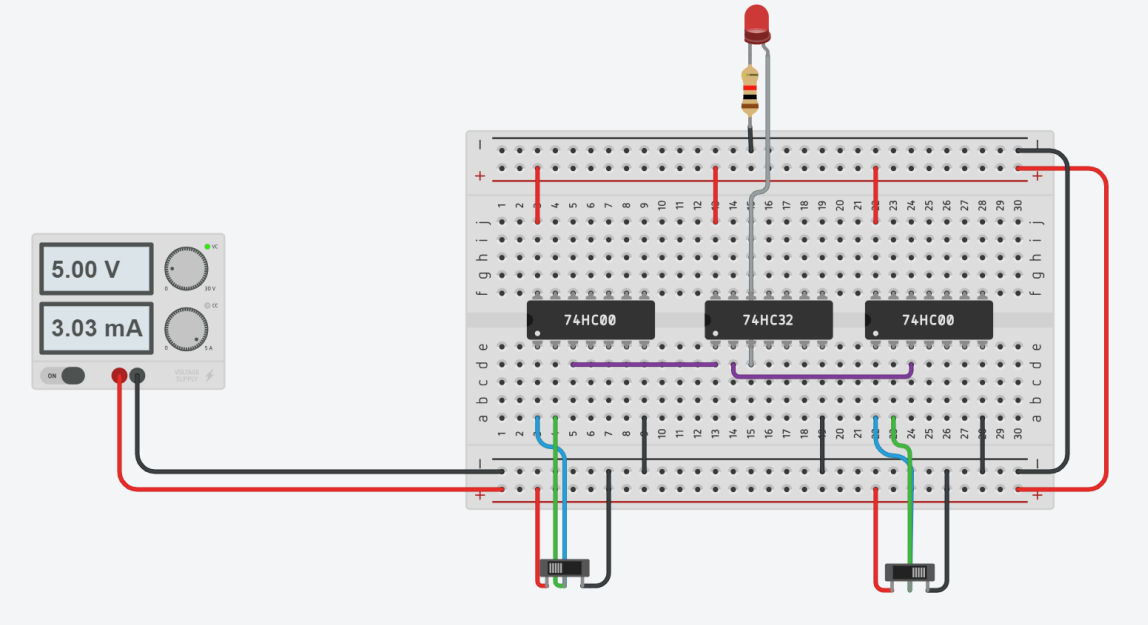
1. Y = A'B'

https://www.tinkercad.com/things/fBXGDnYl0Sh-dsmlab2exp2-1?sharecode=Wz3xleFYr_H-AQkTfTNhp4zFay6bk6M2x68m0eY7z6c



2. Y = A' + B'

https://www.tinkercad.com/things/iHAWsm2o0q4-dsmlab2exp2-2?sharecode=NScncwOS_xr2UMz_CC_RcFlQ6ZLa4GA0aL68fzrA4lM



Observations:

1. Y = A’B’

A	B	A NOR B
0	0	1
0	1	0
1	0	0
1	1	0

2. Y = A’ + B’

A	B	A NAND B
0	0	1
0	1	1
1	0	1
1	1	0

Conclusion:

De Morgan's theorems state that the truth table of Y = A'B' is equivalent to the truth table of the NOR gate, and the truth table of Y = A' + B' is equivalent to the truth table of the NAND gate.

Thus,

1. (A + B)’ = A’B’
2. (AB)’ = A’ + B’