Lab-Report 6

Course Code: CSE-404

Course Name: VLSI Design Lab

Submitted By

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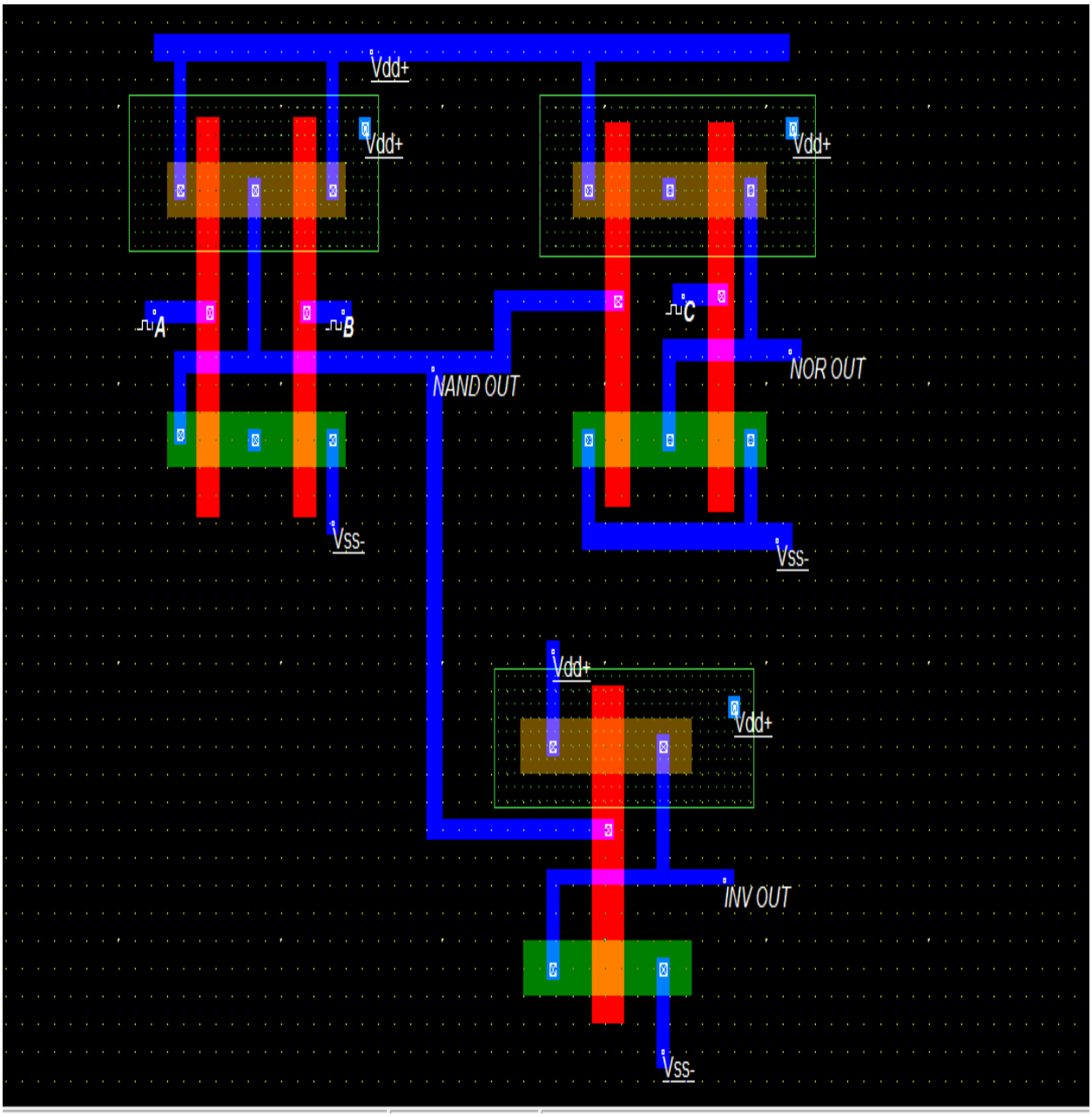
Experiment Name:A 2-input NAND gate is diving a 2-input NOR gate and an inverter using MICROWIND.

Objective:A 2-input NAND gate is diving a 2-input NOR gate and an inverter and see the performance and output wave shape.

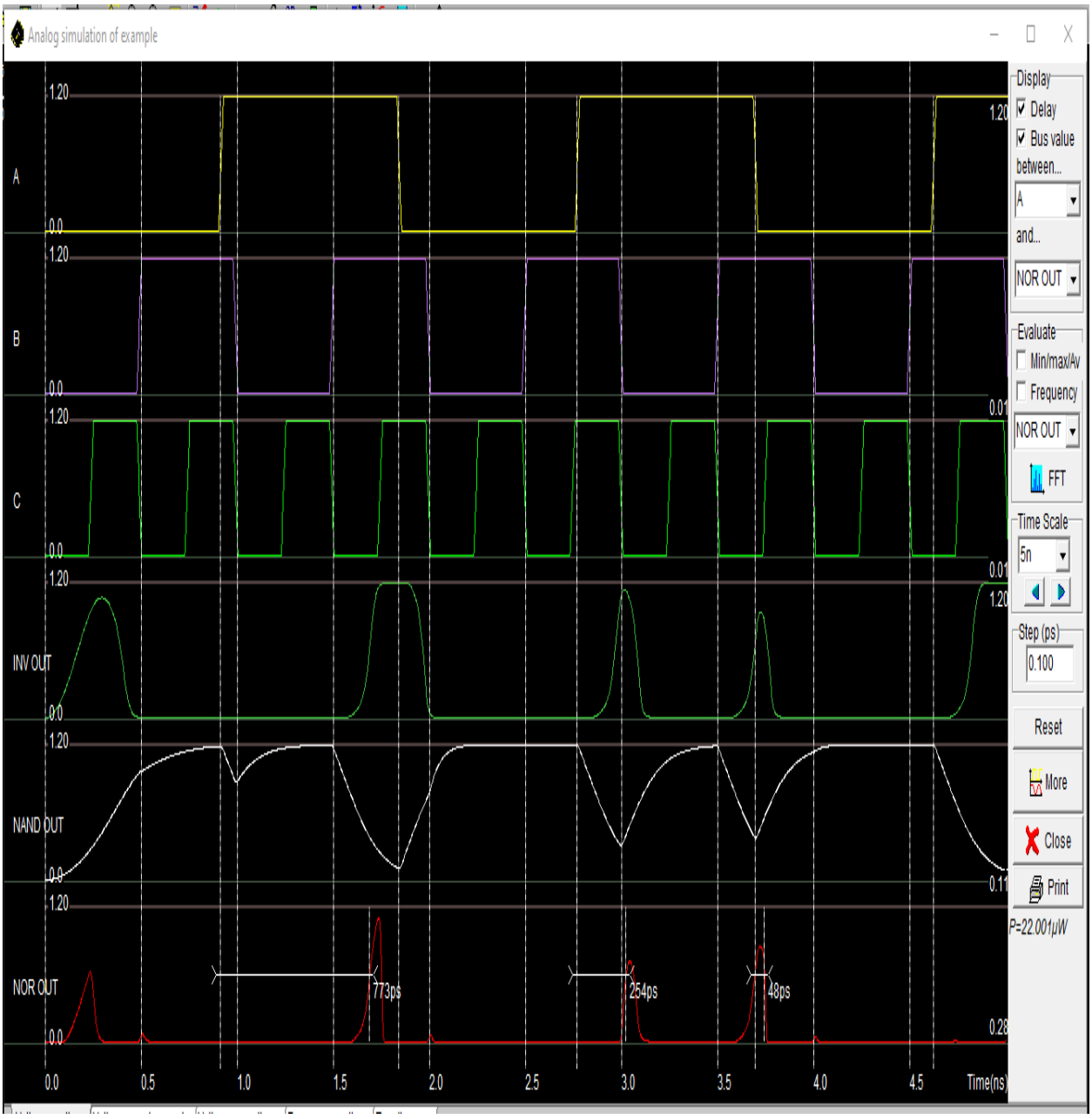
TruthTable:

A	B	C	NAND (AB)	NOR	INVERTER
0	0	0	1	0	0
0	0	1	1	0	0
0	1	0	1	0	0
0	1	1	1	0	0
1	0	0	1	0	0
1	0	1	1	0	0
1	1	0	0	1	1
1	1	1	0	0	1

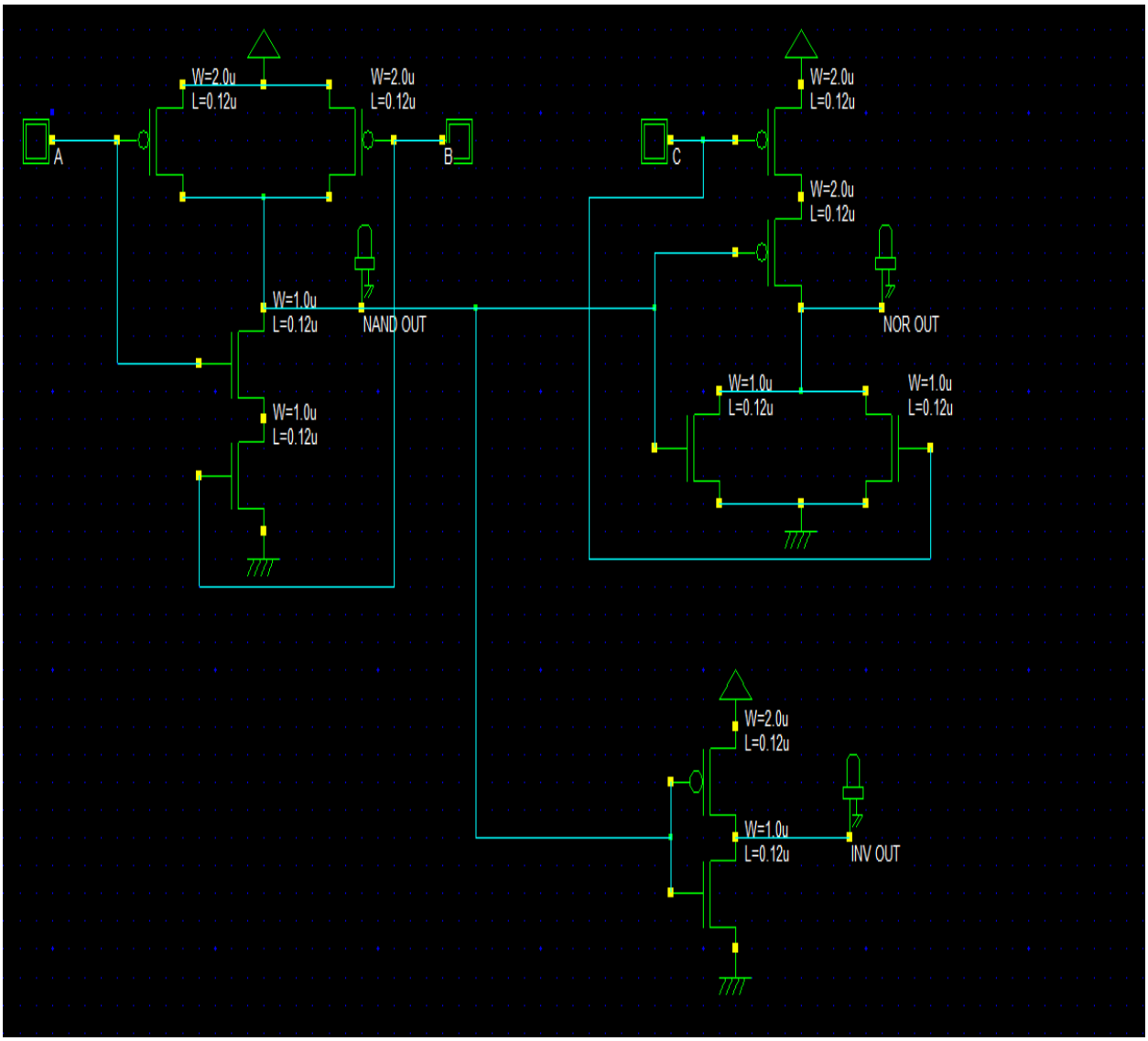
Microwind Design:



Microwind Output:

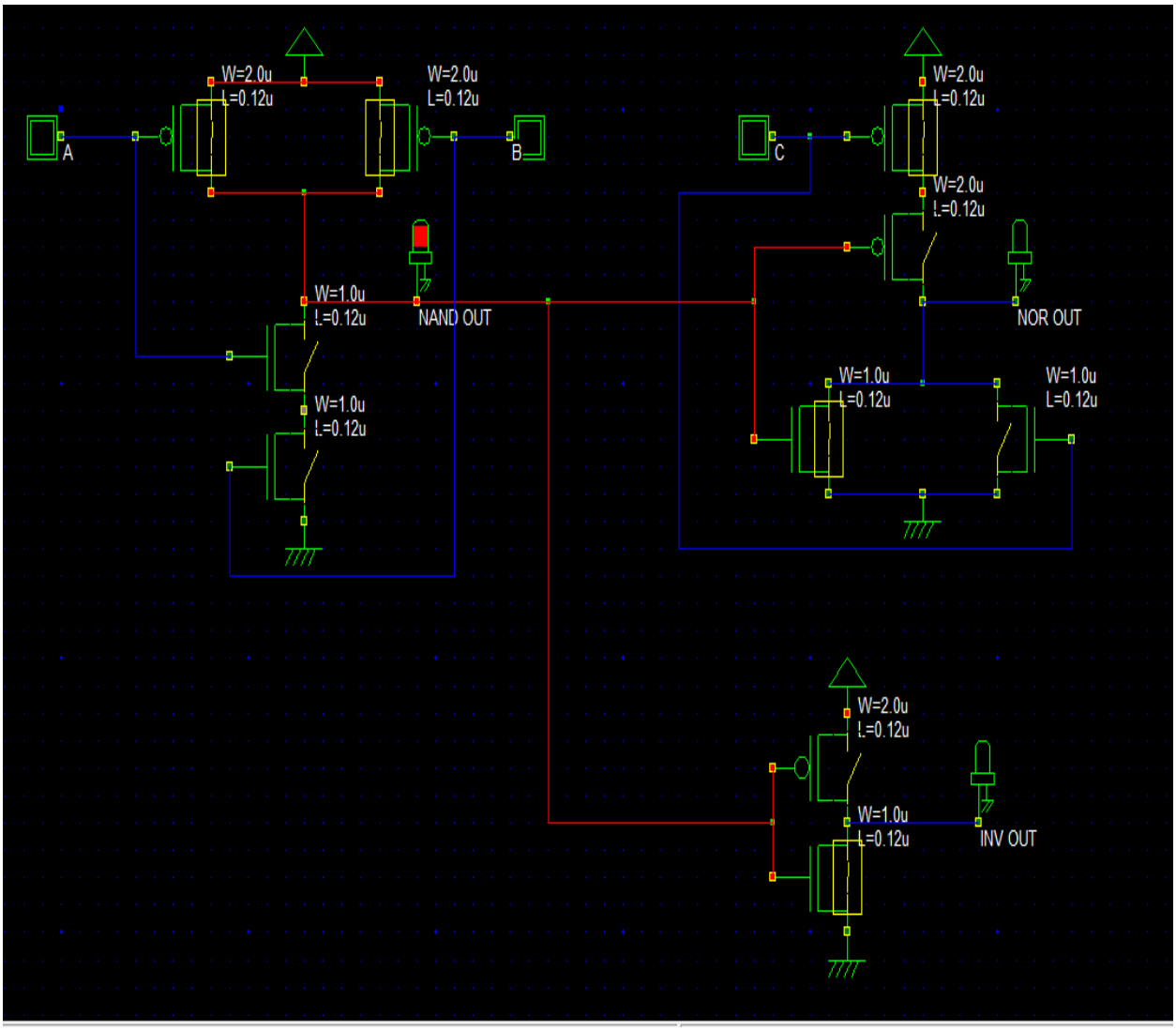


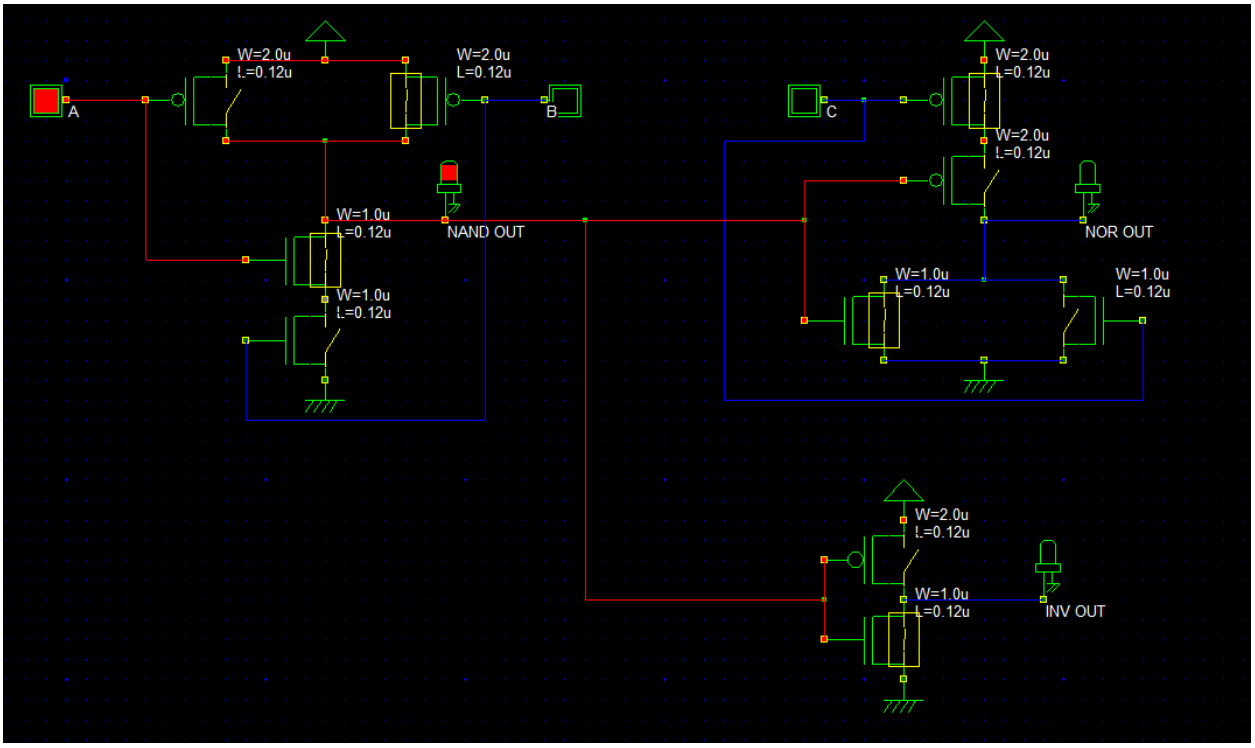
DSCH2 Input:

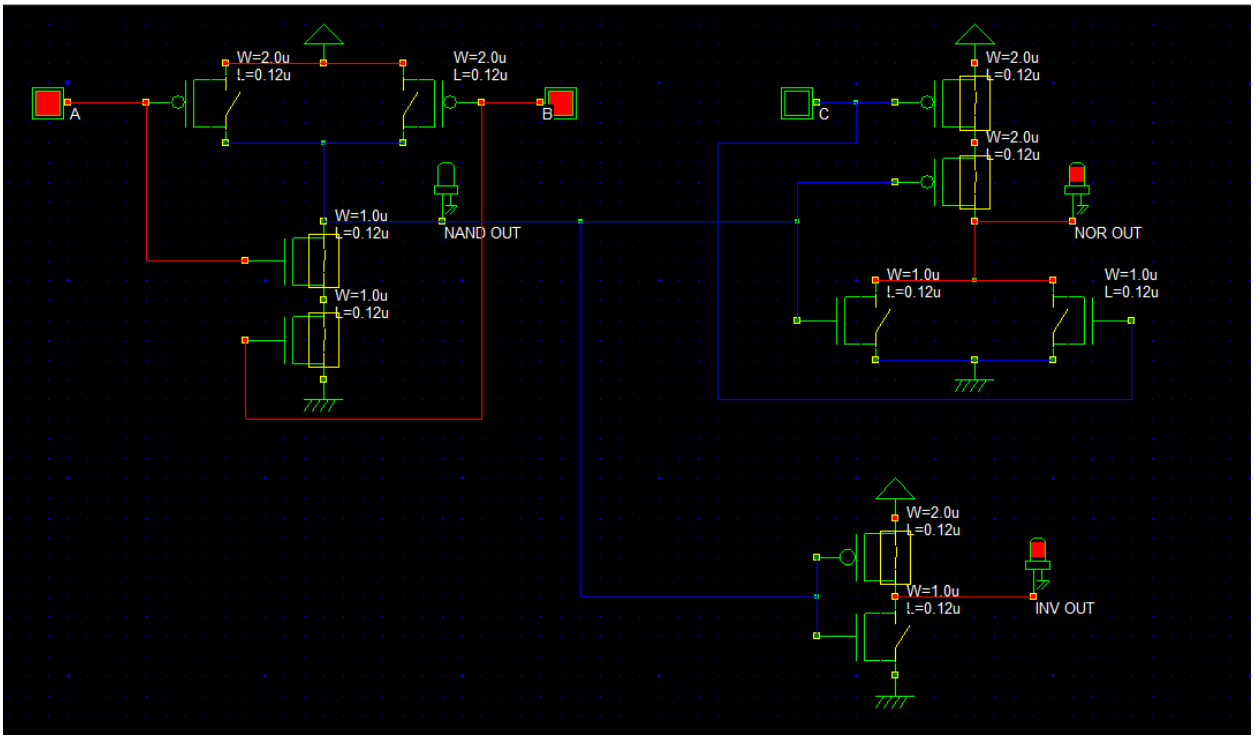

W=2.0u
L=0.12u
W=2.0u
L=0.12u
A
B
C
W=2.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u
L=0.12u
NAND OUT
NOR OUT
W=1.0u
L=0.12u
W=1.0u
L=0.12u
W=1.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u
L=0.12u
INV OUT

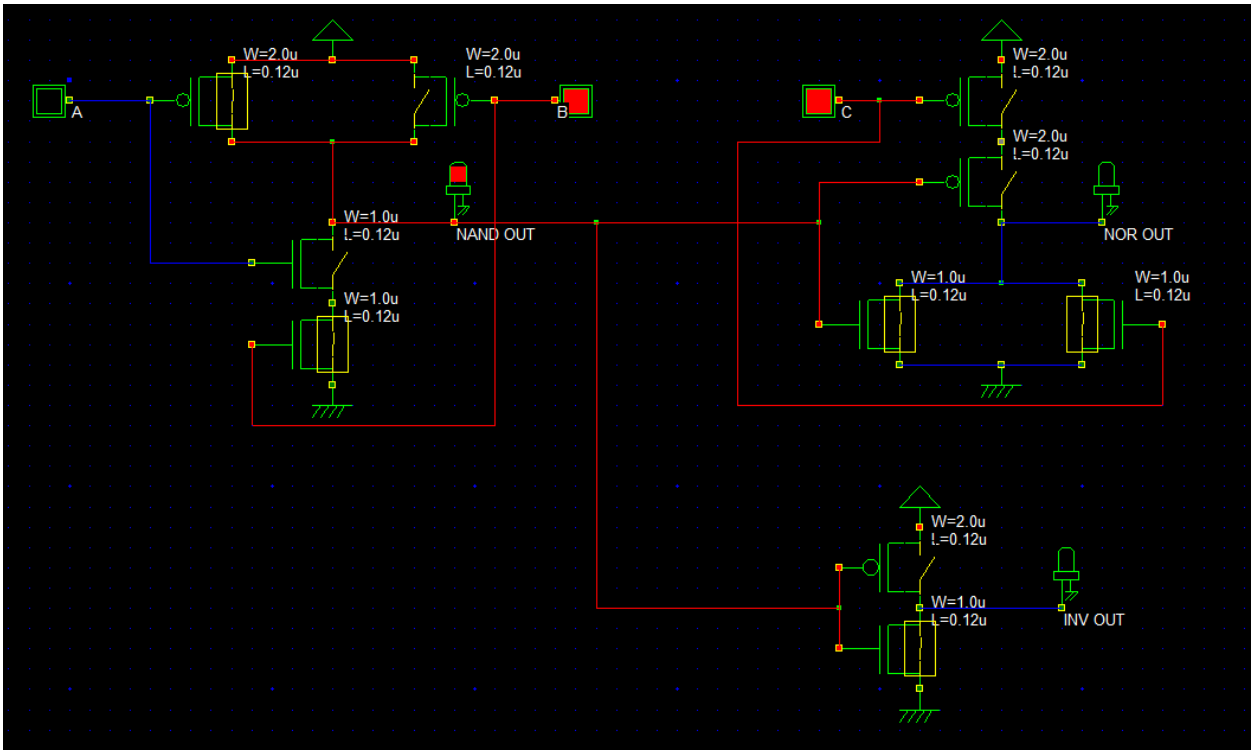
DSCH2 Output:

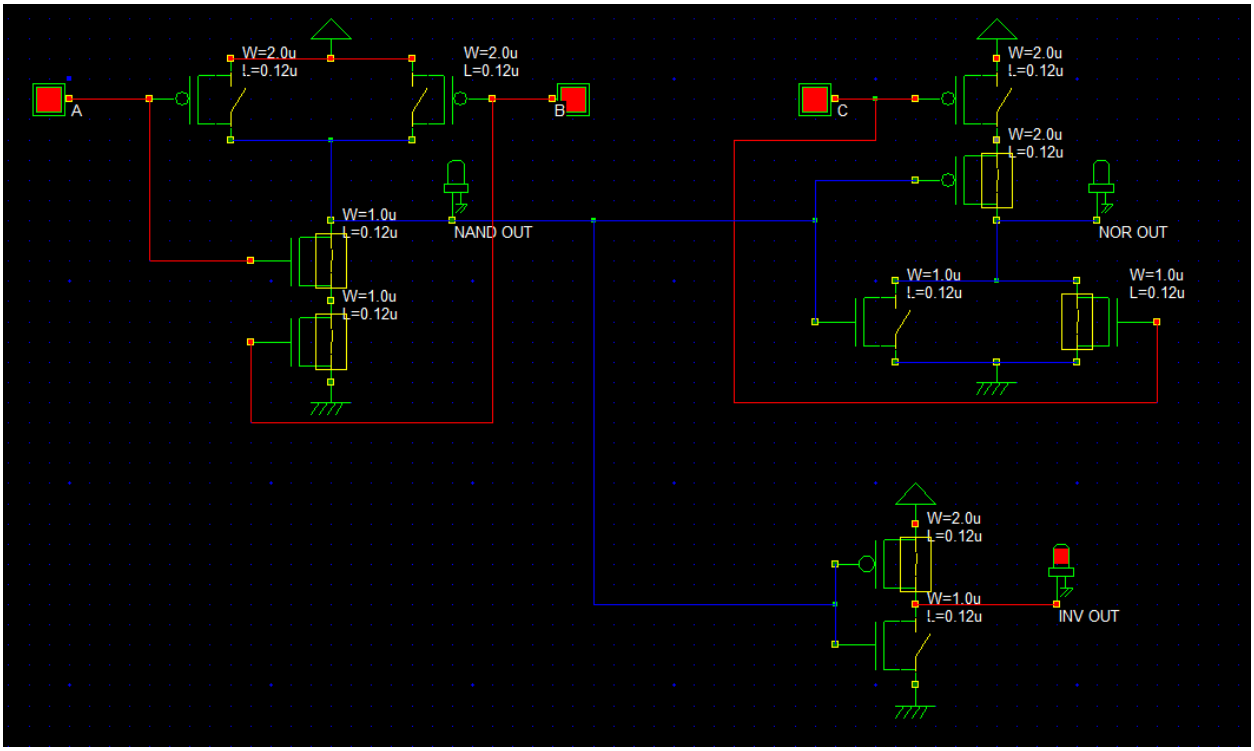
All the outputs are same as the truth table. Here I have given some sample output.



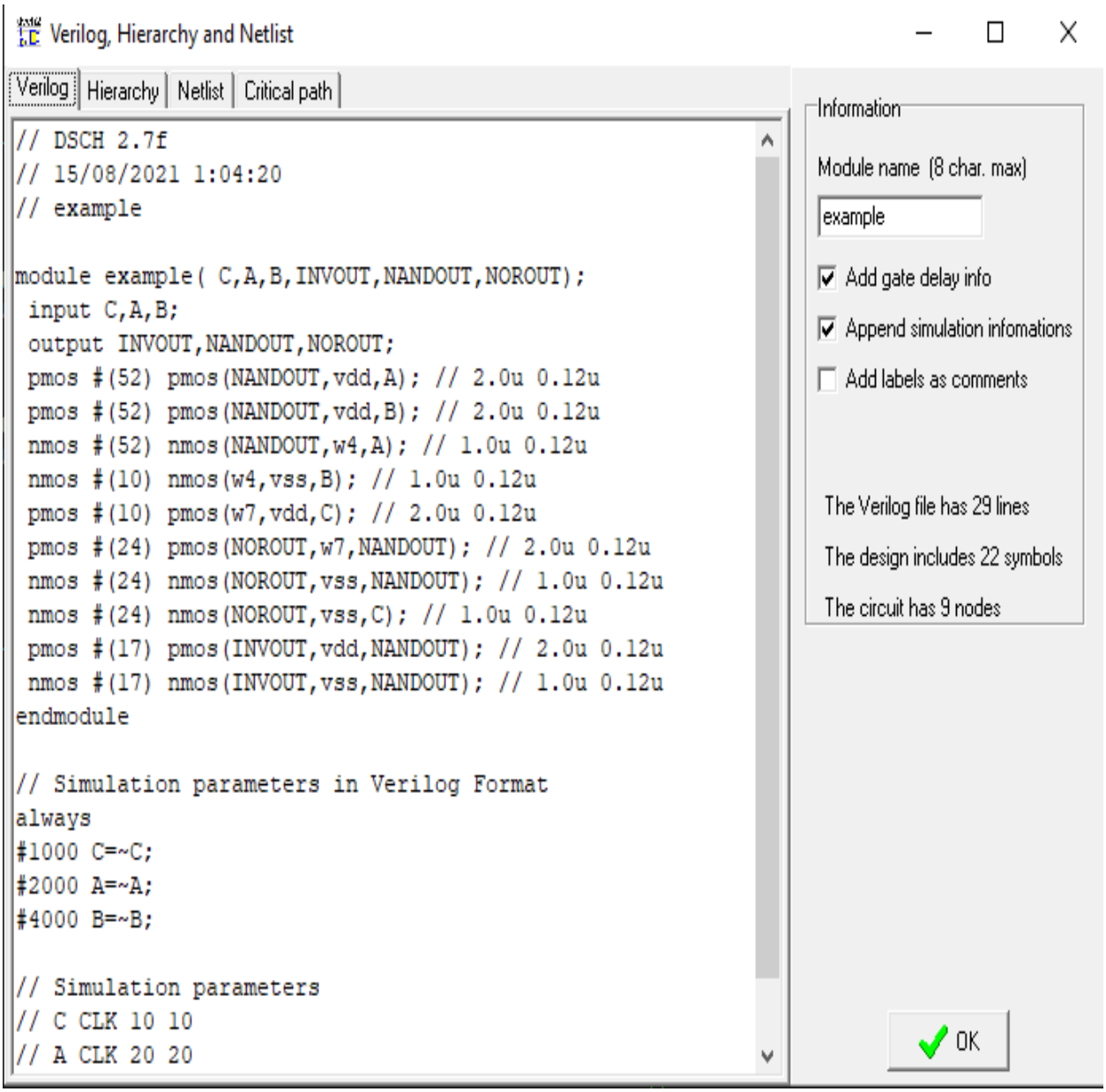

W=2.0u
L=0.12u
A
B
W=2.0u
L=0.12u
W=1.0u
L=0.12u
NAND OUT
W=1.0u
L=0.12u
C
W=2.0u
L=0.12u
W=2.0u
L=0.12u
NOR OUT
W=1.0u
L=0.12u
W=1.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u
L=0.12u
INV OUT


W=2.0u
L=0.12u
A
B
W=2.0u
L=0.12u
W=1.0u
L=0.12u
NAND OUT
W=1.0u
L=0.12u
C
W=2.0u
L=0.12u
W=2.0u
L=0.12u
NOR OUT
W=1.0u
L=0.12u
W=1.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u
L=0.12u
INV OUT

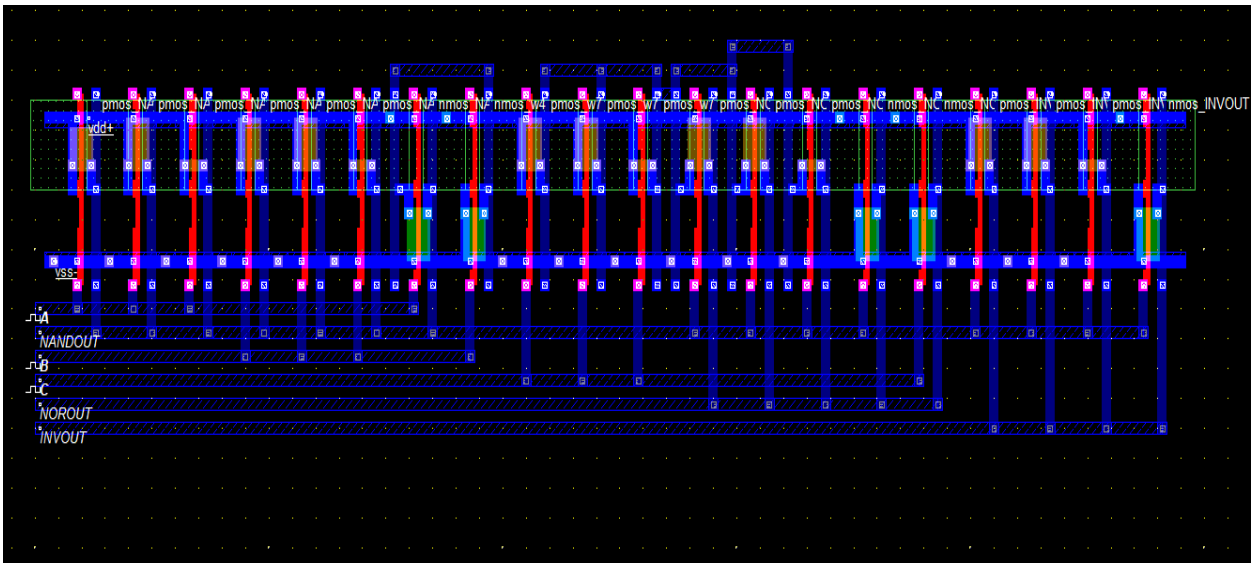

W=2.0u
L=0.12u
W=2.0u
L=0.12u
A
B
C
W=2.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u
L=0.12u
NAND OUT
NOR OUT
W=1.0u
L=0.12u
W=1.0u
L=0.12u
W=1.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u
L=0.12u
INV OUT


W=2.0u
L=0.12u
W=2.0u
L=0.12u
A
B
C
W=2.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u
L=0.12u
NAND OUT
NOR OUT
W=1.0u
L=0.12u
W=1.0u
L=0.12u
W=1.0u
L=0.12u
W=2.0u
L=0.12u
W=1.0u
L=0.12u
INV OUT

Code:


Verilog, Hierarchy and Netlist
Verilog
Hierarchy
Netlist
Critical path
// DSCH 2.7f
// 15/08/2021 1:04:20
// example
module example(C,A,B,INVOUT,NANDOUT,NOROUT);
input C,A,B;
output INVOUT,NANDOUT,NOROUT;
pmos #(52) pmos(NANDOUT,vdd,A); // 2.0u 0.12u
pmos #(52) pmos(NANDOUT,vdd,B); // 2.0u 0.12u
nmos #(52) nmos(NANDOUT,w4,A); // 1.0u 0.12u
nmos #(10) nmos(w4,vss,B); // 1.0u 0.12u
pmos #(10) pmos(w7,vdd,C); // 2.0u 0.12u
pmos #(24) pmos(NOROUT,w7,NANDOUT); // 2.0u 0.12u
nmos #(24) nmos(NOROUT,vss,NANDOUT); // 1.0u 0.12u
nmos #(24) nmos(NOROUT,vss,C); // 1.0u 0.12u
pmos #(17) pmos(INVOUT,vdd,NANDOUT); // 2.0u 0.12u
nmos #(17) nmos(INVOUT,vss,NANDOUT); // 1.0u 0.12u
endmodule
// Simulation parameters in Verilog Format
always
#1000 C=~C;
#2000 A=~A;
#4000 B=~B;
// Simulation parameters
// C CLK 10 10
// A CLK 20 20
Information
Module name (8 char. max)
example
Add gate delay info
Append simulation infomations
Add labels as comments
The Verilog file has 29 lines
The design includes 22 symbols
The circuit has 9 nodes
OK

Compiled Verilog on Microwind:



Output: