

# **Self-Check Laboratory Exercise 4A**

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**March 14th, 2022**

**CSC 34200/34300**

## Part 1: D Latch Component, simulation and verification with Model-Sim

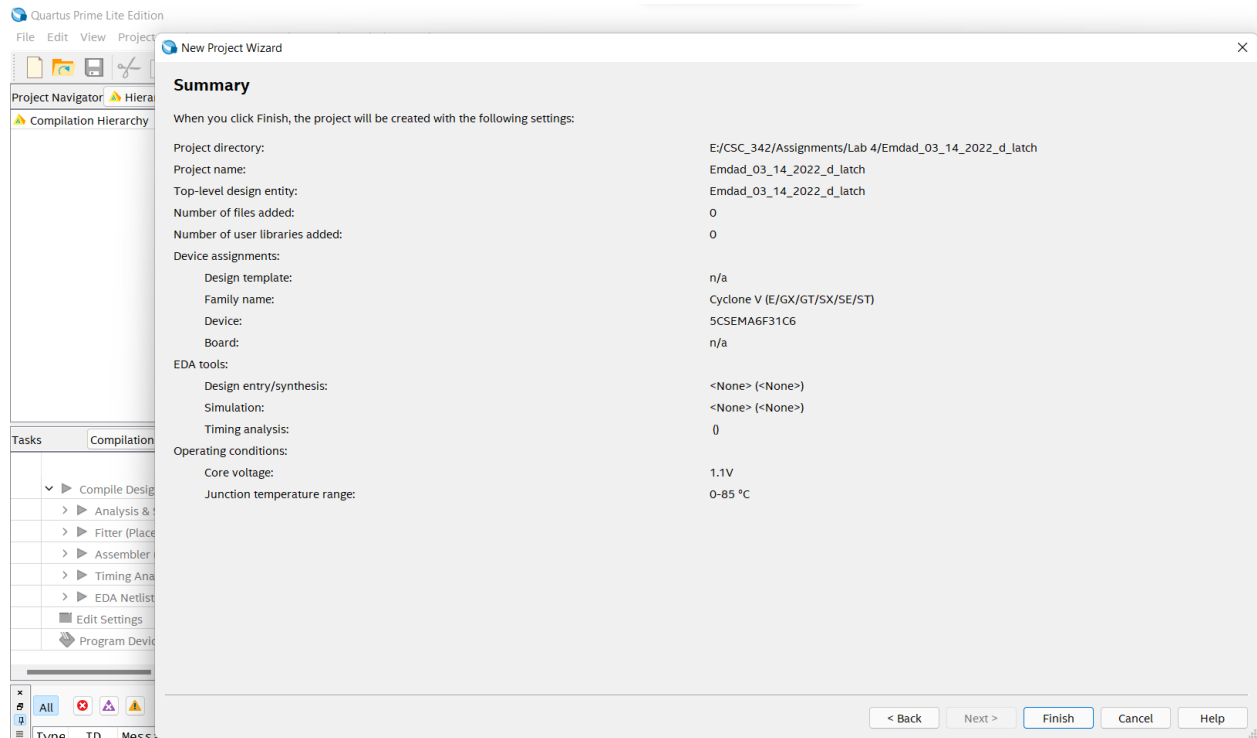


Figure 1: Project Summary

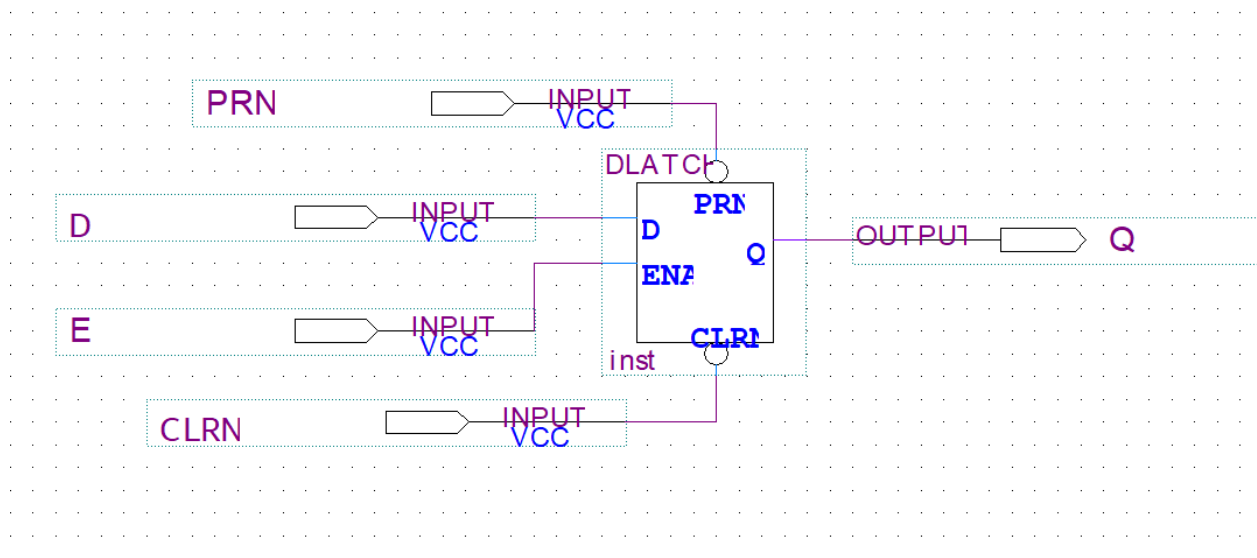


Figure 2: D-Latch Component

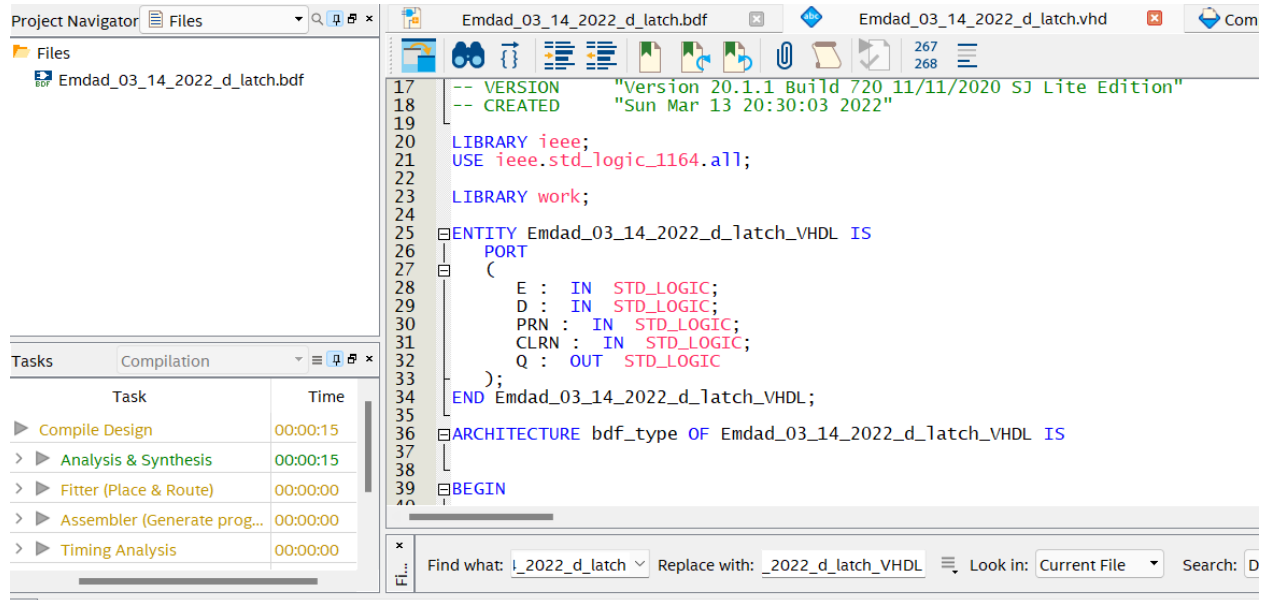


Figure 3: : D Latch VHDL code

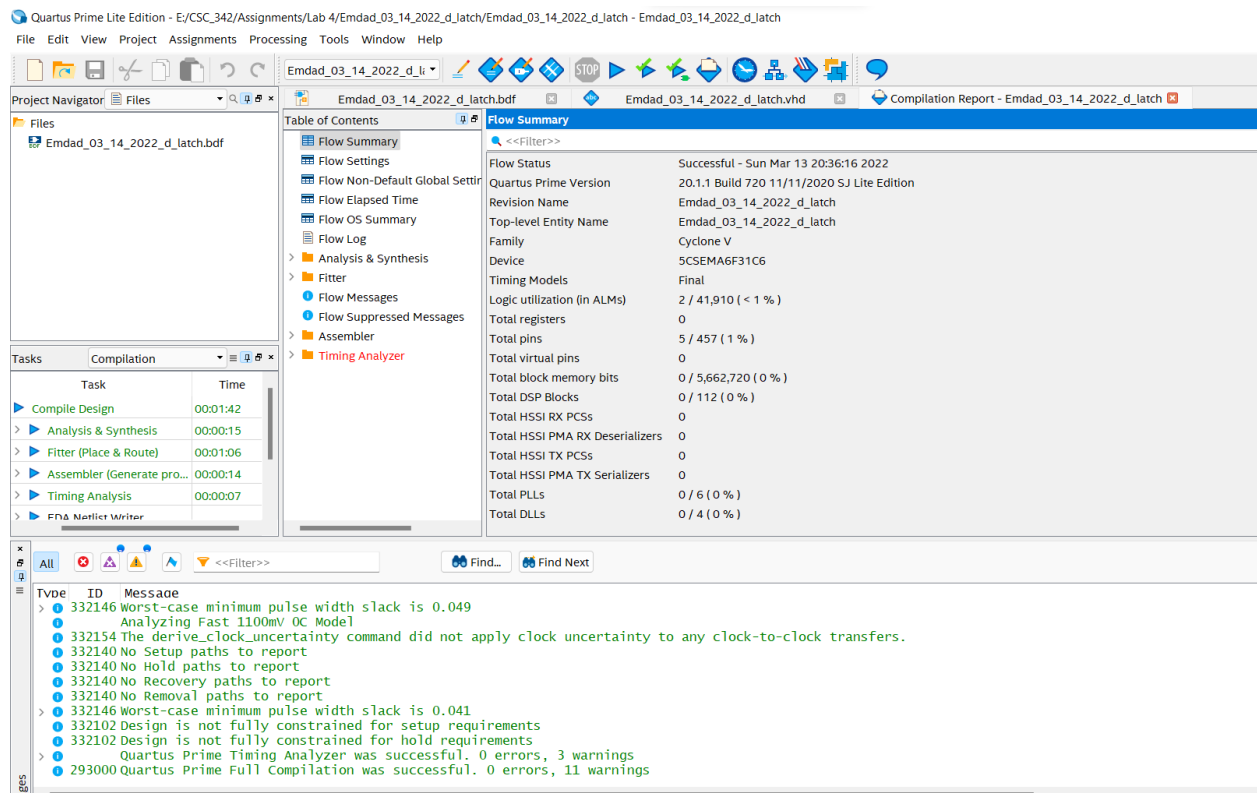


Figure 4: D Latch VHDL code Compilation Successfully

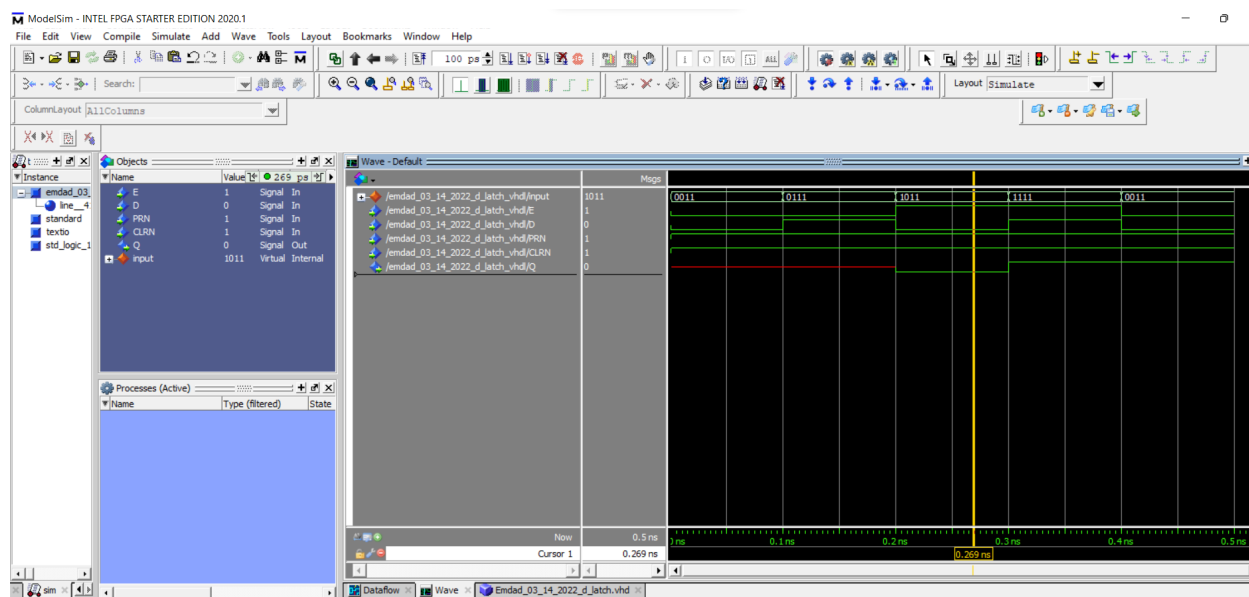
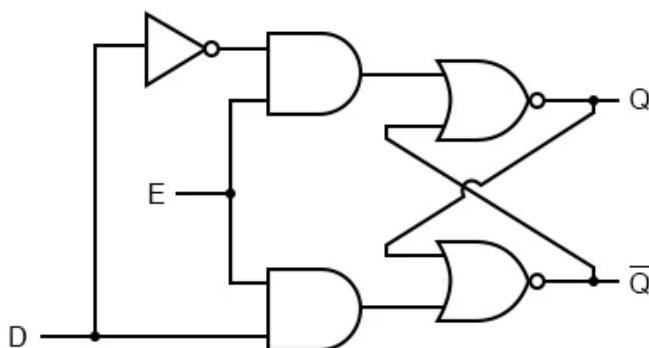


Figure 5: D Latch Simulation Waveform

I did this waveform by following the truth table:



E	D	Q	$\overline{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0

Figure 6: D Latch Truth Table

It has to match the output waveform therefore it is right.

## Part 2: Master-Slave D flip-flop using D Latches and simulation with Model-Sim

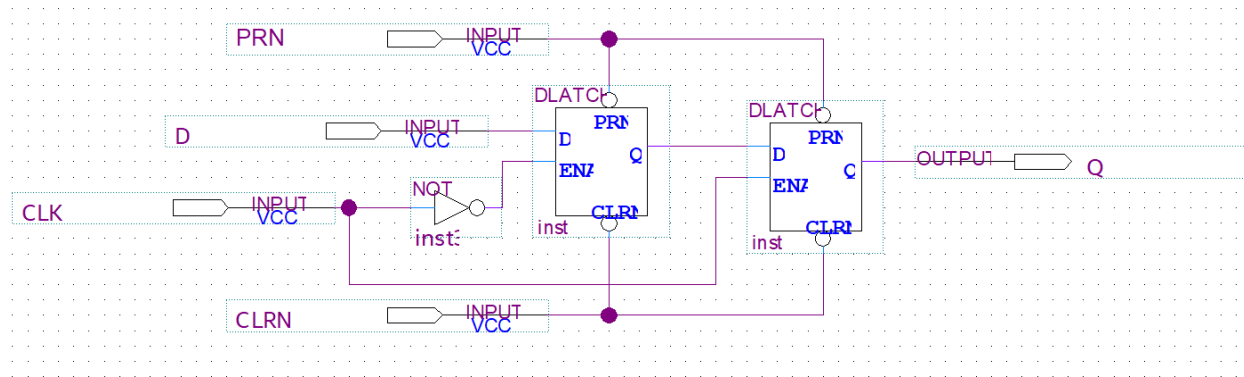


Figure 7: Master-Slave D flip-flop using D Latches

Quartus Prime Lite Edition - E:\CSC\_342\Assignments\Lab 4\Emdad\_03\_14\_2022\_d\_latch\Emdad\_03\_14\_2022\_d\_latch - Emdad\_03\_14\_2022\_d\_latch

File Edit View Project Assignments Processing Tools Window Help

Emdad\_03\_14\_2022\_d\_latch\_master\_slave.bdf

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- Flow Suppressed Messages
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- Timing Analyzer

Flow Summary

Flow Status: Successful - Sun Mar 13 20:36:16 2022

Quartus Prime Version: 20.1.1 Build 720 11/11/2020 SJ Lite Edition

Revision Name: Emdad\_03\_14\_2022\_d\_latch

Top-level Entity Name: Emdad\_03\_14\_2022\_d\_latch

Family: cyclone V

Device: 5CSEMA6F31C6

Timing Models: Final

Logic utilization (in ALMs): 2 / 41,910 (< 1 %)

Total registers: 0

Total pins: 5 / 457 (1 %)

Total virtual pins: 0

Total block memory bits: 0 / 5,662,720 (0 %)

Total DSP Blocks: 0 / 112 (0 %)

Total HSSI RX PCSs: 0

Total HSSI PMA RX Deserializers: 0

Total HSSI TX PCSs: 0

Total HSSI PMA TX Serializers: 0

Total PLLs: 0 / 6 (0 %)

Total DLLs: 0 / 4 (0 %)

Tasks

Compilation

Task

- Compile Design
- Analysis & Synthesis
- Fitter (Place & Route)
- Assembler (Generate program)
- Timing Analysis
- EDA Netlist Writer

Find... Find Next

Types ID Message

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> Running Quartus Prime Create VHDL File
Command: quartus_map --read_settings_files=on --write_settings_files=off Emdad_03_14_2022_d_latch -c Emdad_03_14_2022_d_latch --convert_bdf_to_vhdl="E:\CSC_342\Assignments\Lab 4\Emdad_03_14_2022_d_latch\Emdad_03_14_2022_d_latch_master_slave.bdf"
> 12021 Found 1 design units, including 1 entities, in source file emdad_03_14_2022_d_latch_master_slave.bdf
> 12127 Elaborating entity "" for the top level hierarchy
> Quartus Prime Create VHDL File was successful. 0 errors, 0 warnings
  
```

Figure 8: Compilation Successfully

```

Text Editor - E:/CSC_342/Assignments/Lab 4/Emdad_03_14_2022_d_latch/Emdad_03_14_2022_d_latch - Emdad_03_14_2022_d_latch - [Emdad_03_14_2022_d_latch_master_slave.vhd]
File Edit View Project Processing Tools Window Help
267 268
15
16 -- PROGRAM      "Quartus Prime"
17 -- VERSION      "Version 20.1.1 Build 720_11/11/2020 SJ Lite Edition"
18 -- CREATED      "Sun Mar 13 21:24:08 2022"
19
20 LIBRARY ieee;
21 USE ieee.std_logic_1164.all;
22
23 LIBRARY work;
24
25 ENTITY Emdad_03_14_2022_d_latch_master_slave IS
26 PORT
27 (
28   PRN : IN  STD_LOGIC;
29   D : IN  STD_LOGIC;
30   CLK : IN  STD_LOGIC;
31   CLRN : IN  STD_LOGIC;
32   Q : OUT STD_LOGIC
33 );
34 END Emdad_03_14_2022_d_latch_master_slave;
35
36 ARCHITECTURE bdf_type OF Emdad_03_14_2022_d_latch_master_slave IS
37
38   SIGNAL SYNTHESIZED_WIRE_0 : STD_LOGIC;
39   SIGNAL SYNTHESIZED_WIRE_1 : STD_LOGIC;
40
41 BEGIN
42
43   PROCESS (CLRN, PRN, SYNTHESIZED_WIRE_0, D)
44   BEGIN
45     IF (CLRN = '0') THEN
46       SYNTHESIZED_WIRE_1 <= '0';
47     ELSIF (PRN = '0') THEN
48       SYNTHESIZED_WIRE_1 <= '1';
49     ELSIF (SYNTHESIZED_WIRE_0 = '1') THEN
50       SYNTHESIZED_WIRE_1 <= D;
51     END IF;
52   END PROCESS;
53
54   PROCESS (CLRN, PRN, CLK, SYNTHESIZED_WIRE_1)
55   BEGIN
56     IF (CLRN = '0') THEN
57       Q <= '0';
58     ELSIF (PRN = '0') THEN
59       Q <= '1';
60     ELSIF (CLK = '1') THEN
61       Q <= SYNTHESIZED_WIRE_1;
62     END IF;
63   END PROCESS;
64
65   SYNTHESIZED_WIRE_0 <= NOT(CLK);
66
67 END bdf_type;
68

```

Figure 9: Master-Slave D flip-flop using D Latches VHDL Code

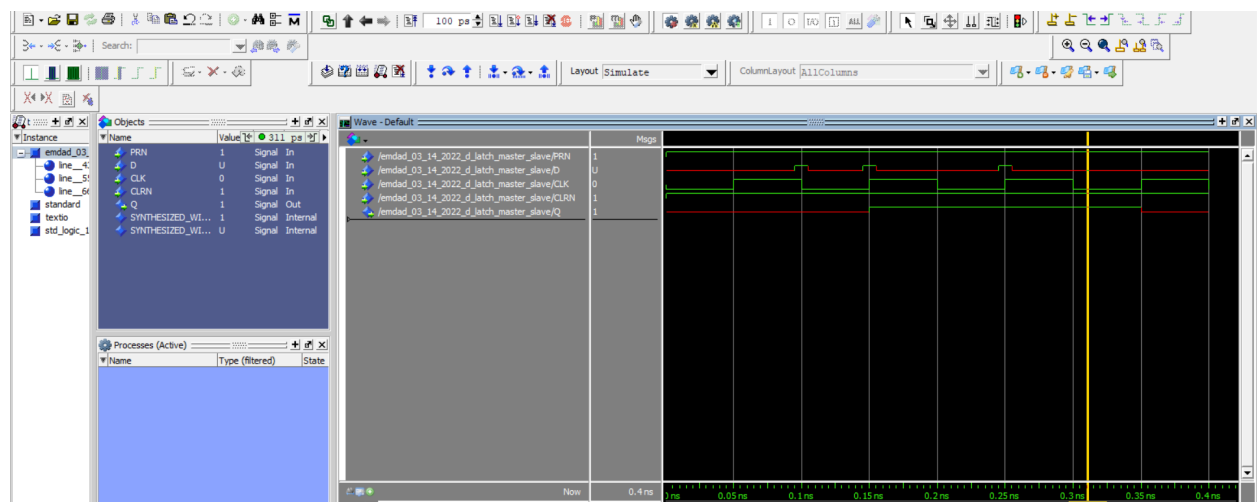


Figure 10: D Latch Simulation Waveform

The waveforms are correct as it has the same waveform as D flip-flop we made from the built-in component.

**Part 3: Using D flip-flop as a component symbol and simulation with Model-Sim**

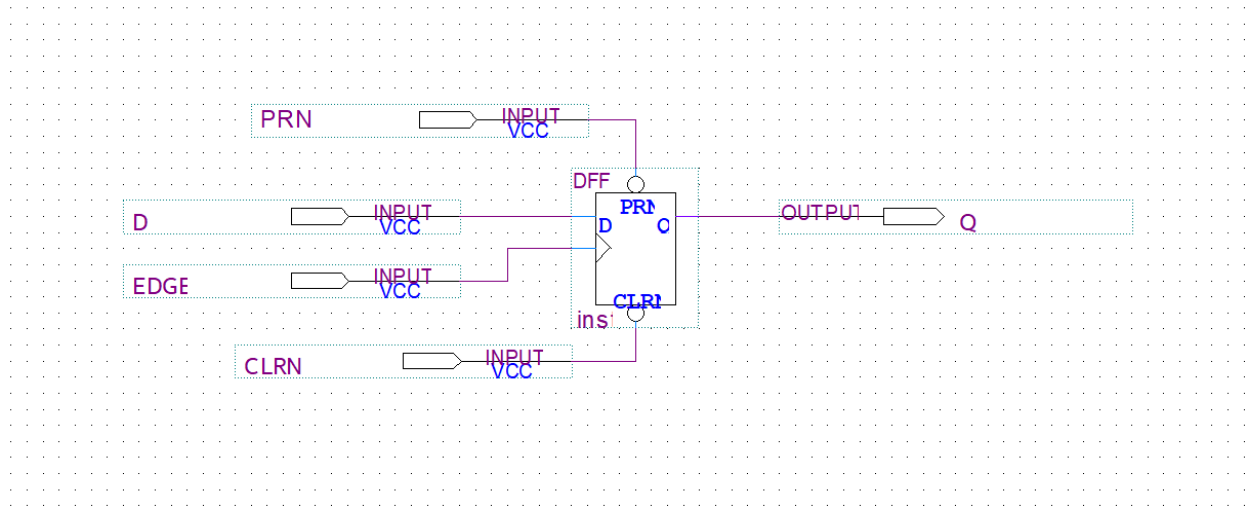
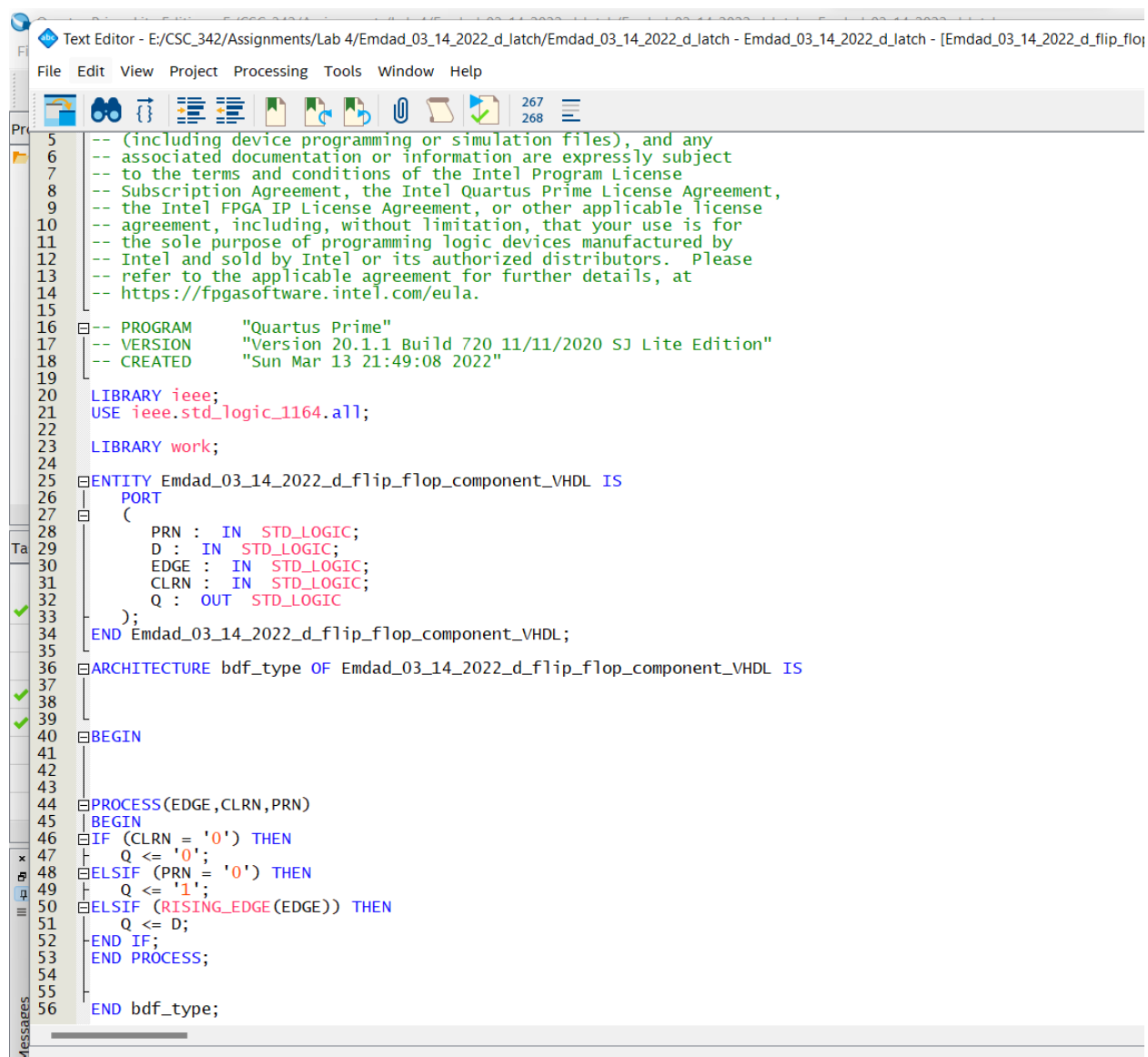


Figure 11: D flip-flop as a component symbol



```

5  -- (including device programming or simulation files), and any
6  -- associated documentation or information are expressly subject
7  -- to the terms and conditions of the Intel Program License
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11 -- the sole purpose of programming logic devices manufactured by
12 -- Intel and sold by Intel or its authorized distributors. Please
13 -- refer to the applicable agreement for further details, at
14 -- https://fpgasoftware.intel.com/eula.
15
16 -- PROGRAM      "Quartus Prime"
17 -- VERSION      "Version 20.1.1 Build 720 11/11/2020 SJ Lite Edition"
18 -- CREATED      "Sun Mar 13 21:49:08 2022"
19
20 LIBRARY ieee;
21 USE ieee.std_logic_1164.all;
22
23 LIBRARY work;
24
25 ENTITY Emdad_03_14_2022_d_flip_flop_component_VHDL IS
26 PORT
27 (
28     PRN : IN  STD_LOGIC;
29     D   : IN  STD_LOGIC;
30     EDGE : IN  STD_LOGIC;
31     CLRN : IN  STD_LOGIC;
32     Q    : OUT STD_LOGIC
33 );
34 END Emdad_03_14_2022_d_flip_flop_component_VHDL;
35
36 ARCHITECTURE bdf_type OF Emdad_03_14_2022_d_flip_flop_component_VHDL IS
37
38
39 BEGIN
40
41
42
43
44 PROCESS(EDGE, CLRN, PRN)
45 BEGIN
46 IF (CLRN = '0') THEN
47     Q <= '0';
48 ELSIF (PRN = '0') THEN
49     Q <= '1';
50 ELSIF (RISING_EDGE(EDGE)) THEN
51     Q <= D;
52 END IF;
53 END PROCESS;
54
55
56 END bdf_type;

```

Figure 12: D flip-flop as a component symbol VHDL Code



Quartus Prime Lite Edition - E:/CSC\_342/Assignments/Lab 4/Emdad\_03\_14\_2022\_d\_latch/Emdad\_03\_14\_2022\_d\_latch - Emdad\_03\_14\_2022\_d\_latch

File Edit View Project Assignments Processing Tools Window Help

Emdad\_03\_14\_2022\_d.li

Project Navigator

Files

- Emdad\_03\_14\_2022\_d\_latch.bdf
- Emdad\_03\_14\_2022\_d\_latch\_master\_slave.bdf
- Emdad\_03\_14\_2022\_d\_flip\_flop\_component\_VHDLbdf

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- Analysis & Synthesis
  - Filter
  - Flow Messages
  - Flow Suppressed Messages
- Assembler
- Timing Analyzer

Flow Summary

<<Filter>>

Flow Status	Successful - Sun Mar 13 20:36:16 2022
Quartus Prime Version	20.1.1 Build 720 11/11/2020 SJ Lite Edition
Revision Name	Emdad_03_14_2022_d_latch
Top-level Entity Name	Emdad_03_14_2022_d_latch
Family	Cyclone V
Device	5CSEMA6F31C6
Timing Models	Final
Logic utilization (in ALMs)	2 / 41,910 (< 1 %)
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Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0 / 6 (0 %)
Total DLLs	0 / 4 (0 %)

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Task

- Compile Design
  - Analysis & Synthesis
  - Fitter (Place & Route)
  - Assembler (Generate programming files)
  - Timing Analysis
  - EDA Netlist Writer

All

<<Filter>>

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Running Quartus Prime Create VHDL File

Command: quartus\_map --read\_settings\_files=on --write\_settings\_files=off Emdad\_03\_14\_2022\_d\_latch -c Emdad\_03\_14\_2022\_d\_latch --convert\_bdf

12021 Found 1 design units, including 1 entities, in source file emdad\_03\_14\_2022\_d\_flip\_flop\_component\_vhdl.bdf

12127 Elaborating entity "" for the top level hierarchy

Quartus Prime Create VHDL File was successful. 0 errors, 0 warnings

Figure 13: Compiled design successful

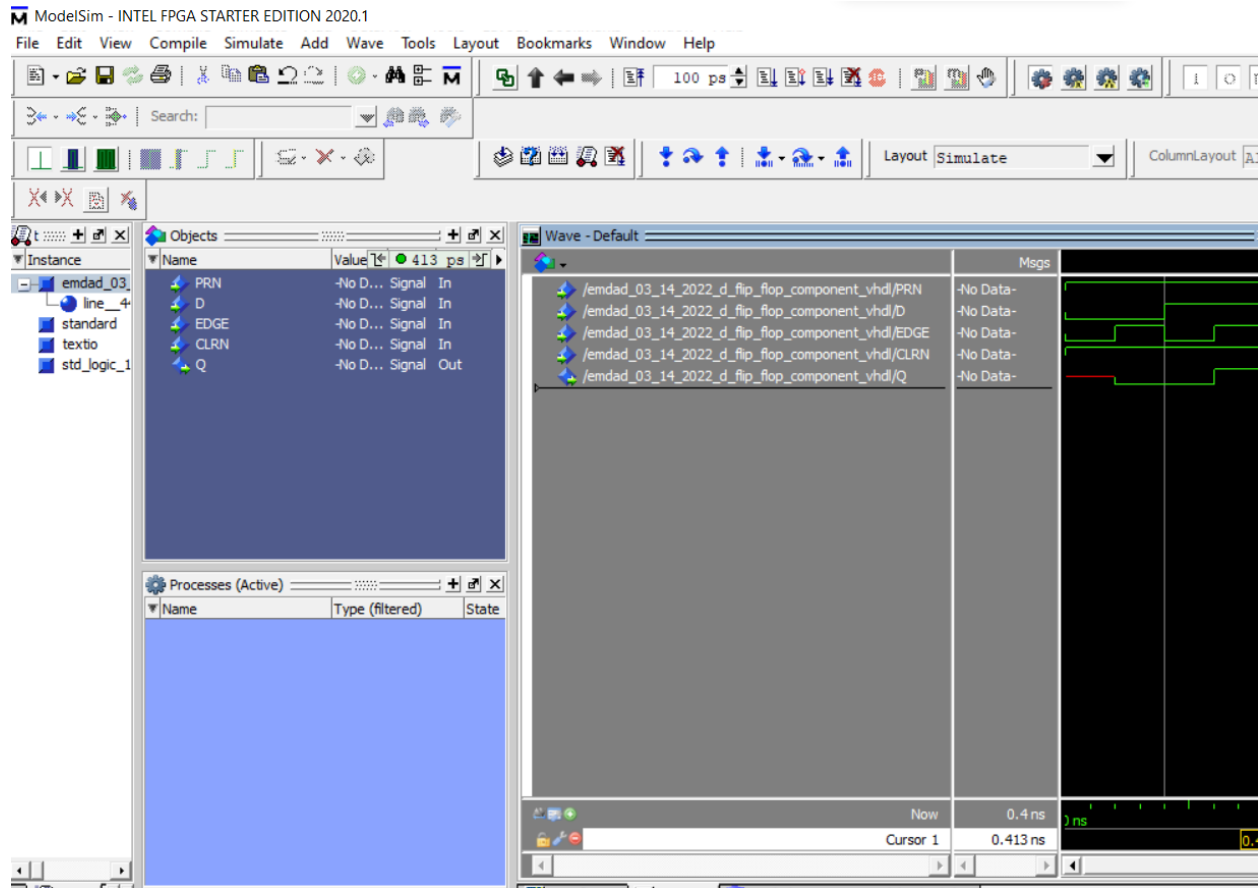


Figure 13: D flip-flop as a component symbol Simulation

As we can see in the picture, the waveform is correct because when EDGE(clock) changes from 0 to 1 and the value of D is transferred to Q which means a positive edge-triggered flip-flop.