Last NAME: Emdad First Name: MdShahid

Computer Science
C.Sc. 342/343

Quiz on Pipeline and Cache

CSc or CPE

Please submit to me as DM on slack by 6:15 PM. Thank you.

May 11, 2022

Please write your name on every page.

NO CORRECTIONS ARE ALLOWED !!!!! You may use back page for notes.

Please answer all questions. No computers are allowed.

Please hand write and sign statements affirming that you will not cheat:

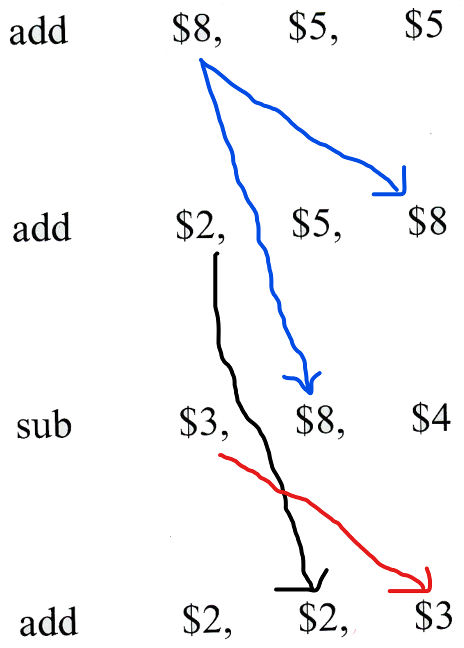
"I will neither give nor receive unauthorized assistance on this exam.
I will use only one computing device to perform this test"

Please hand write and sign **here:** I will neither give nor receive unauthorized assistance on this exam. I will use only one computing device to perform this test.

Shahid

Question 1: (20 points) Pipelined MIPS processor from the book.

Show or list all of the dependencies in this program. For each dependency, indicate which instructions and register are involved.



```
add    $8,    $5,    $5

add    $2,    $5,    $8

sub    $3,    $8,    $4

add    $2,    $2,    $3
```

You can draw the dependencies using ARROWS, or describe them in words:

Following the 5 steps of the instructions execution, the arrows were drawn. It is fetch, decode, execution, branch and register.

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Question 2: (20 points) Reordering Code to Avoid Pipeline Stalls

Consider the following code segment in C:

```
A=B+E;
C=B+ F;
```

Here is the generated MIPS code for this segment, assuming all variables are
in memory and are addressable using relative addressing mode i.e. using offsets from register $t0:

```
lw      $tl, 0($t0)
lw      $t2, 4($t0)
add     $t3, $tl,$t2
sw      $t3, 12($t0)
lw      $t4, 8($t0)
add     $t5, $tl,$t4
sw      $t5, 16($t0)
```

Find the hazards in the following code segment explain, and reorder the instructions to avoid any pipeline stalls.

The hazard in the following code segment is "add" instruction depends on "LW" before executing. There is space for the lw data to move forward. Therefore, "lw" instructions need to go first.

The correct reordered code:

```
lw $t1, 0($t0)
lw $t2, 4($t0)
lw $t4, 8($t0)
add $t3, $t1,$t2
sw $t3, 12($t0)
add $t5, $t1,$t4
SW $t5, 16($t0)
```

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Question 3: (20 points) **Cache computations**

Average Memory Access Time is computed: AMAT = Hit time + (Miss rate × Miss penalty)

Assuming that *memory transfers take a total of 80 clock cycles.*

If the cache has a 95% hit rate and a one-cycle hit time, what is the average memory access time?

Hit time is 1 because it one cycle.
Miss rate = 100% - 95% = 1 - 0.95 = 0.05
Miss penalty = number of clock cycles

AMAT = Hit time + (Miss rate * Miss penalty)
AMAT = 1+(0.05*80)
AMAT = 5

Question 4: (20 points) What are the two characteristics of program memory accesses that caches exploit?

The two characteristics of program memory accesses that caches exploit are temporal locality (in time) and spatial locality (in space). In temporal locality, if a memory location is reference, it will most likely get referenced back soon. In spatial locality, if a memory location is reference, the location with nearby address most like get referenced back soon.

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Question 5: **(10 points)**

Please describe in one sentence what Cache miss is.

Cache miss happens when a program tries accessing data from the cache, but the piece of data is missing/can't be traced.

Question 6: **(10 points)**

Please describe in one sentence what is Cache hit.

Cache hit happens when a program tries accessing data from the cache, and the piece of data was traceable/found.