ModelSim Simulation: Buzzer & Mux4_1

MdShahid Bin Emdad

February 16th, 2022

CSC 34200/34300

Table of Contents

Objective	3
Description of Specifications, and Functionality	3
Explanation	7
Conclusion	,

Objective:

The objective of this assignment is to create a Buzzer circuit simulation using Modelsim and subsequently create mux_4_1 circuit with.

Description of Specifications, and Functionality:

The digital system I used in this assignment is ModelSimSetup-20.1.1. In the VHDL editor, I wrote my VHDL code to get the circuit output and then used Modelsim to simulate and run my circuit over time (ns unit).

I. Buzzer Circuit

In figure 1, I inserted my code from the page and then compiled *buzzer.vhd* successfully.

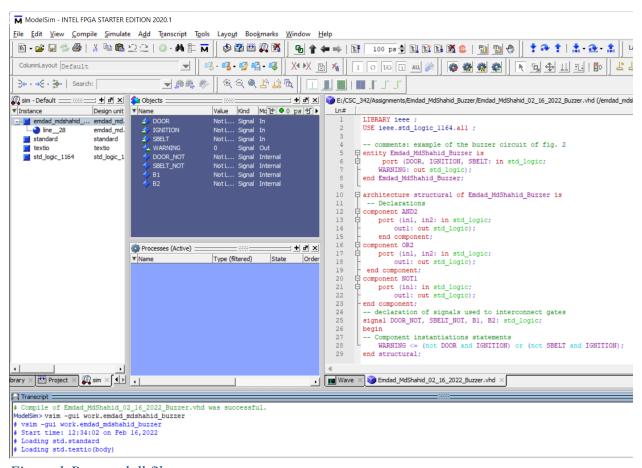
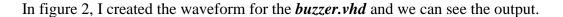


Figure 1:Buzzer vhdl file



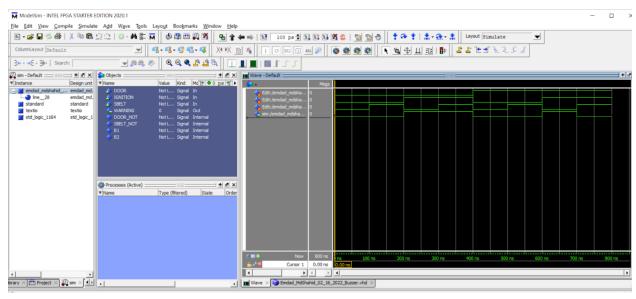


Figure 2: Waveform Output

In figure 3, I did the AND2 component and it compiled successfuly.

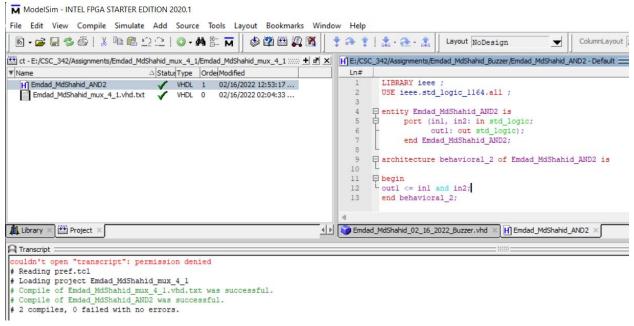


Figure 3: AND2 component

In figure 4, I did the OR2 component and it compiled successfuly.

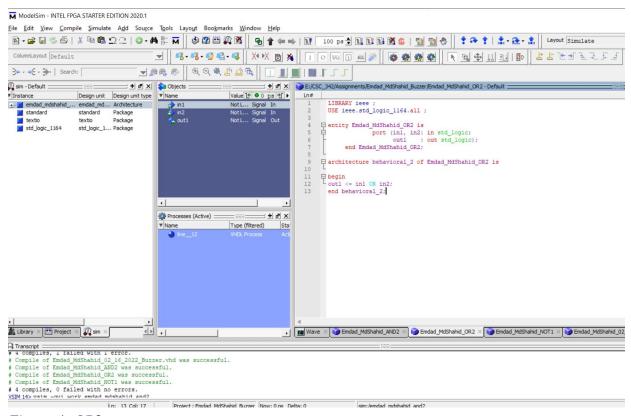


Figure 4: OR2 component

In figure 5, I did the NOT1 component and it compiled successfuly.

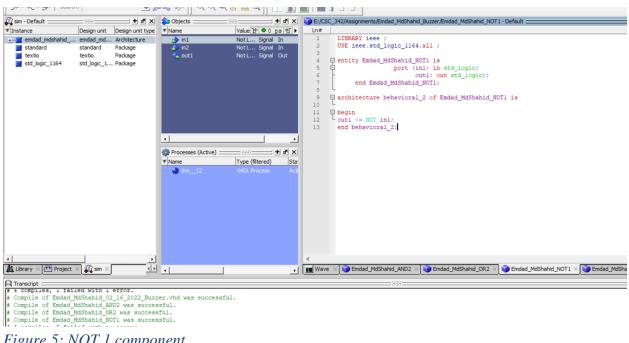


Figure 5: NOT 1 component

II. <u>4:1 mux 1-bit</u>

In figure 6, I added the existed the file in the new project and then compiled it. As we can, the VHDL compiled successfully.

```
M ModelSim - INTEL FPGA STARTER EDITION 2020.1
File Edit View Compile Simulate Add Project Tools Layout Bookmarks Window Help
 Layout NoDesign
                                                                                                                                ColumnLayout AllColumns
📆 Project - E:/CSC_342/Assignments/Emdad_MdShahid_mux_4_1/Emdad_MdShahid_mux_4_1.vhd.txt - Default =
                                △ Status Type Order Modified
                                                                                           library IEEE:
 E E
                                                                                           use IEEE.STD_LOGIC_1164.ALL;
                                                                                         entity Emdad_MdShahid_mux_4_1 is
port (sel : in std logic vec
                                                                                              port (sel : in std logic_vector(2 downto 1);
    A, B, C, D: in std_logic;
    Z : out std_logic);
                                                                                           end Emdad_MdShahid_mux_4_1;
                                                                                    10
11
12
13
14
15
16
17
18
                                                                                           architecture behav_mux_4_1 of Emdad_MdShahid_mux_4_1 is
                                                                                        begin

PR_MUX: process(sel, A, B, C, D)
                                                                                                   case sel is
                                                                                                   when "00" => Z <= A;
when "01" => Z <= B;
when "10" => Z <= C;
                                                                                                     when others => Z <= D;
                                                                                                   end case:
                                                                                               end process PR_MUX;
                                                                                           end behav mux 4 1;
Library × Project ×
                                                                             # Compile of Emdad_MdShahid_mux_4_1.vhd.txt was successful.
```

Figure 6: Mux_4_1

In figure 7, we can see the final output of all the waveforms.

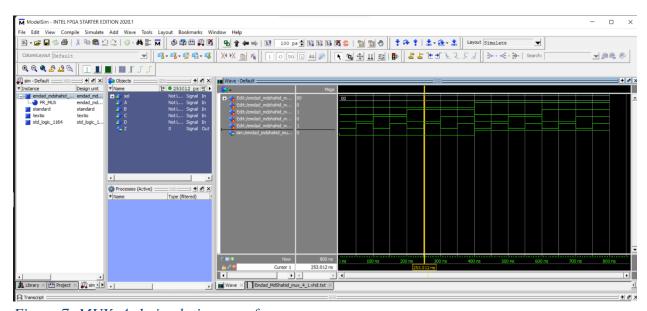


Figure 7: MUX_4_1 simulation waveform

Explanation:

For part A, I used the page code and then compiled them. For the mux_4_1, I did the same thing. I used the boolean expression to check my work. I set the wave and clock pattern and attributes in that way. Then I ran the simulation to see if my output wave matched with the truth table and it did. Hence, the waveforms are right.

Conclusion:

This assignment was helpful to learn modelism and simulation in Modelism software. It was a thorough and brief practice to learn the software. The operations and condition logics were helpful to learn easily. The truth table helped me to get the circuit waveform quicker. I relearned and reviewed the concept again and which will help me in the course further.