Self-Check Laboratory Exercise 4A

MdShahid Bin Emdad

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CSC 34200/34300

Part 1: D Latch Component, simulation and verification with Model-Sim

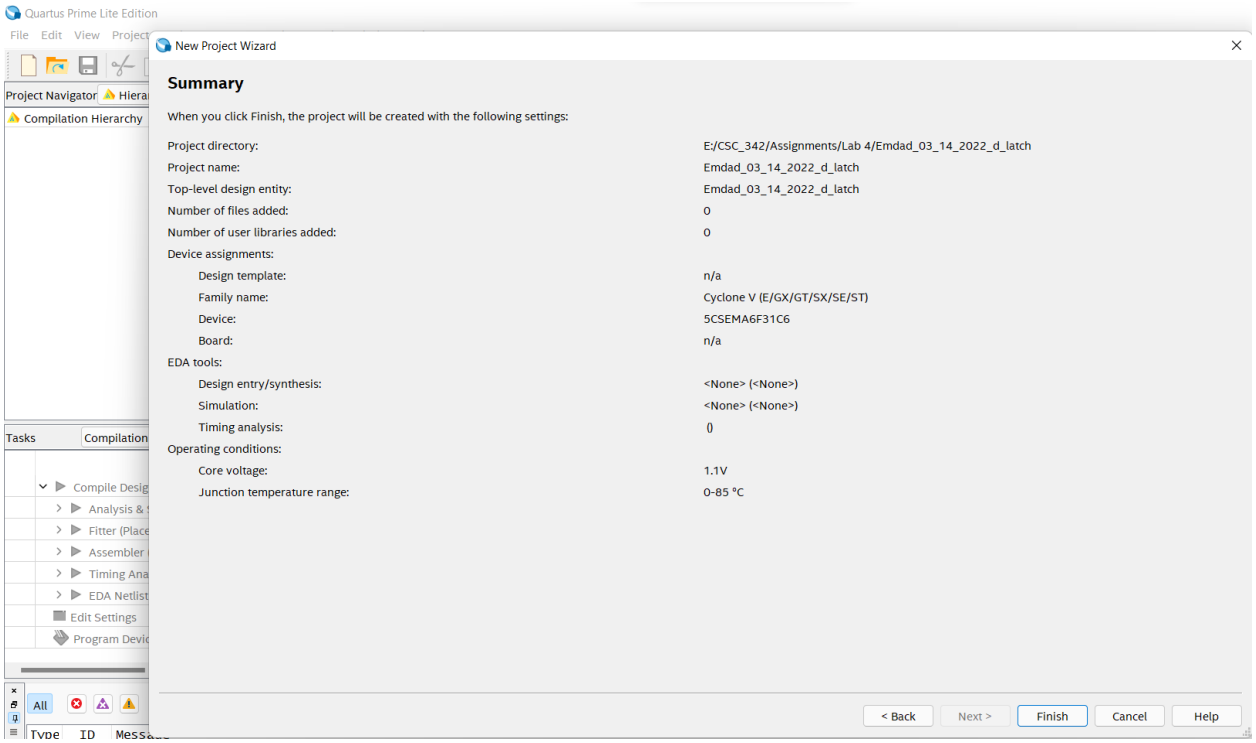


Figure 1: Project Summary

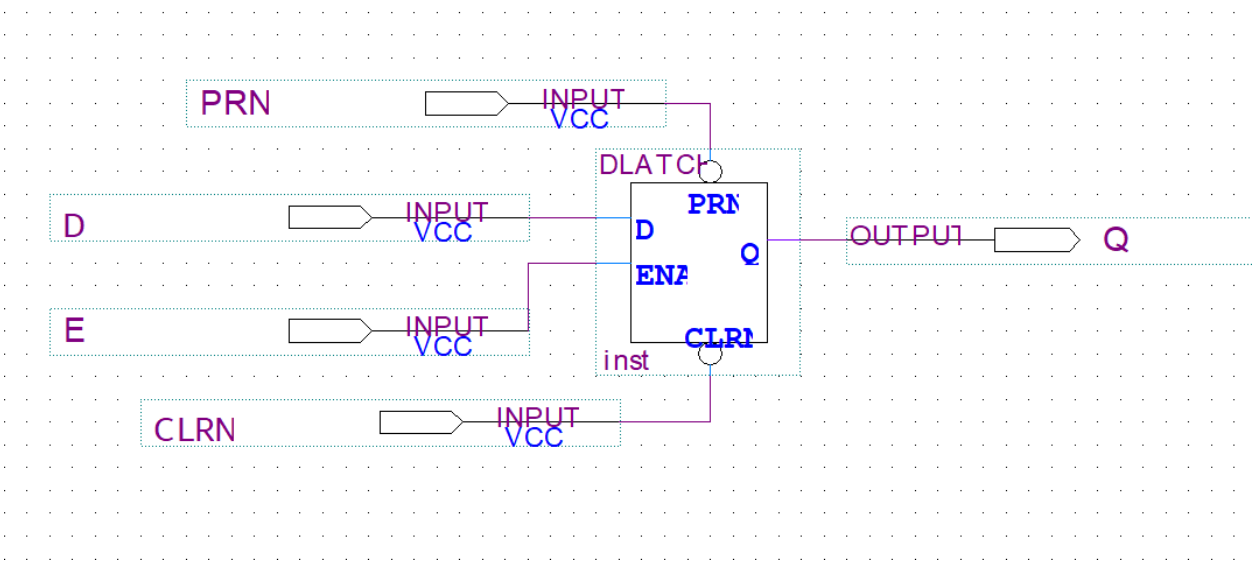


Figure 2: D-Latch Component

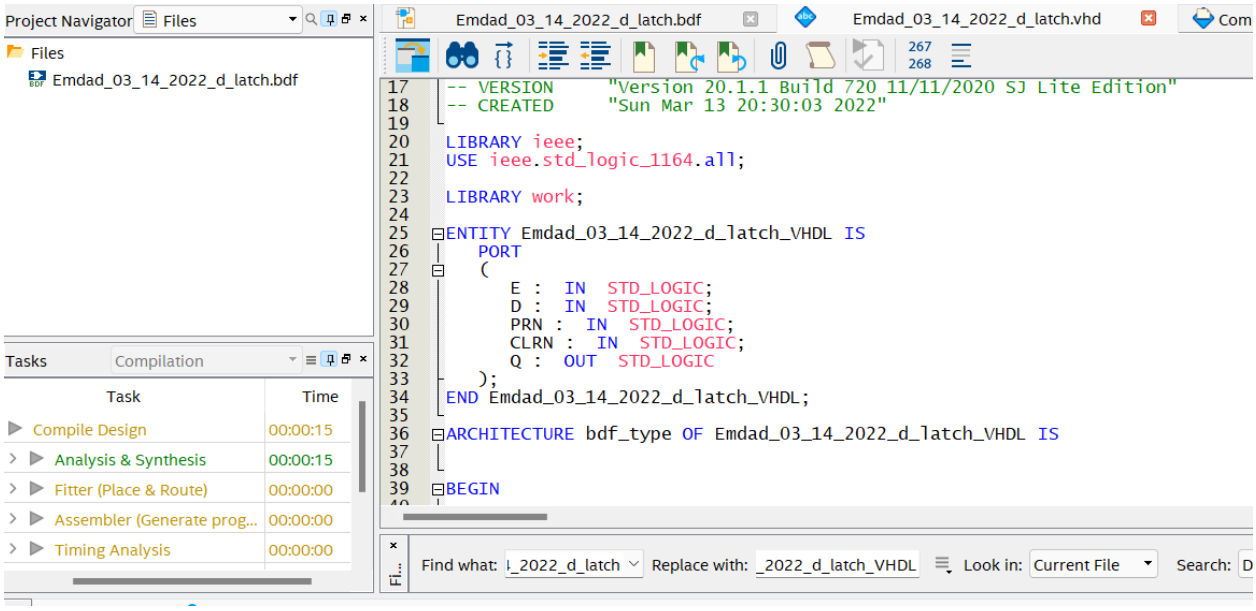


Figure 3: : D Latch VHDL code

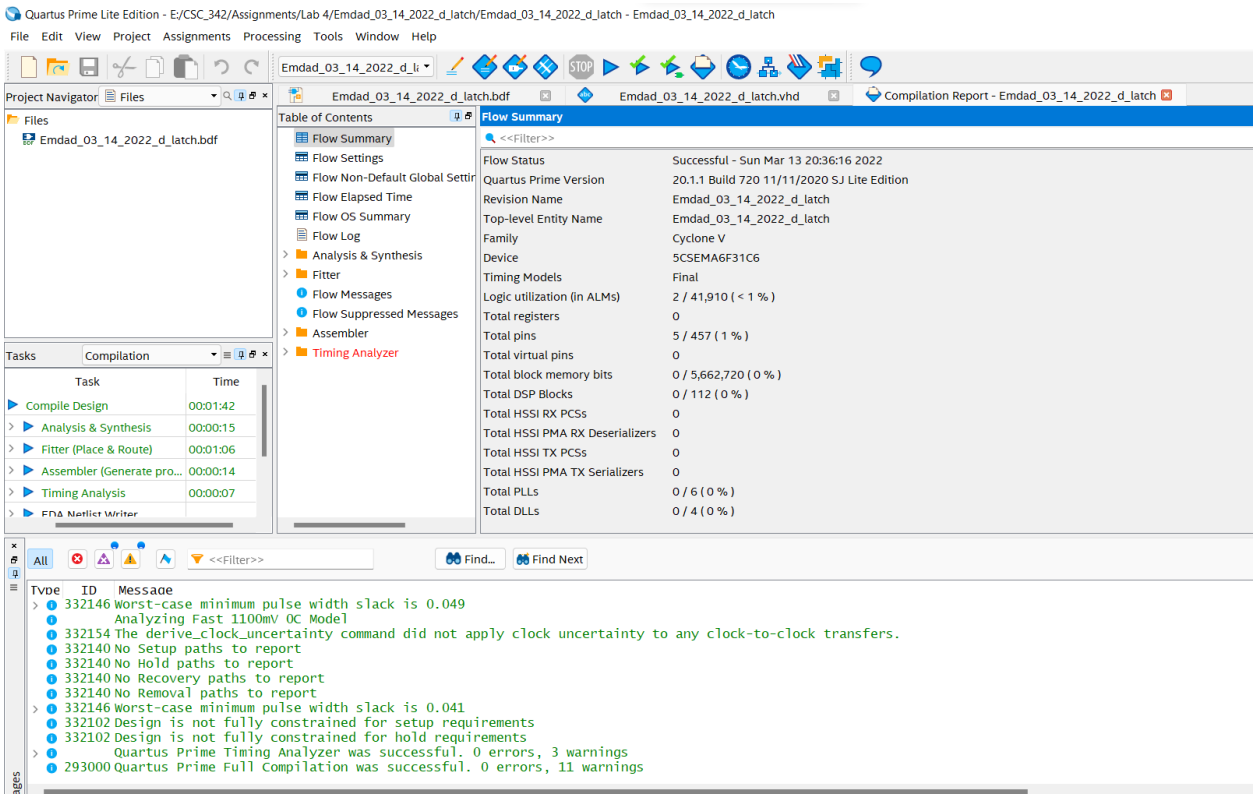


Figure 4: D Latch VHDL code Compilation Successfully

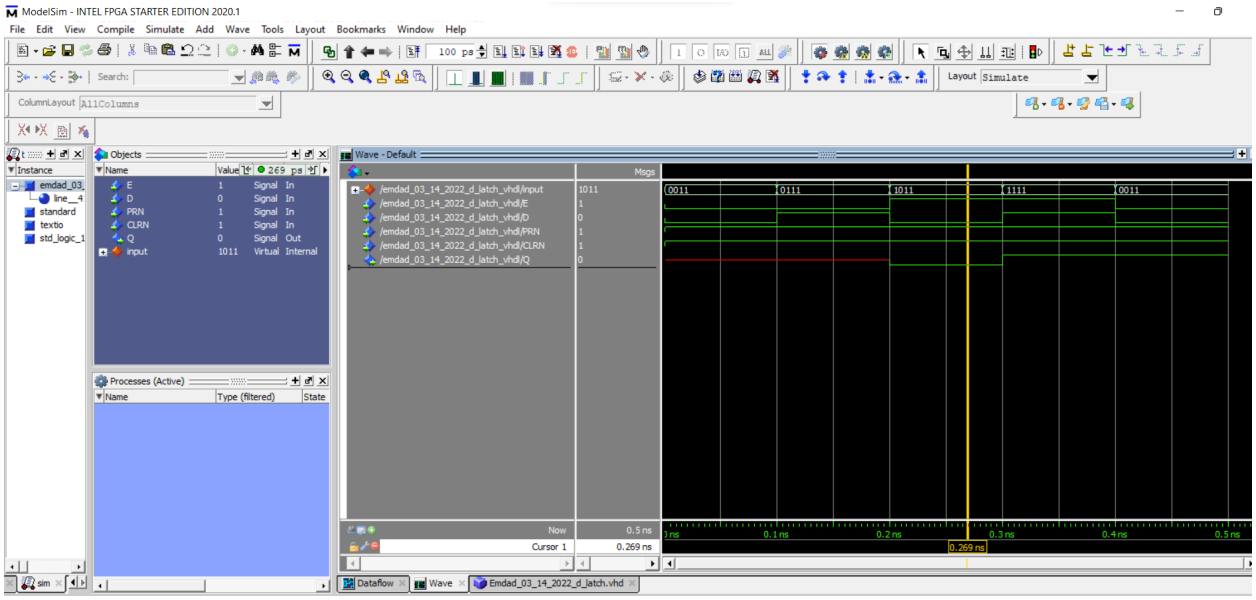
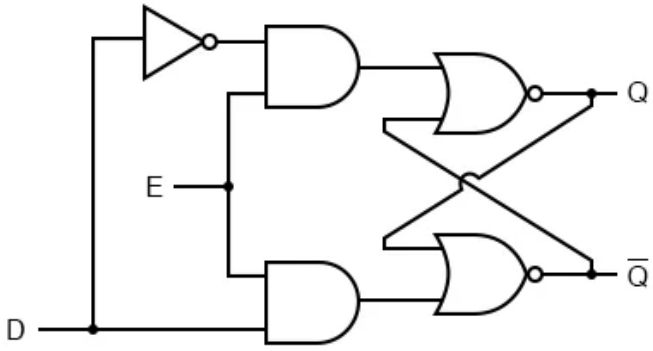


Figure 5: D Latch Simulation Waveform

I did this waveform by following the truth table:



E	D	Q	$\overline{Q}$
0	0	latch	latch
0	1	latch	latch
1	0	0	1
1	1	1	0

Figure 6: D Latch Truth Table

It has to match the output waveform therefore it is right.

Part 2: Master-Slave D flip-flop using D Latches and simulation with Model-Sim

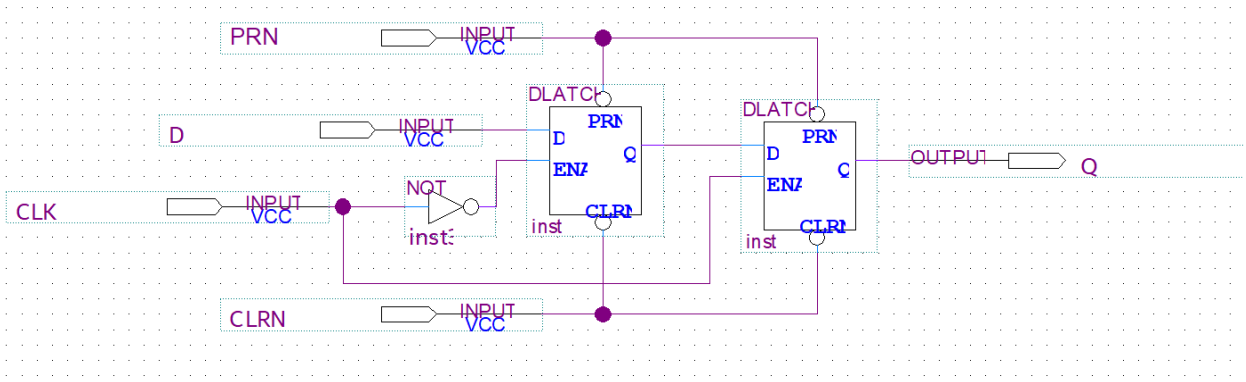


Figure 7: Master-Slave D flip-flop using D Latches

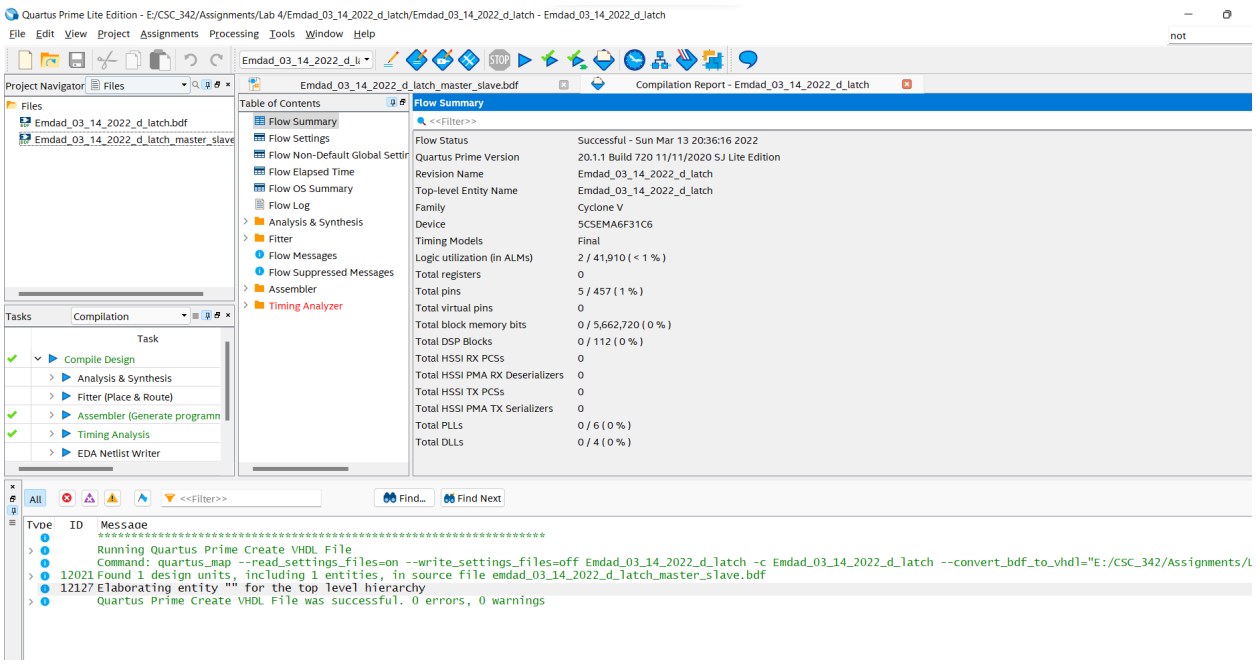


Figure 8: Compilation Successfully

Text Editor - E:/CSC_342/Assignments/Lab 4/Emdad_03_14_2022_d_latch/Emdad_03_14_2022_d_latch - Emdad_03_14_2022_d_latch - [Emdad_03_14_2022_d_latch_master_slave.vhd]

File Edit View Project Processing Tools Window Help

```
-- PROGRAM      "Quartus Prime"
-- VERSION      "Version 20.1.1 Build 720 11/11/2020 SJ Lite Edition"
-- CREATED      "Sun Mar 13 21:24:08 2022"

LIBRARY ieee;
USE ieee.std_logic_1164.all;

LIBRARY work;

ENTITY Emdad_03_14_2022_d_latch_master_slave IS
    PORT
    (
        PRN :  IN  STD_LOGIC;
        D :  IN  STD_LOGIC;
        CLK :  IN  STD_LOGIC;
        CLRN :  IN  STD_LOGIC;
        Q :  OUT  STD_LOGIC
    );
END Emdad_03_14_2022_d_latch_master_slave;

ARCHITECTURE bdf_type OF Emdad_03_14_2022_d_latch_master_slave IS

SIGNAL    SYNTHESIZED_WIRE_0 :  STD_LOGIC;
SIGNAL    SYNTHESIZED_WIRE_1 :  STD_LOGIC;

BEGIN

PROCESS(CLRN,PRN,SYNTHESIZED_WIRE_0,D)
BEGIN
IF (CLRN = '0') THEN
    SYNTHESIZED_WIRE_1 <= '0';
ELSIF (PRN = '0') THEN
    SYNTHESIZED_WIRE_1 <= '1';
ELSIF (SYNTHESIZED_WIRE_0 = '1') THEN
    SYNTHESIZED_WIRE_1 <= D;
END IF;
END PROCESS;


PROCESS(CLRN,PRN,CLK,SYNTHESIZED_WIRE_1)
BEGIN
IF (CLRN = '0') THEN
    Q <= '0';
ELSIF (PRN = '0') THEN
    Q <= '1';
ELSIF (CLK = '1') THEN
    Q <= SYNTHESIZED_WIRE_1;
END IF;
END PROCESS;

SYNTHESIZED_WIRE_0 <= NOT(CLK);

END bdf_type;
```

Figure 9: Master-Slave D flip-flop using D Latches VHDL Code

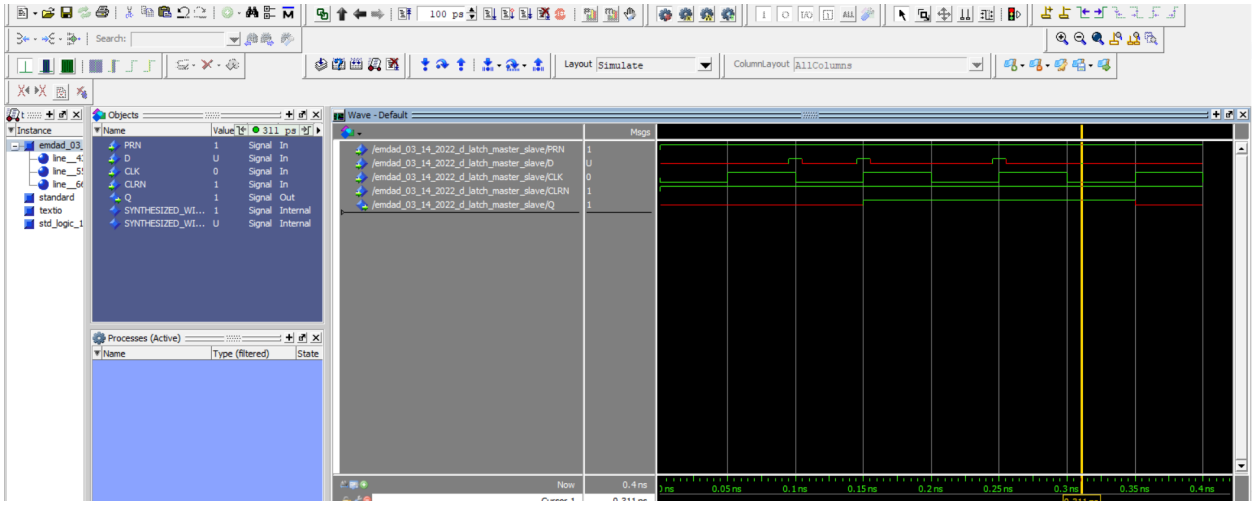


Figure 10: D Latch Simulation Waveform

The waveforms are correct as it has the same waveform as D flip-flop we made from the built-in component.

Part 3: Using D flip-flop as a component symbol and simulation with Model-Sim

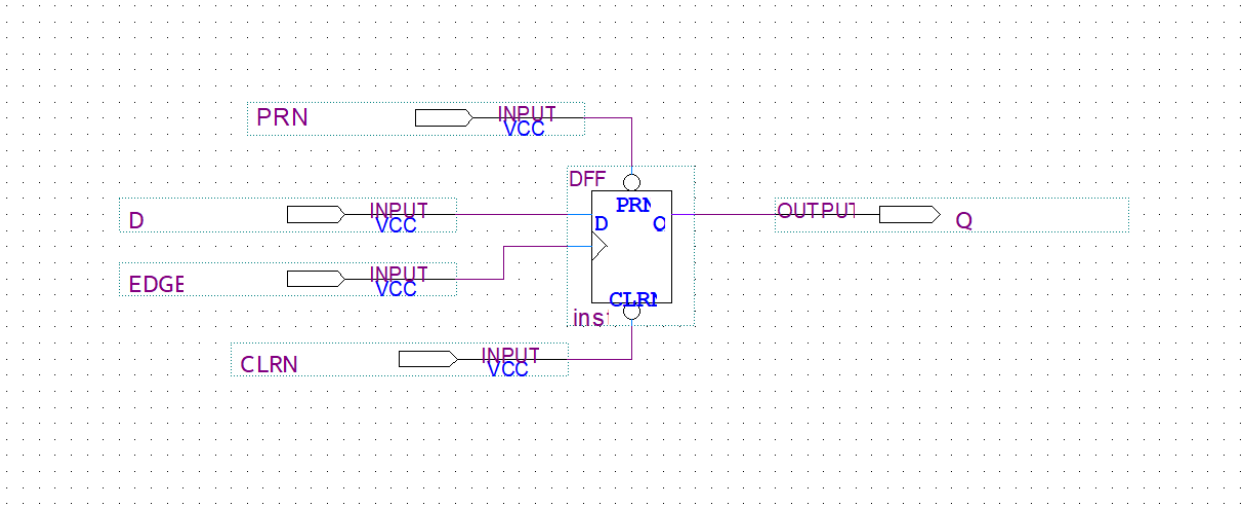


Figure 11: D flip-flop as a component symbol

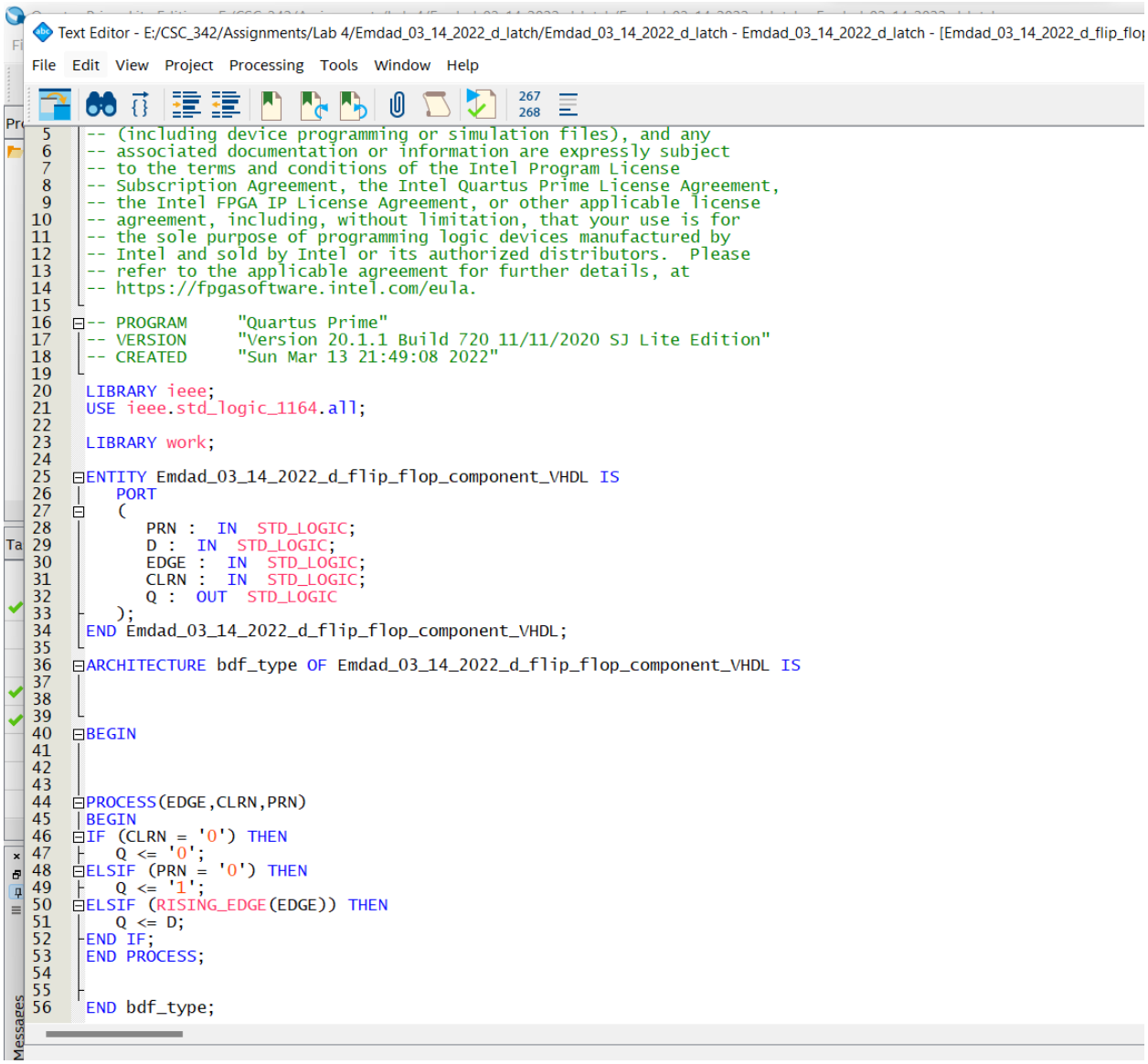


Figure 12: D flip-flop as a component symbol VHDL Code

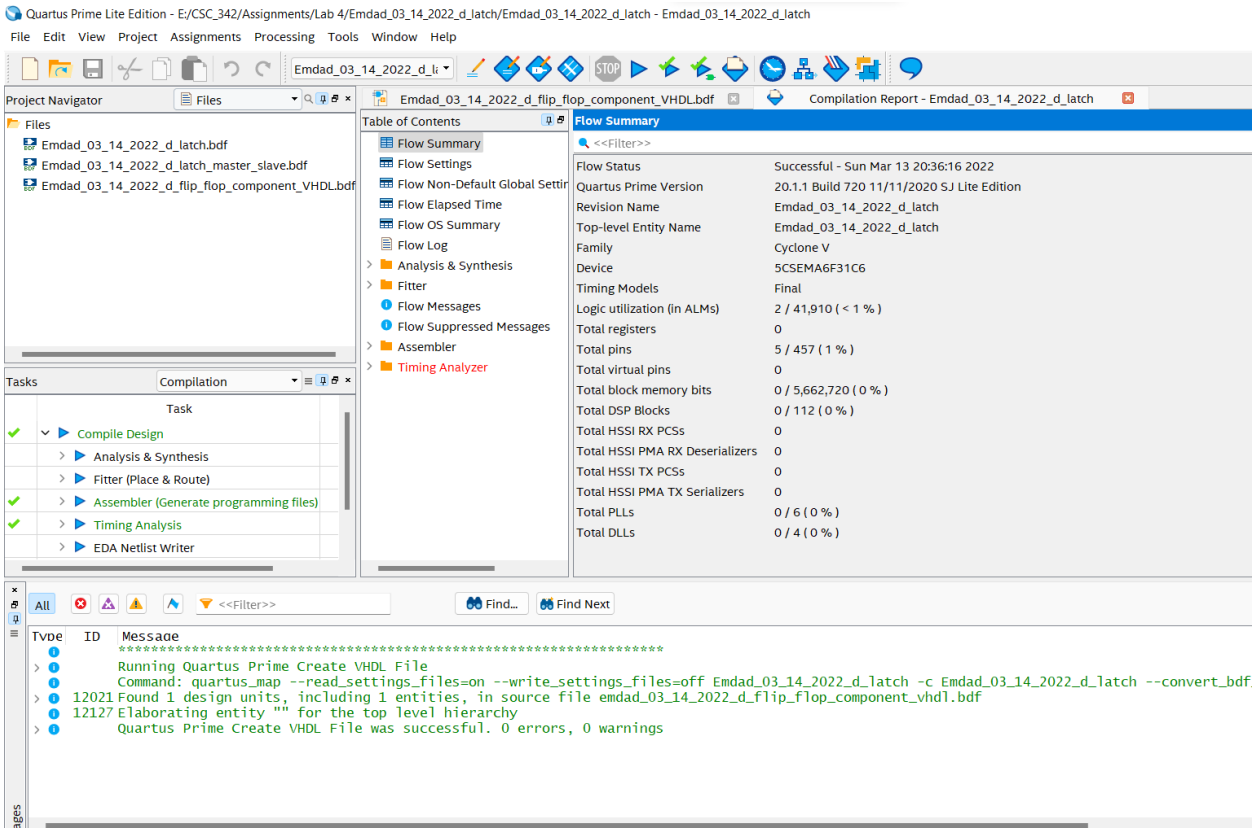


Figure 13: Compiled design successful

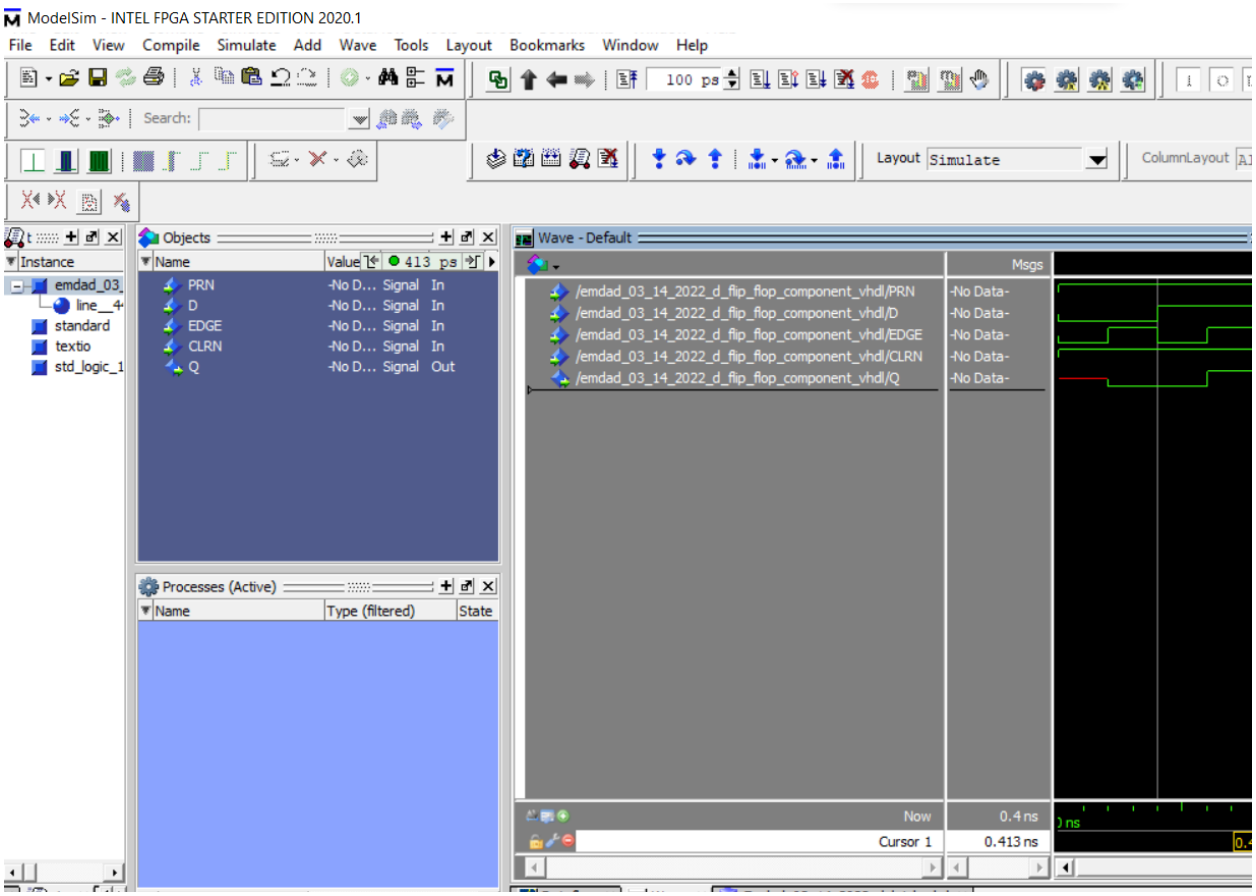


Figure 13: D flip-flop as a component symbol Simulation

As we can see in the picture, the waveform is correct because when EDGE(clock) changes from 0 to 1 and the value of D is transferred to Q which means a positive edge-triggered flip-flop.