Laboratory Project: Review Memory Lab

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CSC 34200/34300

Design An LPM RAM 1-PORT:

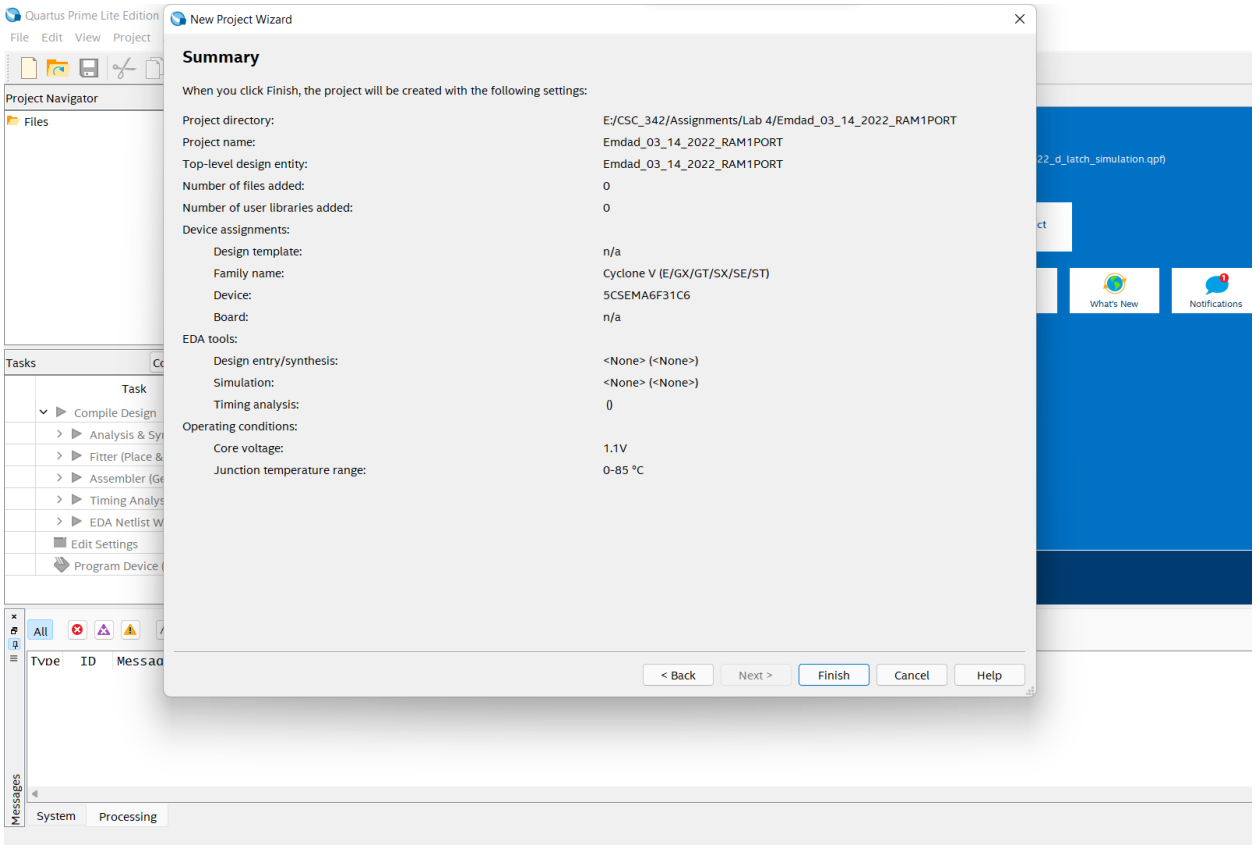

Figure 1: Project Summary

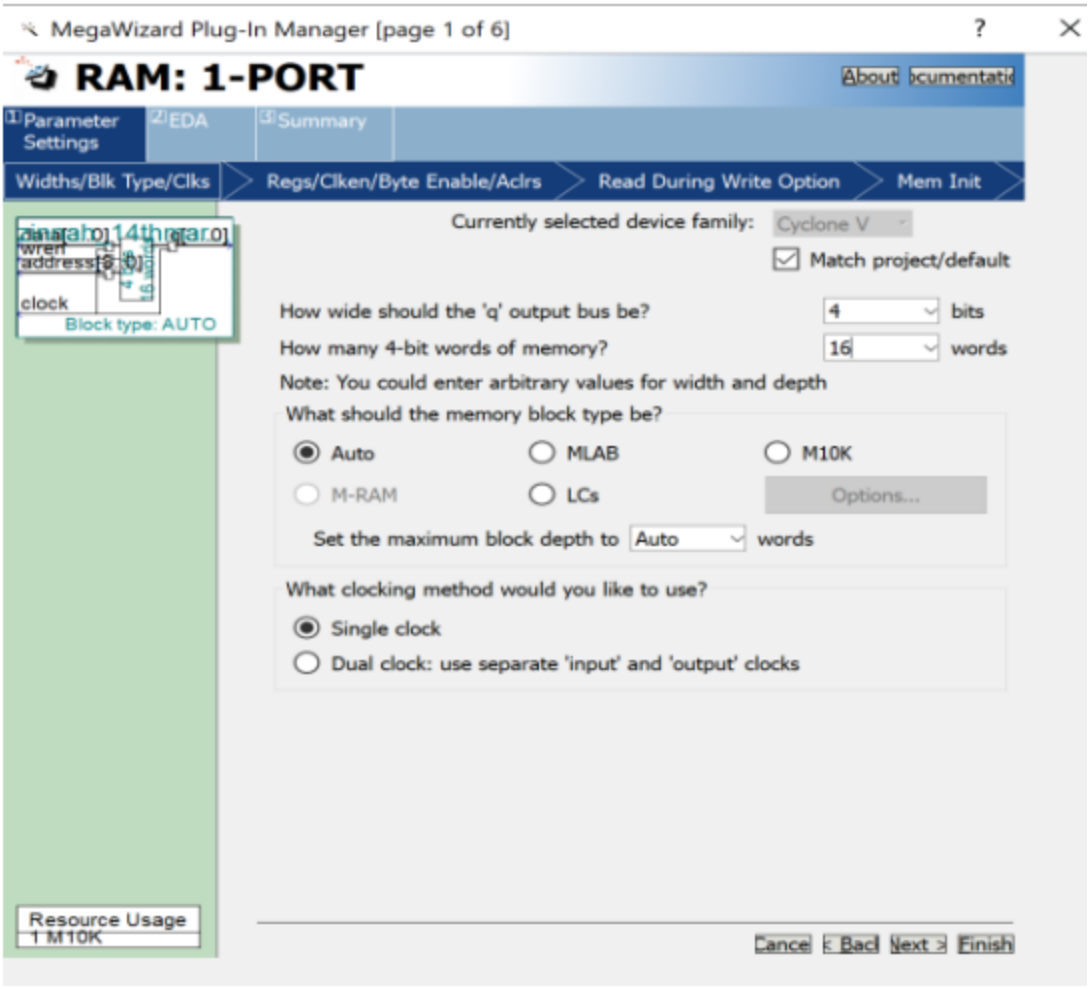

Figure 2: Parameter settings for q output and words of memory

E:/CSC_342/Assignments/Lab 4/Emdad_03_14_2022_RAM1PORT/Emdad_14thMarch_RAM1PORT.vhd

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E:/CSC_342/Assignments/Lab 4/Emdad_03_14_2022_RAM1PORT/Emdad_14thMarch_RAM1PORT.vhd - Default *

```
Ln#
40  LIBRARY altera_mf;
41  USE altera_mf.altera_mf_components.all;
42
43  ENTITY Emdad_14thMarch_RAM1PORT IS
44          PORT
45          (
46                  address         : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
47                  clock           : IN STD_LOGIC  := '1';
48                  data            : IN STD_LOGIC_VECTOR (3 DOWNTO 0);
49                  wren            : IN STD_LOGIC ;
50                  q               : OUT STD_LOGIC_VECTOR (3 DOWNTO 0)
51          );
52  END Emdad_14thMarch_RAM1PORT;
53
54
55  ARCHITECTURE SYN OF emdad_14thmarch_ram1port IS
56
57          SIGNAL sub_wire0        : STD_LOGIC_VECTOR (3 DOWNTO 0);
58
59  BEGIN
60          q    <= sub_wire0(3 DOWNTO 0);
61
62          altsyncram_component : altsyncram
63          GENERIC MAP (
64                  clock_enable_input_a => "BYPASS",
65                  clock_enable_output_a => "BYPASS",
66                  intended_device_family => "Cyclone V",
67                  lpm_hint => "ENABLE_RUNTIME_MOD=NO",
68                  lpm_type => "altsyncram",
69                  numwords_a => 16,
70                  operation_mode => "SINGLE_PORT",
71                  outdata_aclr_a => "NONE",
72                  outdata_reg_a => "CLOCK0",
73                  power_up_uninitialized => "FALSE",
74                  read_during_write_mode_port_a => "NEW_DATA_NO_NBE_READ",
75                  widthad_a => 4,
76                  width_a => 4,
77                  width_byteena_a => 1
78          )
79          PORT MAP (
80                  address_a => address,
81                  clock0 => clock,
82                  data_a => data,
83                  wren_a => wren,
84                  q_a => sub_wire0
85          );
86  END SYN;
```

Figure 3: LPM RAM 1-PORT VHDL Code

It compiled successfully. This is the most interesting project so far as we can use this method further to create LPM Ports without even coding. The LPM module gave it to us. Therefore, it was great learning.