Self-Check Laboratory Exercise 4B

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CSC 34200/34300

Design N-bit Register:

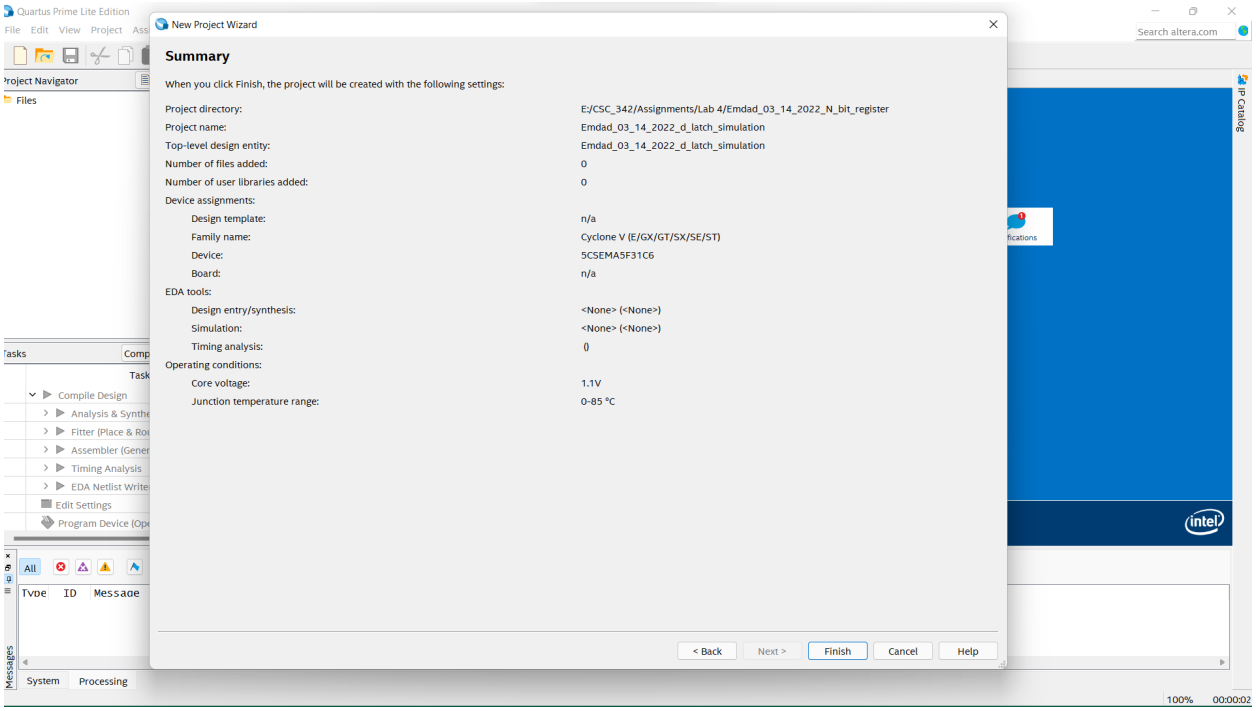

Figure 1: Project Summary

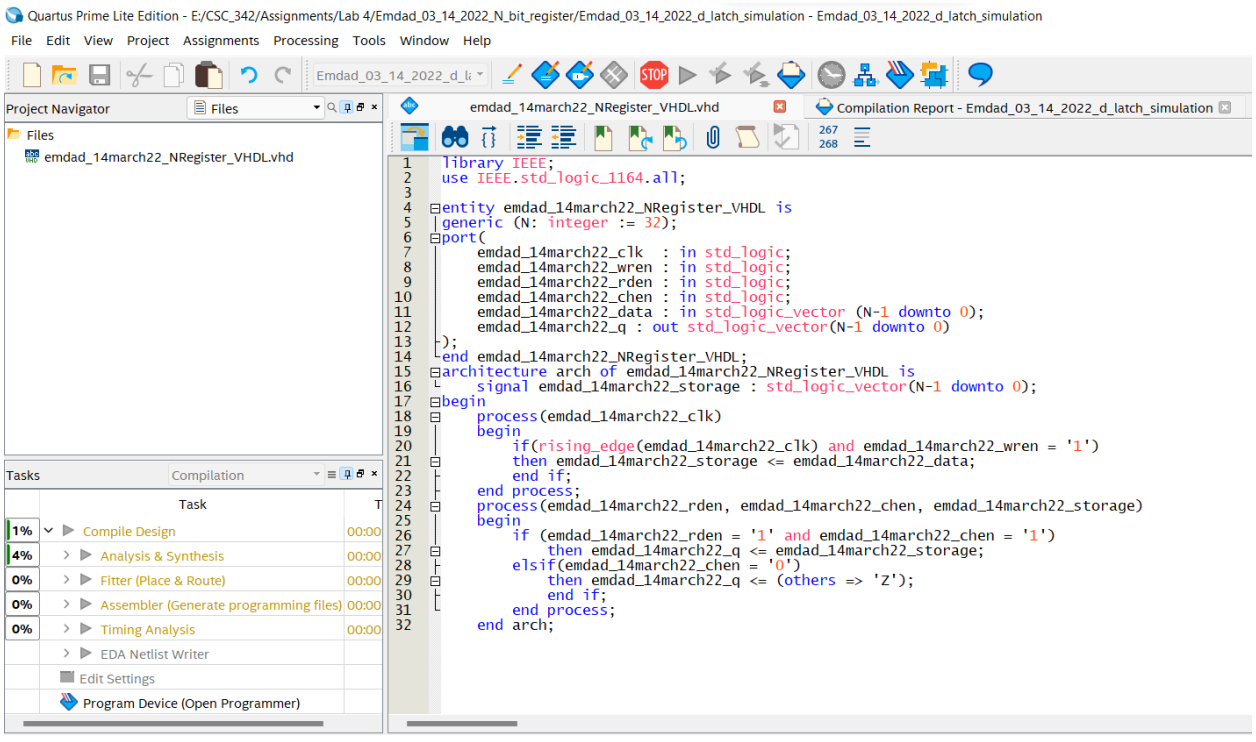

Figure 2: N-bit register VHDL code

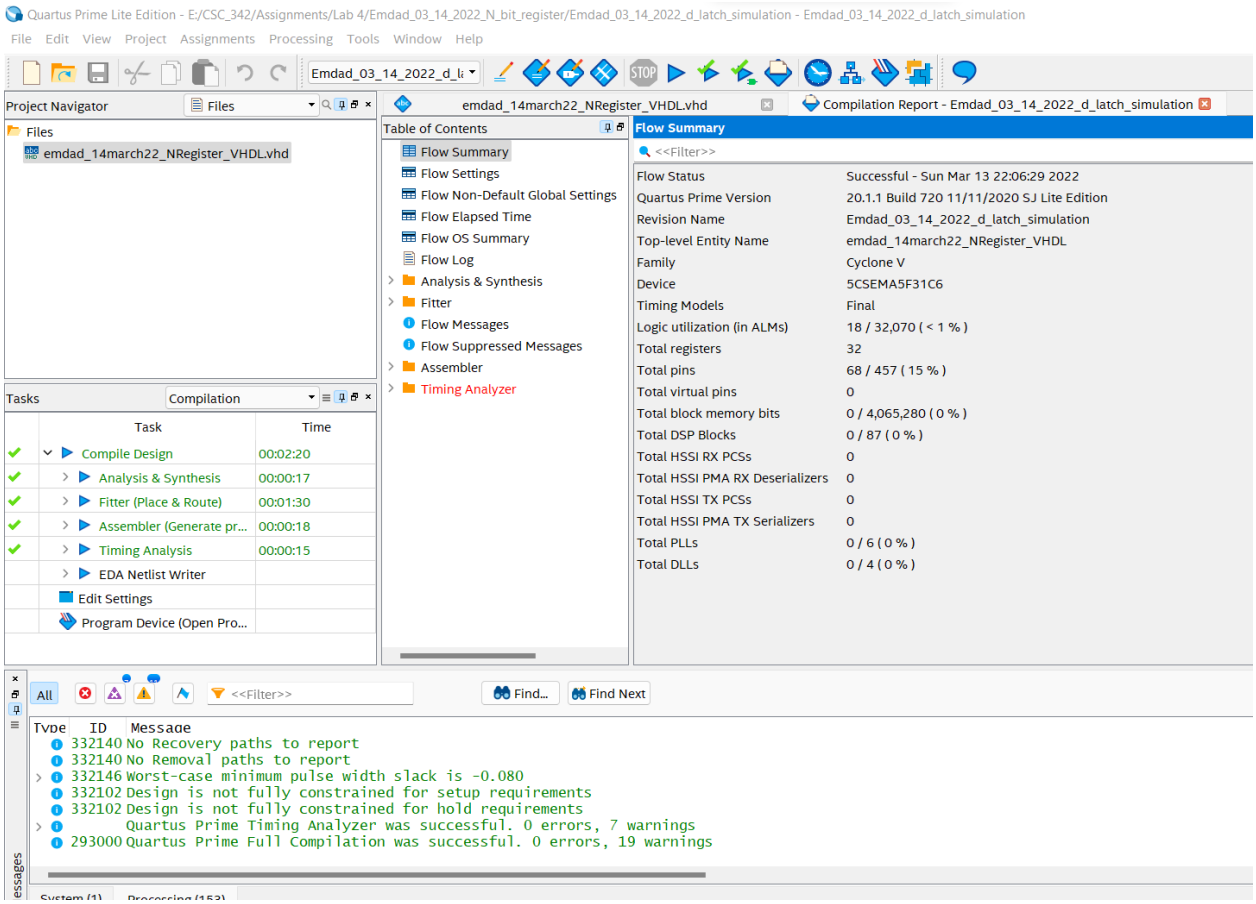

Figure 3: Compiled Successfully

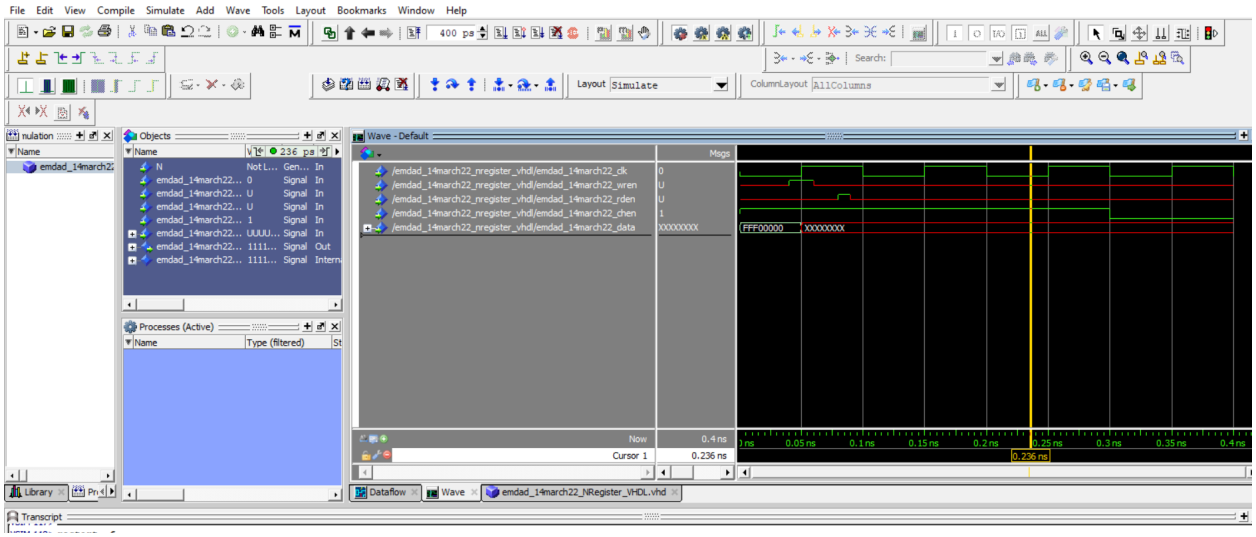

Figure 4: N-bit register simulation

The design is correct because if we observe closely we can see that the read and chip value does not change even if the storage space changes which allows the output to read new data all time.