Computer Science
C.Sc. 342/343
Spring 2022

Last Name: Emdad **First Name:** Md Shahid

Self Test on CPU Controls
To be performed
12:00-1:40 PM and 2:00-3:40 PM on May 4, 2022
Please submit as direct message on Slack to Instructor

Please write your Last Name and First Name on every page:

NO CORRECTIONS ARE ALLOWED!

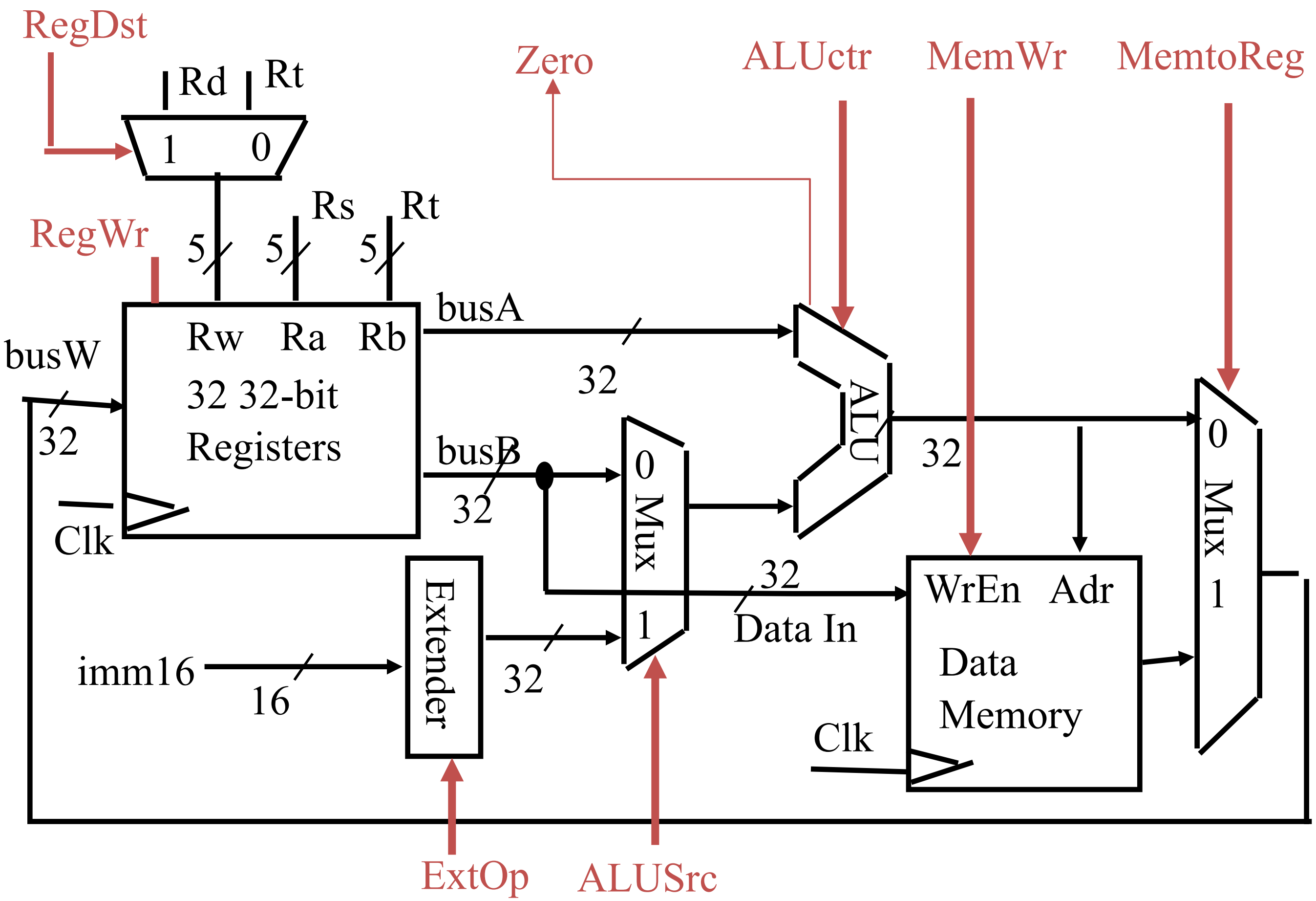
PLEASE SELECT THE CORRECT ROW AND EXPLAIN YOUR ANSWERS IN NO MORE THAN TWO SENTENCES.

Please hand write and sign statements affirming that you will not cheat: Shahid
"I will neither give nor receive unauthorized assistance on this exam.
I will use only one computing device to perform this test"
Please hand write and sign **here:** I will neither give nor receive unauthorized assistance on this exam. I will use only one computing device to perform this test.

Meaning of the Control Signals

- ExtOp: 0 ⇒ “zero” ; 1 ⇒ “sign”
- ALUsrc: 0 ⇒ regB; 1 ⇒ immed
- ALUctr: “add”, “sub”, “or”

- MemWr: 1 ⇒ write memory
- MemtoReg: 0 ⇒ ALU; 1 ⇒ Mem
- RegDst: 0 ⇒ “rt”; 1 ⇒ “rd”
- RegWr: 1 ⇒ write register



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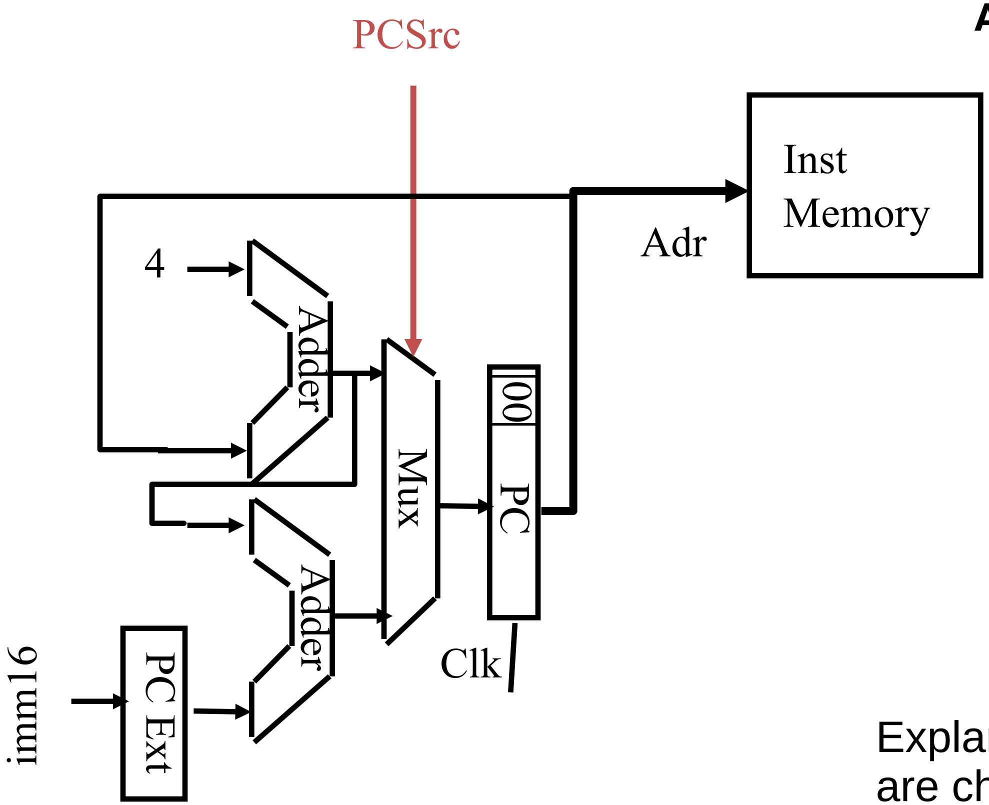
Setting PC Source Control Signal

- PCSrc: 0 ⇒ PC <= PC + 4
  1 ⇒ PC <= PC + 4 + {SignExt(Im16), 2’b00}
- Later in lecture: higher-level connection between mux and branch cond



Answer?	AddU	SubU	ORI	LW	SW	BEQ
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	1
3	0	0	0	1	1	1
4	0	0	1	1	1	1
5	0	1	1	1	1	1
6	1	1	1	1	1	1
7	1	1	1	1	1	X
8	X	X	X	X	X	1
9	None of the above					

Explanation: The answer is 1 because we are checking two adder components by using branch equal. We do not need to use store word and load word and the adders.

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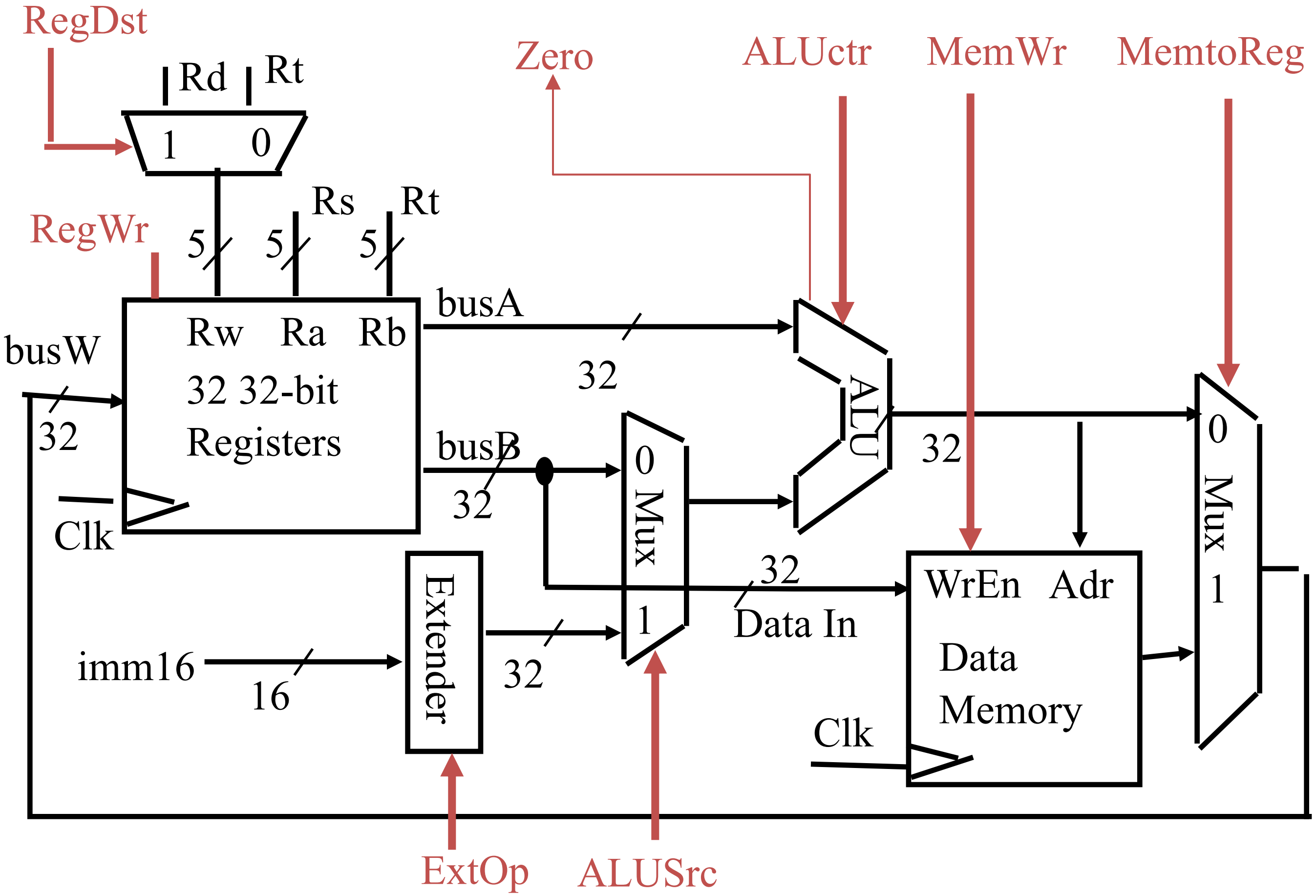

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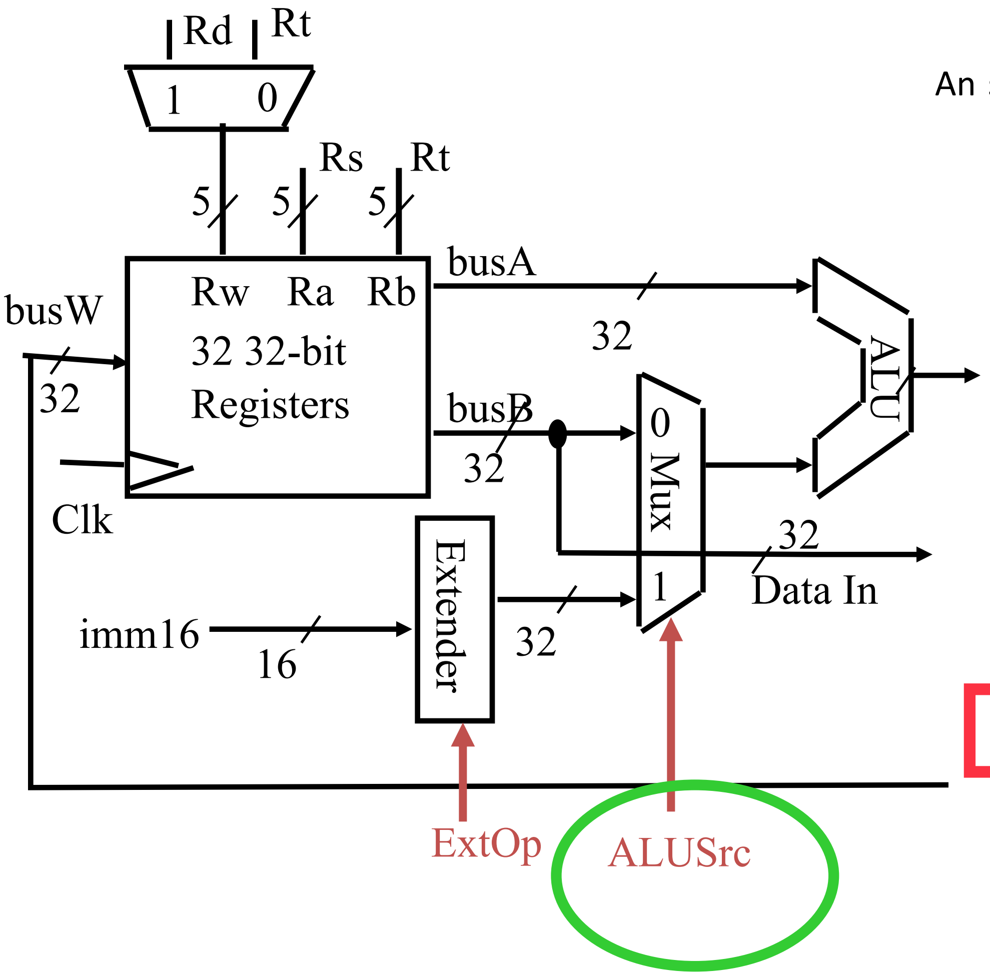
Specify ALU source mux Control

- ALUsrc: 0 ⇒ reg as ALU B input; 1 ⇒ immediate as ALU B input



Answer?	AddU	SubU	ORI	LW	SW	BEQ
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	1
3	0	0	1	1	1	0
4	0	0	0	1	1	1
5	0	0	0	1	1	X
6	1	1	1	1	1	1
7	1	1	1	1	1	X
8	X	X	X	X	X	1
9	None of the above					

The answer is 9 because none of the answer is correct. The input data is only sign extended for those 3 instructions.

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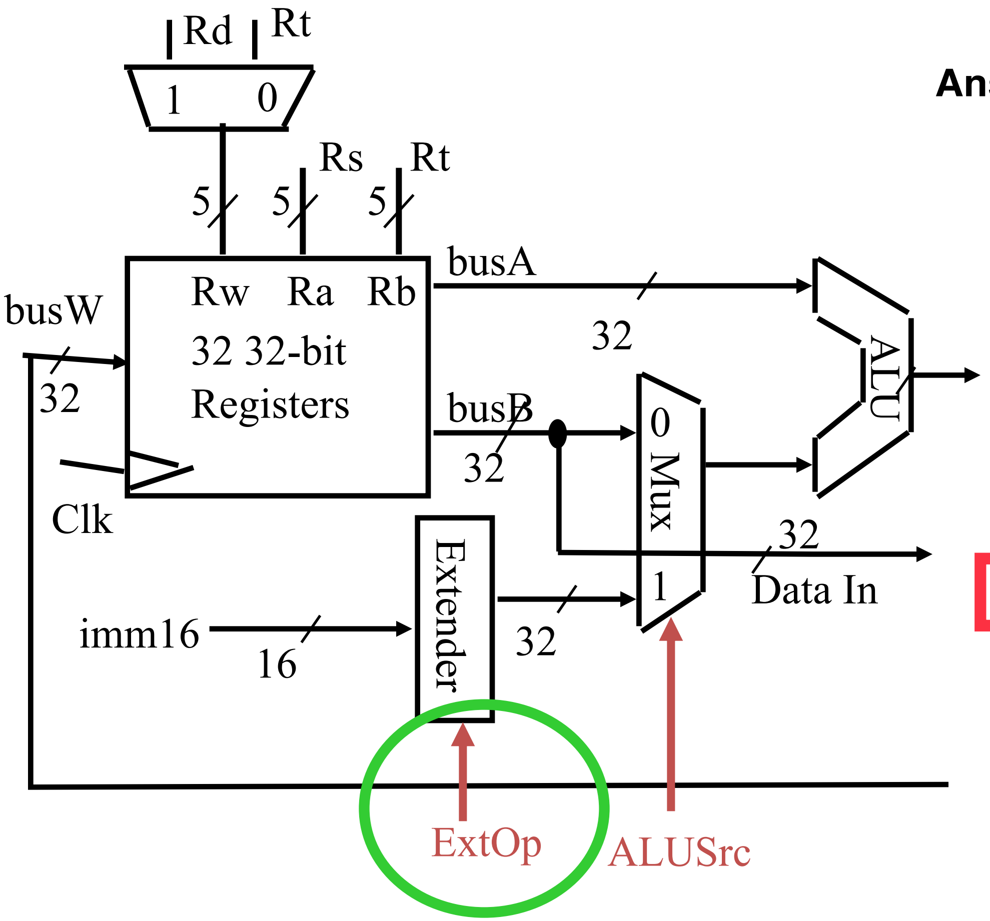
Specify Immediate Extender Op Control

- ExtOp: 0 ⇒ “zero extend immediate” ; 1 ⇒ “sign extend imm.”



Answer?	AddU	SubU	ORI	LW	SW	BEQ
0	0	0	0	0	0	1
1	0	0	0	0	1	1
2	0	0	0	1	1	1
3	0	0	1	1	1	1
4	0	1	1	1	1	1
5	1	1	1	1	1	1
6	X	0	1	1	1	1
7	X	X	0	1	1	1
8	X	X	1	0	0	0
9	None of the above					

The answer is 7 because we are using ExtOp. AddU and SubU, we don't need to extend so we will not use it. ORI is 0 and sign extension for the rest is 1.

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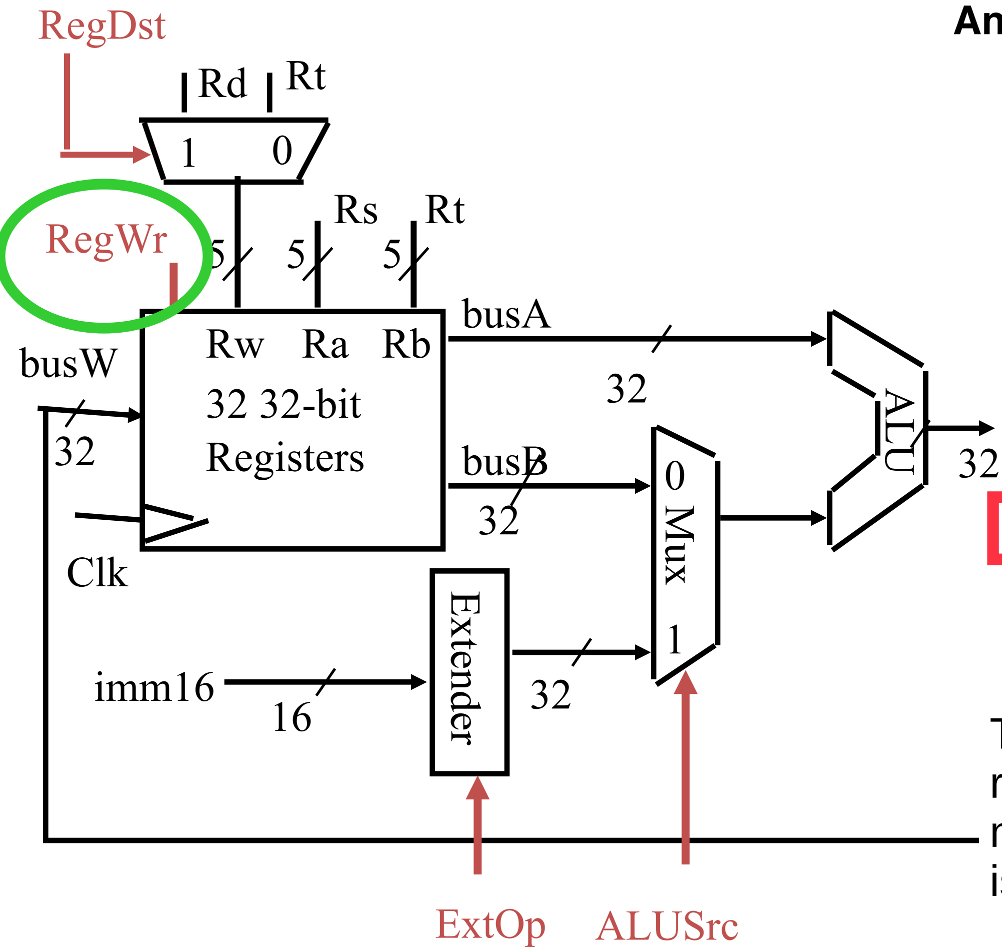
Specify Register Write Control

- RegWr: 1 ⇒ write register



Answer?	AddU	SubU	ORI	LW	SW	BEQ
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	1
3	0	0	0	1	1	1
4	0	0	1	1	1	1
5	0	1	1	1	1	1
6	1	1	1	1	1	1
7	1	1	1	1	0	0
8	1	1	1	1	X	X
9	None of the above					

The answer is 7 because we are using write register. AddU, SubU, ORI and LW is 1 meaning it was enables and for SW and BEQ is 0, meaning write register isnt enabled.

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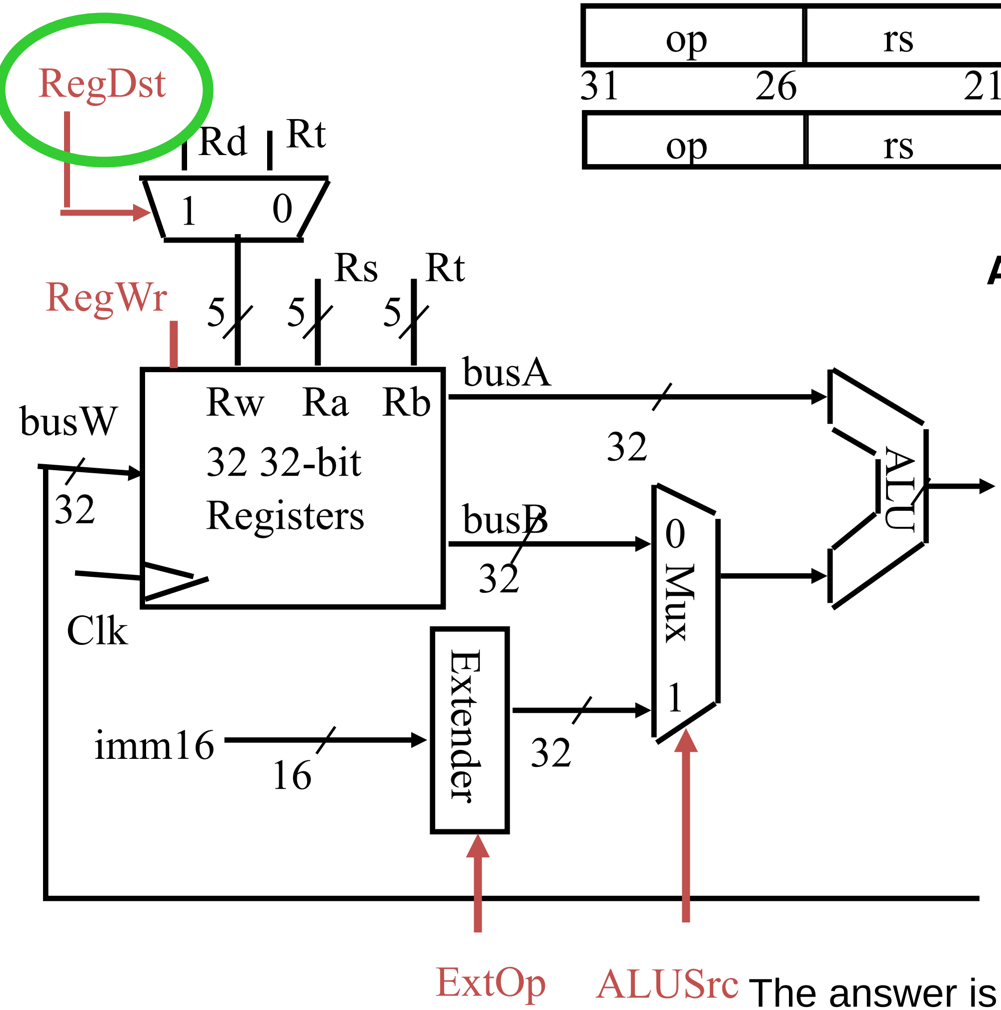
Specify Register Destination Control

- RegDst: 0 ⇒ “rt”; 1 ⇒ “rd”

31 26	21	16	11	6	0
op	rs	rt	rd	shamt	funct

31 26	21	16	0
op	rs	rt	immediate



Answer?	AddU	SubU	ORI	LW	SW	BEQ
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	1
3	0	0	0	1	1	0
4	0	0	1	1	0	0
5	0	1	1	0	0	0
6	1	1	0	0	0	0
7	1	1	0	0	X	X
8	1	1	0	0	0	X
9	None of the above					

The answer is 7 because for destination register, SW and BEQ could either be 0 or 1. AddU and SubU needs to be 1. we only write to rt for the ORI and LW instructions.

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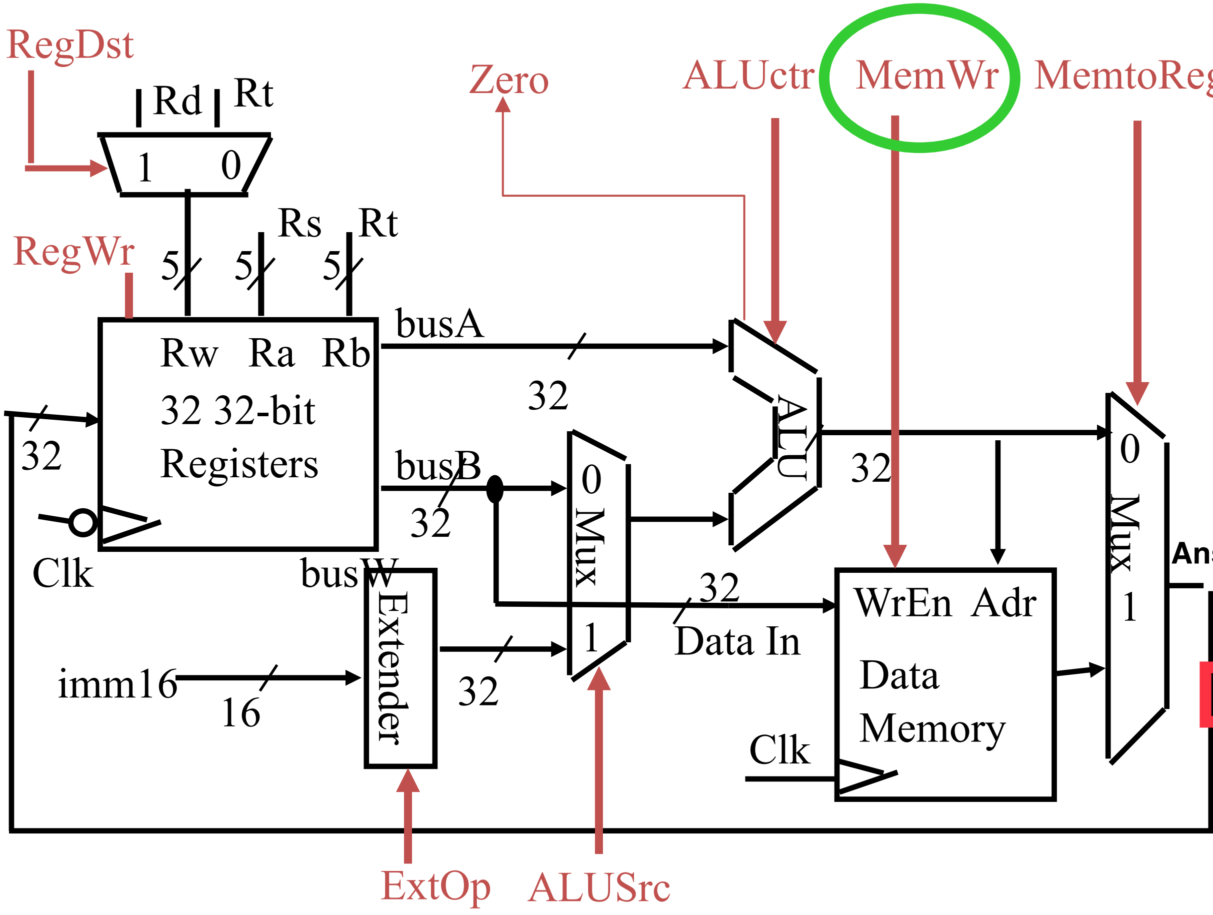
Specify the Memory Write Control Signal

- MemWr: 1 ⇒ write memory



Answer?	AddU	SubU	ORI	LW	SW	BEQ
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	0	0	0	1	0	0
4	0	0	1	0	0	0
5	0	1	0	0	0	0
6	1	0	0	0	0	0
7	0	0	0	0	1	X
8	X	X	X	0	1	X
9	None of the above					

The answer is 2 because SW only writes data to memory so it needs to be 1 to write the memory.

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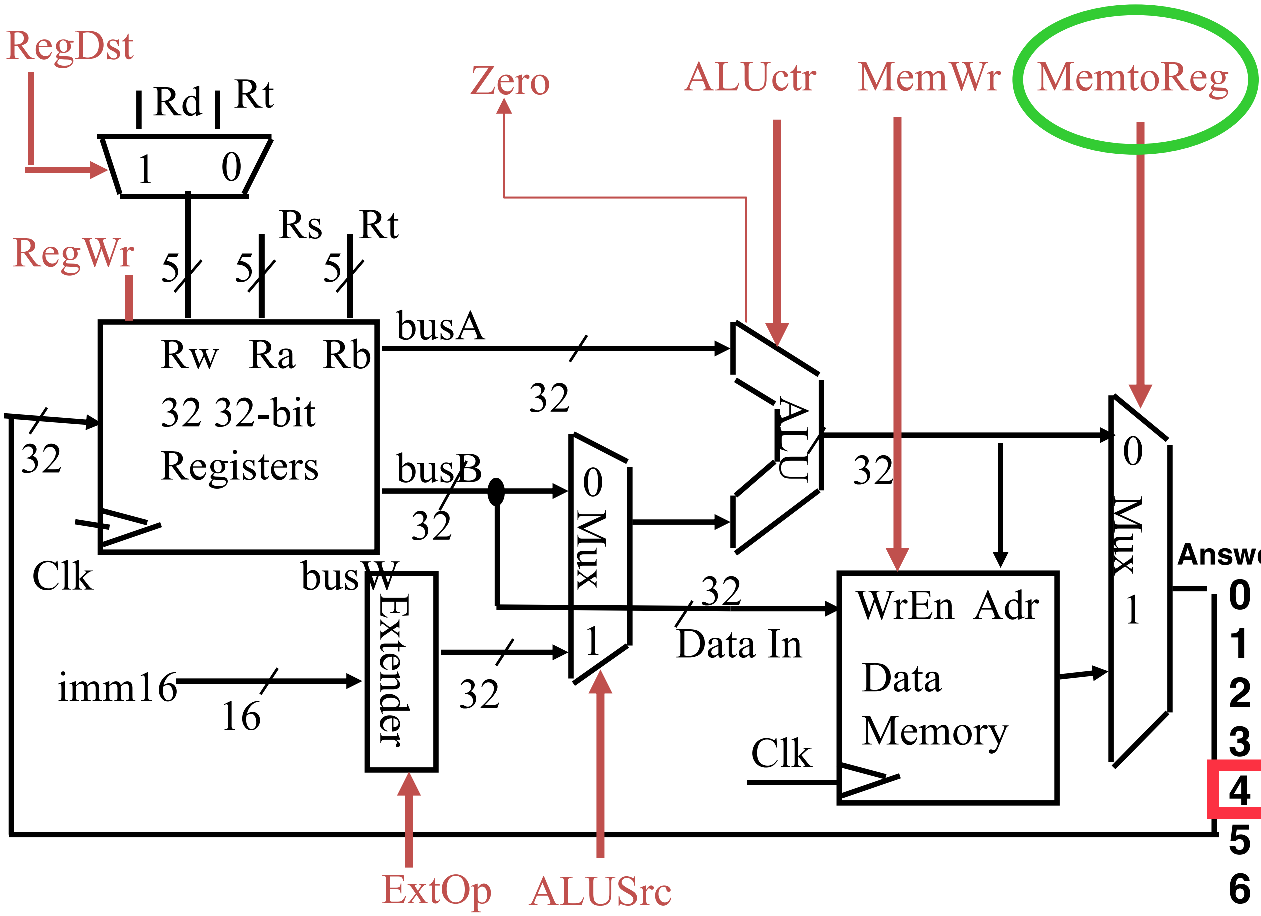
Specify Memory To Register File Mux Control

- MemtoReg:0 ⇒ ALU; 1 ⇒ Mem



Answer?	AddU	SubU	ORI	LW	SW	BEQ
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	0	0	0	1	0
3	0	0	0	1	0	X
4	0	0	0	1	X	X
5	0	1	0	0	0	0
6	1	0	0	0	0	0
7	0	0	0	0	1	X
8	0	0	0	1	0	X
9	None of the above					

The answer is 4 because we need load word enables to read the data from memory. We do not need SW and BEQ so it does not matter.

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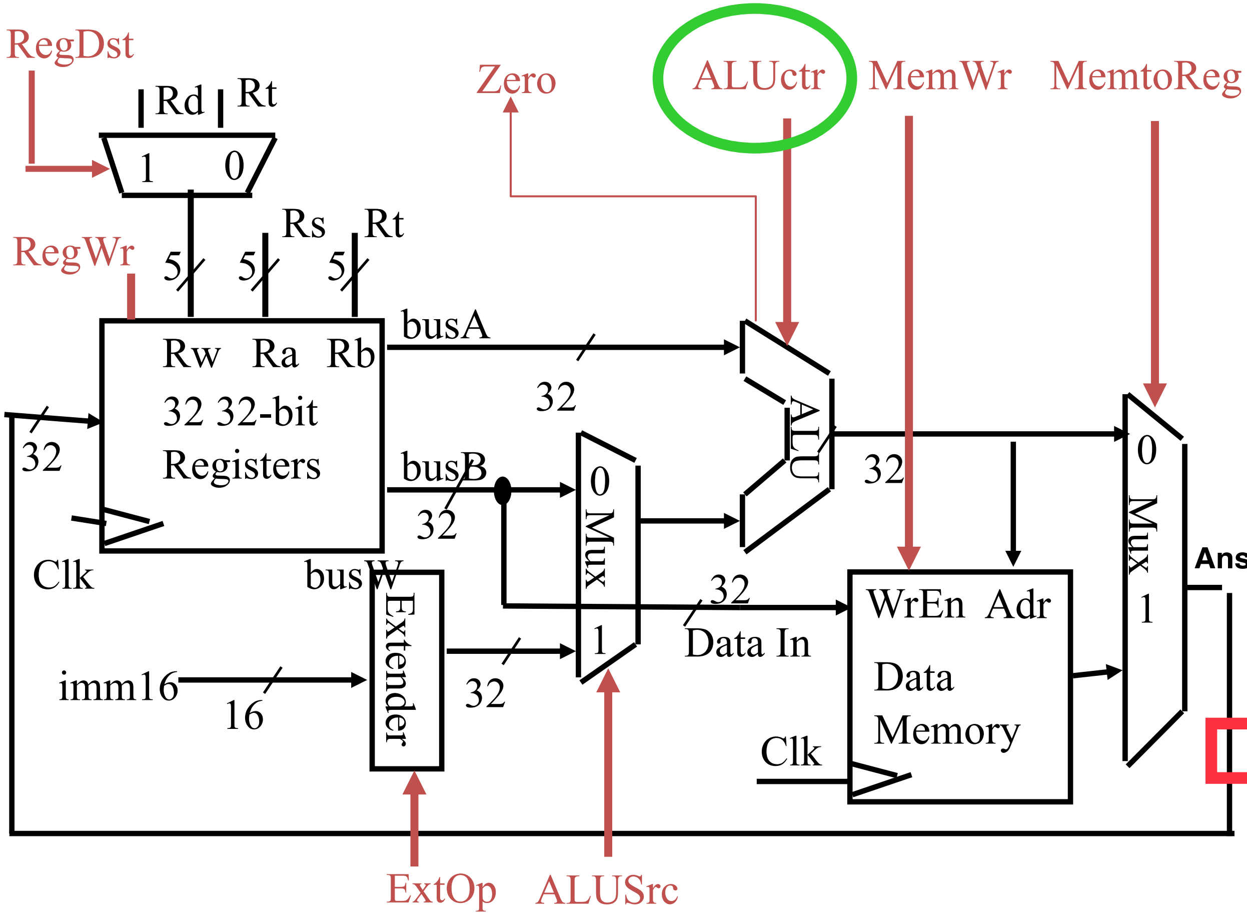
Specify the ALU Control Signals

- ALUctr: 0 ⇒ “add”, 1 ⇒ “sub”, 2 ⇒ “or”



Answer?	AddU	SubU	ORI	LW	SW	BEQ
0	0	0	0	0	0	0
1	0	0	0	0	0	1
2	0	1	0	0	0	1
3	0	1	2	0	0	1
4	0	1	2	0	0	X
5	0	1	2	0	X	X
6	0	1	2	X	X	X
7	X	1	2	X	X	X
8	X	X	2	0	0	1
9	None of the above					

The answer is 3 because we need SubU and BEQ enabled for the ALU control. ORI needs to be 2 for given value and perform "or" instructions for add/sub.

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