Lahore University of Management Sciences

EE-520/CS-622 – Computer Architecture

Fall 2024

Instructor	Adeel Pasha
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Office Hours	TBA
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Secretary/TA	TBA
TA Office Hours	TBA
Course URL (if any)	LMS will be used
Support Services	LUMS offers a range of academic and other services to support students. These are mentioned below, and you are encouraged to use these in addition to in-class assistance from course staff. For a complete list of campus support services available for you click here (https://advising.lums.edu.pk/#supportservices)

Course Basics				
Credit Hours	3			
Lecture(s)	Nbr of Lec(s) Per Week	2	Duration	75 min
Recitation/Lab (per week)	Nbr of Lec(s) Per Week		Duration	
Tutorial (per week)	Nbr of Lec(s) Per Week		Duration	

Course Distribution	
Core	MS DES, MS EE (Electronics and Embedded Systems Stream)
Elective	MS EE, MS CS, BS EE and BS CS
Open for Student Category	EE Seniors, CS Juniors, CS Seniors, EE Graduate Students, CS Graduate Students
Close for Student Category	

COURSE DESCRIPTION

This course extends the concepts of computer organization and uniprocessor architecture to more advanced topics. Hence a strong background in undergraduate level computer architectures is mandatory to take this course. The students are assumed to have taken EE/CS-320, EE-324, CS-225 or similar courses in their undergraduate studies. These topics taught in this course include advanced pipelining, Instruction Level Parallelism (ILP), dynamic scheduling, thread level parallelism (TLP), multi-processors, memory systems, storages, and I/O devices. The course provides the students with current trends and future insight to modern computer architecture design.

COURSE PREREQUISITE(S)

- **EE 322 OR EE 324 OR CS 320 / EE 320 OR CS 225 OR GRAD**

Course Learning Outcomes

CLO1: Describe the performance evaluation criteria of computers and compare performance of different computing systems.

CLO2: Describe advanced concepts for performance improvement in computer architecture like multi-cycle pipeline, dynamic scheduling, dynamic branch prediction, loop unrolling, multi-issue, multi-threading, multi-cores, etc. and analyze their impact on a given machine.

CLO3: Appreciate existing bottlenecks in computer architecture designs (e.g., control and data hazards, exceptions, limited ILP, etc.) and suggest potential solutions.

CLO4: Describe the concepts of memory hierarchy, caches and virtual memory, and analyze their optimizations and contribution toward performance improvement of a computing machine.

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Relation to EE Program Outcomes			
	Related PLOs	Levels of Learning	CLO Attainment checked in
CLO1	PLO1	Cog-2	Midterm, Final, Quizzes
CLO2	PLO1	Cog-2	Midterm, Final, Quizzes
CLO3	PLO2	Cog-5	Midterm, Final, Quizzes
CLO4	PLO2	Cog-4	Final, Quizzes

Grading Breakup and Policy
Assignment(s) (2-3): 10% Quiz(s) (5-6): 15% Class Participation: Attendance: Midterm Examination: 35% Project: Final Examination: 40%

Examination Detail	
Midterm Exam	Yes/No: Yes Combine Separate: NA Duration: 75 – 90 min Preferred Date: TBA Exam Specifications: TBA
Final Exam	Yes/No: Yes Combine Separate: NA Duration: 120 – 180 min Exam Specifications: TBA

Campus supports & Key university policies

Campus Supports

Students are strongly encouraged to meet course instructors and TA's during office hours for assistance in course-content, understand the course's expectations from enrolled students, etc. Beyond the course, students are also encouraged to use a variety of other resources. (Instructors are also encouraged to refer students to these resources when needed.) These resources include Counseling and Psychological Services/CAPS (for mental health), LUMS Medical Center/LMC (for physical health), Office of Accessibility & Inclusion/ OAI (for long-term disabilities), advising staff dedicated to supporting and guiding students in each school, online resources (https://advising.lums.edu.pk/advising-resources), etc. To view all support services, their specific role as well as contact information click here (https://advising.lums.edu.pk/#supportservices).

Academic Honesty/Plagiarism

LUMS has zero tolerance for academic dishonesty. Students are responsible for upholding academic integrity. If unsure, refer to the student handbook and consult with instructors/teaching assistants. To check for plagiarism before essay submission, use similarity@lums.edu.pk. Consult the following resources: 1) Academic and Intellectual Integrity (http://surl.li/gpvwb), and 2) Understanding and Avoiding Plagiarism (http://surl.li/gpvwo).

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LUMS Academic Accommodations/ Petitions policy

Long-term medical conditions are accommodated through the Office of Accessibility & Inclusion (OAI). Short-term emergencies that impact studies are either handled by the course instructor or Student Support Services (SSS). For more information, please see Missed Instrument or 'Petition' FAQs for students and faculty (https://rb.gy/8sj1h)

LUMS Sexual Harassment Policy

LUMS and this class are a harassment-free zone. No behavior that makes someone uncomfortable or negatively impacts the class or individual's potential will be tolerated.

To report sexual harassment experienced or observed in class, please contact me. For further support or to file a complaint, contact OAI at oai@lums.edu.pk or harassment@lums.edu.pk. You may choose to file an informal or formal complaint to put an end to the offending behavior. You can also call their Anti-Harassment helpline at 042-35608877 for advice or concerns. *For more information: Harassment, Bullying & Other Interpersonal Misconduct: Presentation (http://surl.li/gpvwt)*

COURSE OVERVIEW

Lecture	Topics	Recommended Readings	Related CLO
1.	Introduction to Computer Architecture	Ch-1	CLO1
2.	Performance Metrics of a System	Ch-1	
3.	Review – principles of Instruction Set Architecture (ISA)	Appendix-A	
4.			
5.	Pipelining overview, basics, limitations, different types of hazards, static branch prediction	Appendix-C	CLO2, CLO3
6.			
7.			
8.			
9.	Instruction Level Parallelism (ILP), static and dynamic scheduling, Tomasulo's algorithm, dynamic branch prediction	Ch-3	
10.			
11.			
12.			
13.	Hardware Speculation		
14.			
15.	Midterm Exam		
16.	Superscalar and VLIW architectures	Ch-3	CLO2, CLO3
17.			
18.	Limitations to ILP and Thread Level Parallelism (TLP)	Ch-5	
19.	Review – basics of caches, cache misses, hits, types and organization	Appendix-B, Ch-2	
20.			
21.			
22.			
23.	Simultaneous Multi-Threading (SMT), multiprocessors, memory hierarchy, cache coherence	Ch-5	
24.			
25.			
26.			
27.	System protection: virtual memory and virtual machines	Ch-2	CLO4
28.			
	Final Exam		

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Textbook(s)/Supplementary Readings
Textbook: "**Computer Architecture: A Quantitative Approach" by John L. Hennessy and David A. Patterson, 6th Ed.** Supplementary Reading: **Hand-outs and online links will be provided where needed**

Complex Engineering Problem, Problem Based learning OR Open-ended Labs	
Complex Engineering Problem Details	Included: NA Nature and details of Complex Engineering Problem: Assessment in:
Problem Based learning	Included: NA Nature and details of Problem Based learning: Assessment in:
Open ended Labs	Included: NA Nature and details of Open-ended Lab: Assessment in:

Rubric Based Assessment of CLO	
Rubric Details	Rubric used for CLOs: NA CLO-wise details of each rubric design per assessment module:

Prepared by:	**Dr. Adeel Pasha (Instructor EE-520/CS-622)**
Date:	**Updated: June 10, 2024**