Lecture 5
EE 421 / CS 425
Digital System Design

Fall 2025

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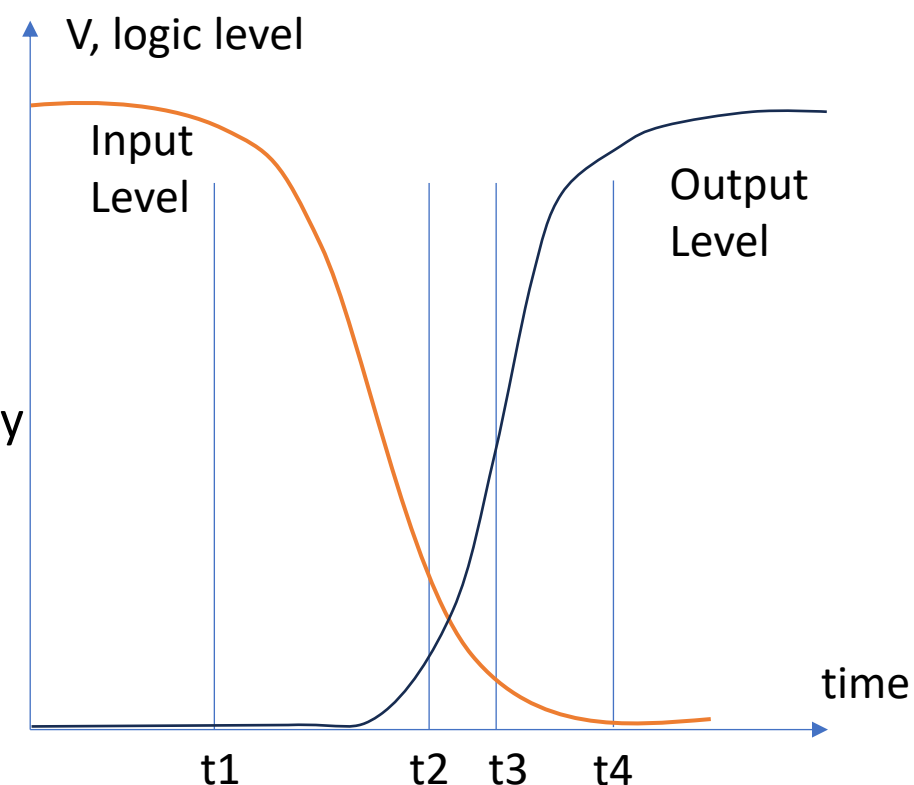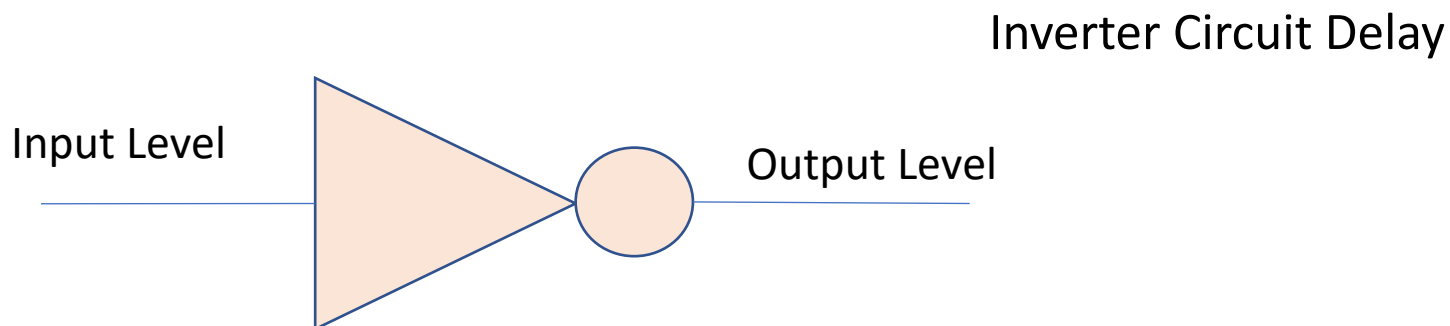**QUIZ 1 NEXT LECTURE**

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Topics

- Pulse Circuits

- Timing Related Effects in Combinational Circuits

- Glitches

- Hazards

- Identify and Remove Glitches and Hazards

- If we have time, we may start

  - Review of Sequential Digital Logic Circuits

  - Basics of Latches

  - Basics of Flipflops
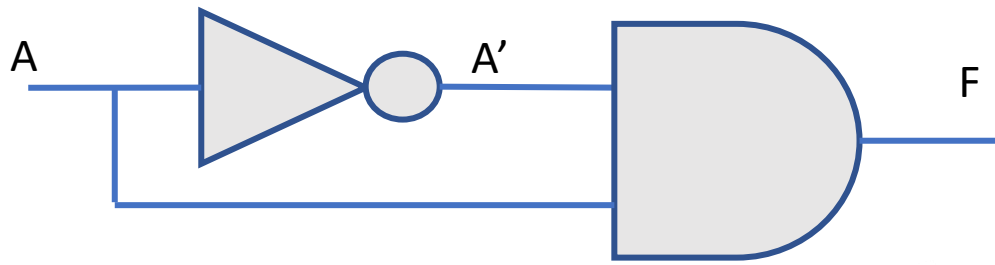
- QUIZ 1 NEXT LECTURE

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Timing Waveforms

Every physical circuit has some processing delay; once the input has settled, **the correct output appears after some time**.
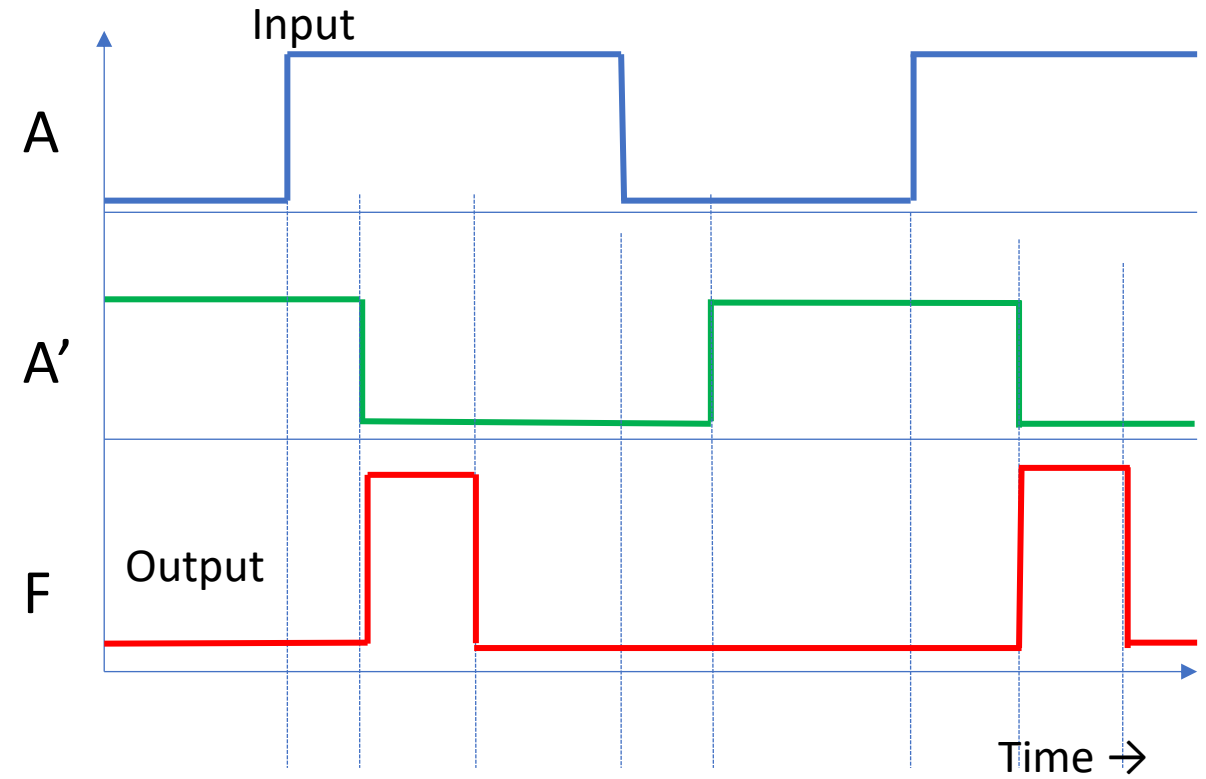
Propagation delay from a gate is defined by:
tplh = time delay in output going from low to high
tphl = time delay in output going from high to low

Input Level

Output Level

Inverter Circuit Delay

V, logic level

Input Level

Output Level

time

t1   t2   t3   t4

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A simple pulse circuit

A ▷○— A'

F

Each gate has Propagation Delay

Input

A

A'

F Output
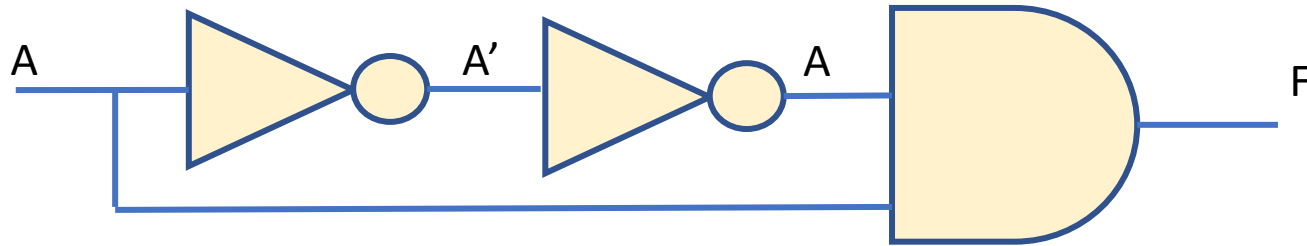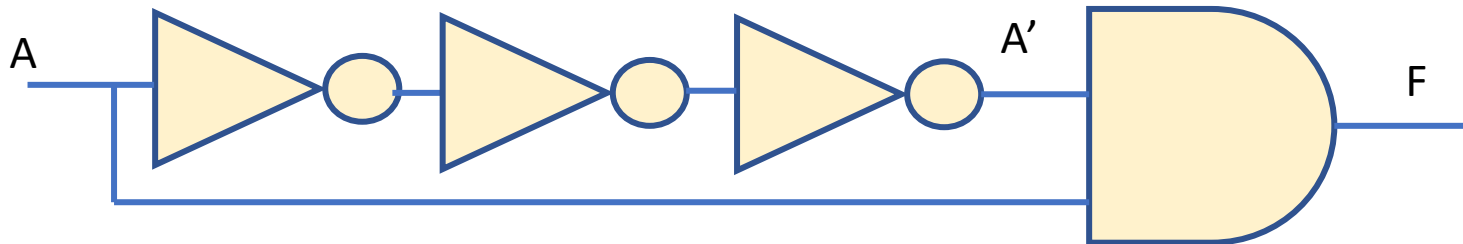
Time →

Question: What will be the Output if there are two inverters in series?

Question: What will be the Output if there are three inverters in series?

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# Two and Three Inverters in simple pulse circuit

A — A' — A — F

For even number of Inverters:
Check input A transitions from
0 to 1 and from 1 to 0
Pulse behaviour is not observed
(Hint: Check whether F is like A?)

A — A' — F

For Odd number of Inverters:
At 0 to 1 transitions at A, a pulse will
appear at F. The pulse width is proportional
to number of inverters as their propagation
delay adds up

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A Pulse Shaper Circuit
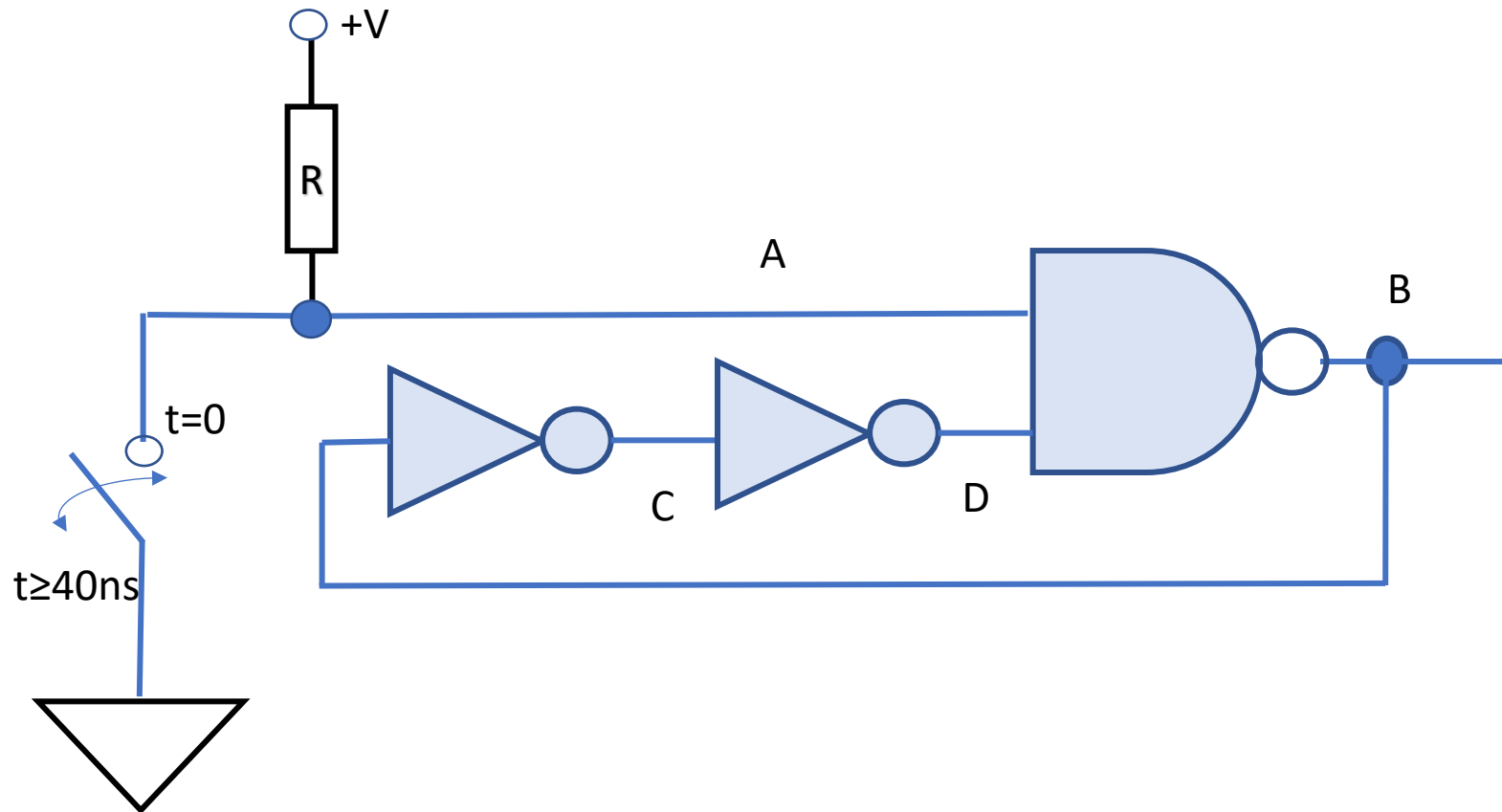
Case 1:

Assume propagation delay of gates as 10ns

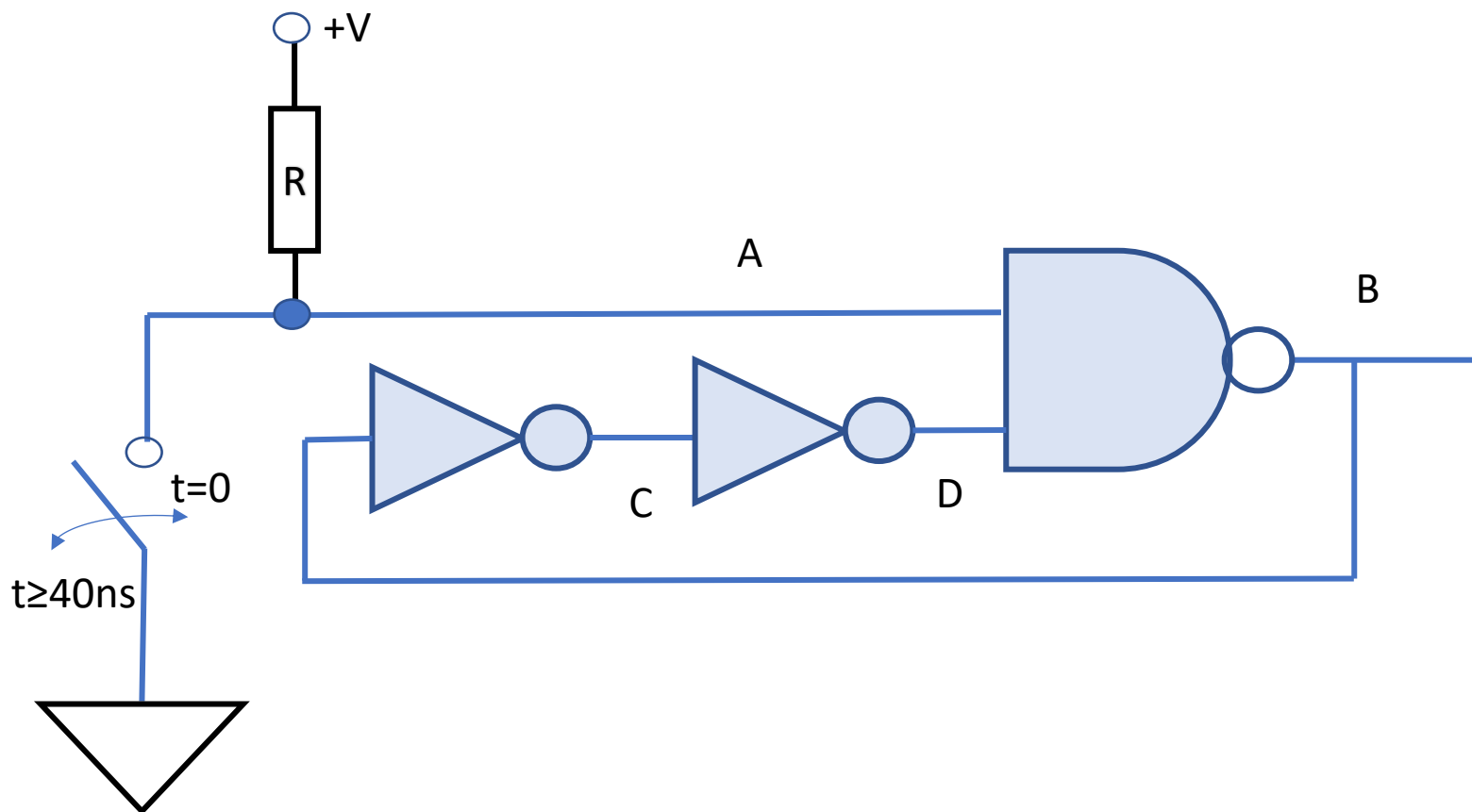Switch is closed at **t=0ns**, thus:

A goes to '0' at time t=0ns
B goes to '1' at time t=10ns
C goes to '0' at time t=20ns
D goes to '1' at time t=30ns

Since D='1', A='0', hence:
Output B='0' always for A='0' in steady state

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Pulse Shaper Circuit – Case 2

Case 2:
Assume propagation delay of gates as 10ns

Output B was in steady state = '0' while Switch was closed at t=0

Now Switch is opened at t=40ns
So A goes to '1' at t=40ns
B goes to '0' after 10ns at t=50ns
C goes to '1' at t = 60ns
D goes to '0' at t = 70ns

Now D='0' and A='1', hence B='1' at t=80ns
C goes to '0' at t=90ns
D goes to '1' at t=100ns
Since A ='1' and D='1' so B='0' at t=110ns

The cycle will start repeating automatically

We get an **OSCILLATOR**

Time Period of this oscillator is determined by propagation delay of gates

Same behavior can be obtained from a NOR gate circuit with some changes

Glitches and Hazards

Glitch: An Unwanted Pulse at the Output of a Combinational Logic Circuit. Glitch is dependent upon Inputs and how the circuit is configured
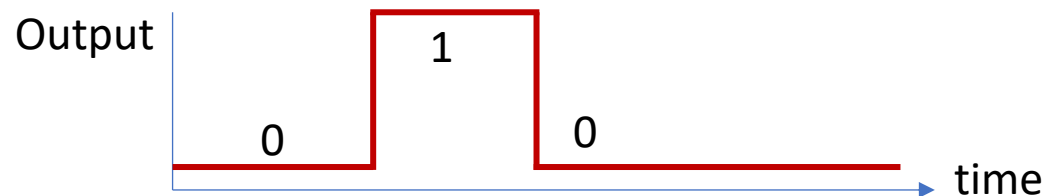
Hazard: A Combinational Logic Circuit with a potential to produce Glitches is called a Hazard.

Possible Reasons:

1. Using Un-Stable Input Signals

2. Not Considering Propagation Delays in high-speed designs
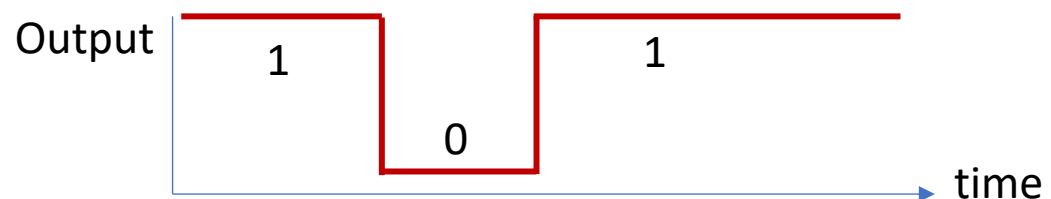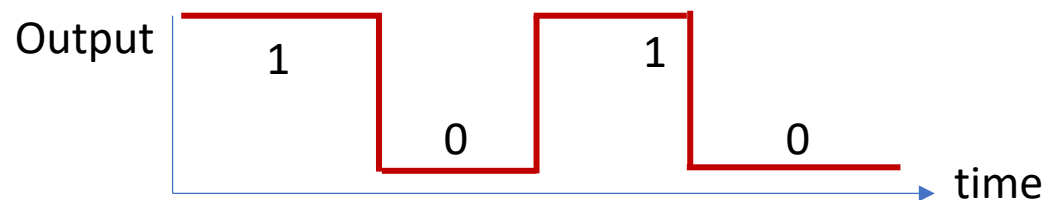
3. Using Asynchronous Inputs

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Kinds of Hazards

Output

1

0   0

→ time

Input Changes cause output to change from '0' to '1' to '0'
STATIC ZERO HAZARD

Output

1   1

0

→ time

Input Changes cause output to change from '1' to '0' to '1'
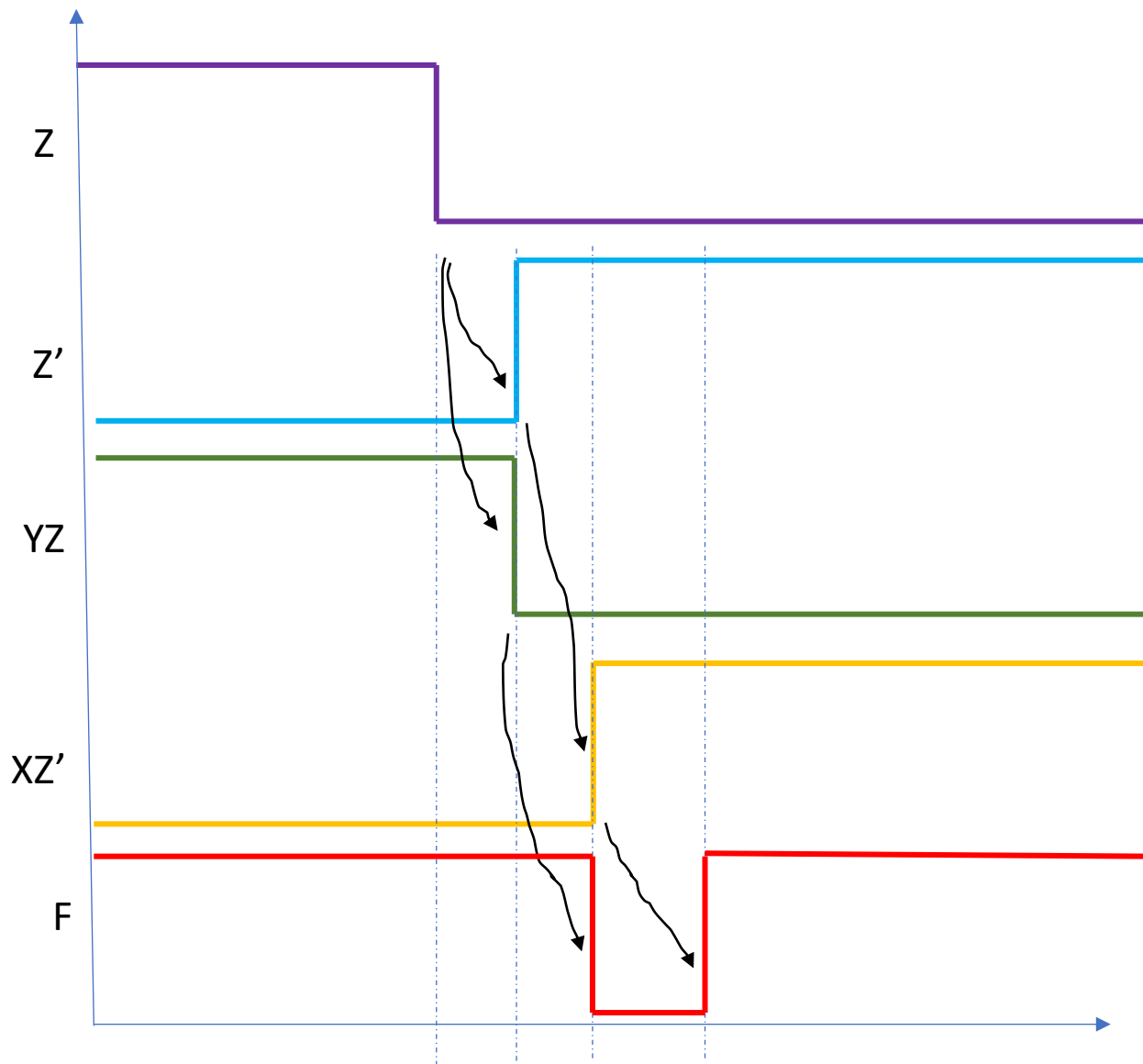**STATIC ONE HAZARD**

Output

1   1

0   0

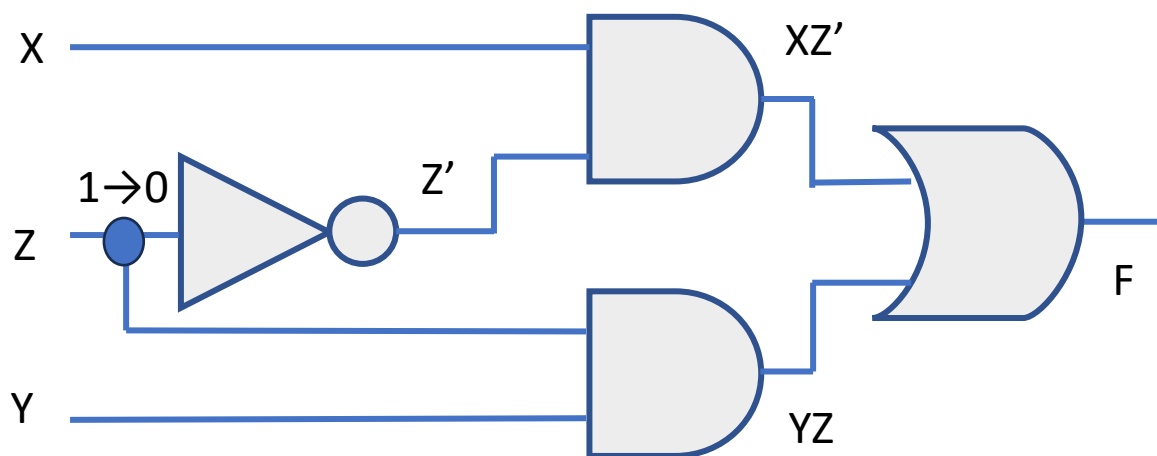→ time

Input Changes cause two or more changes from '1' to '0' to '1' to '0', Or changes from '0' to '1' to '0' to '1'
DYNAMIC HAZARD

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Circuit with Static 1 Hazard

Static 1 Hazard Observed

Example of Static 0 Hazard

A=0

C= 0 → 1

0→1

C'= 1 → 0

1→0

0→1→0

Fpos

Fpos = 0 without glitch

B=0

A, B = 0

C

C'

A+C

(B+C')

Fpos

Static 0 Hazard

time

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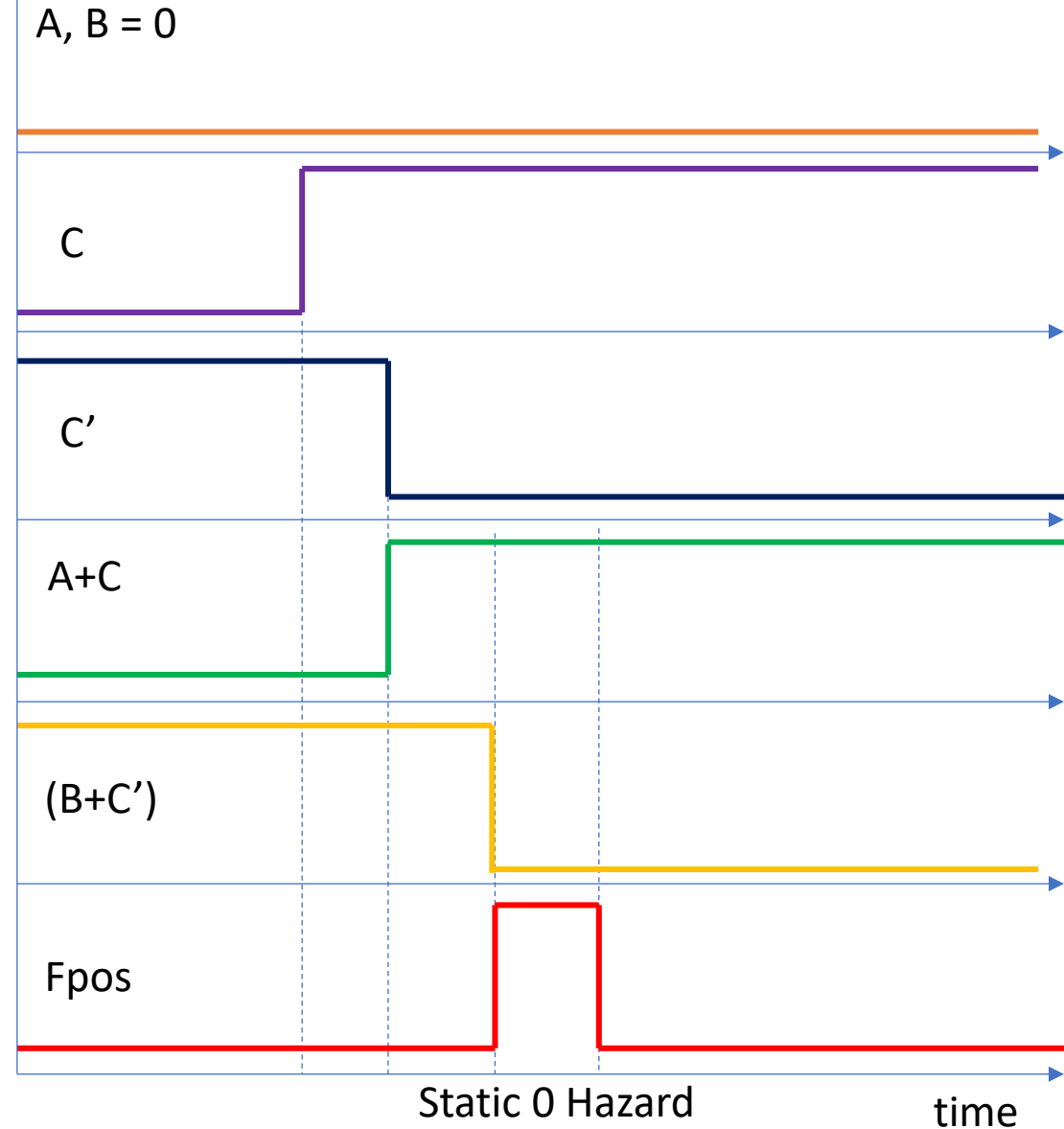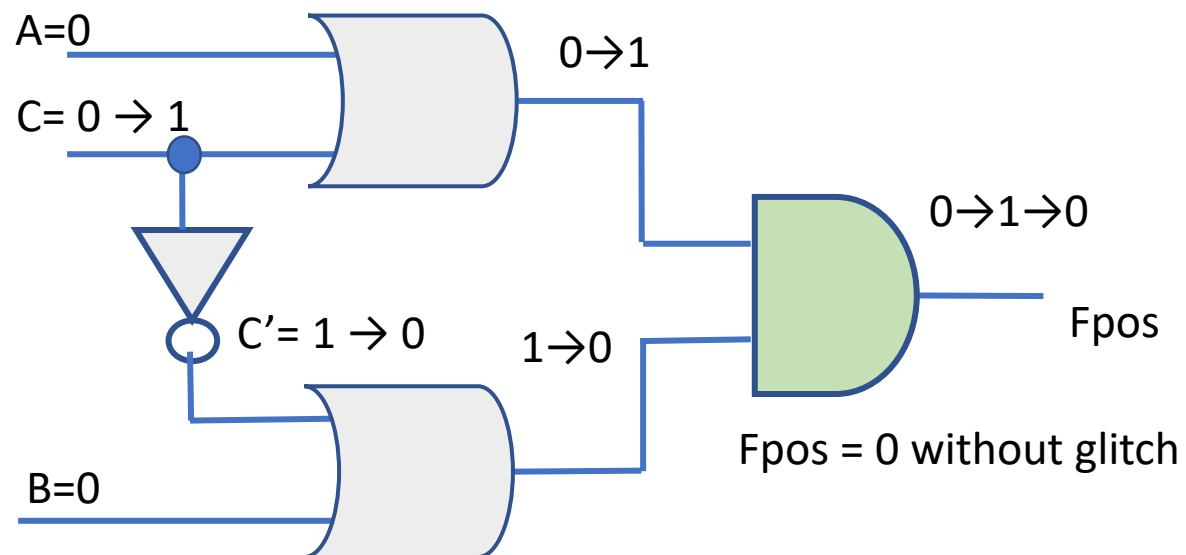
K Maps to Identify Hazards

X

$1 \to 0$

Z'

Z

Y

XZ'

YZ

F
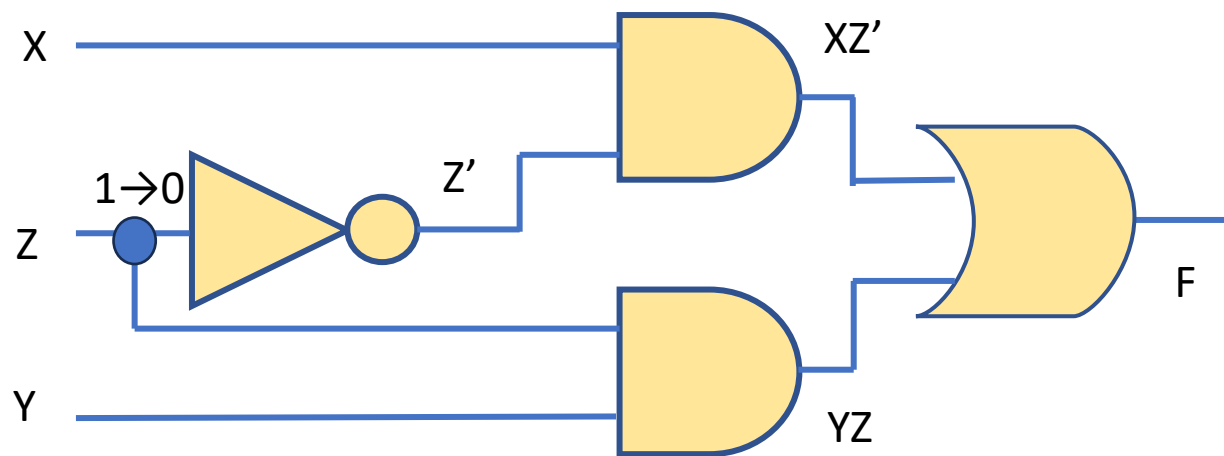
F=XZ' + YZ

Z, XY	00	01	11	10
0	0	0	1	1
1	0	1	1	0

XZ'

YZ

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How to Know about Hazards?

- A properly designed two level SOP (AND-OR) circuit has no Static-0 Hazard

- This type of SOP circuits can have Static-1 Hazards

- Look at the K-Map again and we notice that there is no single product term that covers the inputs XYZ=111 and XYZ=110. Thus glitch to 0 is possible if the AND gate covering the other combination goes to 1.

- To Eliminate Such Hazards:

- Include an extra product term (AND gate) to cover the hazard input. This is where the adjacent 1s exist in K-Maps but are not covered. This is called 'Adding a Consensus Term'

Hazard Free two level SOP Circuit
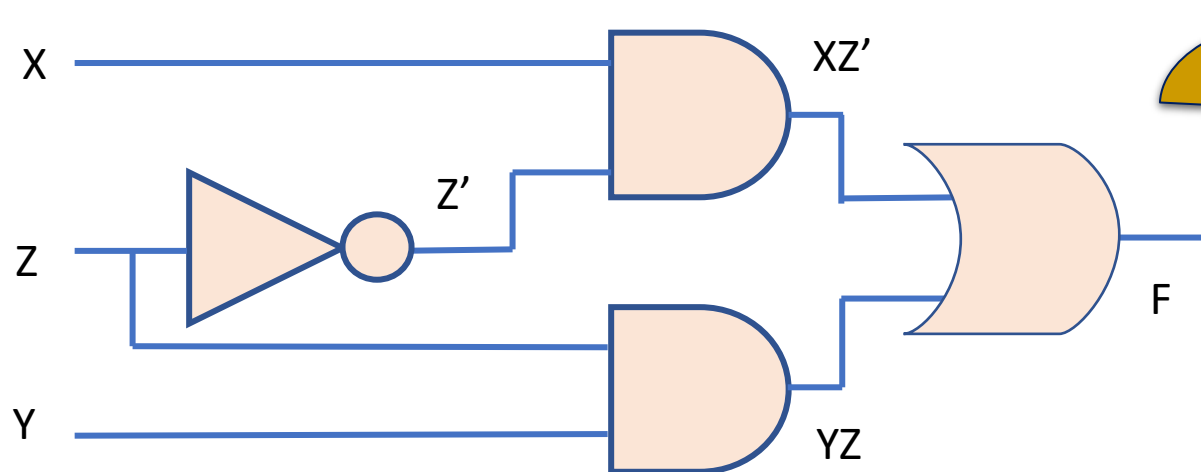
Z, XY	00	01	11	10
0	0	0	1	1
1	0	1	1	0

YZ

Consensus Term
XY

XZ'
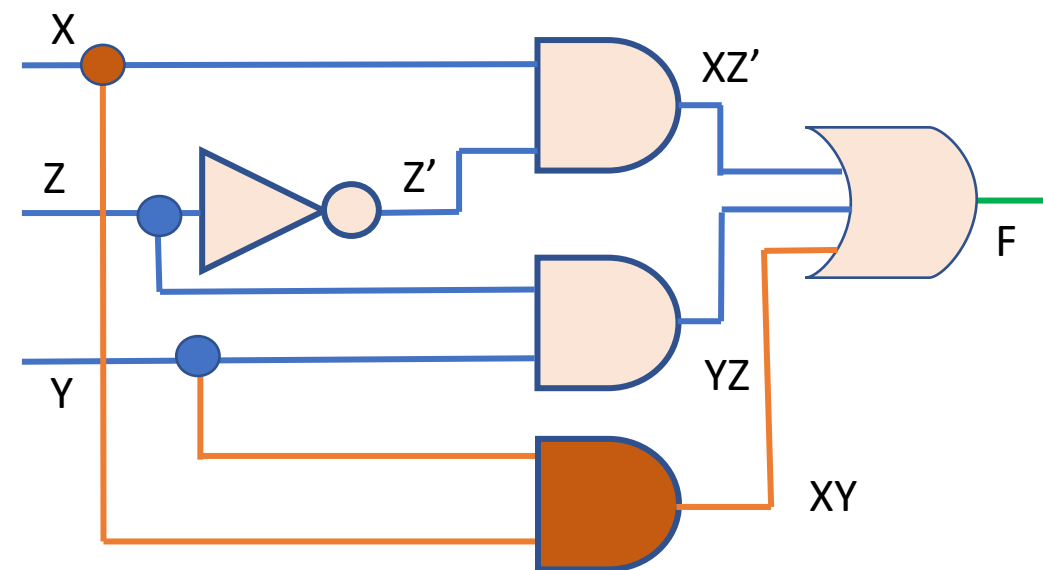
F including Consensus Term = XY + YZ + XZ'

**Final Hazard Free Circuit
Including Extra Consensus Circuit**

The Adjacent 1s in K-Map are now Covered

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Using K-Map to Identify Static 1 Hazard in 4 input variables

AB, CD	00	01	11	10
00	0	1	1	0
01	1	1	0	0
11	1	1	1	1
10	0	0	1	1

Given K-Map with Minimal Grouping

Identify the Hazards

Adjacent 1s that are not in the same group

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K-Map Groups to Eliminate Static 1 Hazard

XY'Z'

W'XY'

WXZ'

YZ, WX	00	01	10	11
00	0	1	1	0
01	1	1	0	0
11	1	1	1	1
10	0	0	1	1

AB, CD	00	01	10	11
00	0	1	1	0
01	1	1	0	0
11	1	1	1	1
10	0	0	1	1

YZ

W'Z

WY

Minimal Expression:

F=XY'Z' + W'Z + WY

Hazard Free Expression:

F=XY'Z' + W'Z + WY + W'XY' + YZ + WXZ'

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K-Map Grouping to Eliminate Static 0 Hazard

POS = Grouping of Zeros

AB, CD	00	01	10	11
00	1	1	0	0
01	1	1	1	1
11	0	0	1	1
10	0	0	0	0

(B + C')

(A' + C)

Minimal Mapping without Hazard Consideration

F=(A' + C) (B + C')

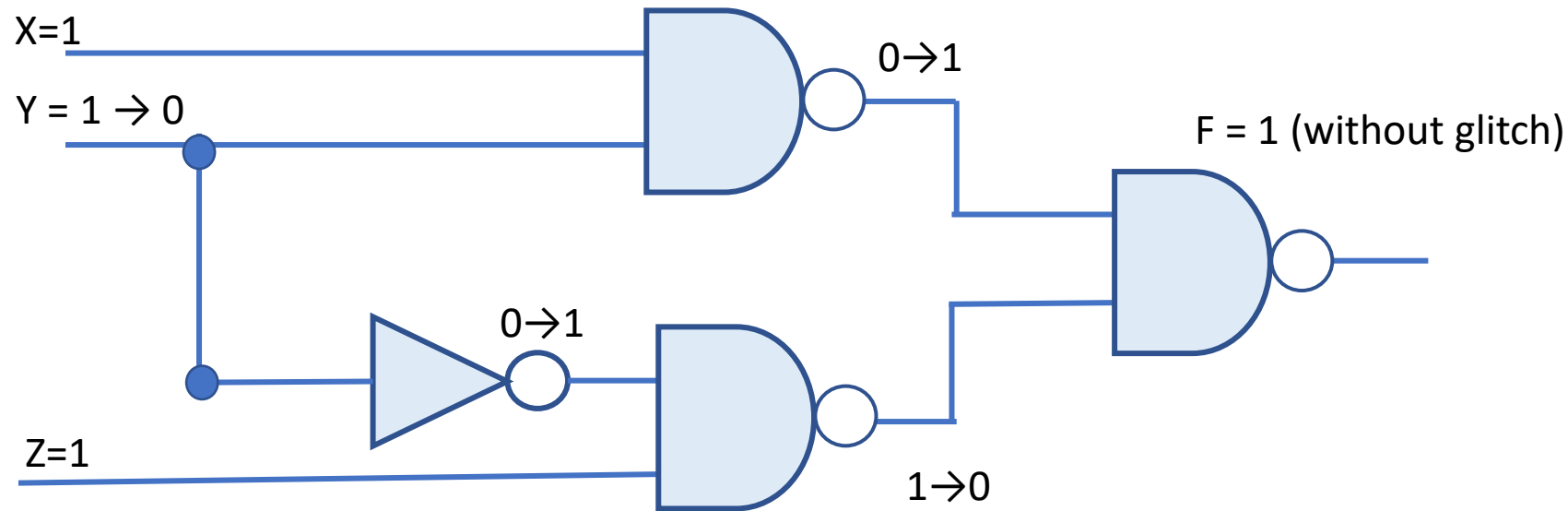| AB, CD	00	01	10	11
00	1	1	0	0
01	1	1	1	1
11	0	0	1	1
10	0	0	0	0

(A'+B)

Additional Cover for Static 0 Hazard prevention

F=(A' + C) (B + C') (A' + B)

Now free from Static 0 Hazard

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Example of Static 0 Hazard

$X=1$

$Y = 1 \rightarrow 0$

$0 \rightarrow 1$

F = 1 (without glitch)

$0 \rightarrow 1$

Z=1

$1 \rightarrow 0$

$F=(X+Y').(Y+Z)$

When Y changes from 1 to 0, both inputs of Nand Gate F may be equal to 1, Causing the output to momentarily go to 0 when it should have stayed at 1.

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Dynamic Hazards

- Dynamic Hazard is the possibility of an output changing more than once as the result of a single input transition.

- These can occur if there are multiple paths with different delays from the input to the output

- Dynamic Hazards do not occur in properly designed two level AND-OR or OR-AND Circuits.

- Thus remove all Static-1 and Static-0 Hazards in the two-level SOP or POS design and the possibility of Dynamic Hazards is minimized.
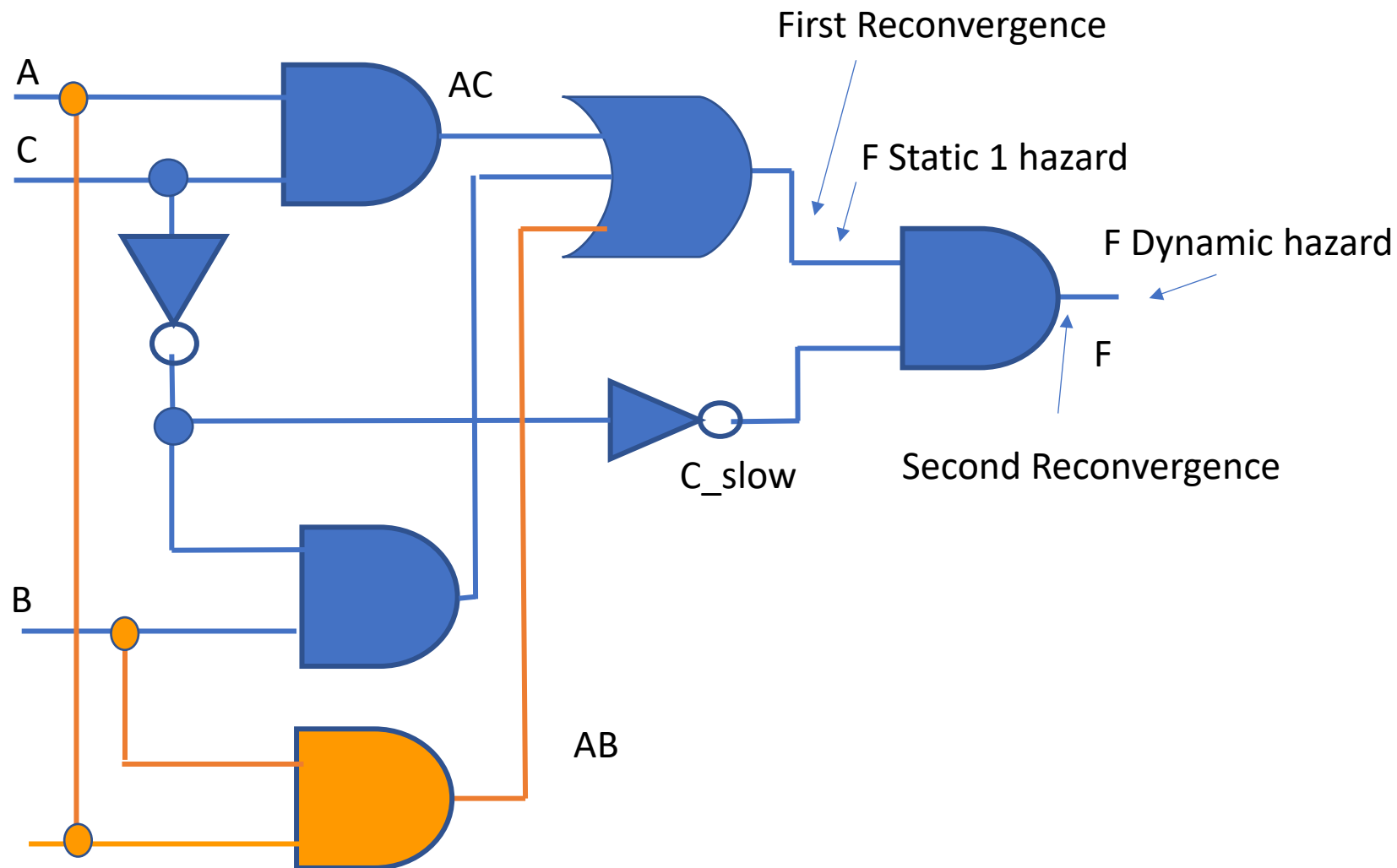
Circuit containing Dynamic Hazard

First Reconvergence

F Static 1 hazard

F Dynamic hazard

F

C_slow

Second Reconvergence
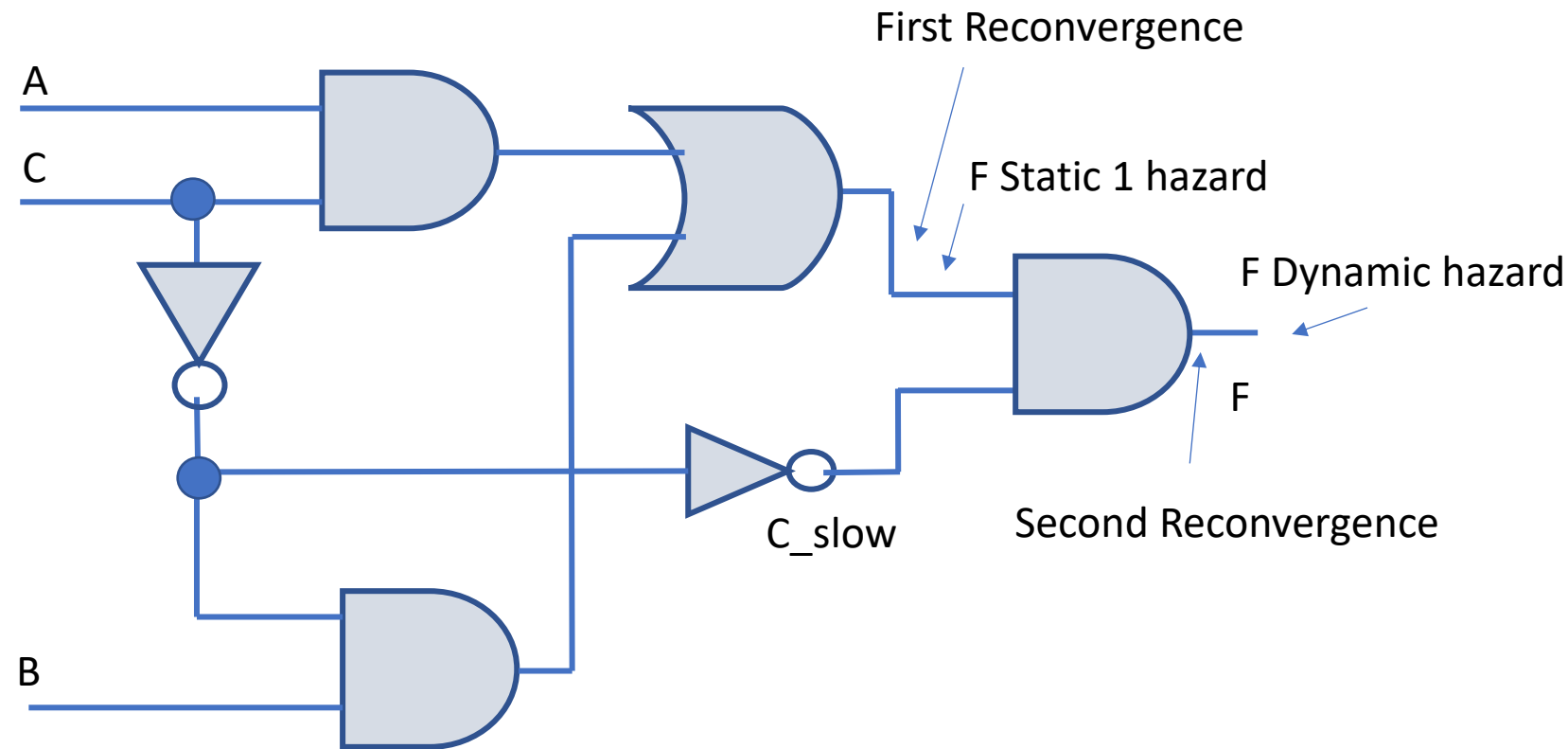
Try changing
ABC from 110 to 111

Solution: Make K Map and add redundant cover for C

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Redundant Circuit to remove Dynamic Hazard

First Reconvergence

F Static 1 hazard

F Dynamic hazard

A

C

AC

B

AB

C_slow

Second Reconvergence

F

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- **We may start review of Sequential Elements and Circuits**

Latches and Flipflops - Definitions

- **Latches:** Level Sensitive storage elements; that can transition at any point in time

- **Flipflops:** Edge Sensitive storage elements, that transition at clock edges, either rising or falling

- **Asynchronous Sequential Logic:** Based on latches and un-clocked transitions

- **Synchronous Sequential Logic:** Based on flipflops and only clocked transitions

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Fundamental Element – SR Latch
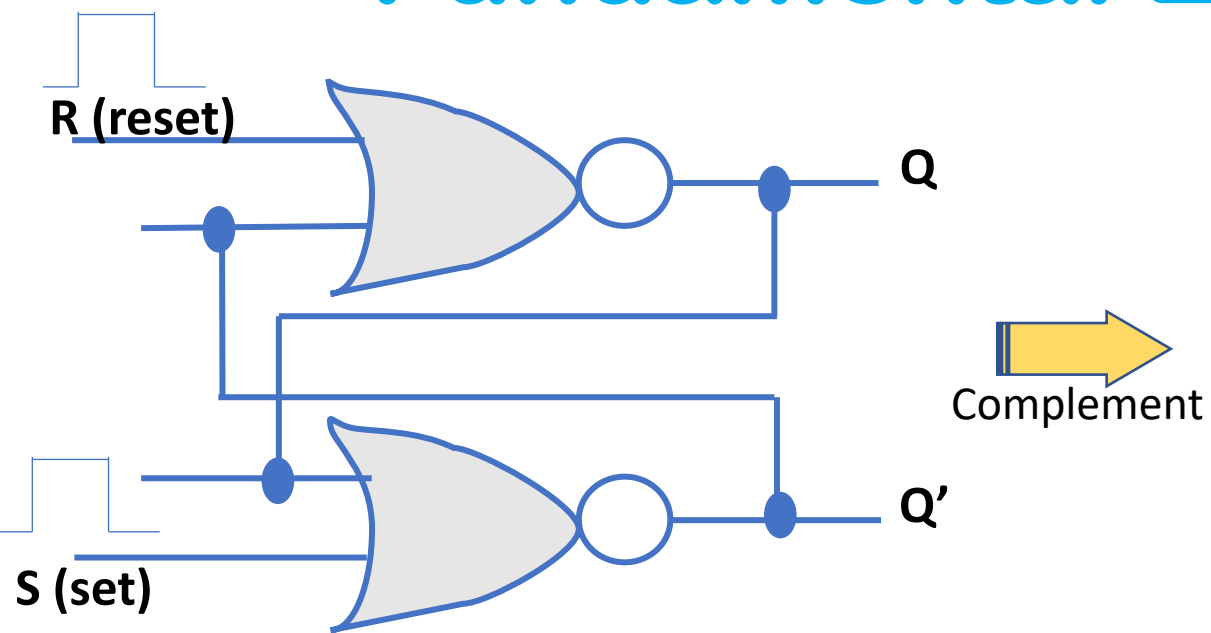
Complement
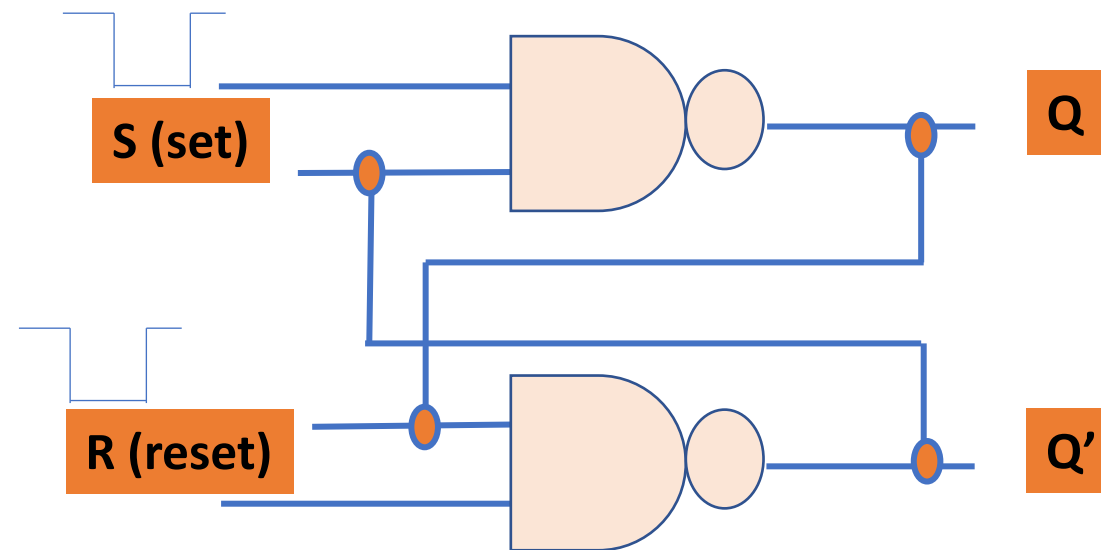
SR Latch Using 2 Input NOR Gate – Function Table

S (Set)	R (Reset)	Q	Condition
0	0	Q (=1 after S=1, R=0)	Hold
0	0	Q (=0 after S=0, R=1)	Hold
0	1	0	Reset
1	0	1	Set
1	1	0	Not Allowed

RACE Condition

SR Latch Using 2 Input NAND Gate – Function Table

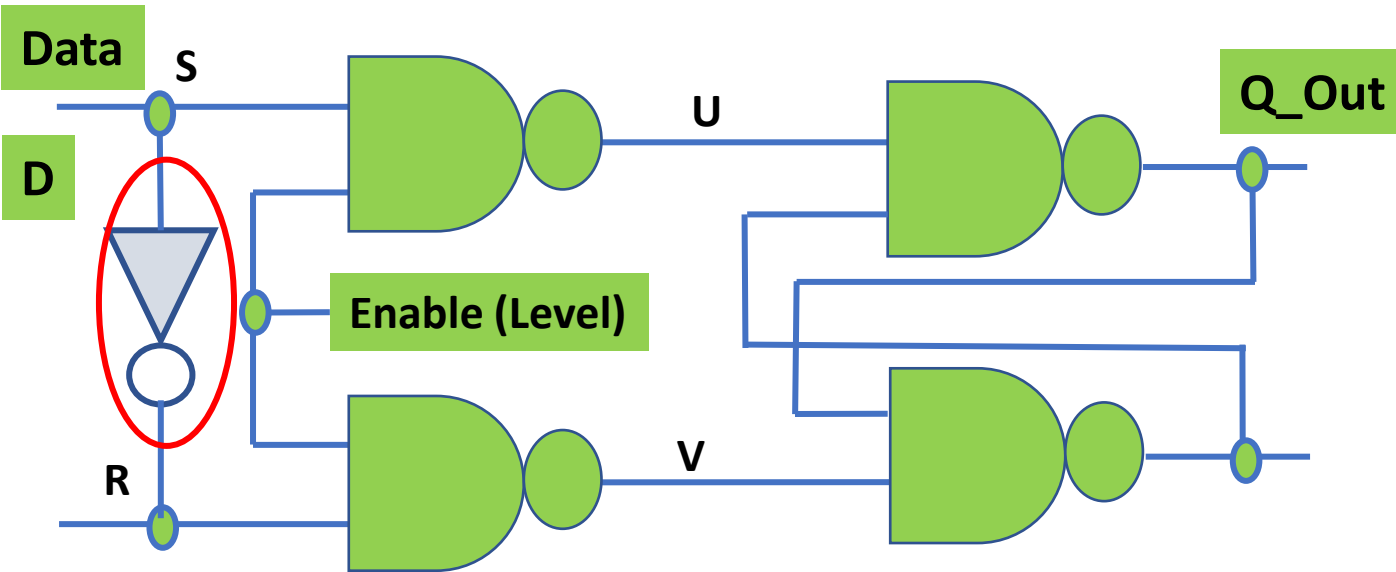| S	R	Q	Condition
0	0	1	Not Allowed
0	1	1	Set
1	0	0	Reset
1	1	Q (=0 after S=1, R=0)	Hold
1	1	Q (=1 after S=0, R=1)	Hold

RACE Condition

Transparent Latch

- An additional 'Enable' input is provided

- Definition: Output of Transparent Latch changes in response to the data input only when the Latch is 'Enabled'.

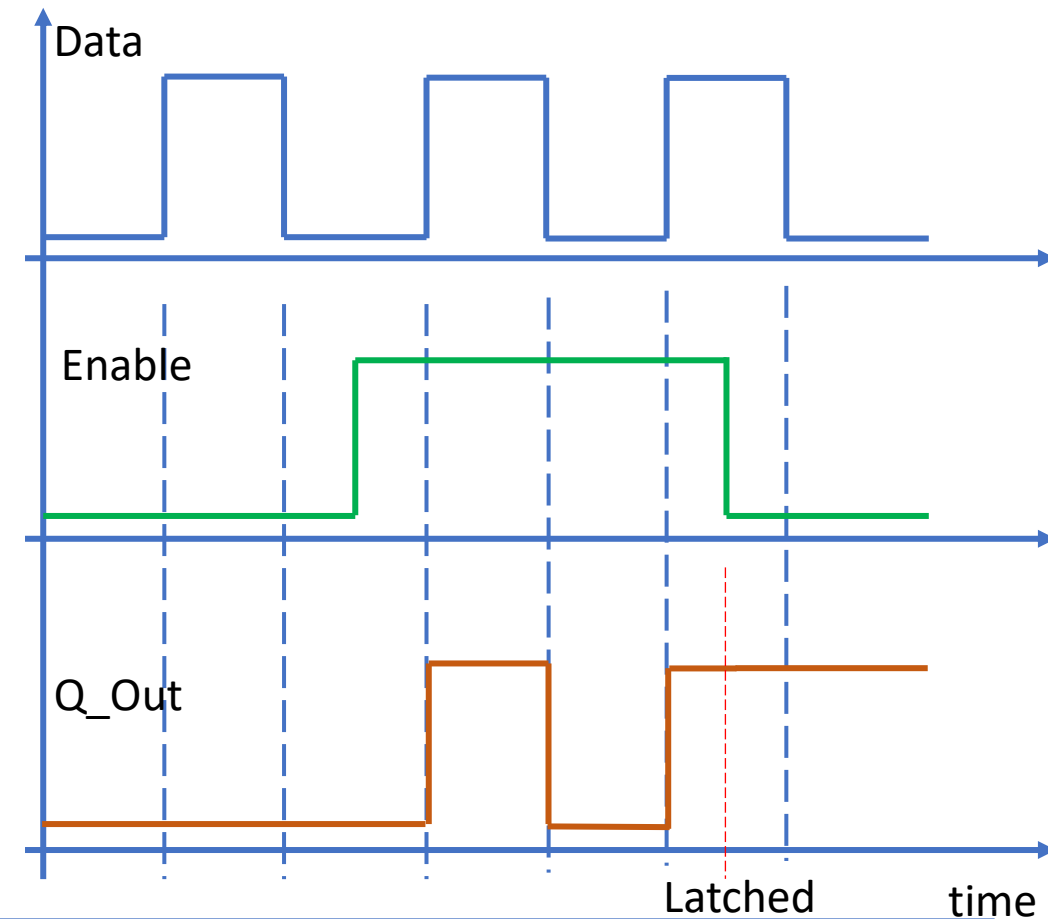- Changes in input are straight away visible at the output

Transparent Latch Circuit

Timing Diagram – With Input Inverter
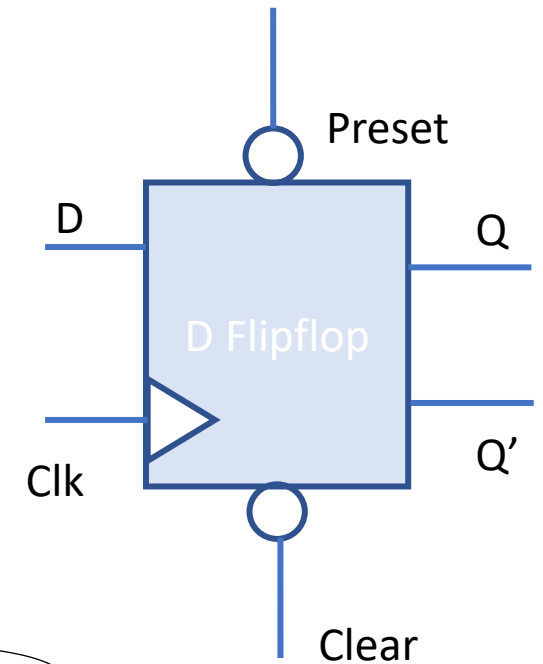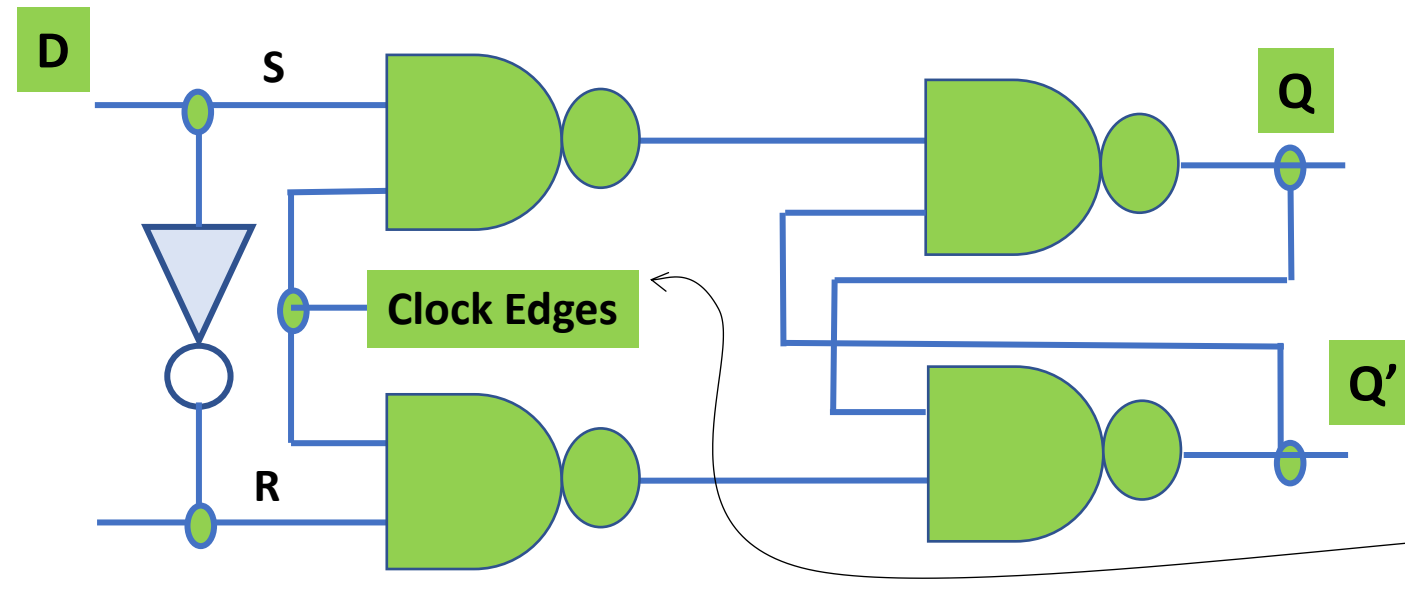
SR Latch With Enable (Without Inverter)

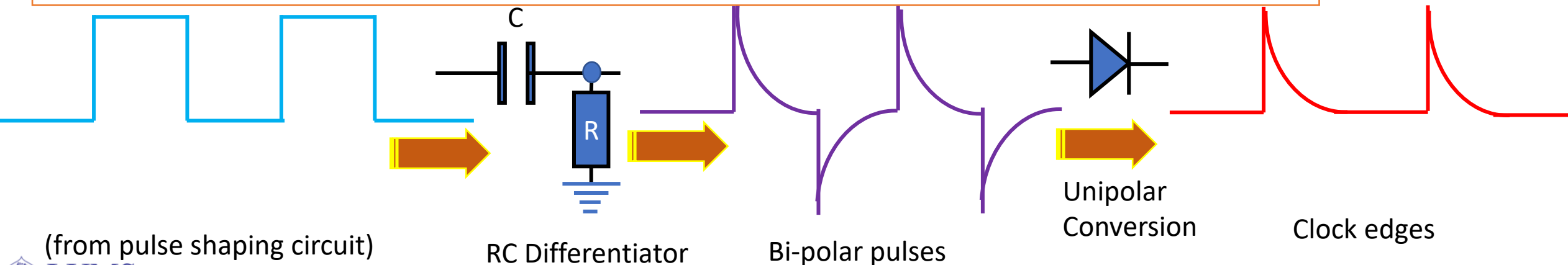| En	S	R	Next State of Q
0	X	X	No Change
1	0	0	No Change
1	0	1	Q=0; Reset State
1	1	0	Q=1; Set State
1	1	1	Not Allowed

When Enable is '0'; U='1' and V='1'; Hold Condition in SR Latch

Only these two states are valid when inverter is inserted

D Flipflop from Transparent Latch

D

S

Clock Edges

Q

Q'

R

Preset

D

Clk

D Flipflop

Q

Q'

Clear

NOTE: Usually a Master-Slave Arrangement is used where output is available after clock goes 0 to 1 to 0

C

R

(from pulse shaping circuit)

RC Differentiator

Bi-polar pulses

Unipolar Conversion

Clock edges

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Timing Definitions

- Setup Time: The duration of time the Data needs to be present before the arrival of clock.

- Any Data activity, in tandem with clock edge, violates setup time and will not be recorded in the D flipflop

- Hold Time: The time for which data has to remain stable after the removal of clock edge.

- If the Data changes too soon, the internal circuit may not have settled with the new value.
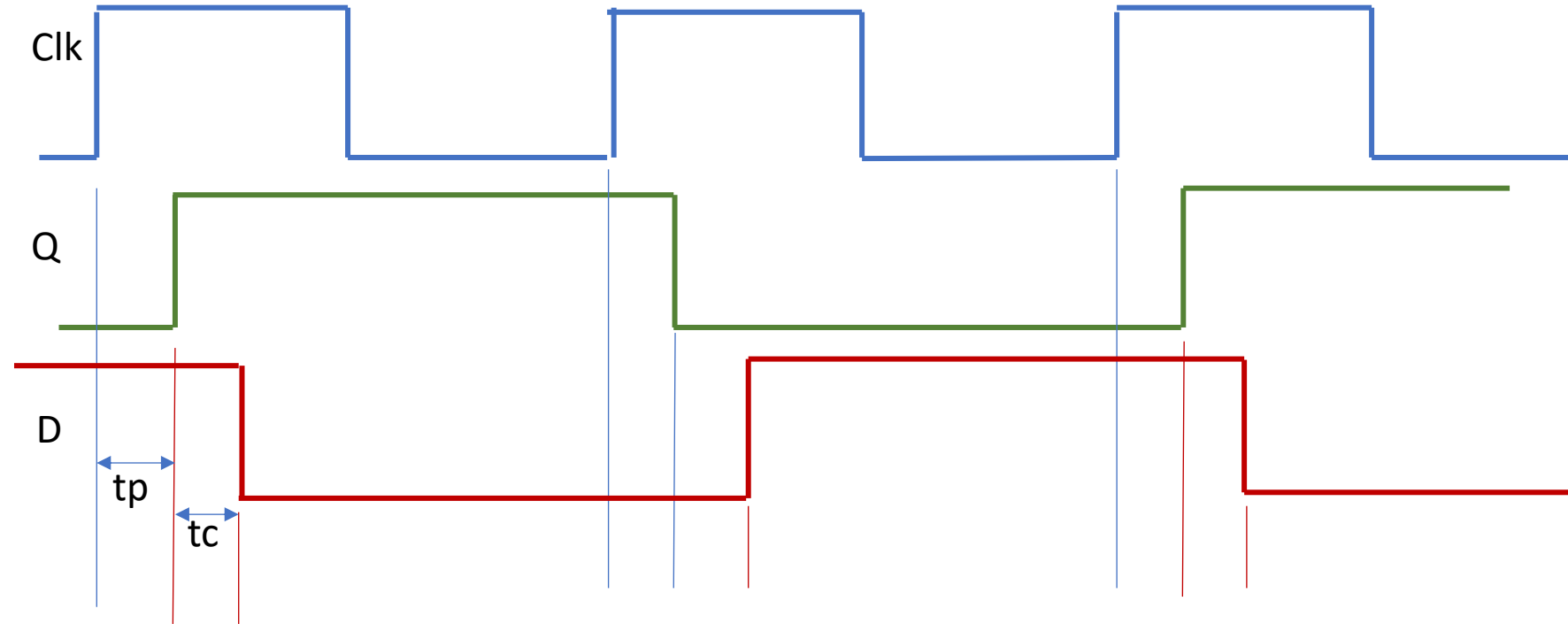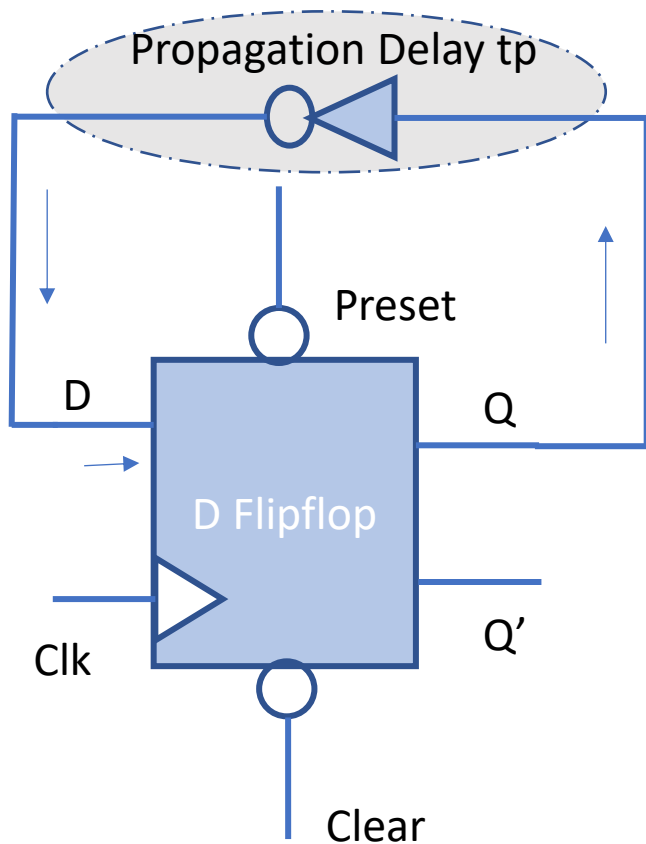
Setup and Hold Times
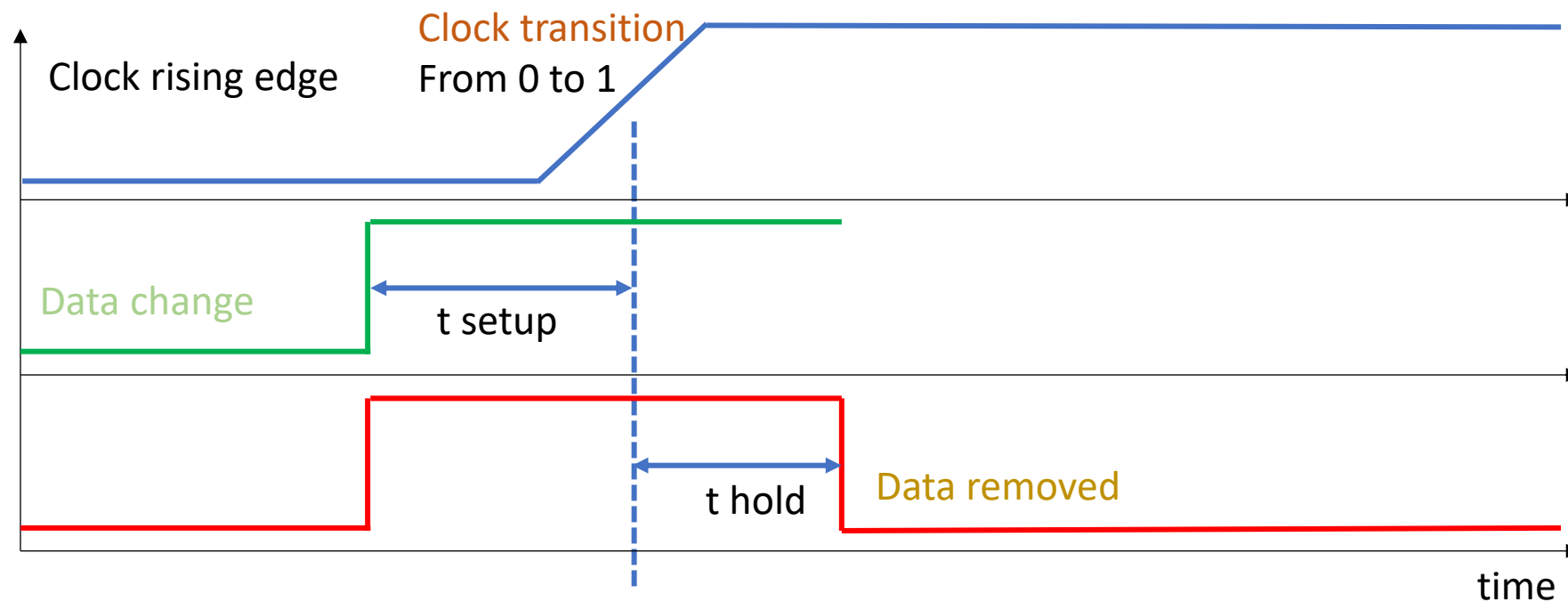
Maximum clock frequency has to be slower than (t setup + t hold) to maintain correct data

These timings needed both ways, slow data and fast clock; as well as slow clock and fast data

Timing in a simple frequency divider

If the current output of flipflop is 1, a value of 0 will appear at D after propagation delay of inverter

Assuming that next active edge of clock arrives after setup time has elapsed, the output of flipflop will go to 0

A continuous waveform with period twice the period of Clk is observed at Q

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