Lecture 19
EE 421 / CS 425
# Digital System Design

Fall 2024

Shahid Masud

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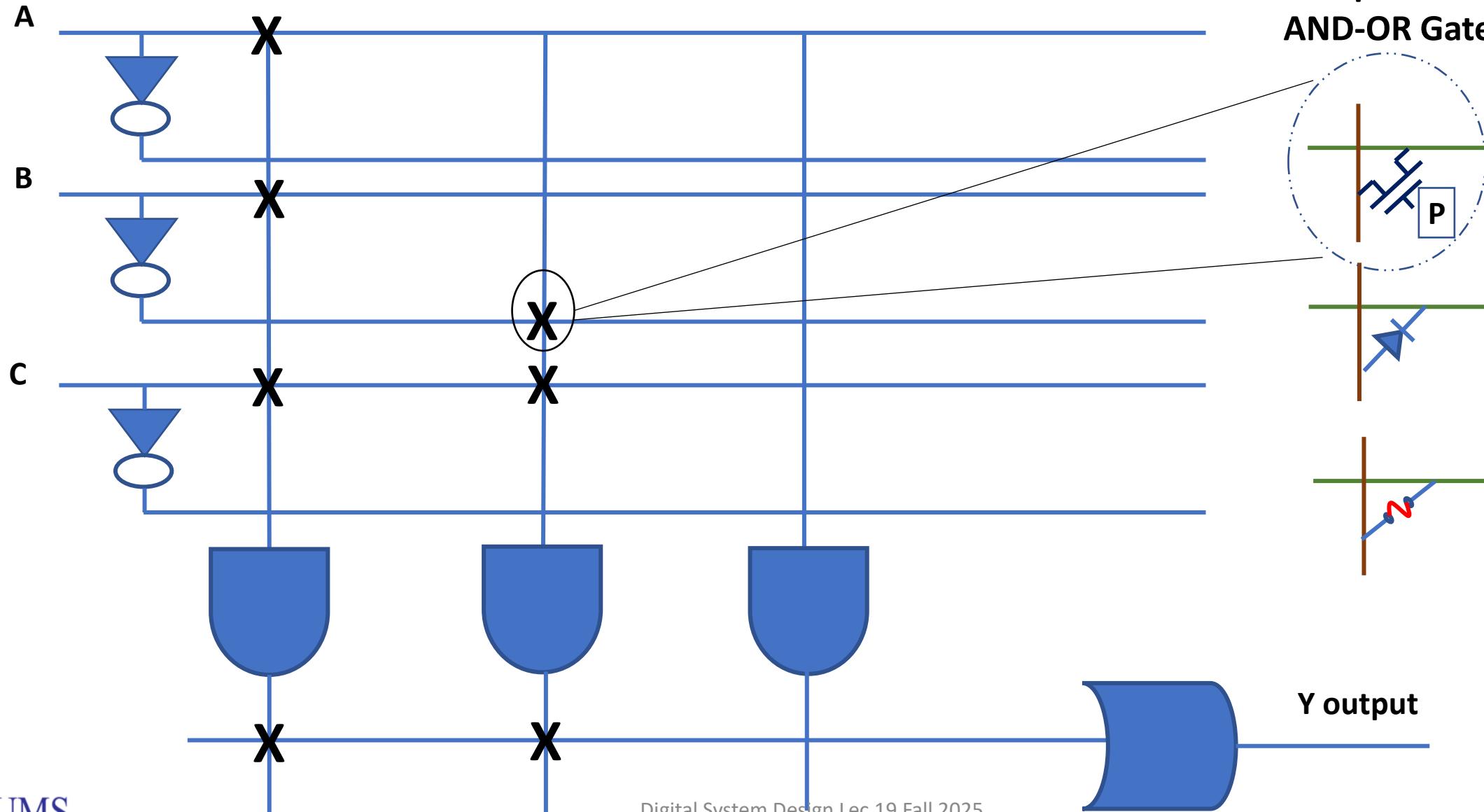
Topics

- PAL, PLA, Examples, Polarity Control Circuit in I/O (Recap)

- Datasheet of PLA/PAL

- Example of an I/O Block for SPLD

- Field Programming technology

- CPLD Architecture

- CPLD Examples from Xilinx and Altera

- Logic Expander – Shareable and Parallel

- Output Block of PLD

- FPGA Architecture

QUIZ NEXT
Tuesday

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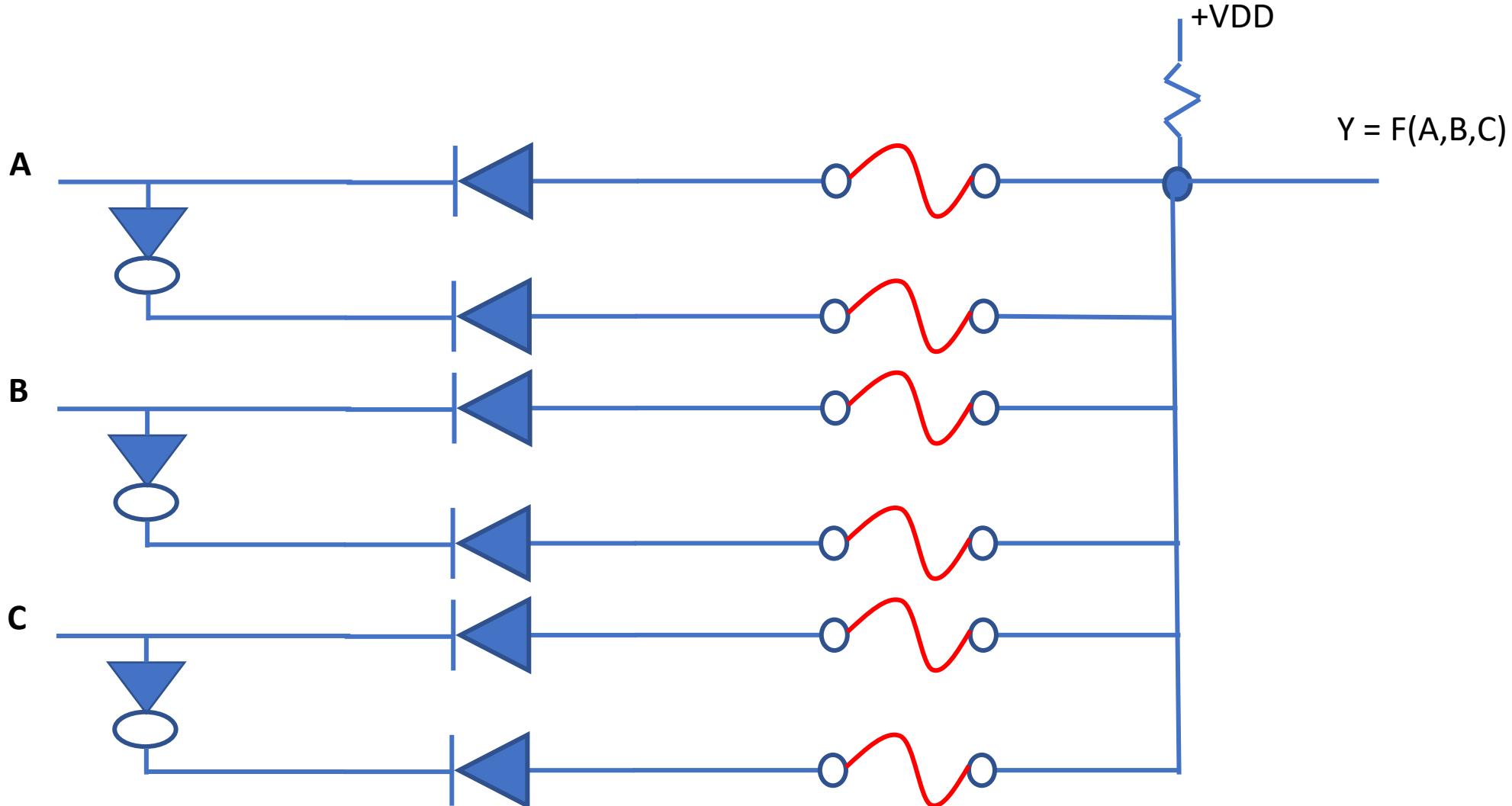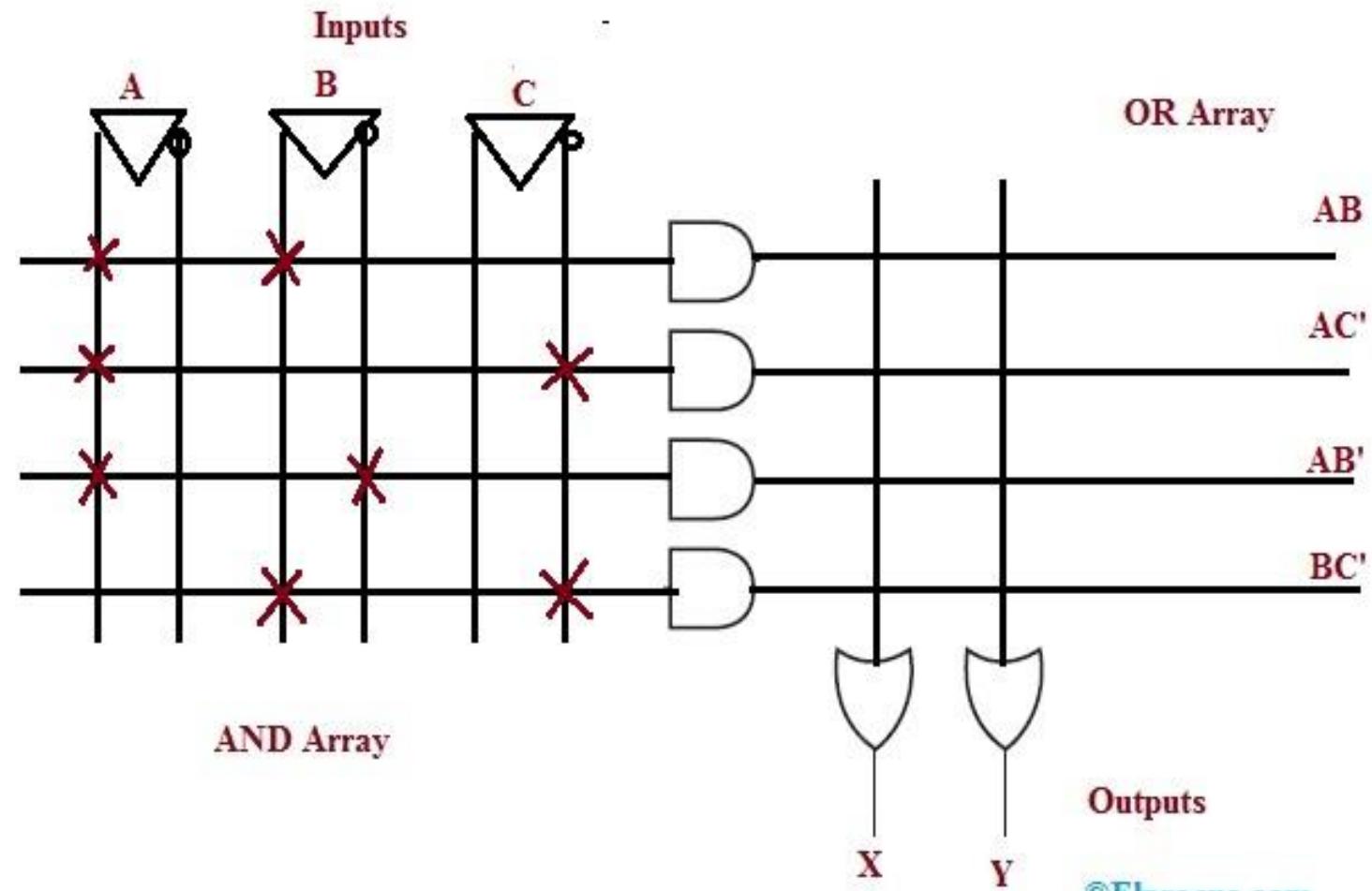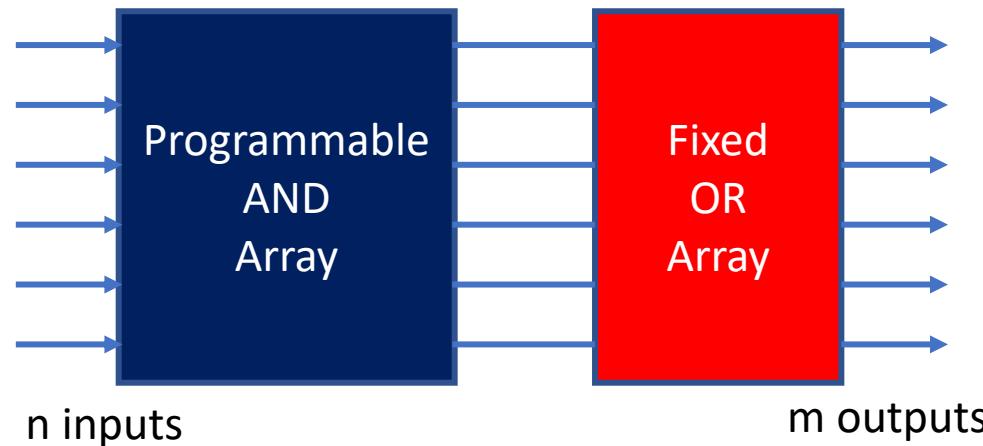
AND-OR Logic Array

PLA = Programmable Logic Array Comprises Programmable AND-OR Gates

Y output

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Fuse Programmable Logic Array
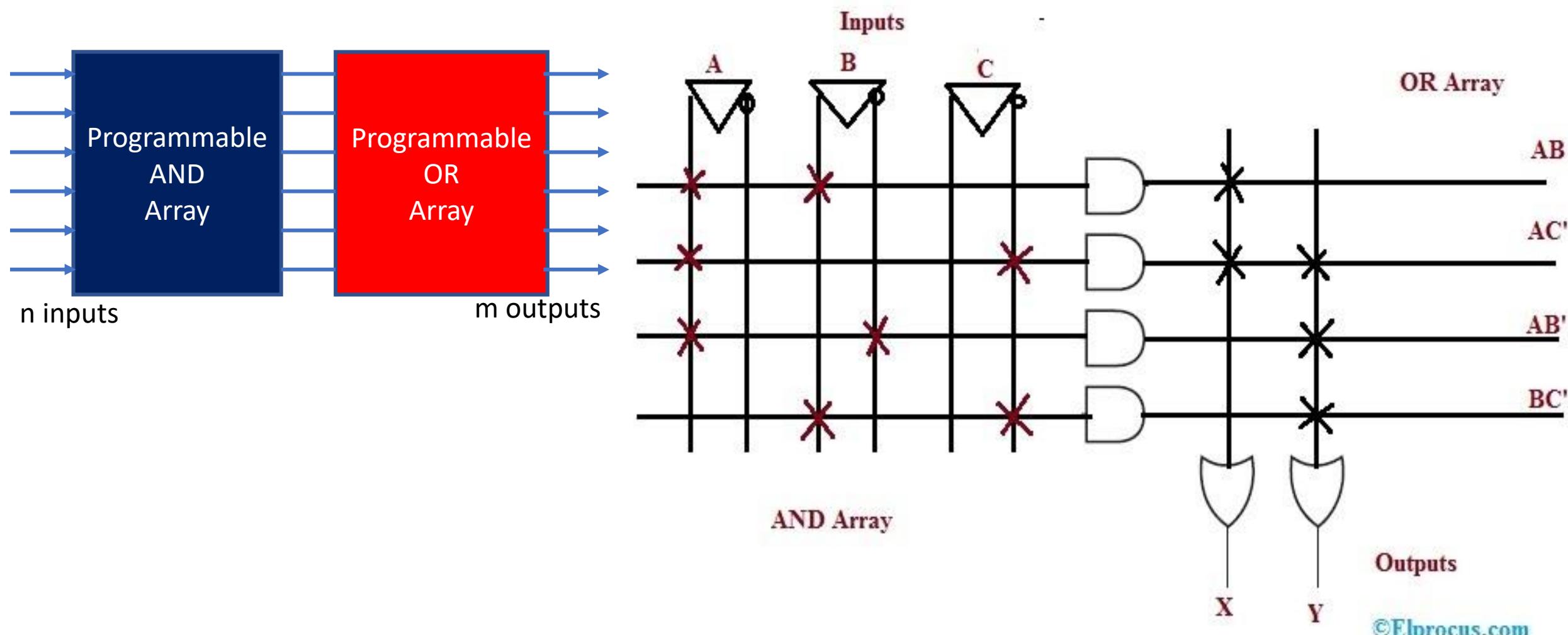
PAL – Programmable Array Logic

Programmable AND Array

Fixed OR Array

n inputs

m outputs

Inputs

A B C

OR Array

AB

AC'

AB'

BC'

AND Array

Outputs

X Y

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https://www.elprocus.com/what-are-pal-and-pla-design-and-differences/

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PLA – Programmable Logic Array

https://www.elprocus.com/what-are-pal-and-pla-design-and-differences/

For Exercise

input

OR plane

AND plane

output

Inputs

AND plane
(Programmable
interconnect)

OR plane
(Programmable interconnect)

Outputs

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Example of PLA

AB   A'C'   A'B'C   A'B

$Z_1 = AB + A'C'$

$Z_2 = A'B'C + A'B$
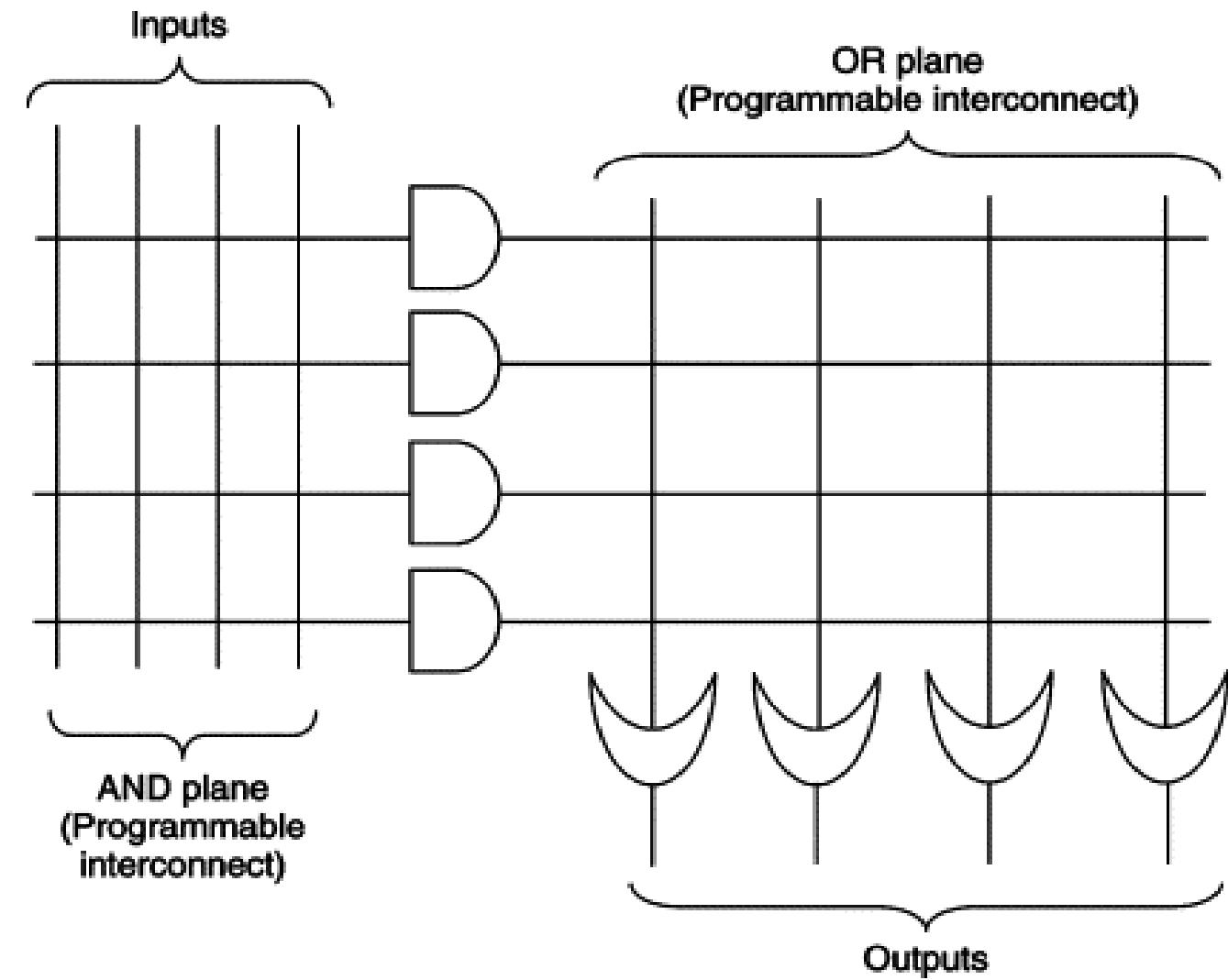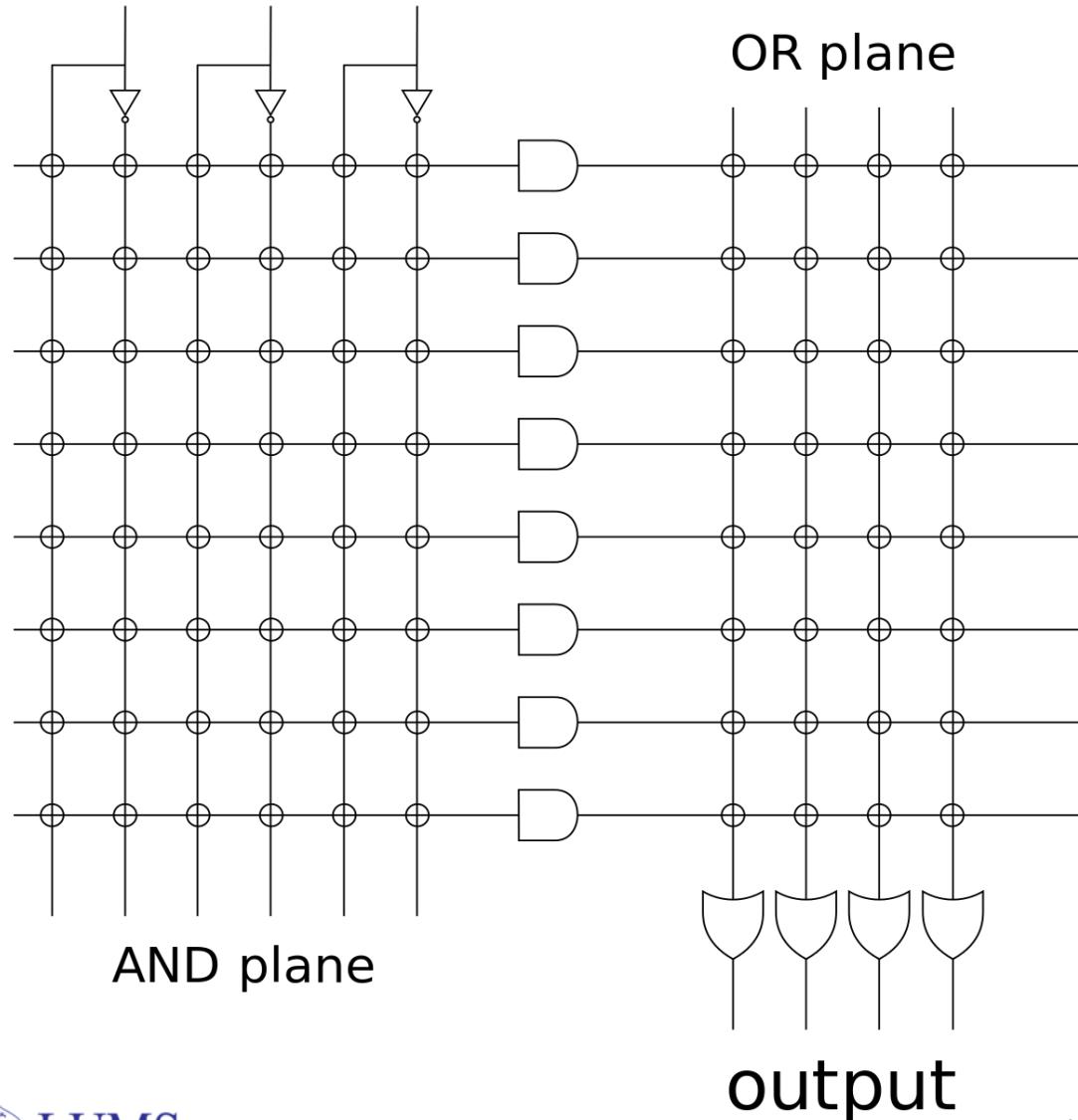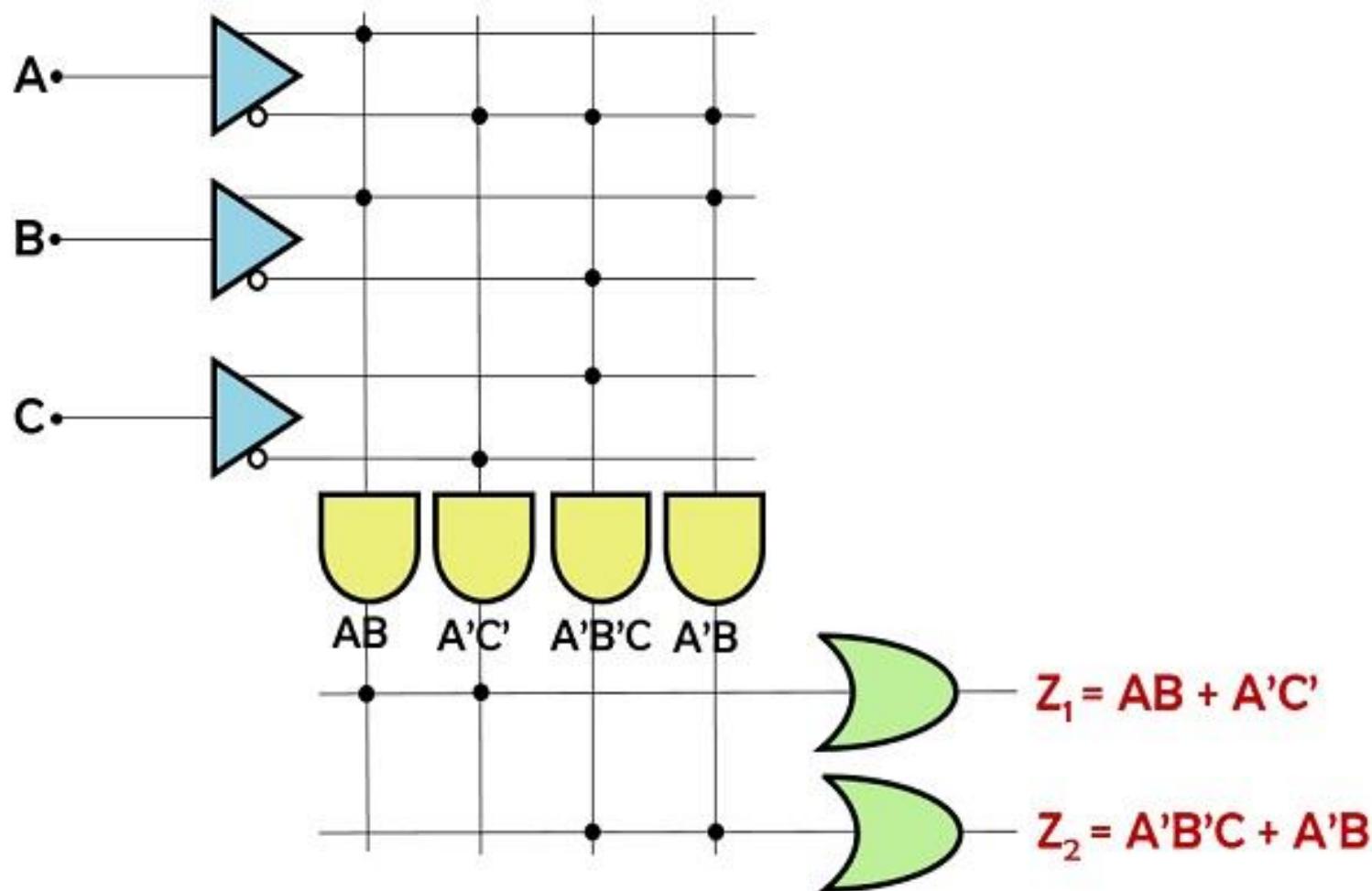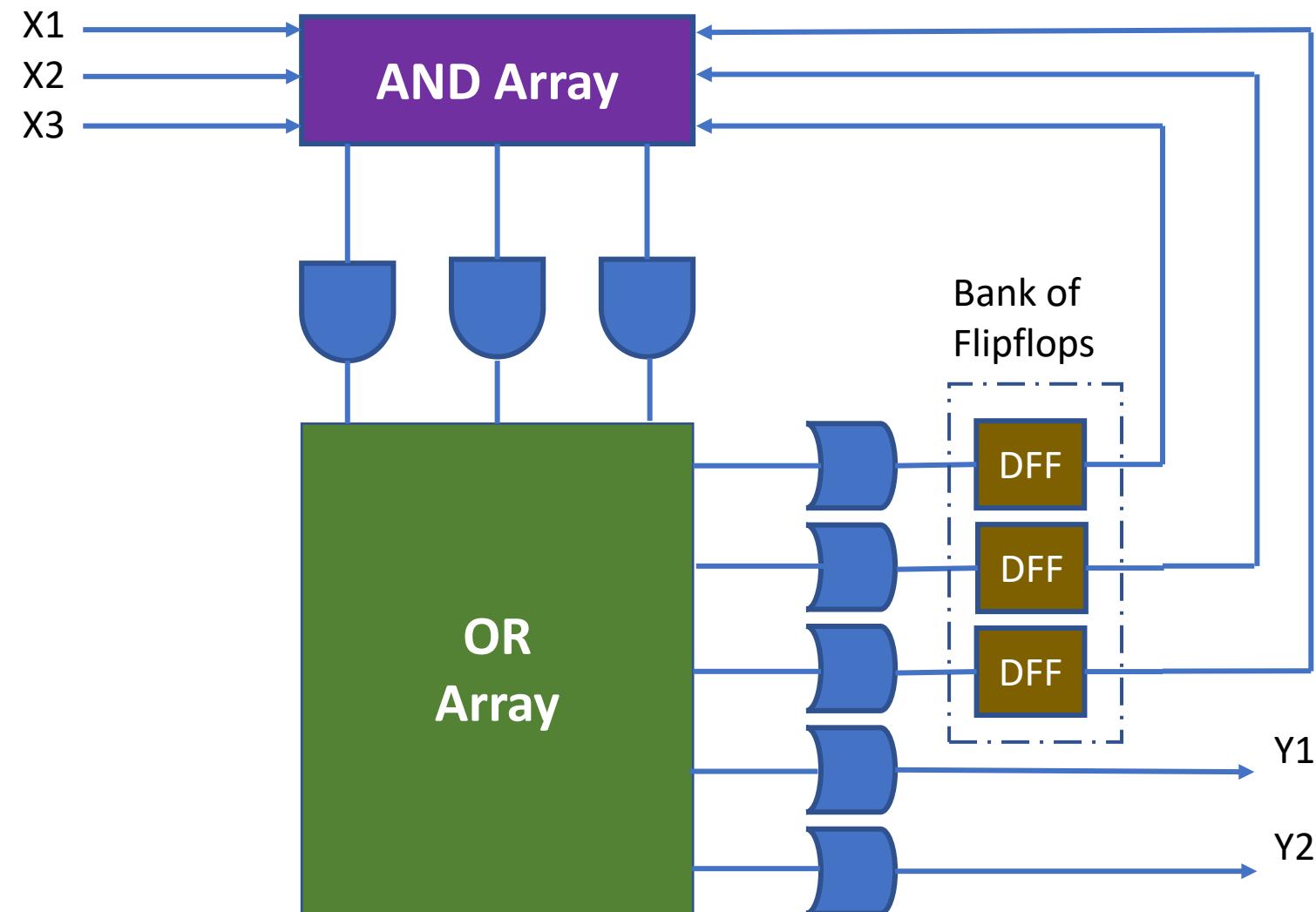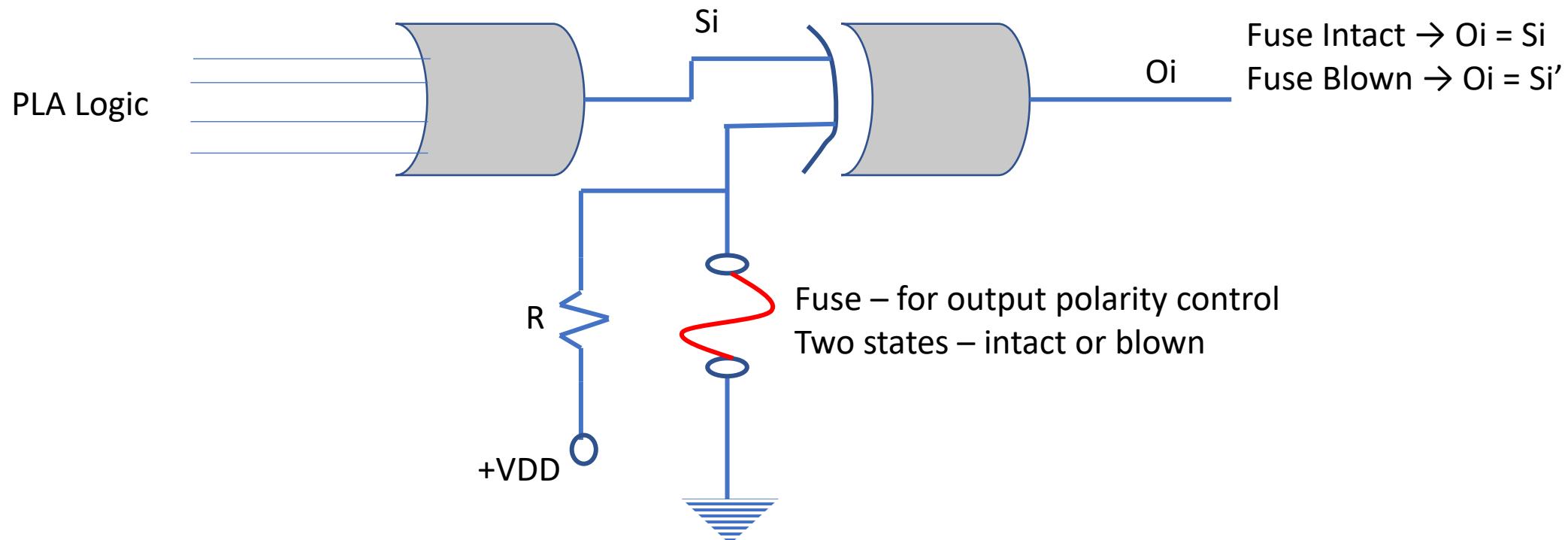
Implementation of Programmable Logic Array

Electronics Coach

https://electronicscoach.com/programmable-logic-array.html

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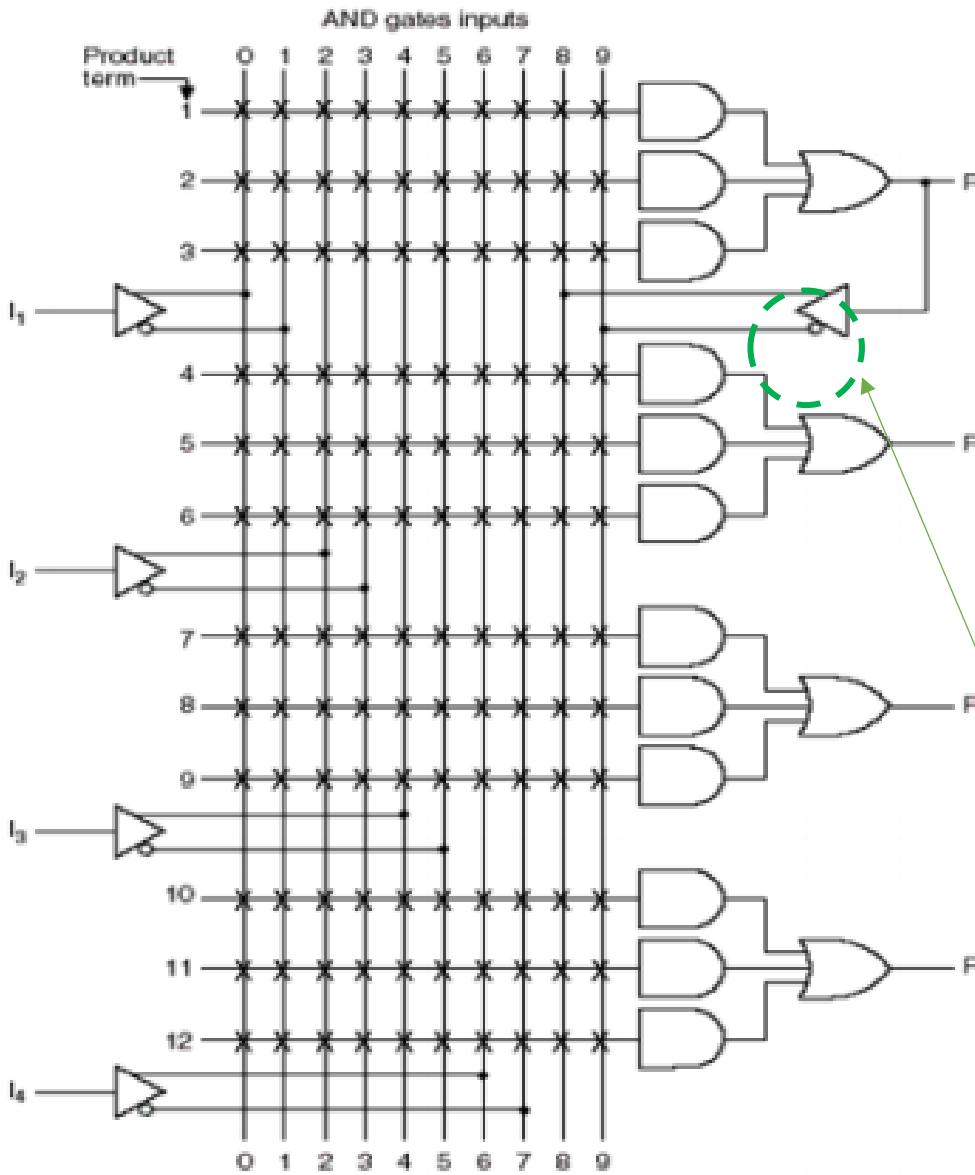
Sequential Circuits with PLD – Mealy Machine

Output Polarity Control

PLA Logic

Si

Oi

Fuse Intact → Oi = Si
Fuse Blown → Oi = Si'

R

Fuse – for output polarity control
Two states – intact or blown

+VDD

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PAL – Programmable Array Logic Example
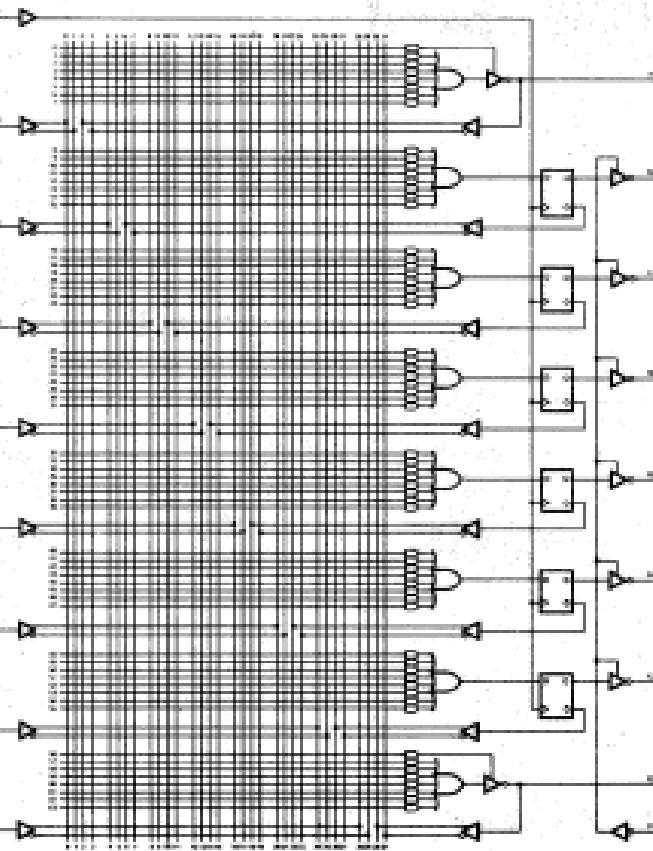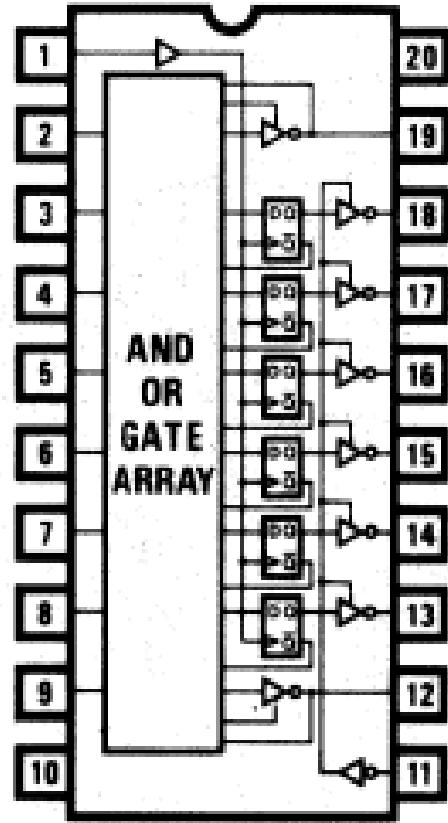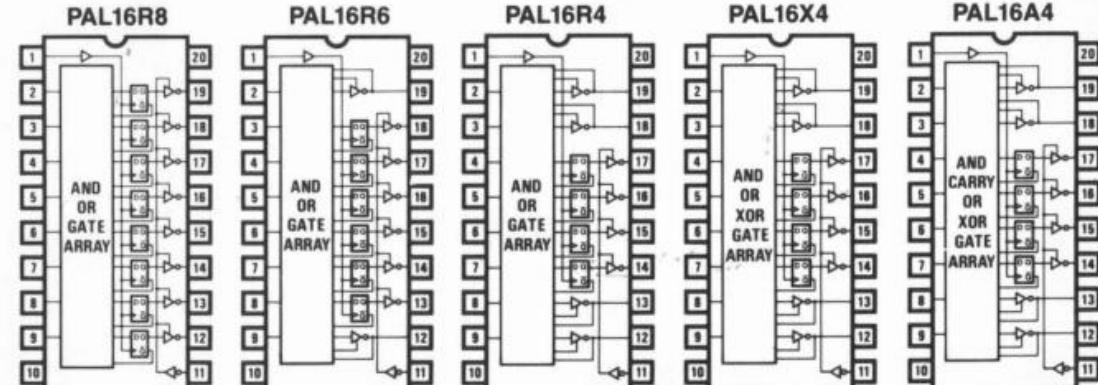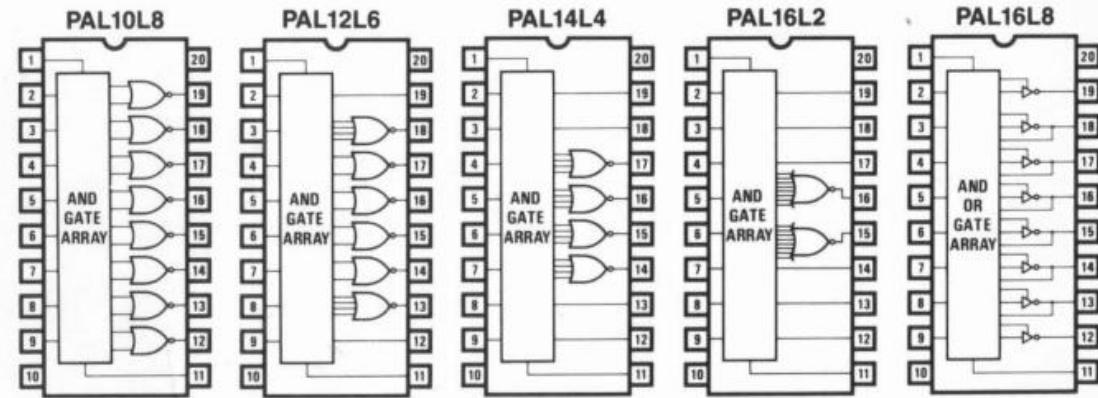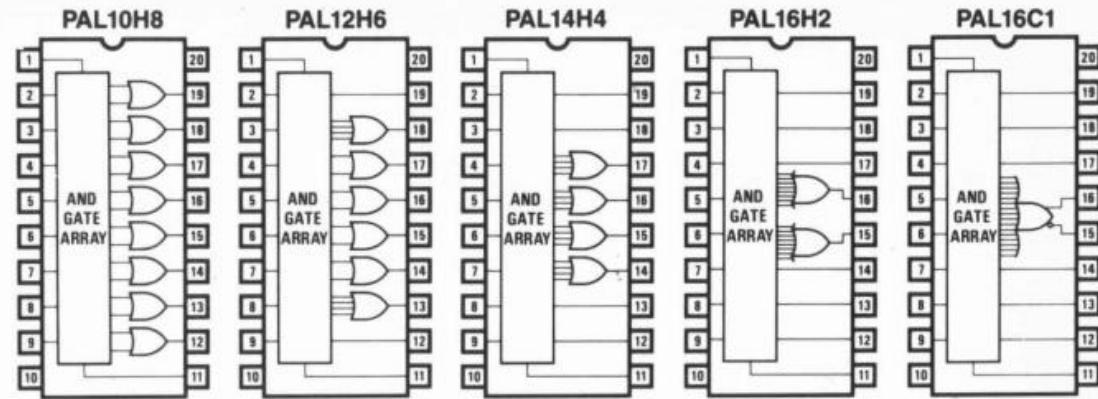
- PAL Device is a PLD with fixed OR array and a programmable AND array
- As only AND gates are programmable, PAL is easier to program but it is less flexible compared to PLA devices

Example device:

- This device has 4 inputs and 4 outputs.
- Each input has a buffer and inverter, output is from fixed OR gate
- The device has 4 sections: Each section comprises 3 wide AND-OR array, meaning three programmable AND arrays in each section
- Each AND gates has 10 programmable input connections
- One of the outputs (see F1) can be fed back to the inputs of AND gate through programmable connections

https://faculty.kfupm.edu.sa/COE/aimane/coe202/PLDs.pdf

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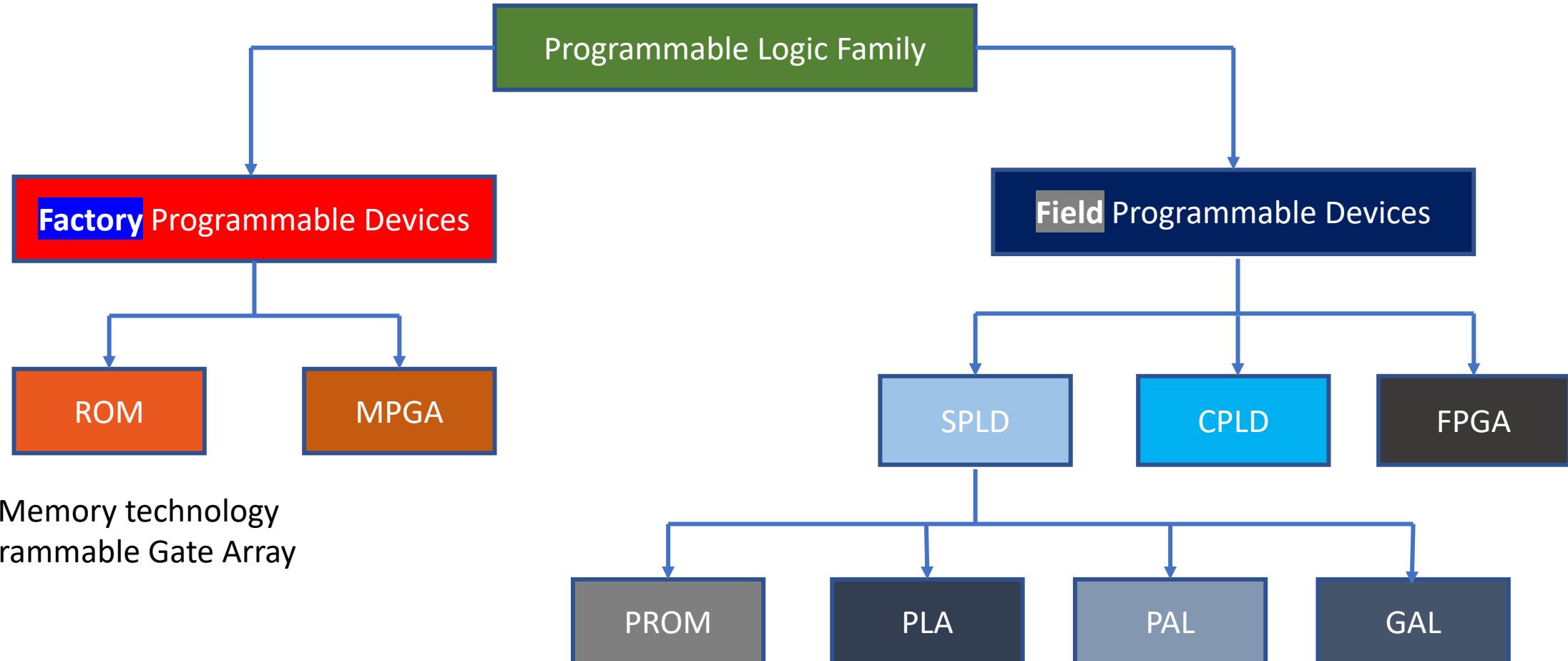
PLA Family Examples

PAL16R6

PAL16R6 Logic Diagram

20-Pin PAL Logic Symbols

PAL10H8 PAL12H6 PAL14H4 PAL16H2 PAL16C1

PAL10L8 PAL12L6 PAL14L4 PAL16L2 PAL16L8

PAL16R8 PAL16R6 PAL16R4 PAL16X4 PAL16A4

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Datasheet of PLA / PAL

- Go through PAL and PLA Datasheet for some examples

Programmable Logic Broad Classification

```
                    ┌──────────────────────────────┐
                    │ Programmable Logic Family     │
                    └──────────────────────────────┘
         ┌────────────────────┴────────────────────────┐
┌─────────────────────────────┐          ┌─────────────────────────────┐
│ Factory Programmable Devices│          │ Field Programmable Devices  │
└─────────────────────────────┘          └─────────────────────────────┘
      ┌──────────┴──────────┐        ┌──────────────┼──────────────┐
  ┌────────┐         ┌────────┐  ┌────────┐    ┌────────┐    ┌────────┐
  │  ROM   │         │  MPGA  │  │  SPLD  │    │  CPLD  │    │  FPGA  │
  └────────┘         └────────┘  └────────┘    └────────┘    └────────┘
```

Read only Memory technology
Mask Programmable Gate Array

```
        ┌──────────┬──────────┬──────────┐
   ┌────────┐ ┌────────┐ ┌────────┐ ┌────────┐
   │  PROM  │ │  PLA   │ │  PAL   │ │  GAL   │
   └────────┘ └────────┘ └────────┘ └────────┘
```

Simple and Complex Programmable Logic Devices
Field Programmable Gate Array
Generic Array Logic (complex PAL by lattice semi), Programmable Logic Array

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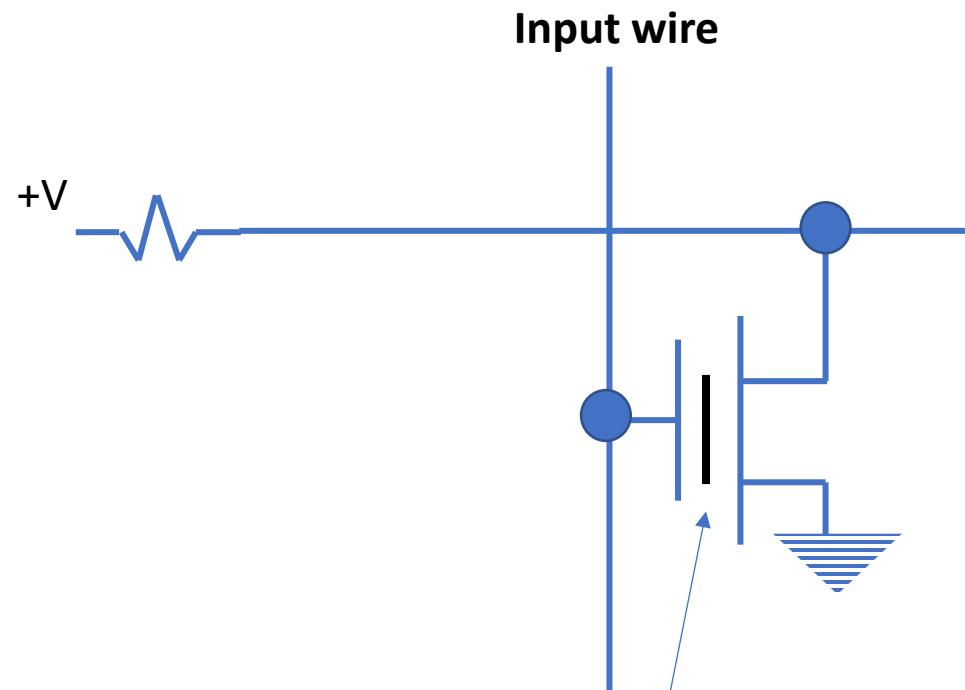
Programmable Hardware Devices Comparison

Table 3-1: *A Comparison of Programmable Devices*

	SPLD	CPLD	FPGA
Density	Low Few hundred gates	Low to Medium 500 to 12,000 gates	Medium to High 3,000 to 5,000,000 gates
Timing	Predictable	Predictable	Unpredictable
Cost	Low	Low to Medium	Medium to High
Major Vendors	Lattice Semiconductor Cypress AMD	Xilinx Altera	Xilinx Altera Lattice Semiconductor Actel
Example Device Families	**Lattice Semiconductor** GAL16LV8 GAL22V10 **Cypress** PALCE16V8 **AMD** 22V10	**Xilinx** CoolRunner XC9500 **Altera** MAX	**Xilinx** Virtex Spartan **Altera** Stratix **Lattice** Mach ECP **Actel** Accelerator

Ref: Roth &
John Book

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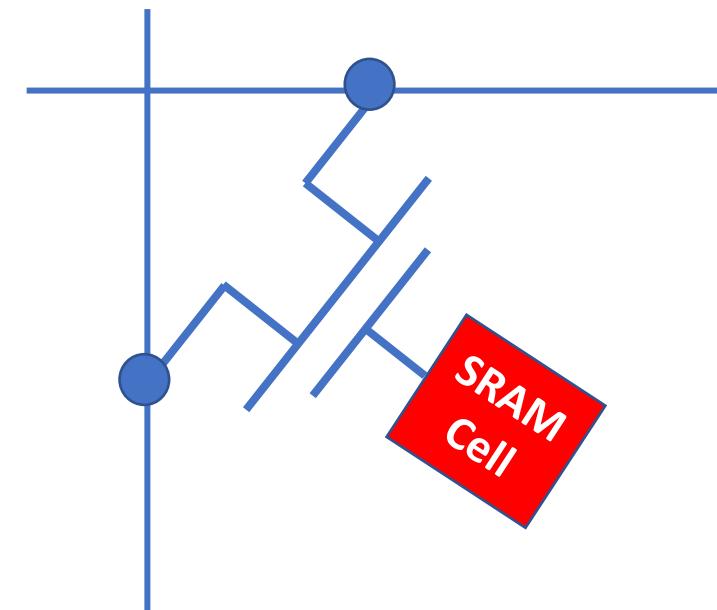
Interconnect Technology for Field Programming

EEPROM / FLASH

SRAM

Input wire

+V
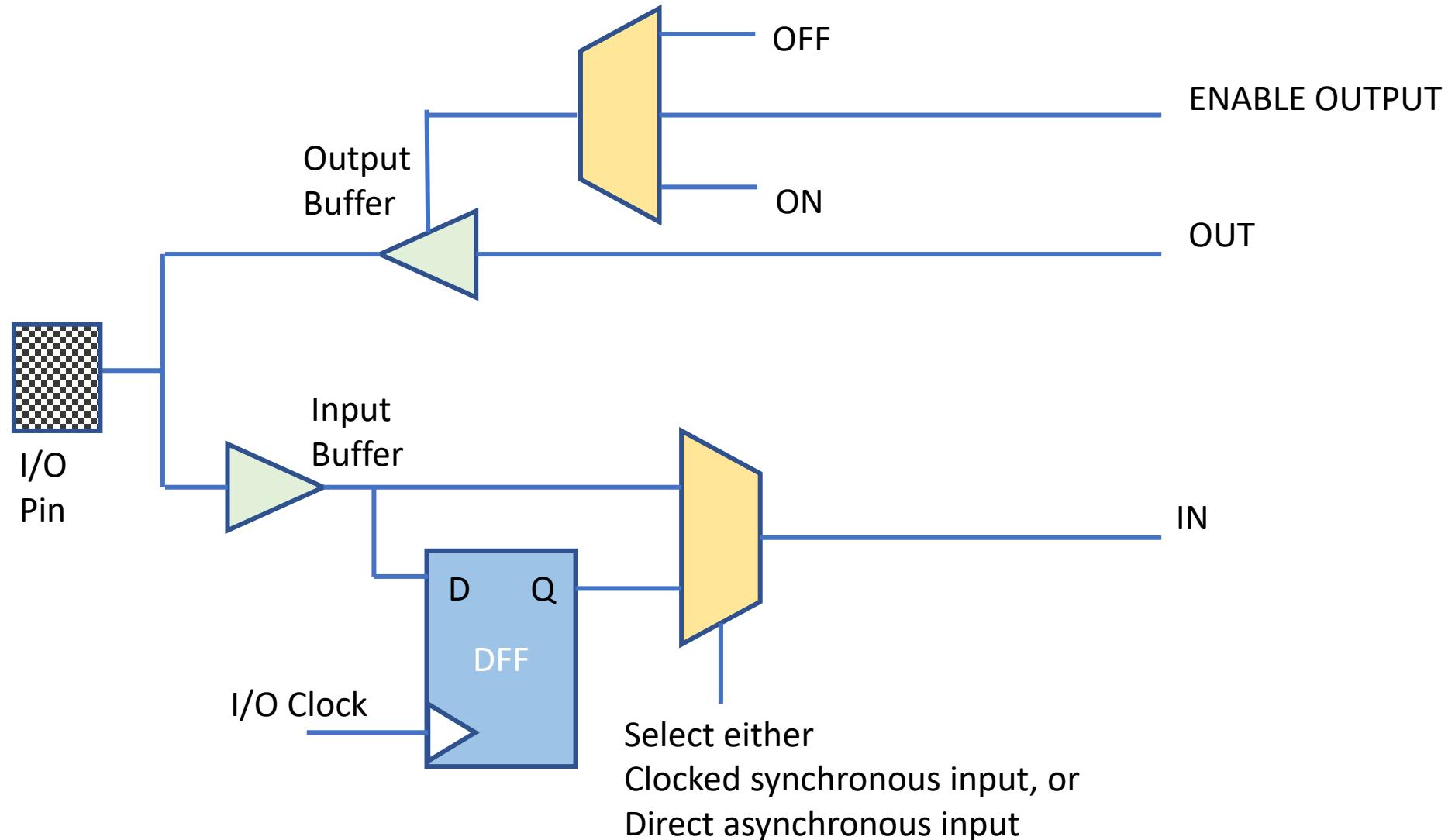
Floating Gate
Tunneling process
Used in EEPROM, USB Flash drive, etc.

SRAM
Cell

SRAM Cell is connected to Gate terminal
MOS Switch behaves as per stored value in SRAM

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Concept of a Programmable I/O Block

OFF

ENABLE OUTPUT

Output
Buffer

ON

OUT

I/O
Pin

Input
Buffer

IN

D   Q

DFF

I/O Clock

Select either
Clocked synchronous input, or
Direct asynchronous input

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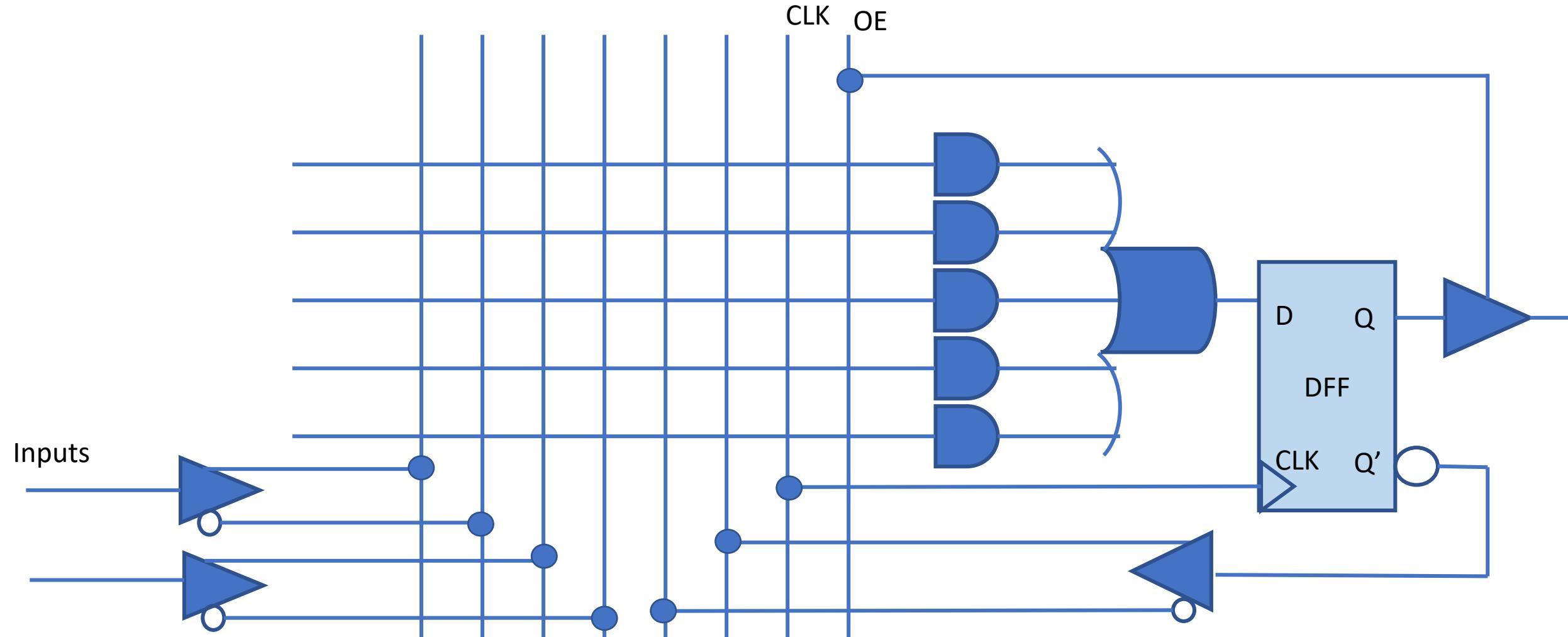
Introducing CPLD – Complex Programmable Logic Devices

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Description of Basic (Registered) Macrocell
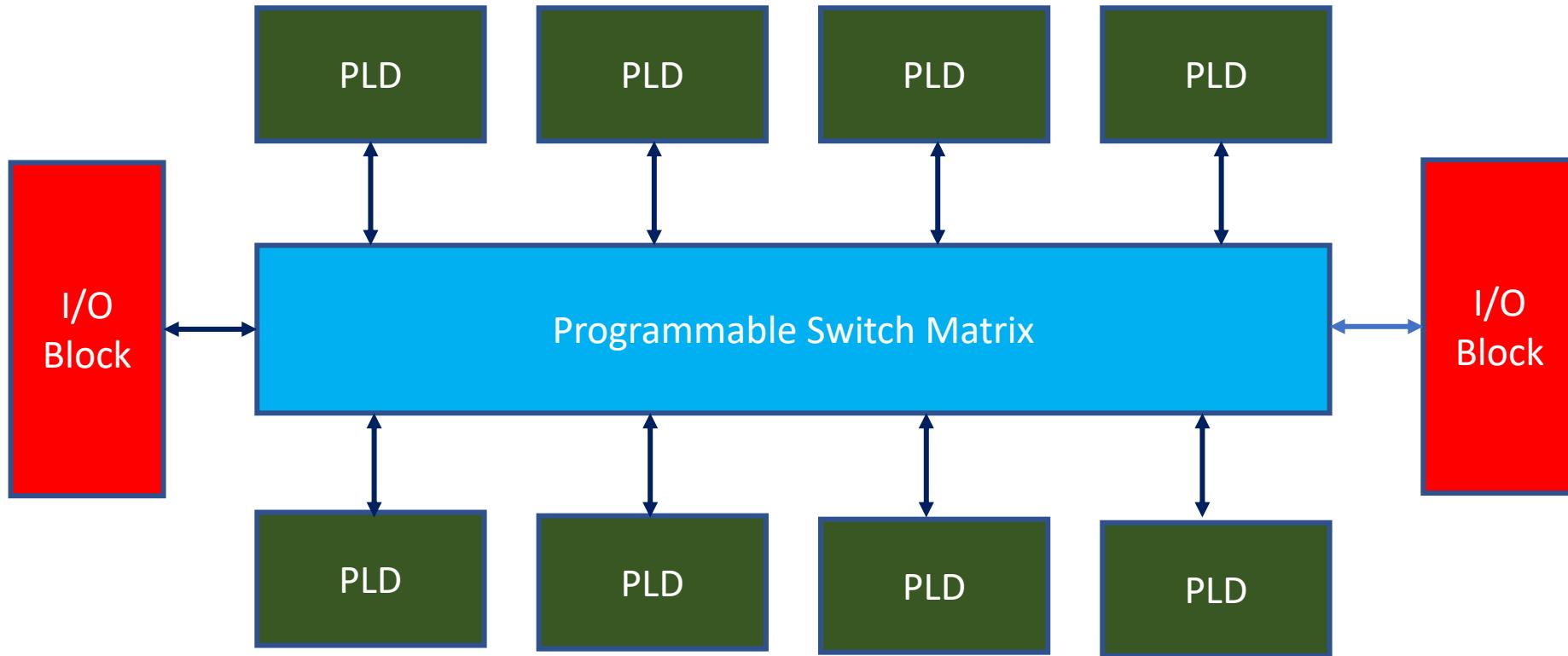
- Each section of an SPLD is called a macrocell that contains SOP combinational logic and an optional Flipflop

- A typical SPLD has from 8 to 10 macrocells within one chip

- All Flipflops are connected to common CLK input

- All three-state buffers at Flipflop output are controlled by a common OE input

Basic Macrocell Logic

PAL that includes a DFF is called a Registered PAL

Generic CPLD Configuration
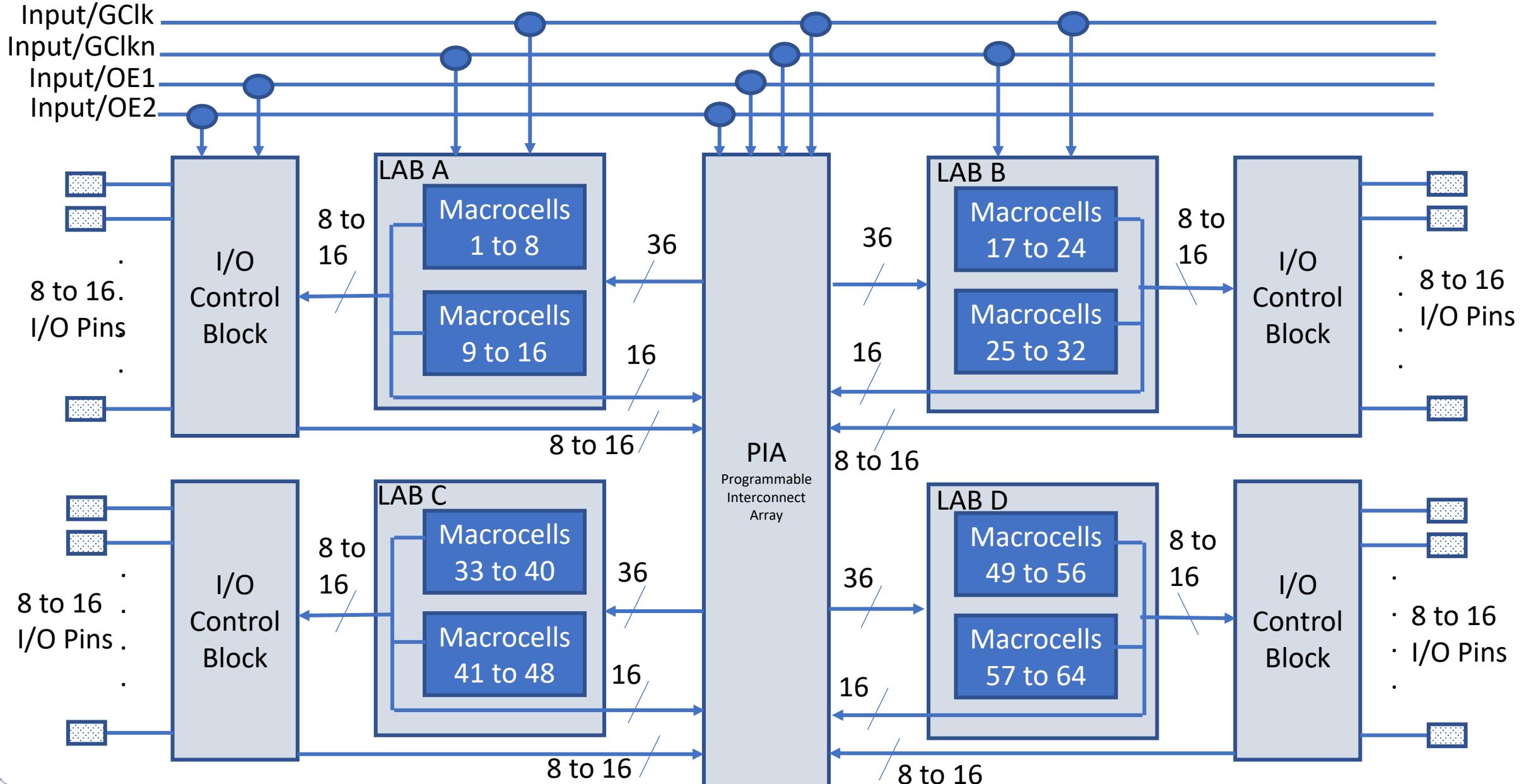
Description of CPLD

- Structured Array of PLD blocks
- Programmable On-Chip Interconnection Fabric
- Have higher number of inputs without much increase in area
- 100% connectivity between macrocells, BUT not all outputs of macrocells are connected to OUTPUT
- Wide Fan-In AND gates are used at INPUTS
- Outputs of macrocells can be routed within the chip to form more complex logic blocks
- The Interconnect Array selects signals from I/O blocks or macrocell outputs and connects them back to function block inputs
- The I/O blocks provide an interface between bidirectional physical I/O pins and the interior of the CPLD

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Details of Generic CPLD Configuration

- Collection of individual PLD gate arrays on a single integrated circuit

- Each I/O pin is driven by a 3-state buffer and can be programmed to act as Input or Output pin

- Each PLD typically contains 8 to 16 macrocells

- If a macrocell has unused product terms, they can be used by nearby macrocells

- The outputs of macrocells can be routed to inputs of other macrocells to form complex multi-level logic functions

- Different manufactures offer variations in PLD design, programmable switching matrix and different types of I/O blocks

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Altera 7000 Series CPLD Architecture

Input/GClk
Input/GClkn
Input/OE1
Input/OE2

LAB A

Macrocells 1 to 8

Macrocells 9 to 16

LAB B

Macrocells 17 to 24

Macrocells 25 to 32

LAB C

Macrocells 33 to 40

Macrocells 41 to 48

LAB D

Macrocells 49 to 56

Macrocells 57 to 64

I/O Control Block

PIA
Programmable Interconnect Array

8 to 16 I/O Pins

8 to 16 · I/O Pins

8 to 16
36
16
8 to 16

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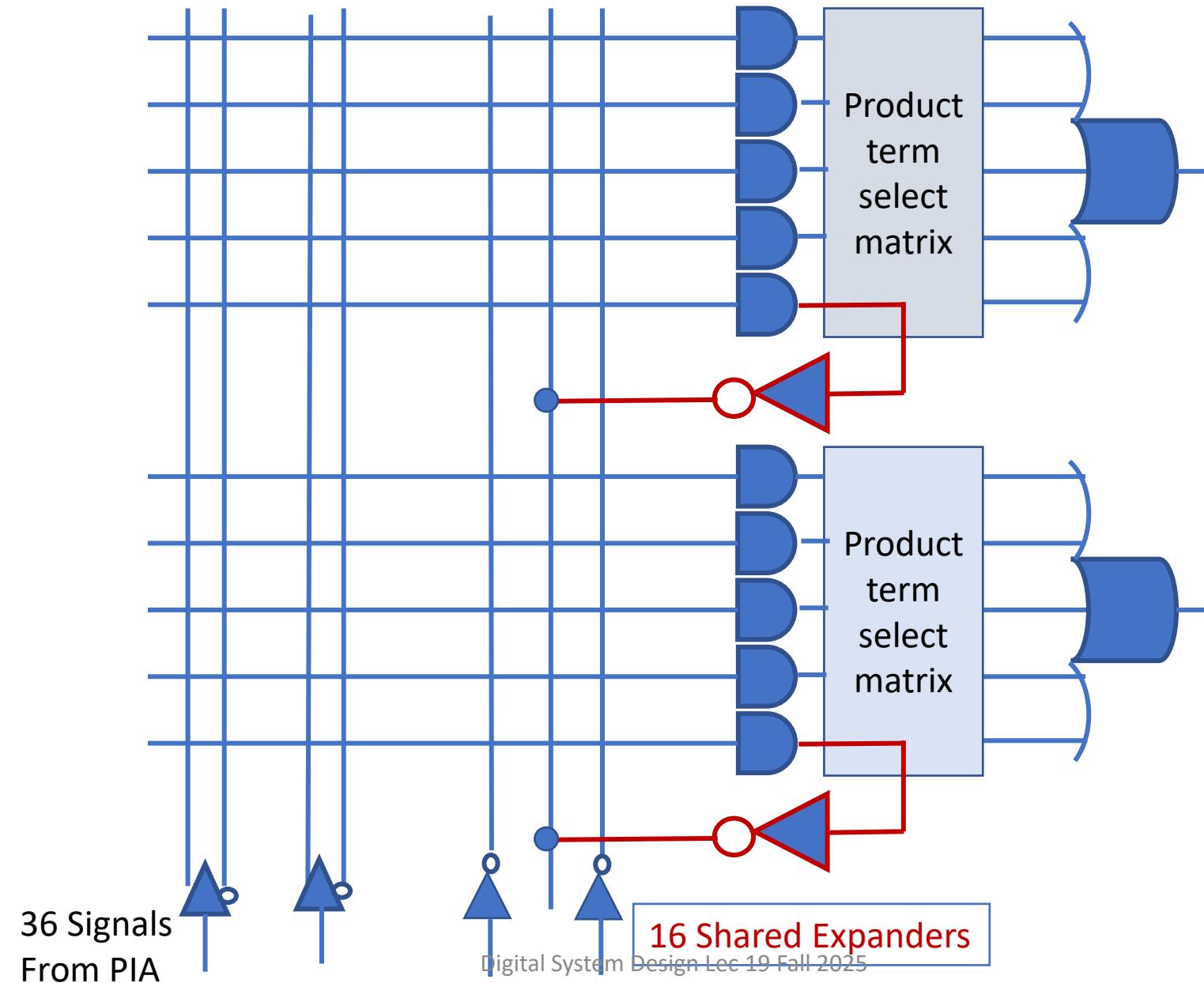
Details of Altera 7000 CPLD

- Floating gate EEPROM Configuration memory cells
- Architecture consists of an array of logic array blocks (**LAB**), programmable interconnect array (**PIA**) and an array of programmable I/O blocks
- Each LAB has 36 inputs and 16 outputs
- Each LAB consists of 16 macrocells providing both combinational and sequential logic
- PIA provides full connectivity between LAB and I/O Cells
- I/O Control block connects I/O Pins and PIA and LAB
- Global input clk (GCLK) and Global Clear (GCLR) connect to all macrocells
- Each macrocell can provide five product terms to its product-term-select matrix

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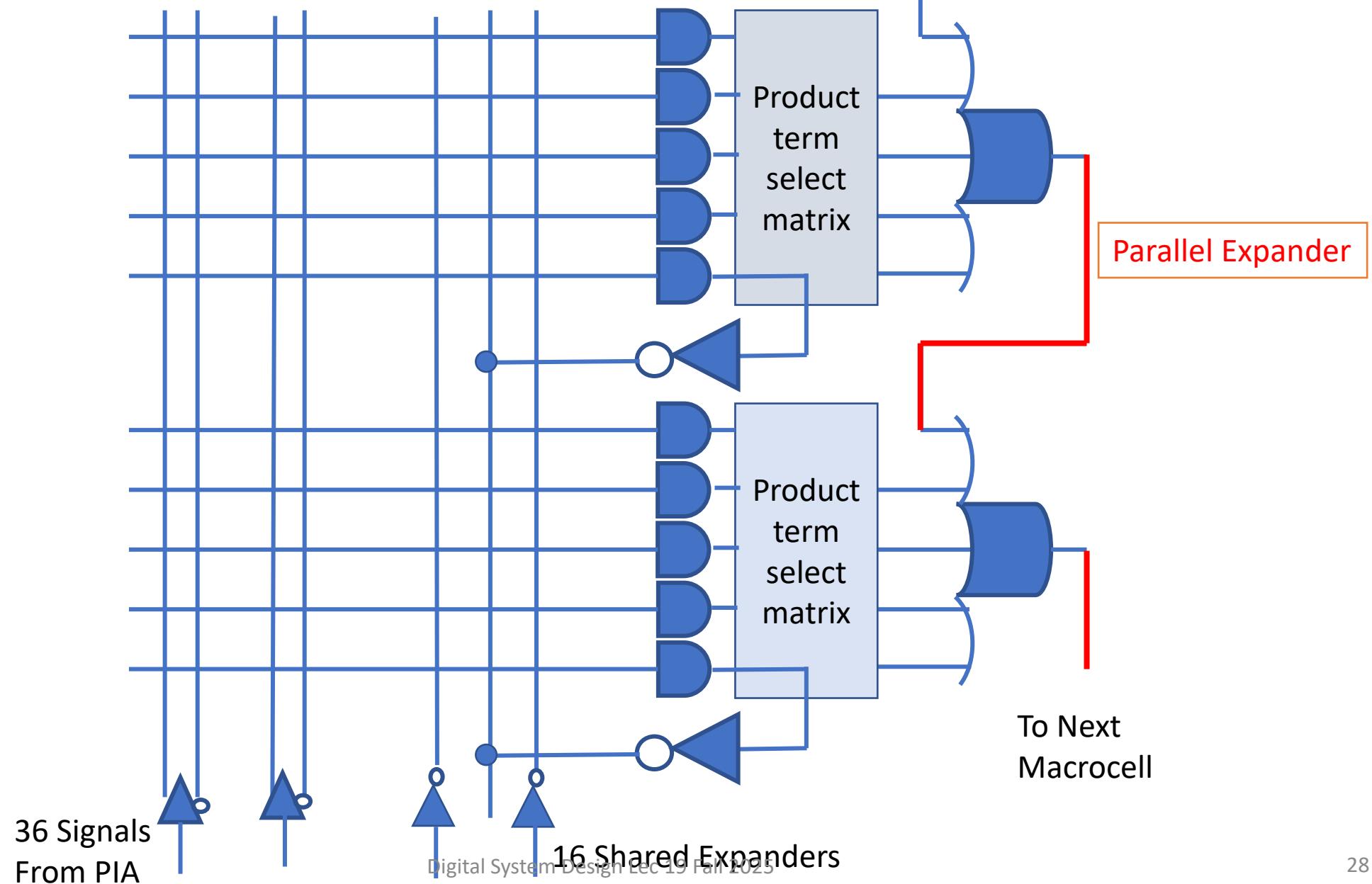
PIA and I/O

- The PIA provides full connectivity with predictable timing between LAB, dedicated inputs and I/O Pins

- The I/O Control block establishes connectivity between I/O Pins and PIA and LABs

- From 8 to 16 LAB outputs can be programmed to route through I/O Pins; and from 8 to 16 I/O Pins can be programmed to route through the I/O Control block to the PIA

- Altera architecture uses a PIA to connect LABs and I/O Pins. All signals are available throughout the device. The timing is thus predictable. The alternative is 'Channel-Routed Architecture' that is more denser but the timing is un-predictable as delays are routing-dependent

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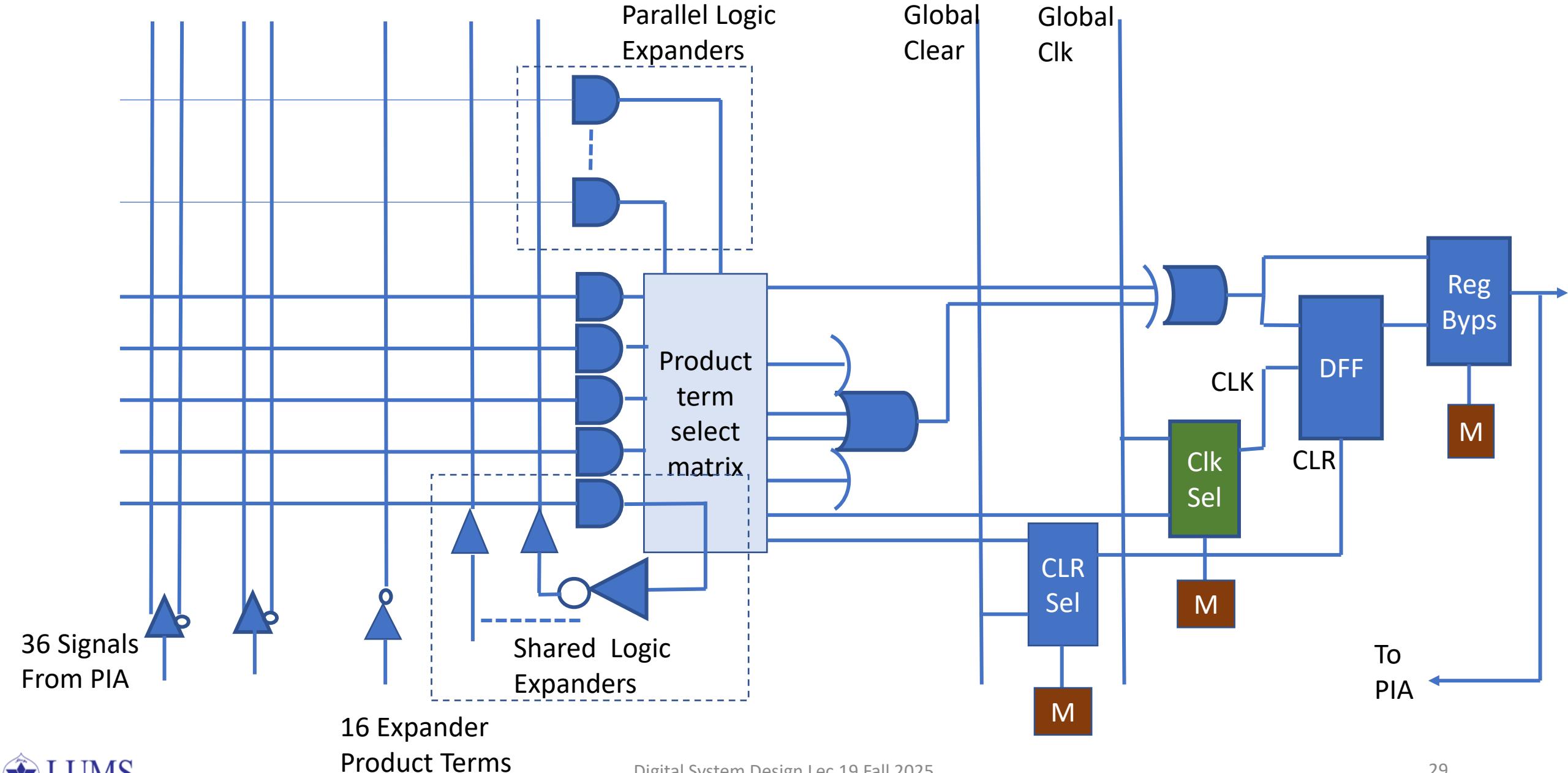
Shareable Expander in Altera 7000 CPLD


36 Signals
From PIA

16 Shared Expanders
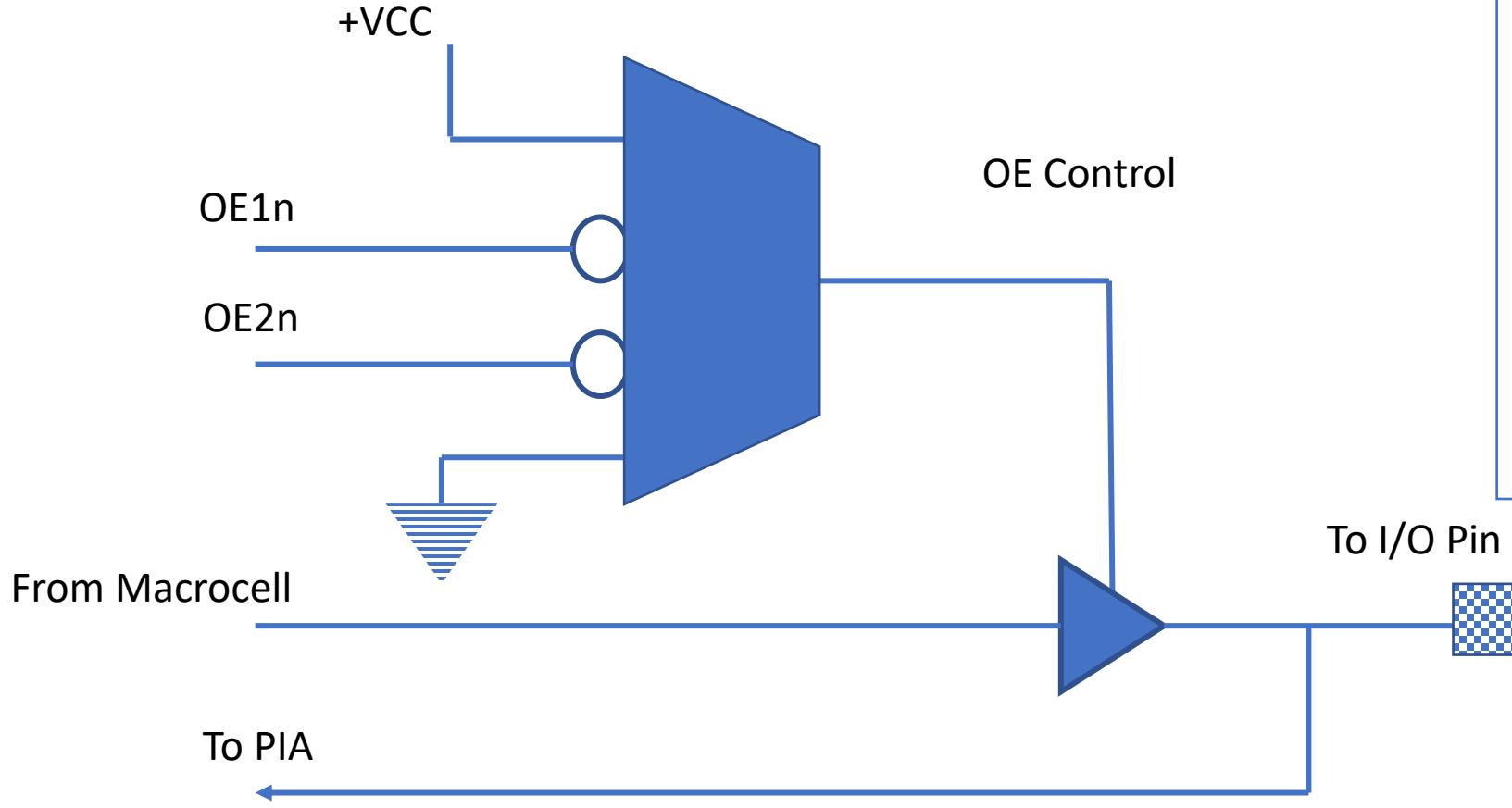
Parallel Expander in Altera 7000 CPLD

From Previous Macrocell

Product term select matrix

Parallel Expander

Product term select matrix

To Next Macrocell

36 Signals From PIA

16 Shared Expanders

Altera 7000 Series Macrocell Architecture

Parallel Logic Expanders

Global Clear

Global Clk

Product term select matrix

Reg Byps

DFF

Clk Sel

CLK

CLR

CLR Sel

M

M

M

M

Shared Logic Expanders

36 Signals From PIA

16 Expander Product Terms

To PIA

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Altera 7000 Series I/O Control Block

+VCC

OE Control

OE1n

OE2n

From Macrocell

To I/O Pin

To PIA
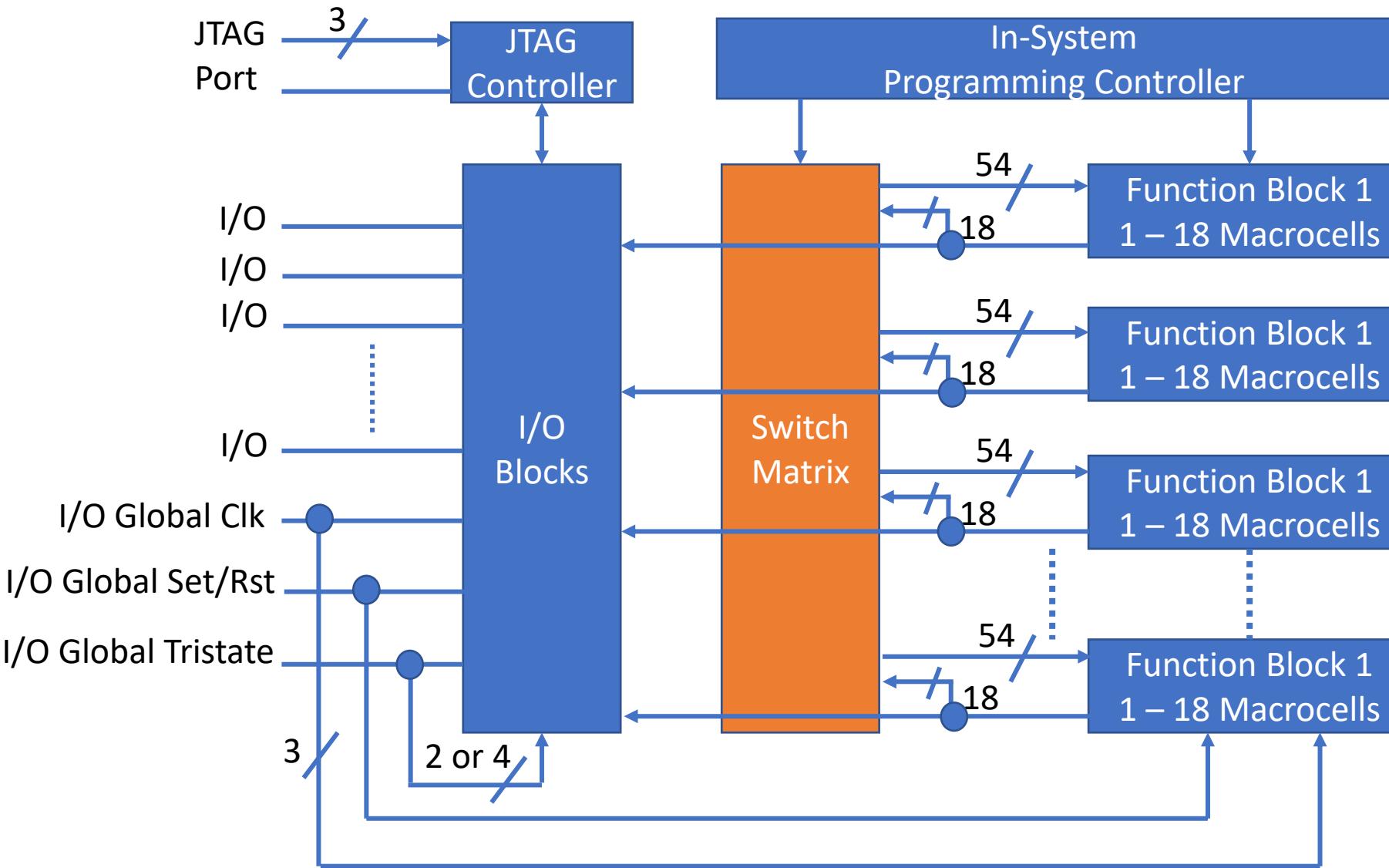
Each I/O Pin can be configured to be dedicated input pin, output pin Or bi-dir under control of OE1, OE2.

VCC will hardwire the I/O pin to output of macrocell.

GND will isolate macrocell and I/O pin Will be an input pin only.

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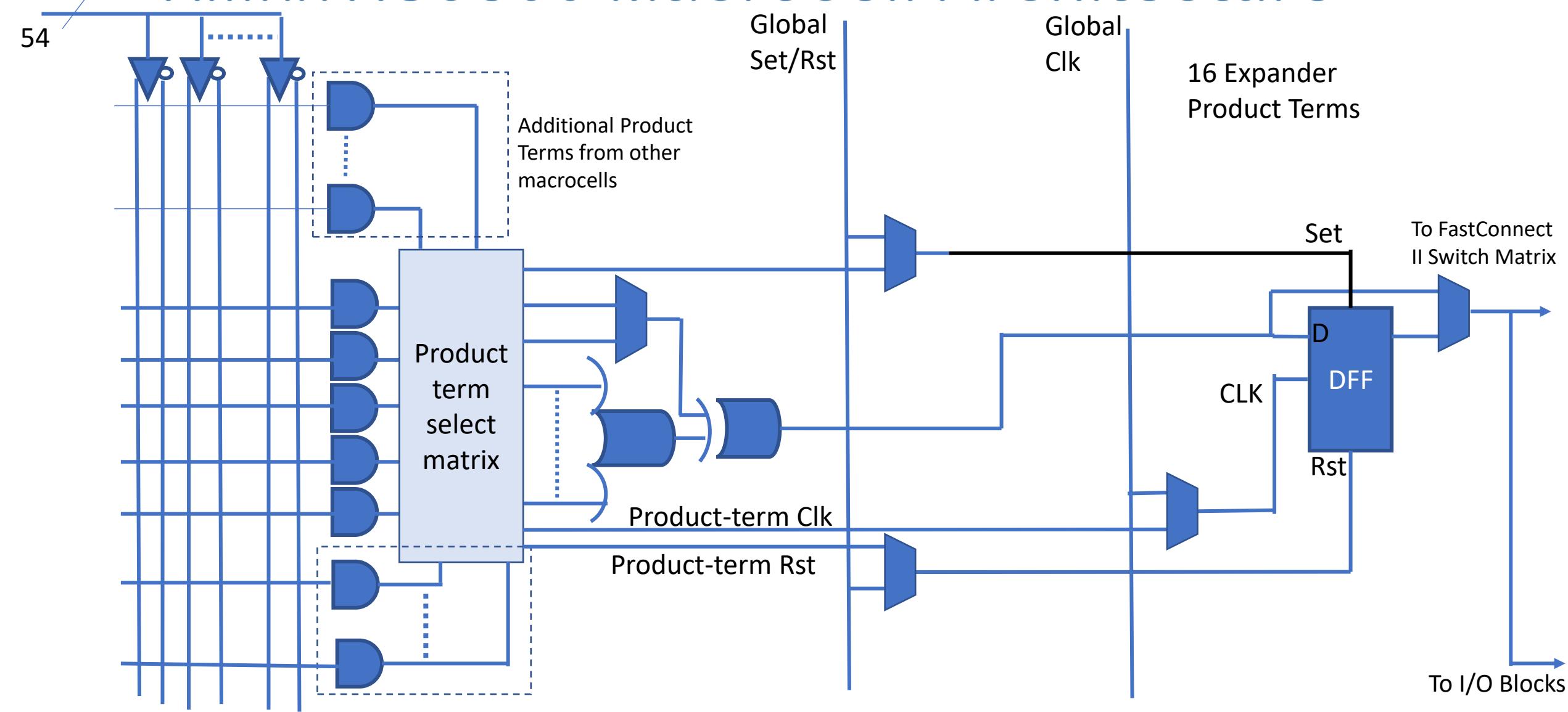
Xilinx XC9500 CPLD Architecture

JTAG Port — 3 → JTAG Controller

In-System Programming Controller

I/O Blocks

Switch Matrix

I/O
I/O
I/O
...
I/O

I/O Global Clk
I/O Global Set/Rst
I/O Global Tristate

54 / → Function Block 1
1 – 18 Macrocells
18

54 / → Function Block 1
1 – 18 Macrocells
18

54 / → Function Block 1
1 – 18 Macrocells
18

54 / → Function Block 1
1 – 18 Macrocells
18

3 /
2 or 4 /

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Details of Xilinx 9500 CPLD

- Flash based EEPROM Technology

- Comprises Few (4) Functional Blocks

- Each functional block contains 18 independent macrocells

- Each functional block has 54 inputs and 18 outputs

- Product-term-allocator allocates upto 90 product terms in each macrocell in a functional block to form SOP expressions

- Each macrocell can receive five direct product terms from the AND array and up to 10 more product terms can be made available from other un-committed product terms in other macrocells from same functional block

- Partial SOP terms can be combined from several macrocells

- Each macrocell can be independently configured for combinational or sequential functionality

# Xilinx XC9500 Macrocell Architecture

54

Global Set/Rst

Global Clk

16 Expander Product Terms

Additional Product Terms from other macrocells

Product term select matrix

Set

To FastConnect II Switch Matrix

D

DFF

CLK

Rst

Product-term Clk

Product-term Rst

To I/O Blocks

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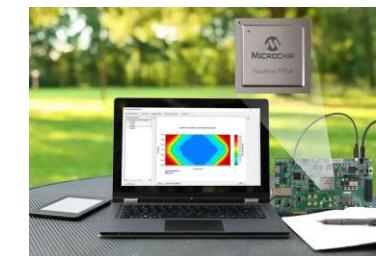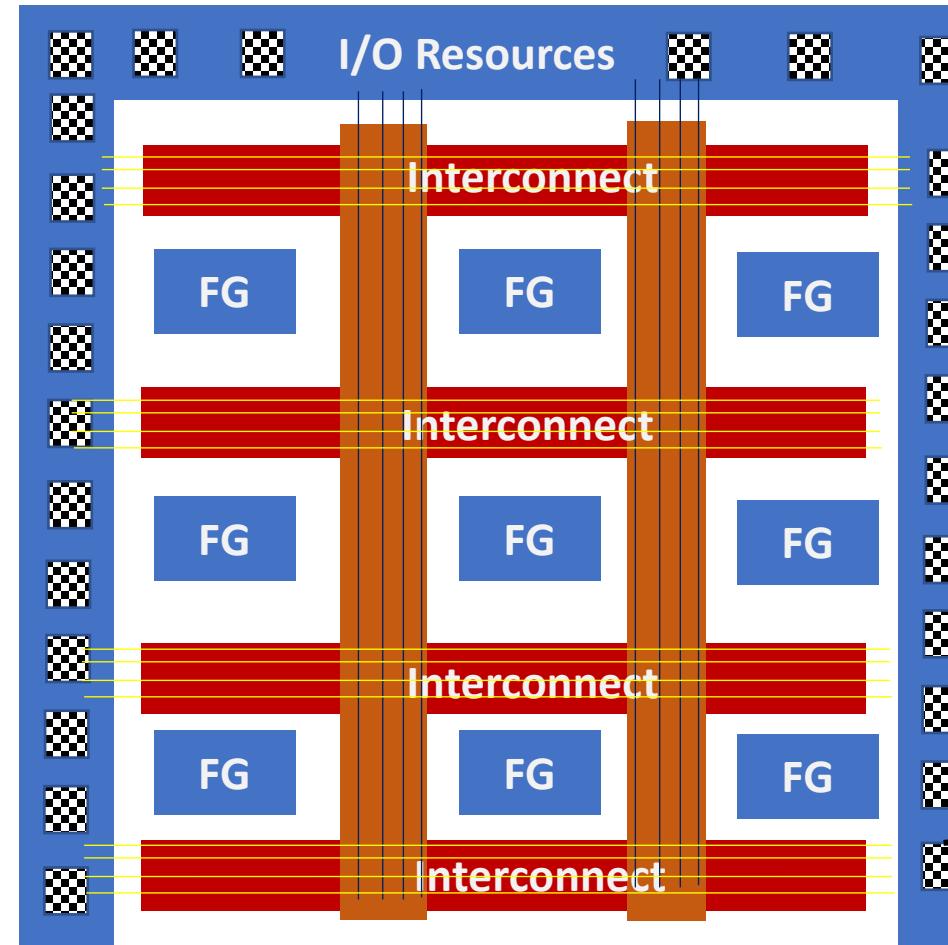
Field Programmable Gate Arrays
FPGA

Field Programmable Gate Arrays
Generic Architecture

I/O Resources

Interconnect

FG FG FG

Interconnect

FG FG FG

**Interconnect**

FG FG FG

Interconnect

FG = function generator for
**Logic implementation**
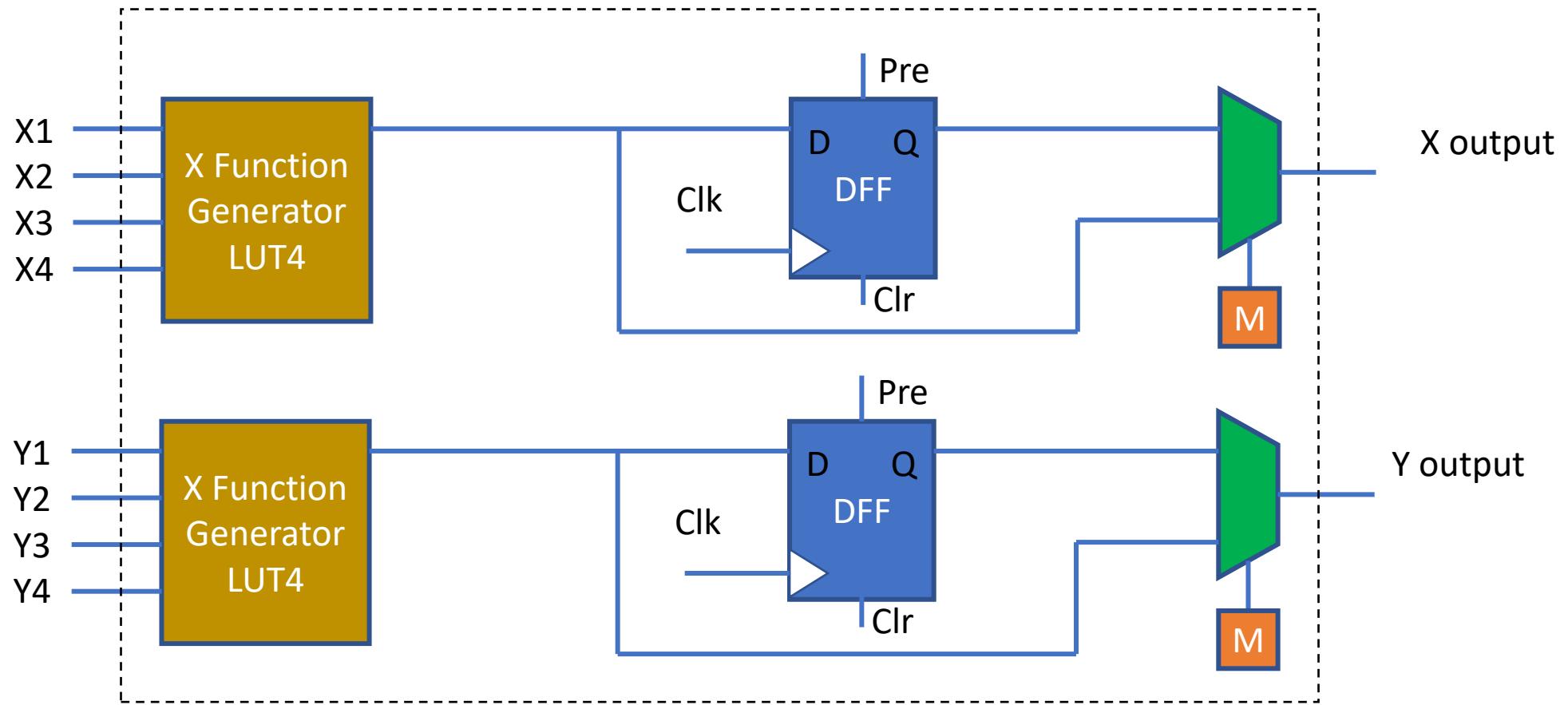
I/O Blocks

USB or
JTAG Cable

SRAM Configuration Memory

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# Lookup Table (LUT) based Configurable Logic Blocks
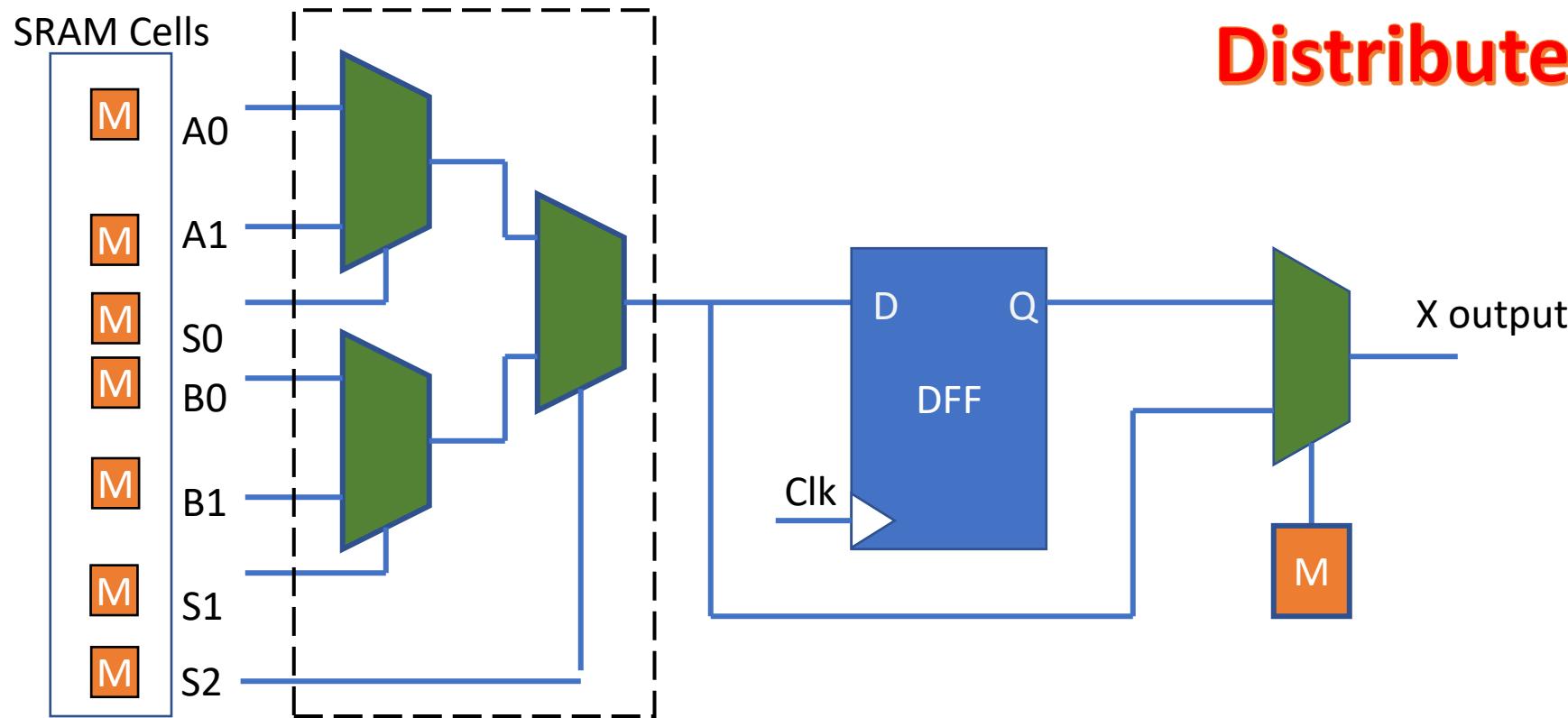
Details of LUT based CLB

- Uses a four-variable look-up table and a flipflop as the basic configurable hardware element. Several of these are combined in different families and types

- Any two functions X and Y of four variables each can be generated in the LUT

- Flipflops at the output can be used. DFF have external preset and clear as well as clock selection mechanism

- Output multiplexer selects from un-registered or registered output
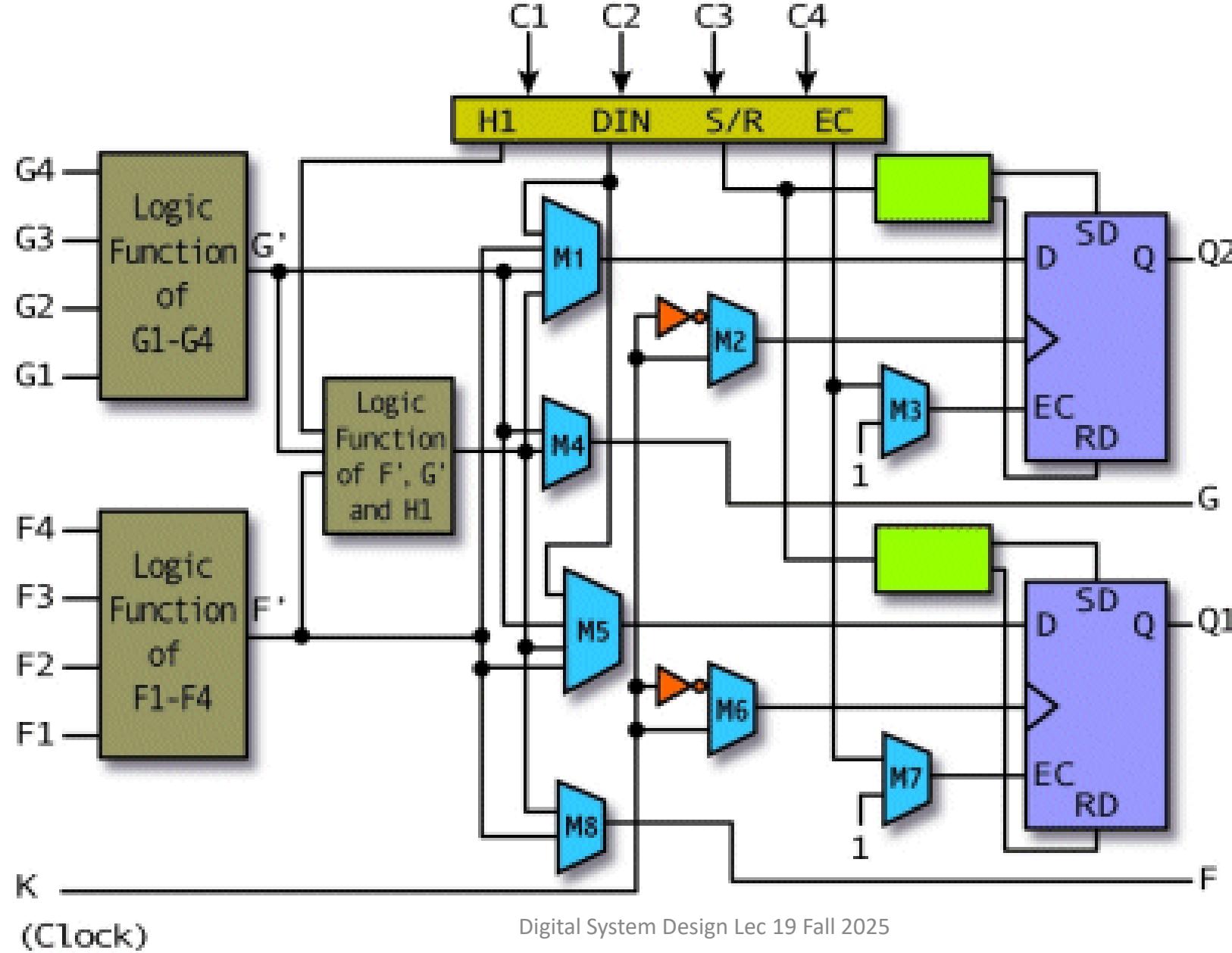
Configurable Logic Blocks based on Multiplexers

Where is Distributed Memory?

4:1 MUX to generate required SOP Expression

Xilinx 4000 CLB

LUT Configuration and Extension

2 Four-input function generators (Look Up Tables)
1 Three-input function
2 Registers:
- Pos. or Neg. edge-trig. Synchronous and asynchr. Set/Reset
Possible functions:
- any fct of 5 var.
- two fcts of 4 var. + one fct of 3 var.
- some fct of 9 var.