Lecture 20

EE 421 / CS 425

Digital System Design

Fall 2025

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Topics

- Recap – CPLD Architecture and Some Examples
- FPGA Architectures
- Configurable Logic Block
- Configurable I/O Blocks
- Distributed RAM, Block RAM, Dual Port Memory
- Special Features and DSP Slice in FPGA

Quiz on Tuesday

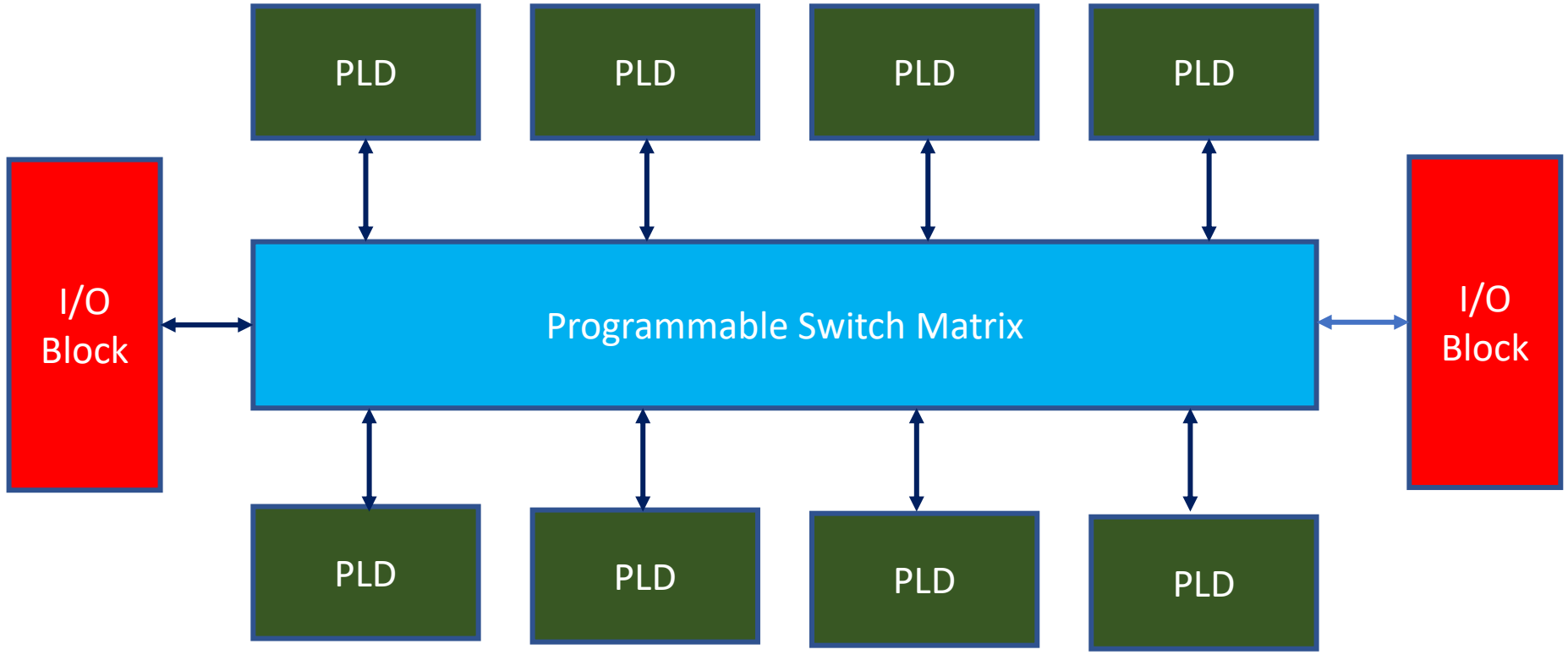
Recap from last lecture

- CPLD from Xilinx and Altera
- Architecture Differences between CPLD Families
- Important Building Blocks of CPLD
- Limitations of CPLD
- Predictable Timing Performance of CPLD
- How can logic complexity of CPLD macrocell be enhanced?
  - Expanders, etc.
- Programmable Output, Registered Output

Description of Basic (Registered) Macrocell

- Each section of an SPLD is called a macrocell that contains SOP combinational logic and an optional Flipflop
- A typical SPLD has from 8 to 10 macrocells within one chip
- All Flipflops are connected to common CLK input
- All three-state buffers at Flipflop output are controlled by a common OE input

Generic CPLD Configuration

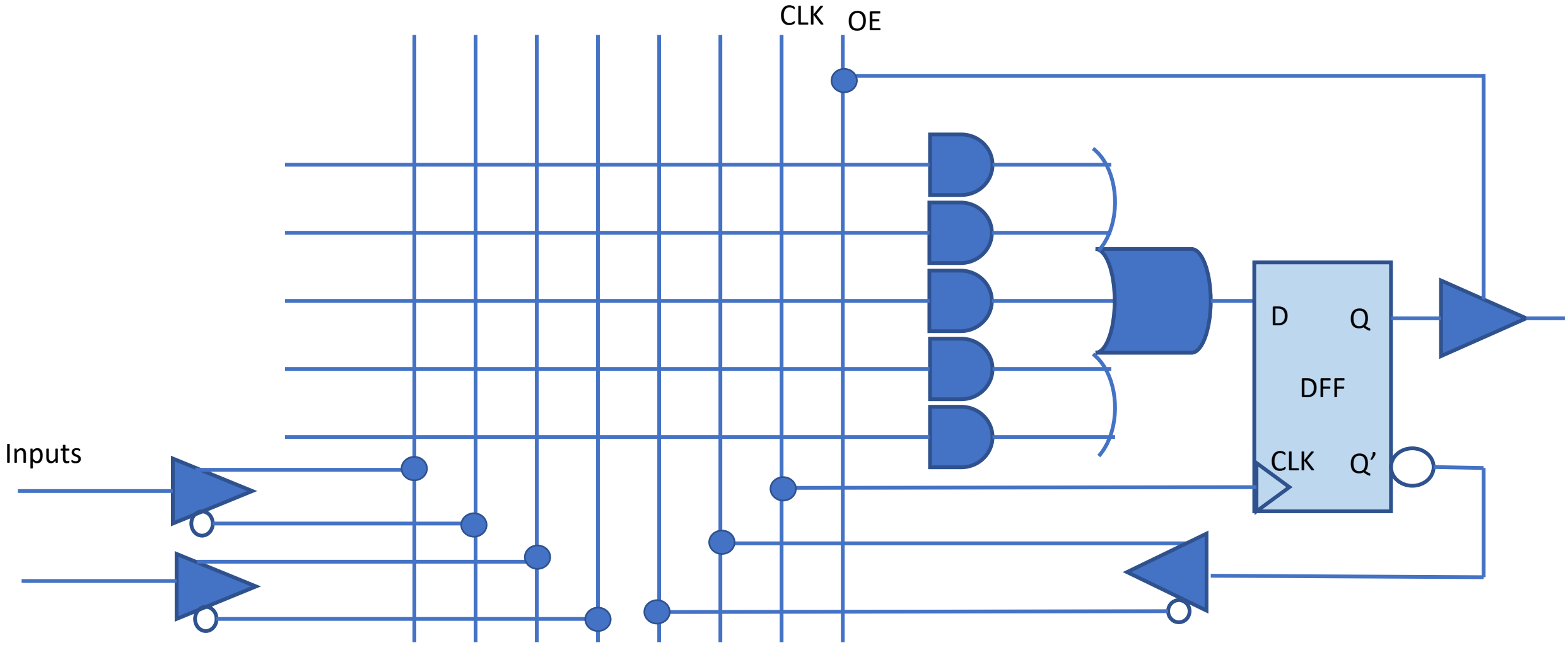


Details of Generic CPLD Configuration

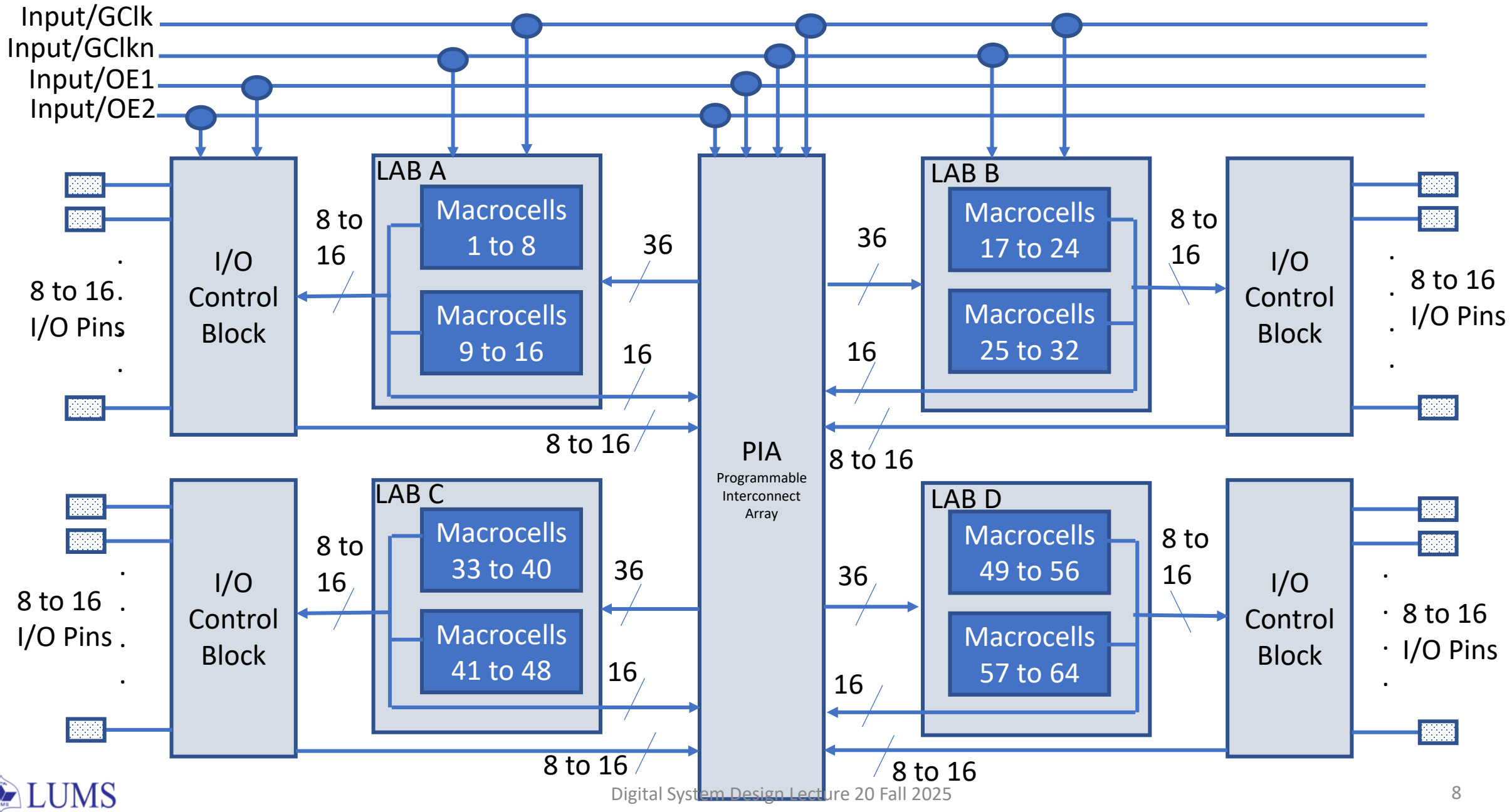
- Collection of individual PLD gate arrays on a single integrated circuit
- Each I/O pin is driven by a 3-state buffer and can be programmed to act as Input or Output pin
- Each PLD typically contains 8 to 16 macrocells
- If a macrocell has unused product terms, they can be used by nearby macrocells
- The outputs of macrocells can be routed to inputs of other macrocells to form complex multi-level logic functions - expanders
- Different manufactures offer variations in PLD design, programmable switching matrix and different types of I/O blocks

Basic Macrocell Logic

PAL that includes a DFF is called a Registered PAL



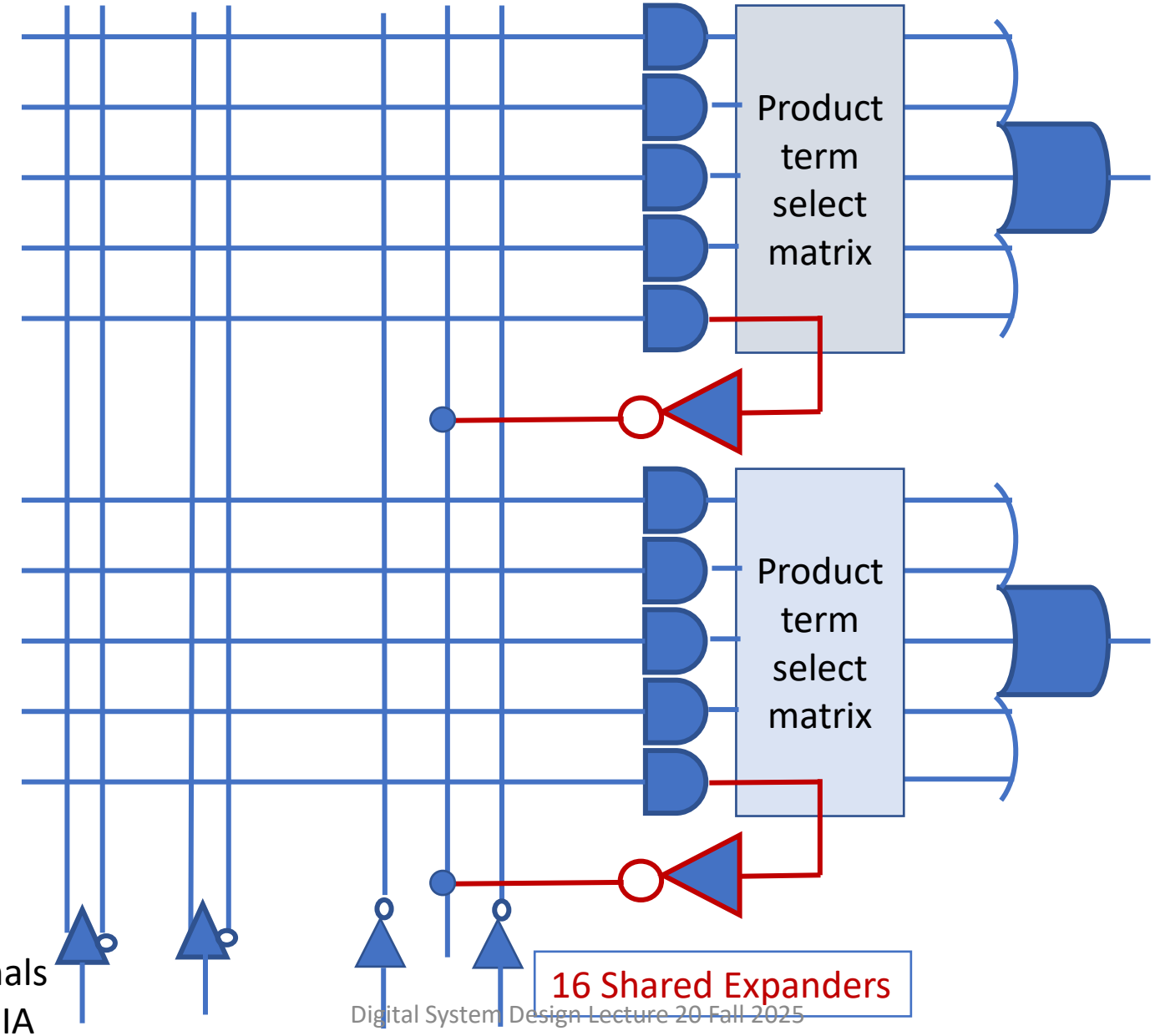
Altera 7000 Series CPLD Architecture



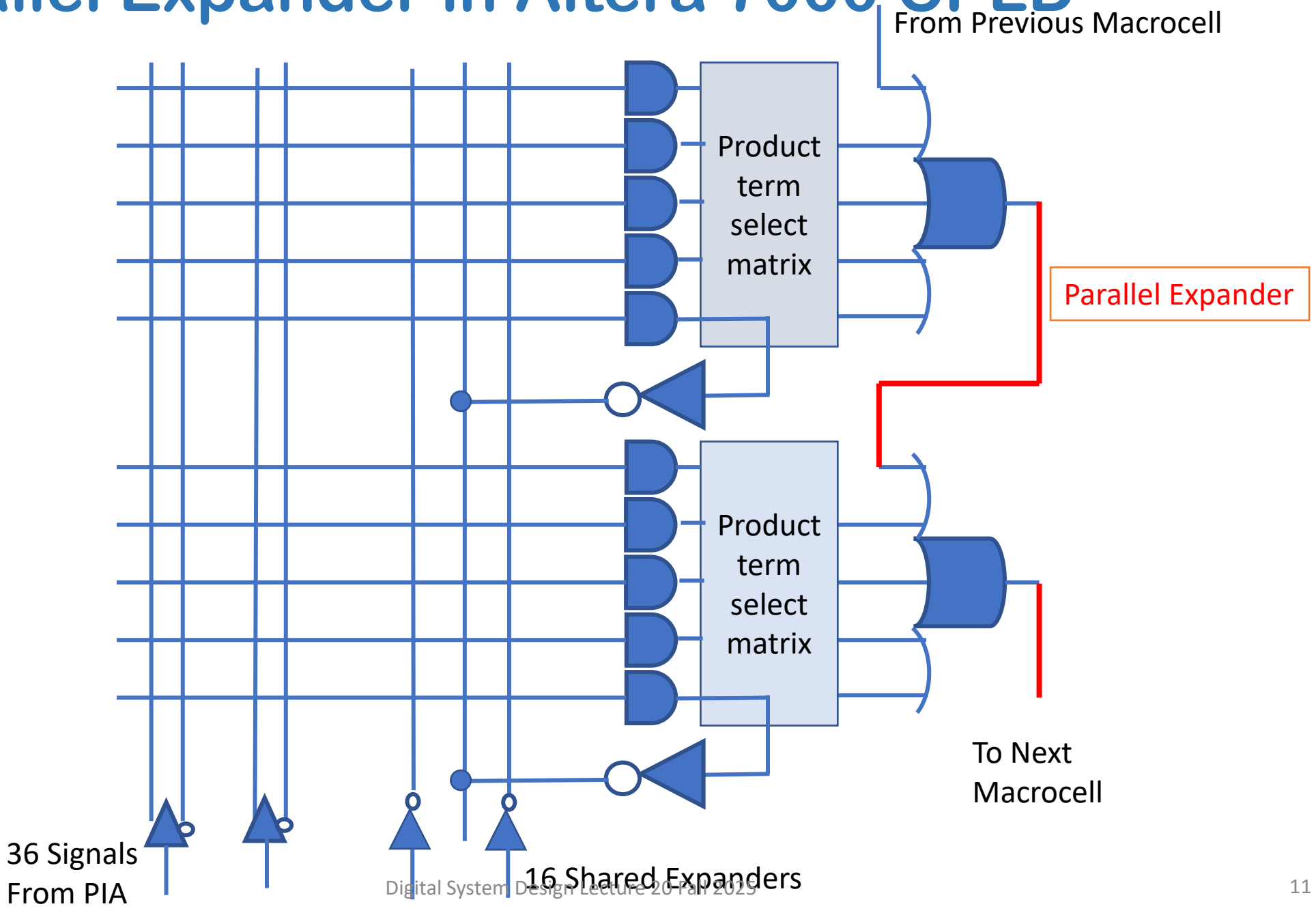
PIA and I/O

- The PIA provides full connectivity with predictable timing between LAB, dedicated inputs and I/O Pins
- The I/O Control block establishes connectivity between I/O Pins and PIA and LABs
- From 8 to 16 LAB outputs can be programmed to route through I/O Pins; and from 8 to 16 I/O Pins can be programmed to route through the I/O Control block to the PIA
- Altera architecture uses a PIA to connect LABs and I/O Pins. All signals are available throughout the device. The timing is thus predictable. The alternative is 'Channel-Routed Architecture' that is more denser but the timing is un-predictable as delays are routing-dependent

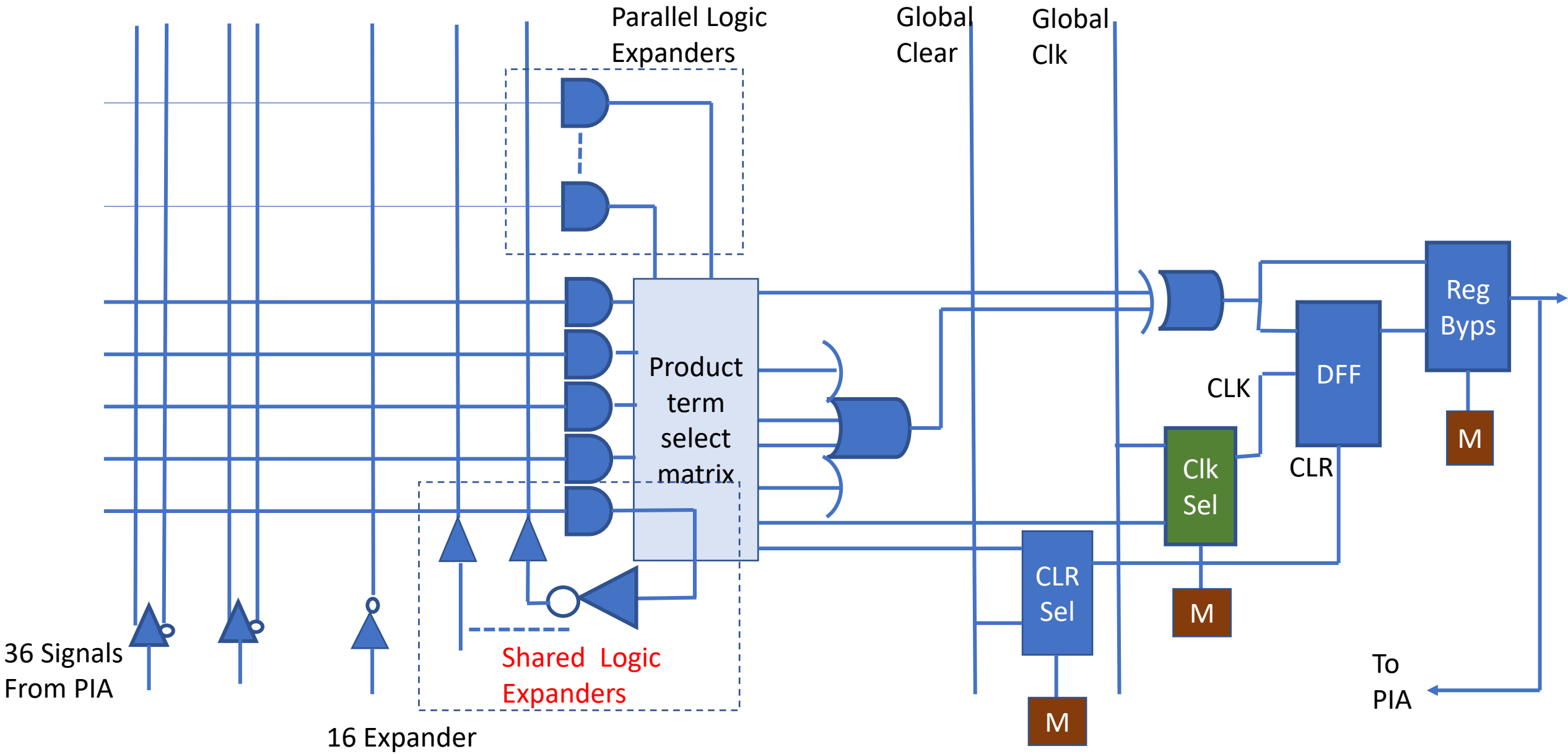
Shareable Expander in Altera 7000 CPLD



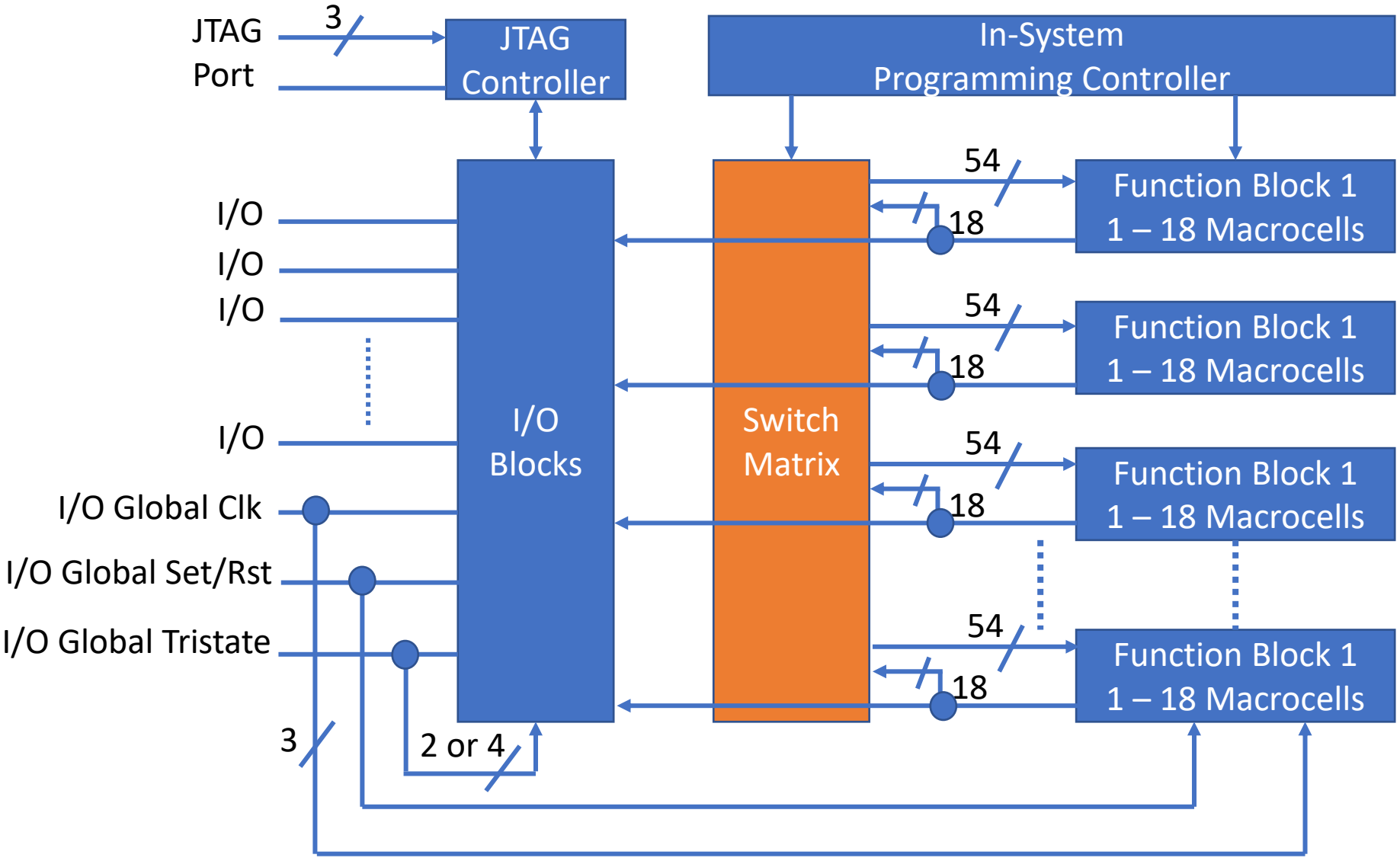
Parallel Expander in Altera 7000 CPLD



Altera 7000 Series Macrocell Architecture



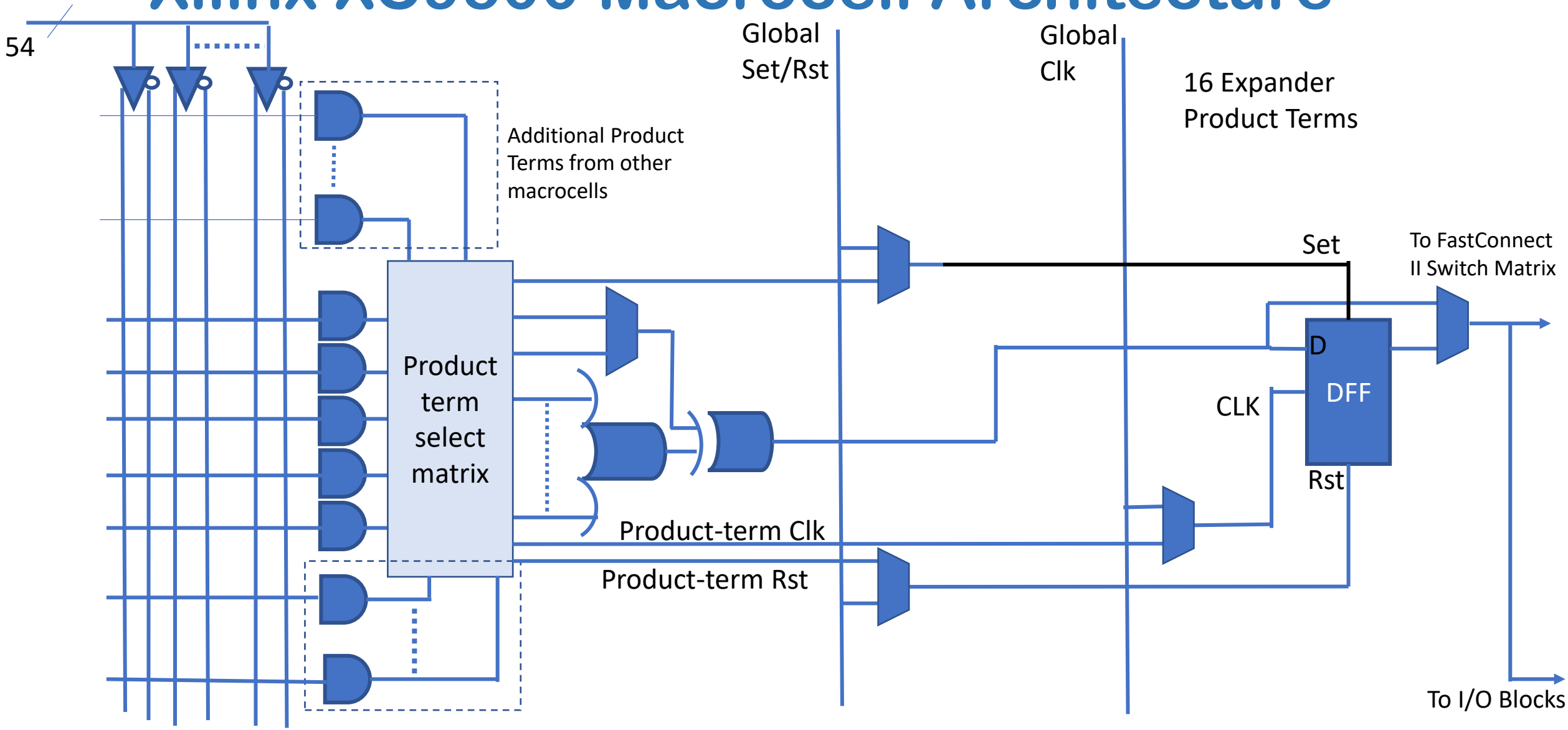
Xilinx XC9500 CPLD Architecture



Details of Xilinx 9500 CPLD

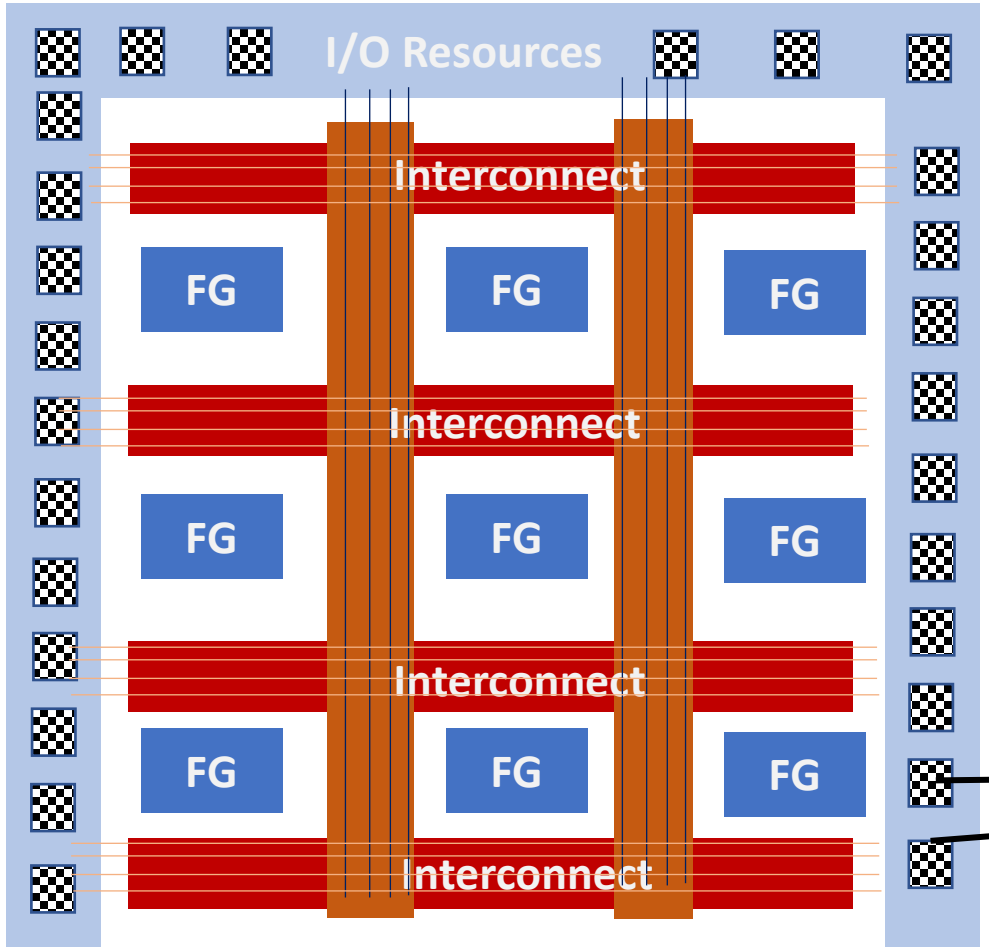
- Flash based EEPROM Technology
- Comprises Few (4) Functional Blocks
- Each functional block contains 18 independent macrocells
- Each functional block has 54 inputs and 18 outputs
- Product-term-allocator allocates upto 90 product terms in each macrocell in a functional block to form SOP expressions
- Each macrocell can receive five direct product terms from the AND array and up to 10 more product terms can be made available from other un-committed product terms in other macrocells from same functional block
- Partial SOP terms can be combined from several macrocells
- Each macrocell can be independently configured for combinational or sequential functionality

Xilinx XC9500 Macrocell Architecture



Field Programmable Gate Arrays
FPGA

Field Programmable Gate Arrays Generic Architecture



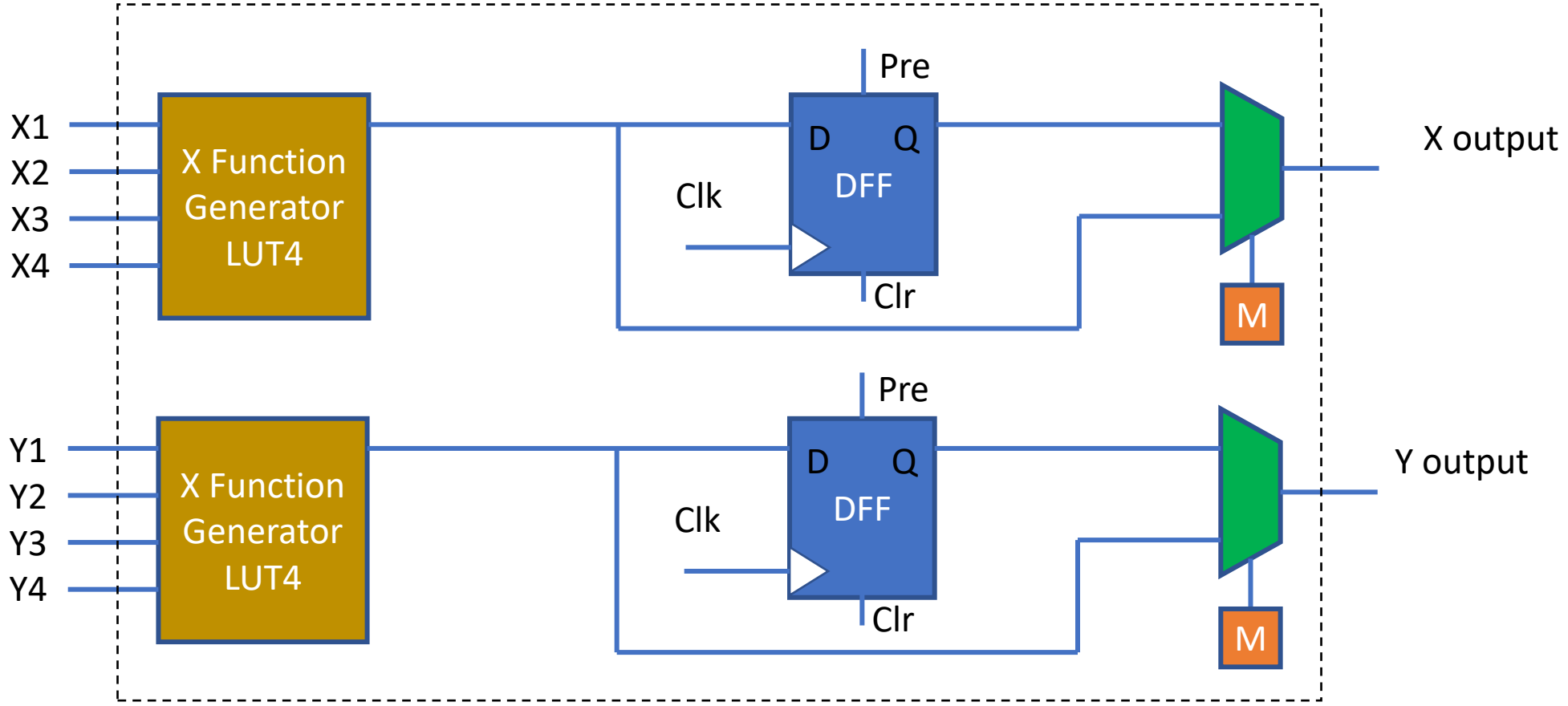
FG = function generator for Logic implementation

I/O Blocks

USB or JTAG Cable

SRAM Configuration Memory

Lookup Table (LUT) based Configurable Logic Blocks

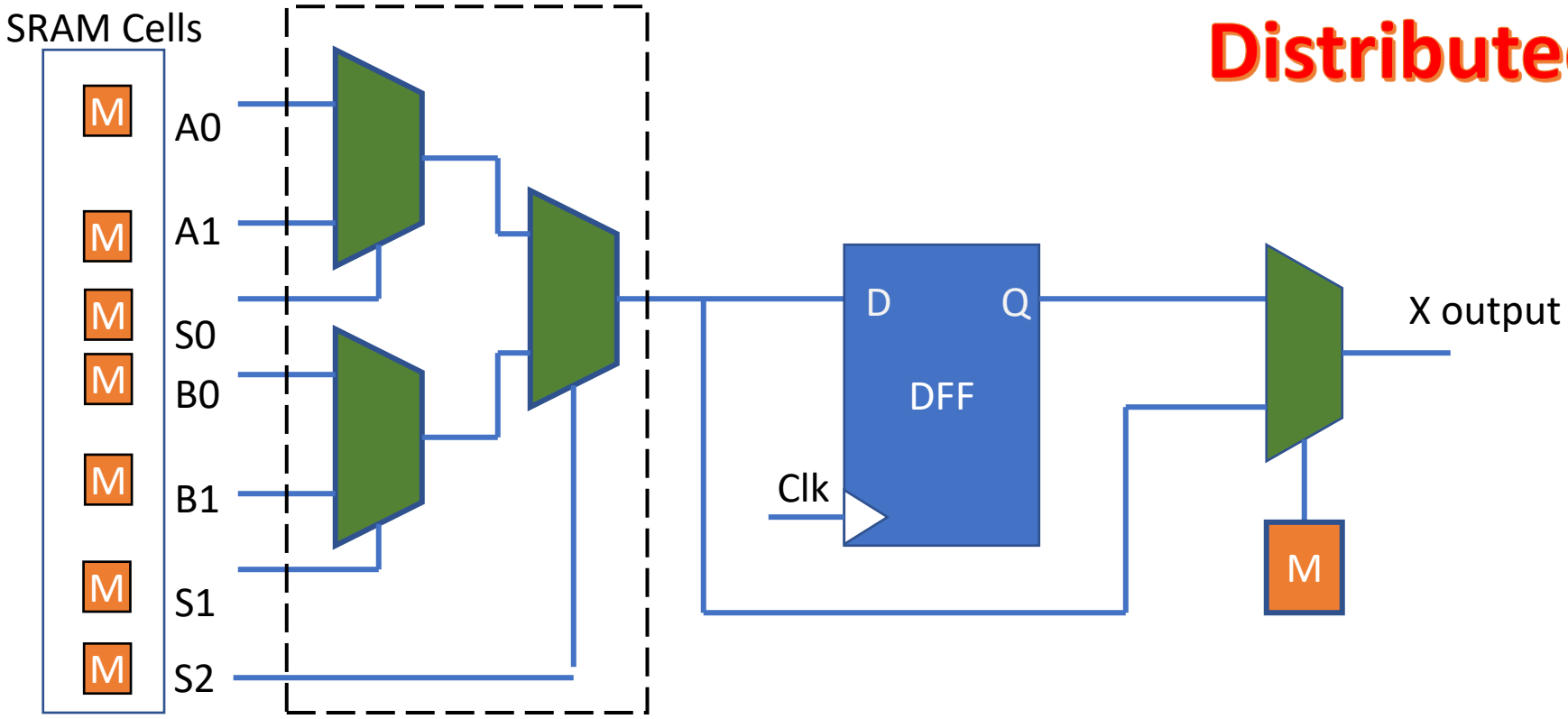


Details of LUT based CLB

- Uses a four-variable look-up table and a flipflop as the basic configurable hardware element. Several of these are combined in different families and types
- Any two functions X and Y of four variables each can be generated in the LUT
- Flipflops at the output can be used. DFF have external preset and clear as well as clock selection mechanism
- Output multiplexer selects from un-registered or registered output

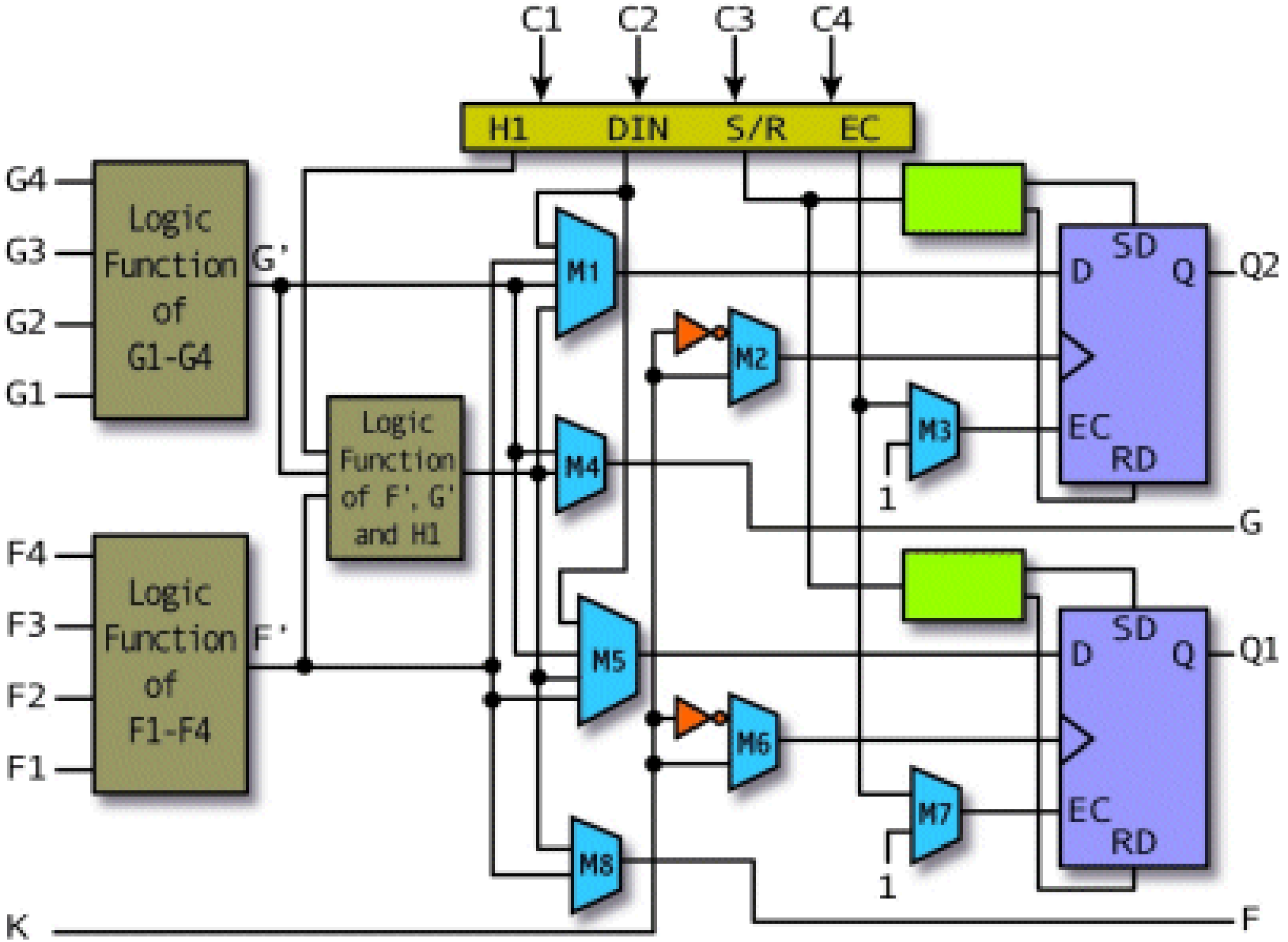
Configurable Logic Blocks based on Multiplexers

Where is Distributed Memory?



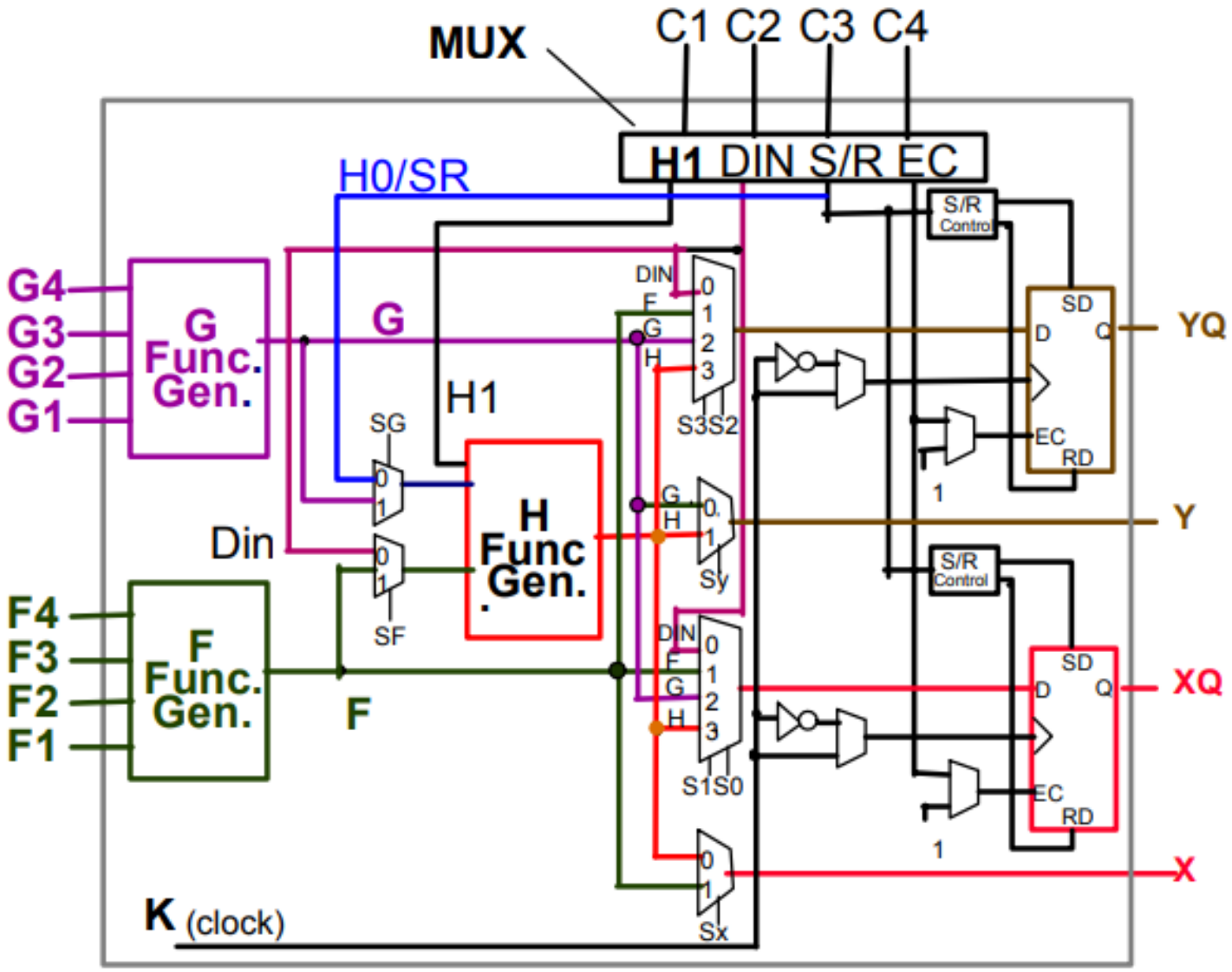
4:1 MUX to generate required SOP Expression

Xilinx 4000 CLB



LUT Configuration and Extension

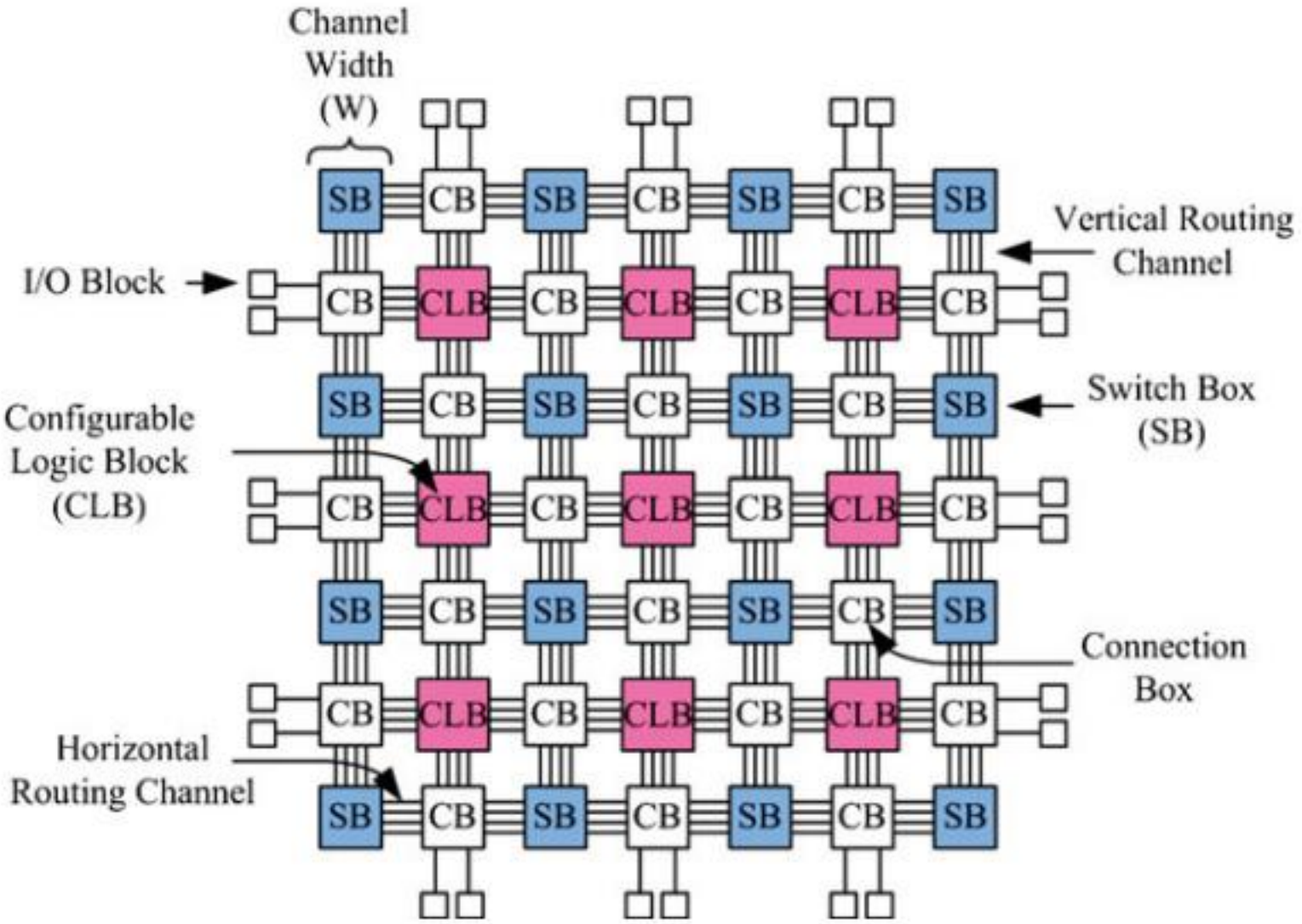
2 Four-input function generators (Look Up Tables)
1 Three-input function
2 Registers:
- Pos. or Neg. edge-trig. Synchronous and asynchr. Set/Reset
Possible functions:
- any fct of 5 var.
- two fcts of 4 var. + one fct of 3 var.
- some fct of 9 var.



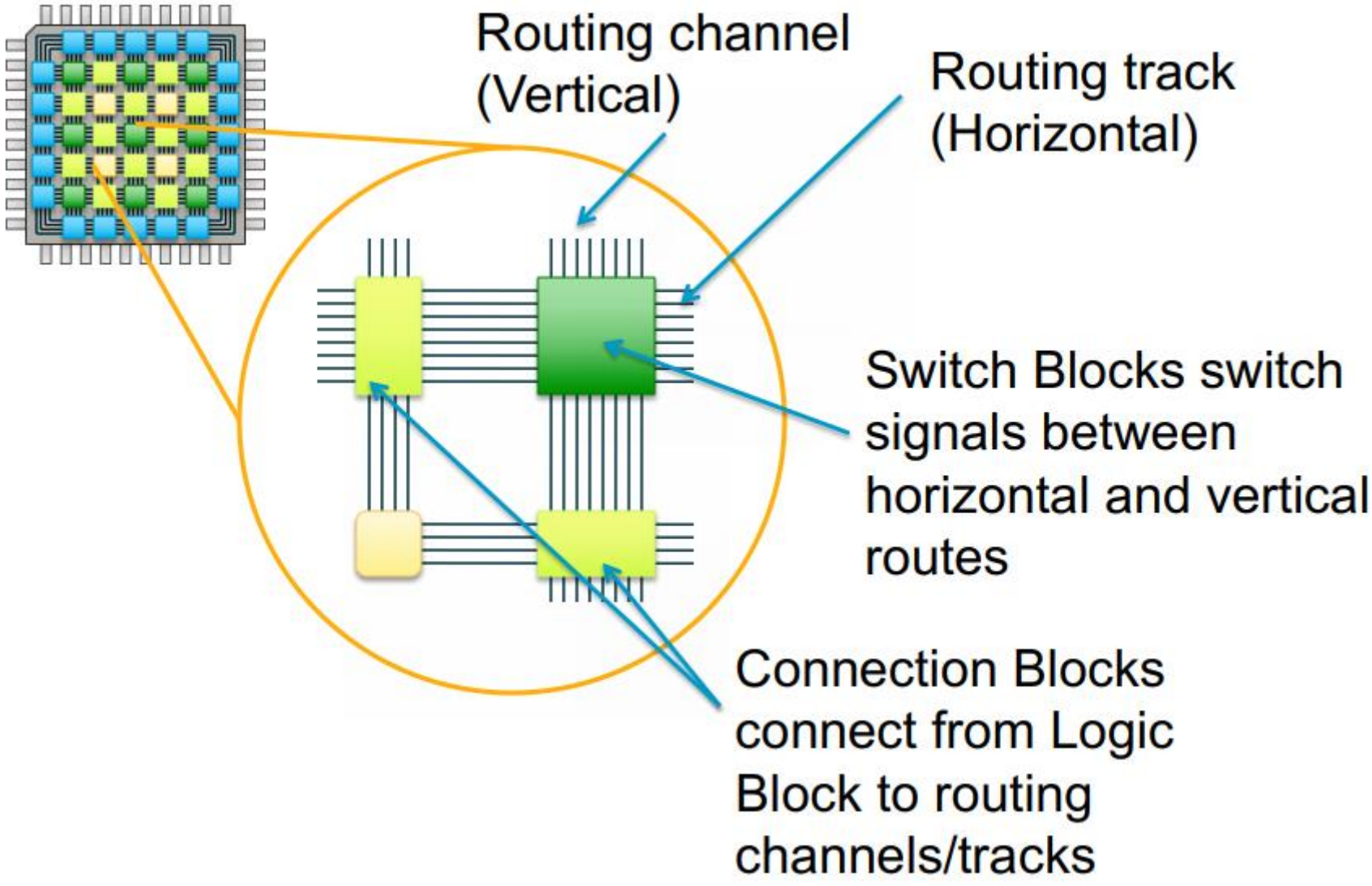
Interconnects

- FPGA in Symmetric Array Configuration (Eg Xilinx)
  - General Purpose Interconnect
  - Direct Interconnects
  - Global Lines
- FPGAs in hierarchical interconnect routing architecture (Eg Altera)
- FPGA in Row Based Configuration (Eg Actel)
- FPGAs in Sea of Gates Fine-Grained Configuration (Eg IBM)

Mesh Based FPGA Routing Architecture



Switching Blocks and Connection Blocks



Configuration SRAM for Routing

Early FPGA used pass gate transistors controlled by SRAM cells to connect wires

This results in slow speed for large FPGA

Adding some tri-state buffers improves speed but costs area

Recent FPGA use a multiplexer built out of pass gates followed by a buffer that cannot be tri-stated

The pass transistors in this direct-drive approach switch can be small as they are lightly loaded, while the buffer can be larger to drive the significant capacitance of a routing wire segment

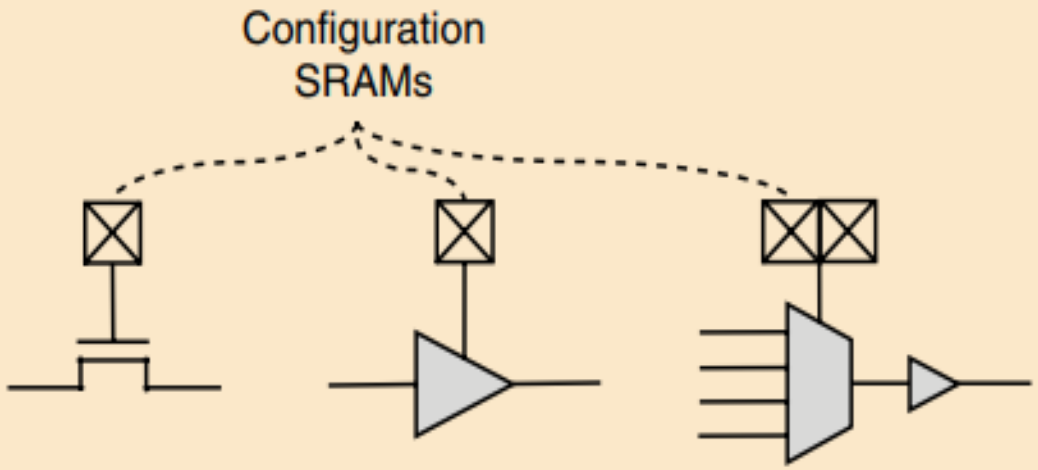
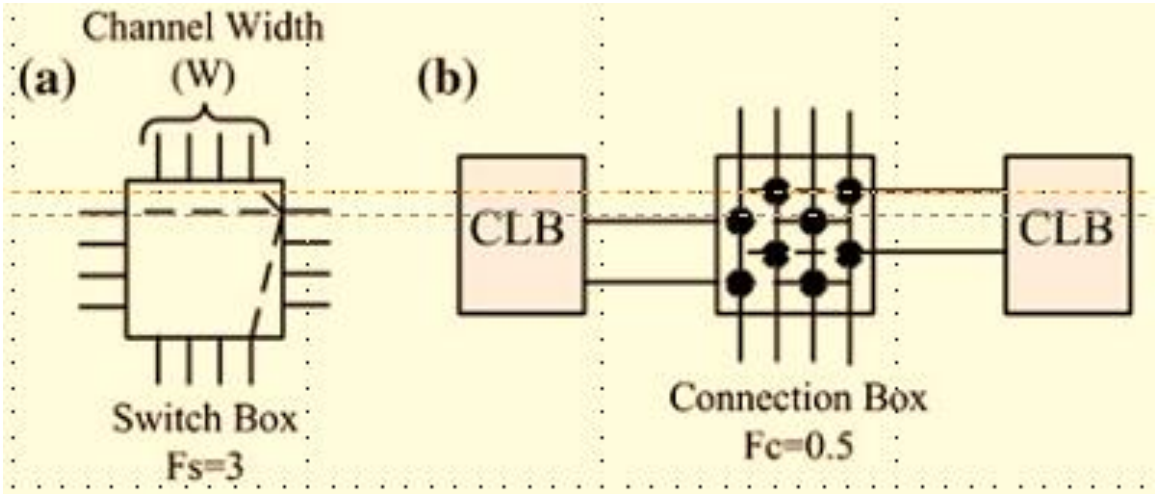


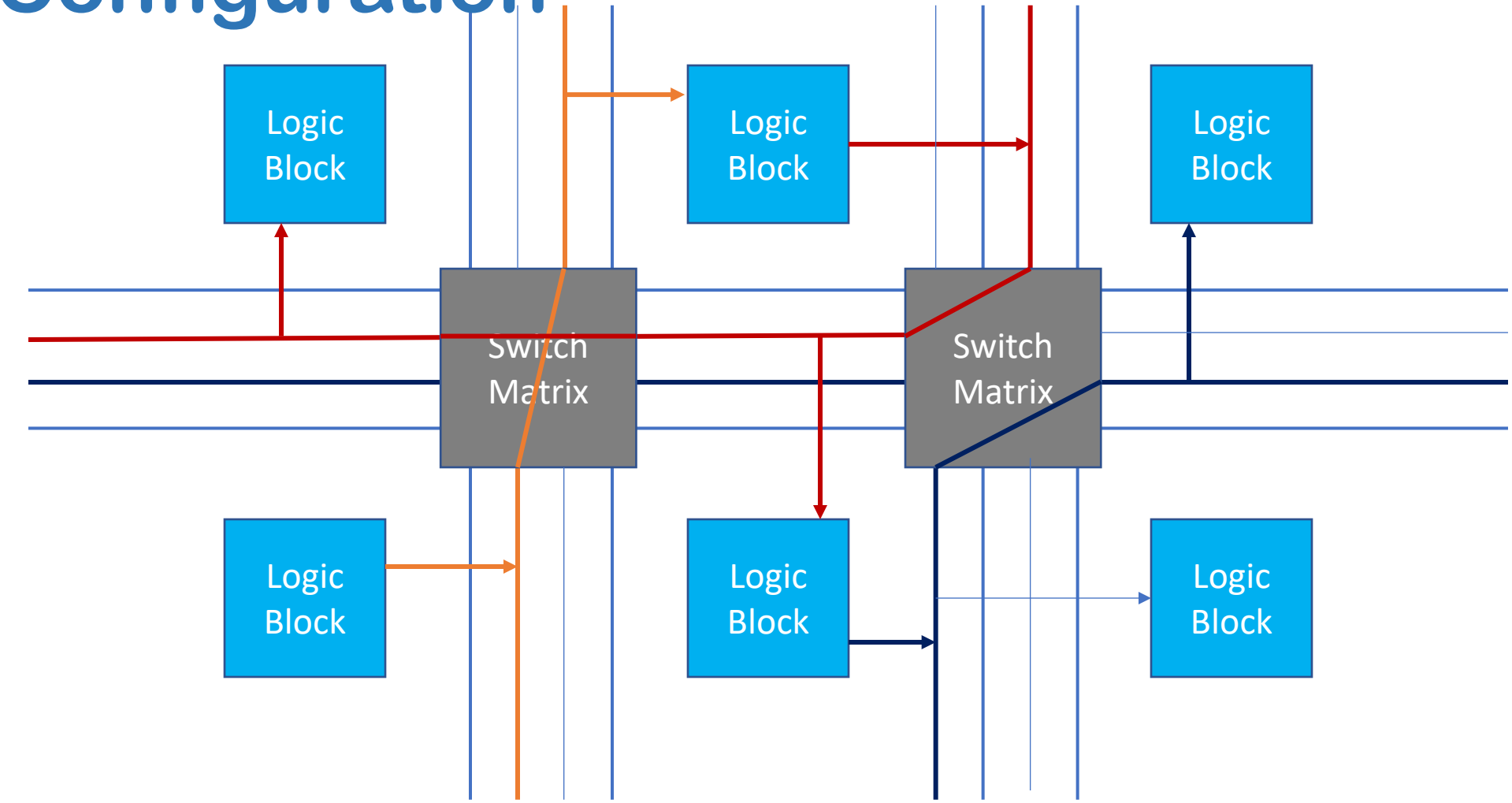
Figure 10. Different implementations for SRAM-controlled programmable switches using pass transistors (left), tri-state buffers (middle), or buffered multiplexers (right).

Connection Box and Switching Box - Example

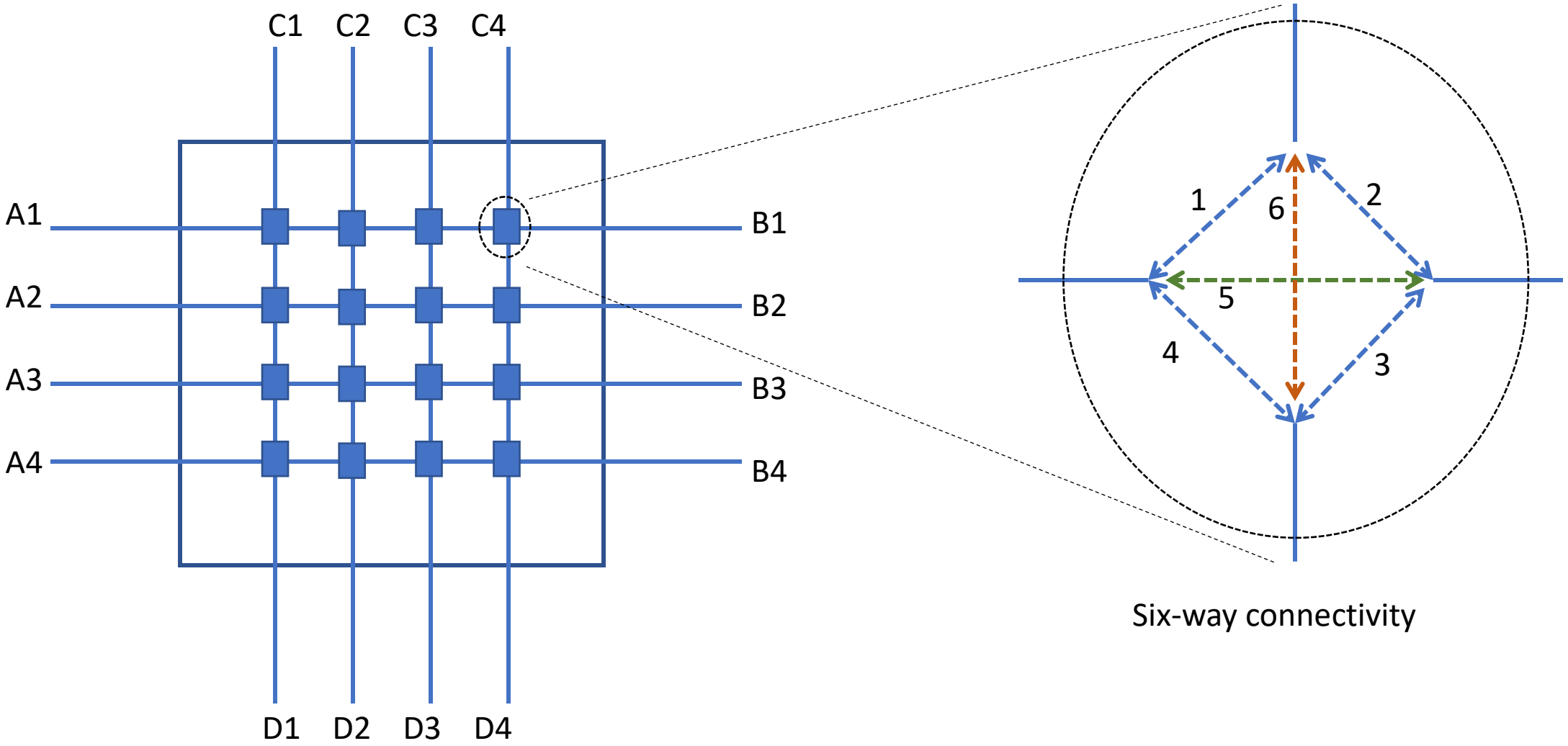
- FPGA routing occupies 80% of total area, logic is 20%
- In Mesh based routing, horizontal and vertical routing tracks are interconnected through Switch Boxes (SB)
- Logic Blocks are connected to the routing network through Connection Boxes (CB)
- Flexibility of Connection Box (FC) is the number of routing tracks of adjacent channels which are connected to pin of a block
- An FC(in) of 1.0 means that all the tracks of adjacent routing channel are connected to the input pin of the logic block
- Flexibility of Switch (FS) is the total number of tracks with which every track entering in the switch box connects to
- Channel Width (CW) is the number of tracks in a routing channel, used in all horizontal and vertical channels of the architecture
- FS=3 means each track incident on it is connected to 3 tracks of adjacent routing channels
- FC(in) =0.5 means each input of the logic block is connected to 50% of the tracks of adjacent routing channels



Symmetric (Matrix) Based FPGA Configuration

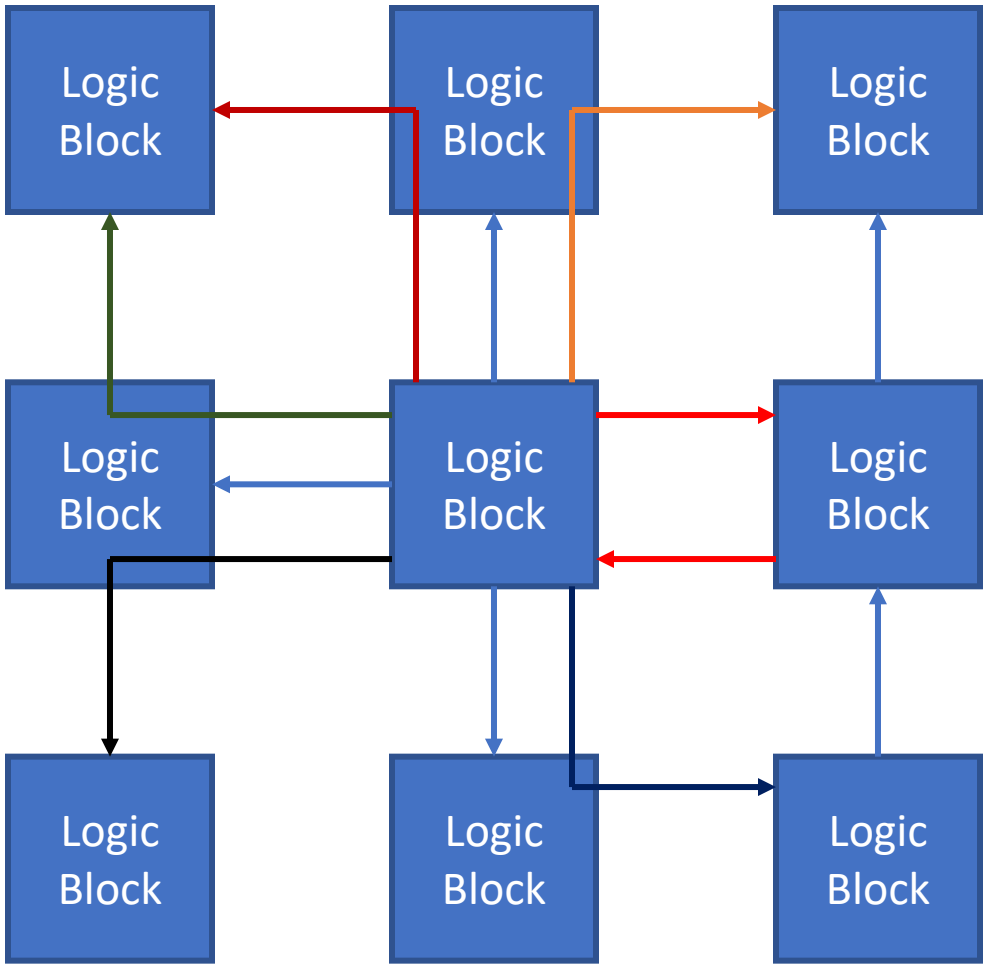


Routing Matrix for General Purpose Interconnection in FPGA



Six-way connectivity

Direct Interconnection to Neighboring Blocks



Switch Block Architecture

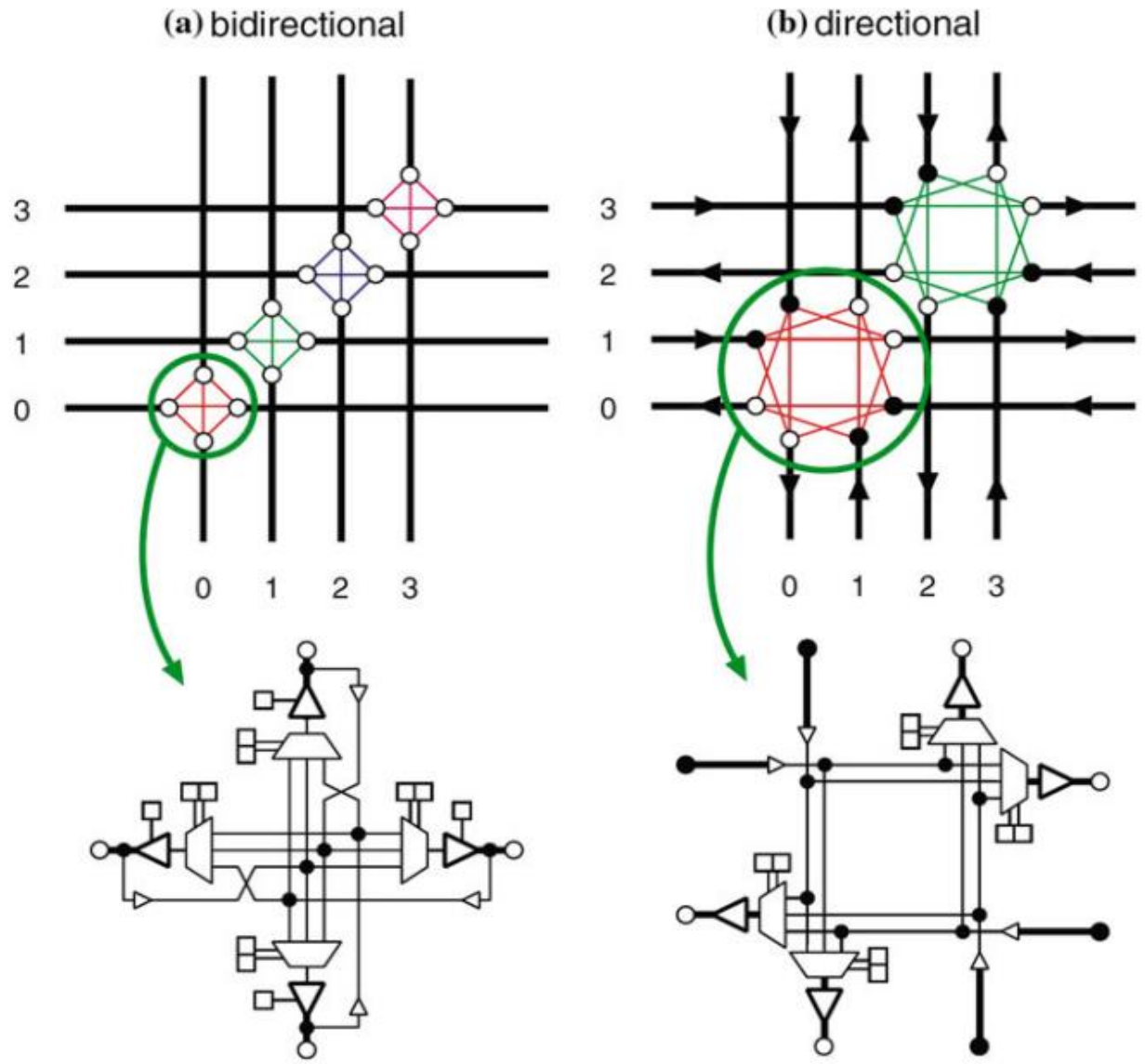


Fig. 2.7 Switch block, length 1 wires [51]

Island Style Routing Architecture

The other type of FPGA interconnect is *island-style*, as depicted in Fig. 9. This architecture was pioneered by Xilinx and is inspired by the fact that a regular two-dimensional layout of horizontal and vertical directed wire segments can be efficiently laid out. As shown in Fig. 9, island-style routing includes three components: routing wire segments, connection blocks (multiplexers) that connect function block inputs to the routing wires, and switch blocks (programmable switches) that connect routing wires together to realize longer routes. The placement engine in FPGA CAD tools chooses which function block implements each element of a design in order to minimize the required wiring. Consequently, most connections between function blocks span a small distance and can be implemented with a few routing wires as illustrated by the red connection in Fig. 9.

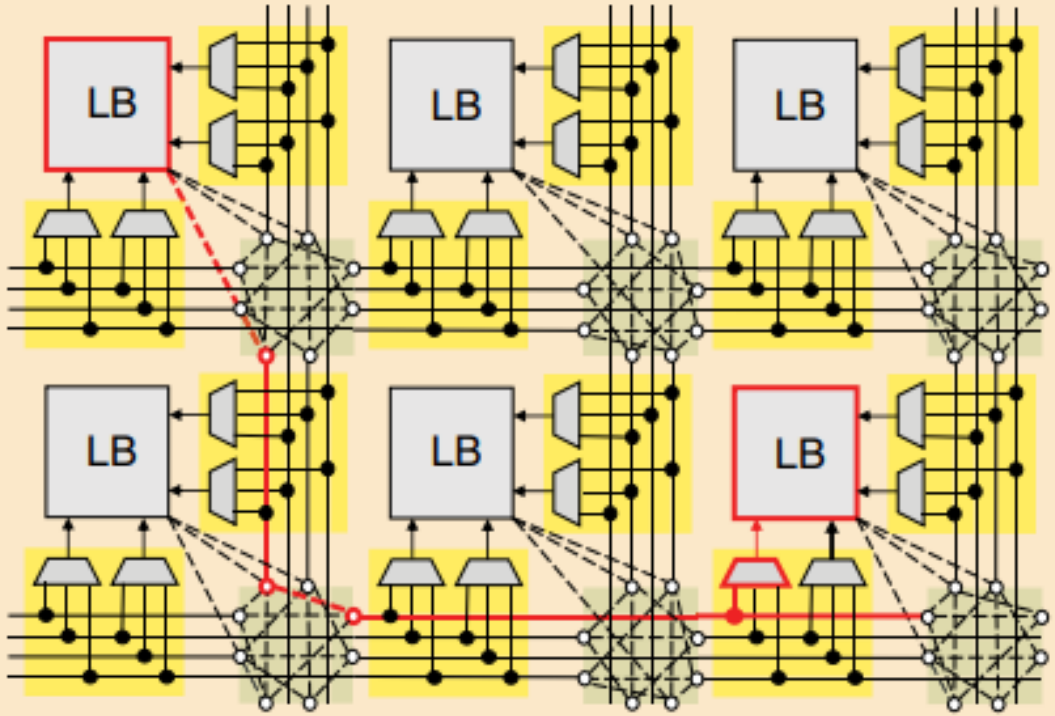


Figure 9. Island-style routing architecture. Thick solid lines are routing wires while dashed lines are programmable switches. Connection and switch blocks are shaded in yellow and green, respectively.

Hierarchical Routing Architecture in FPGA

Hierarchical Routing is inspired by the fact that:
(i) higher level modules instantiate lower level modules; and
(ii)Communication is more frequent between modules that are closer in hierarchy

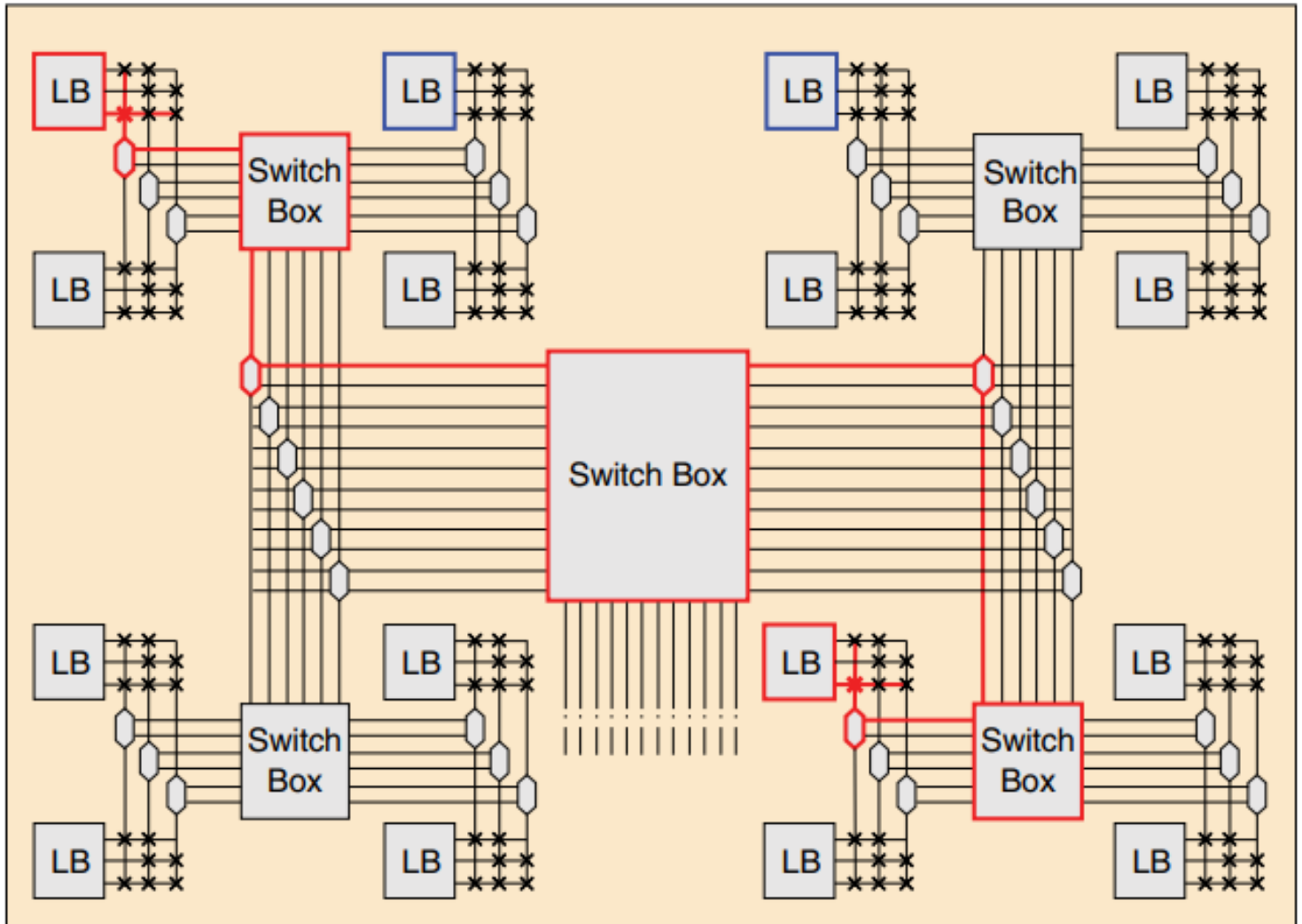
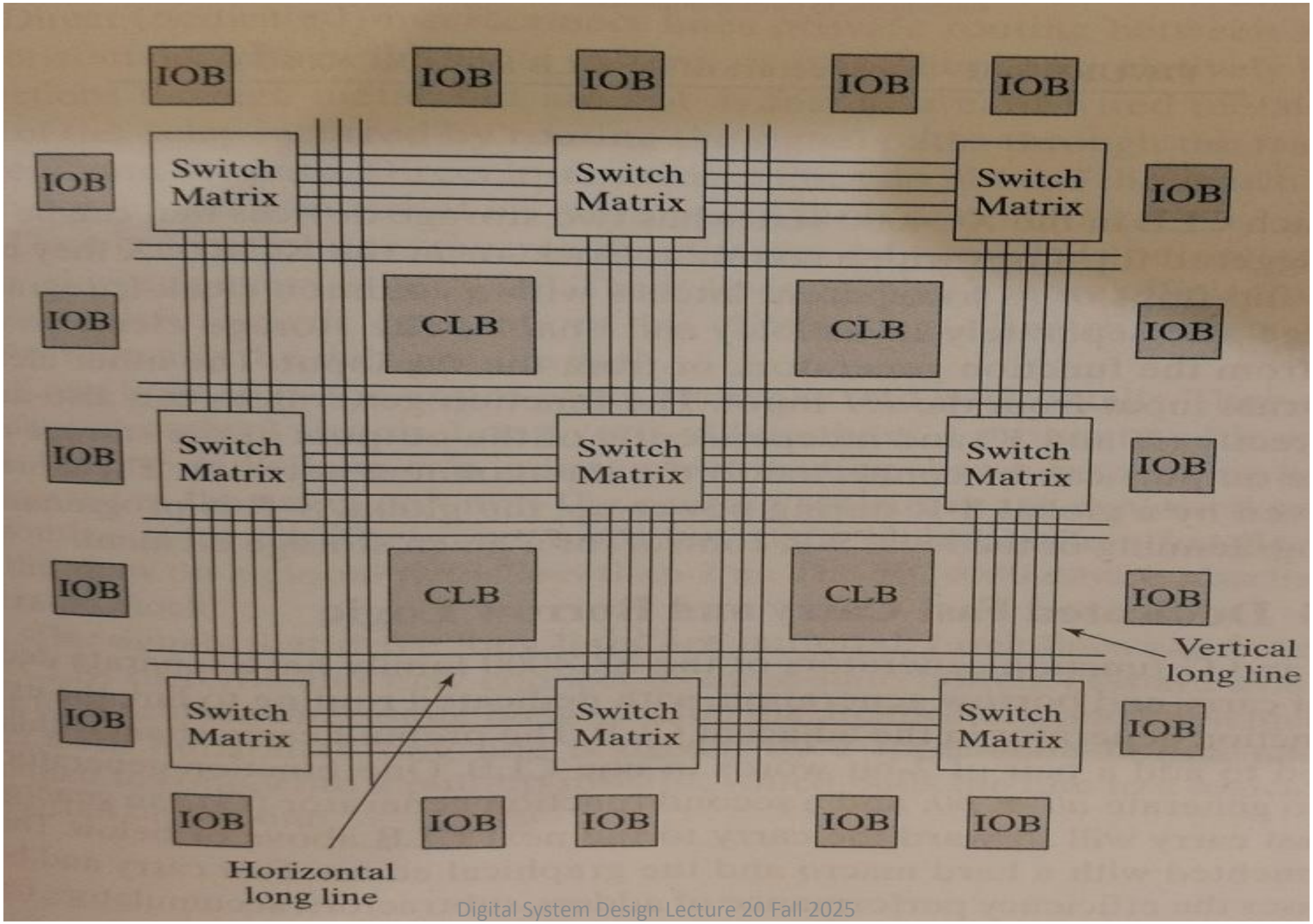


Figure 8. Routing architecture in hierarchical FPGAs.

Xilinx 4000 FPGA Top Level Architecture



Xilinx 4000 Routing Resources with CLB

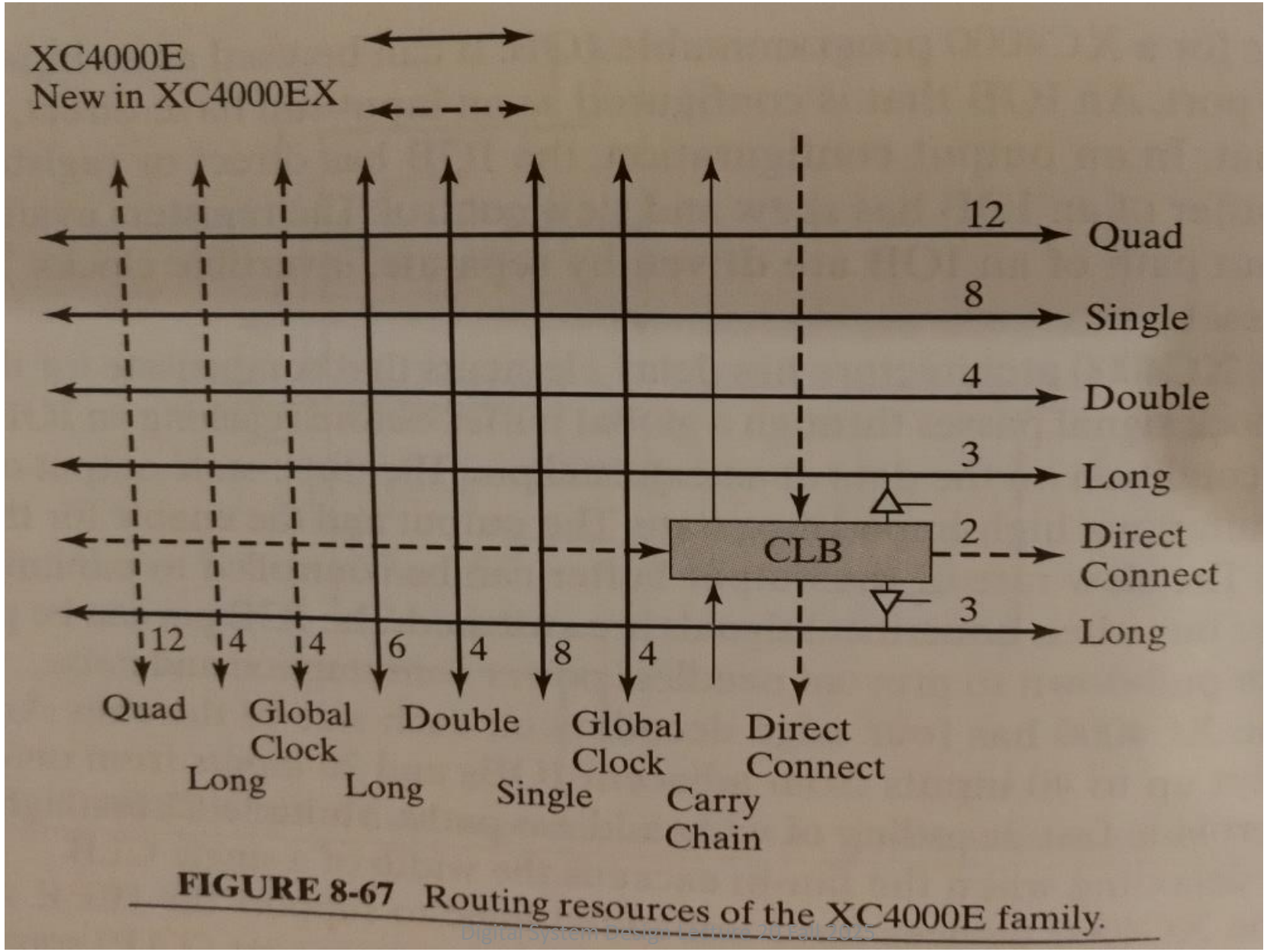
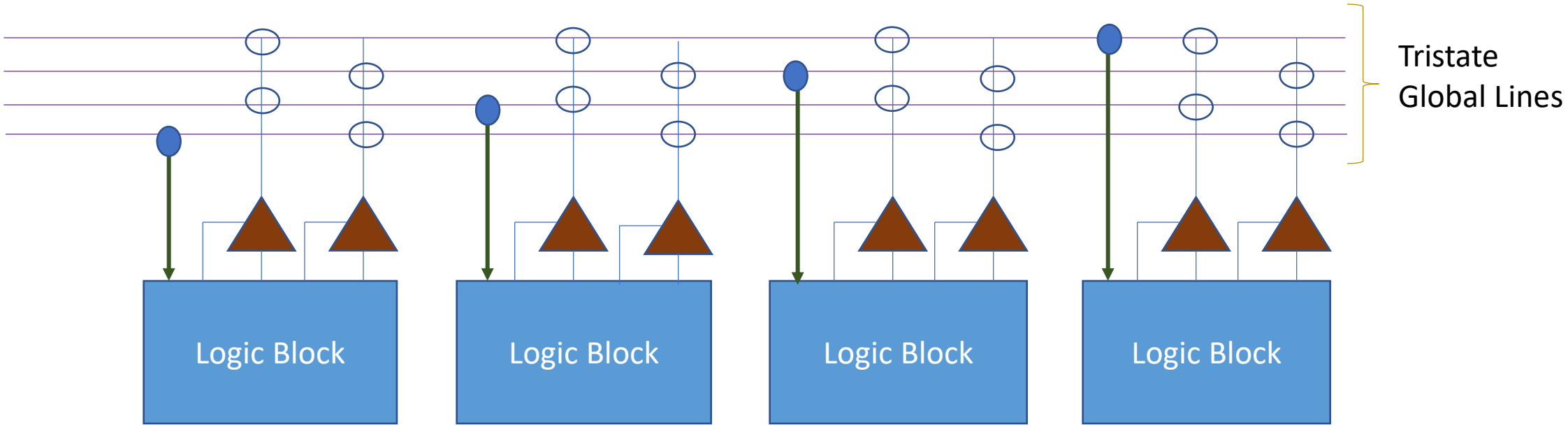


FIGURE 8-67 Routing resources of the XC4000E family.

Global Interconnection Lines in FPGA



Xilinx 4000 Different types of Interconnects

Simplified diagram

3 types:

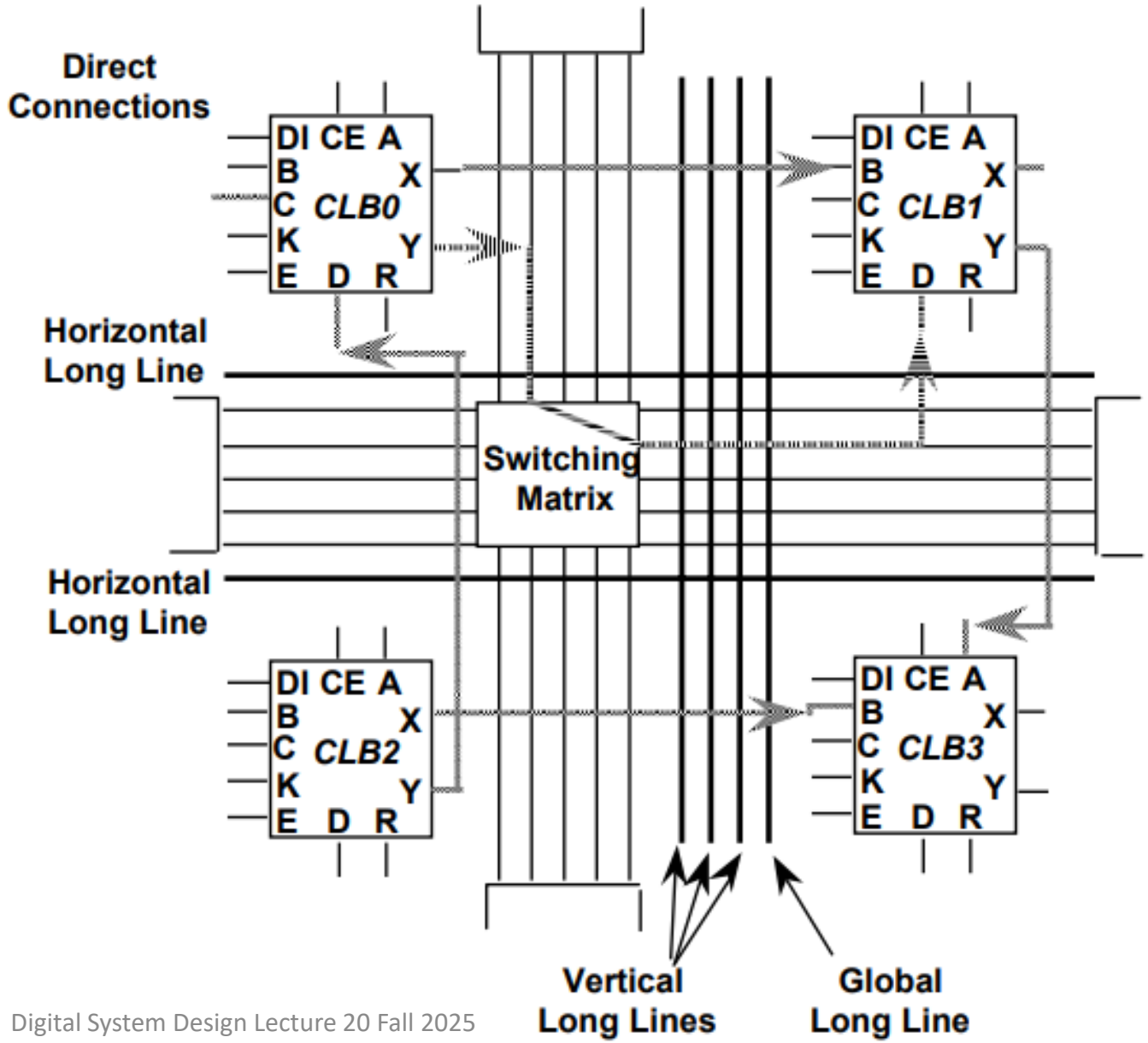
* Fast Direct Connections

* General Purpose Connections with Switching Matrix

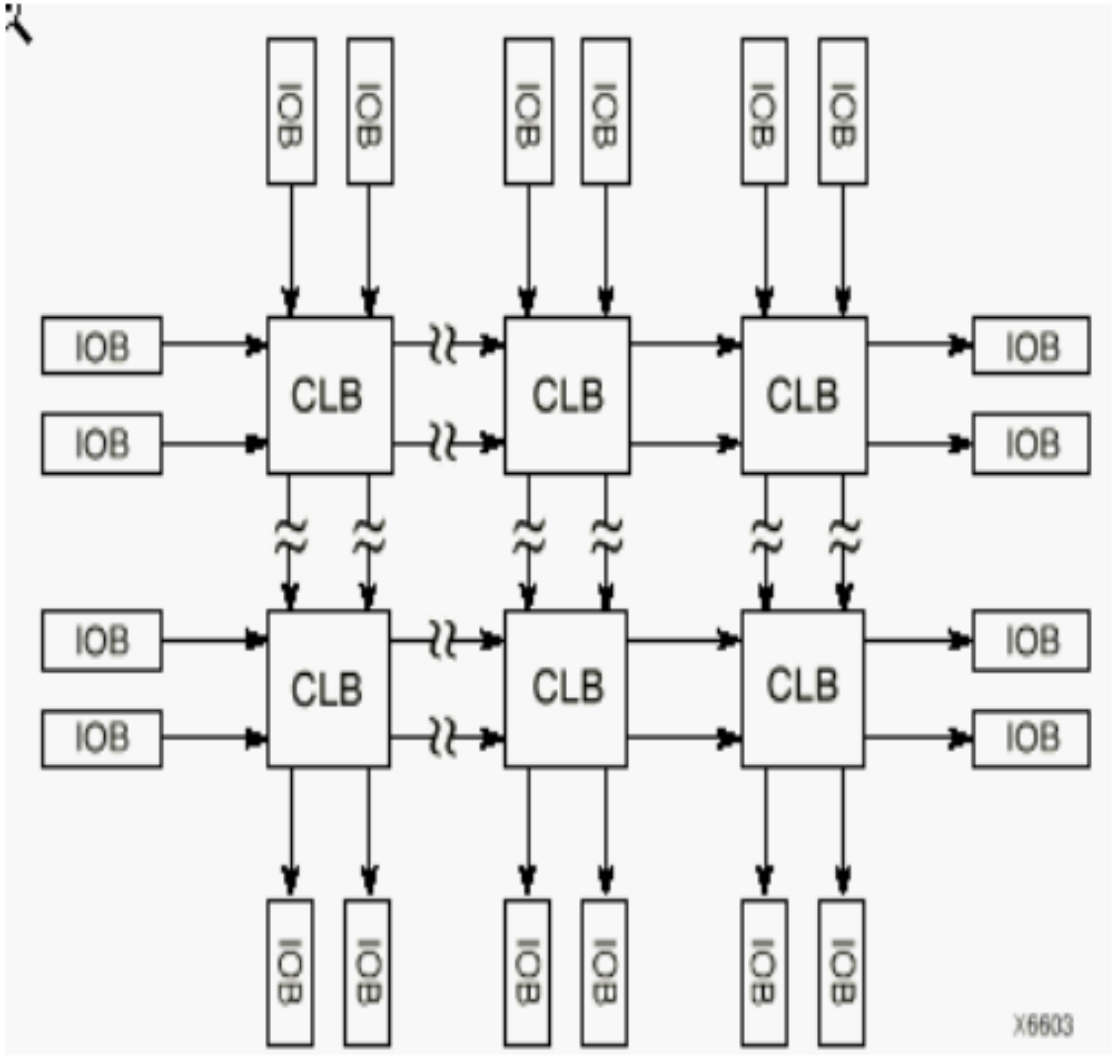
* Horizontal/Vertical Long Lines

Types of lines:

* Single length (8)
* Double length (4)
* Long lines (6)
* Global lines (4)

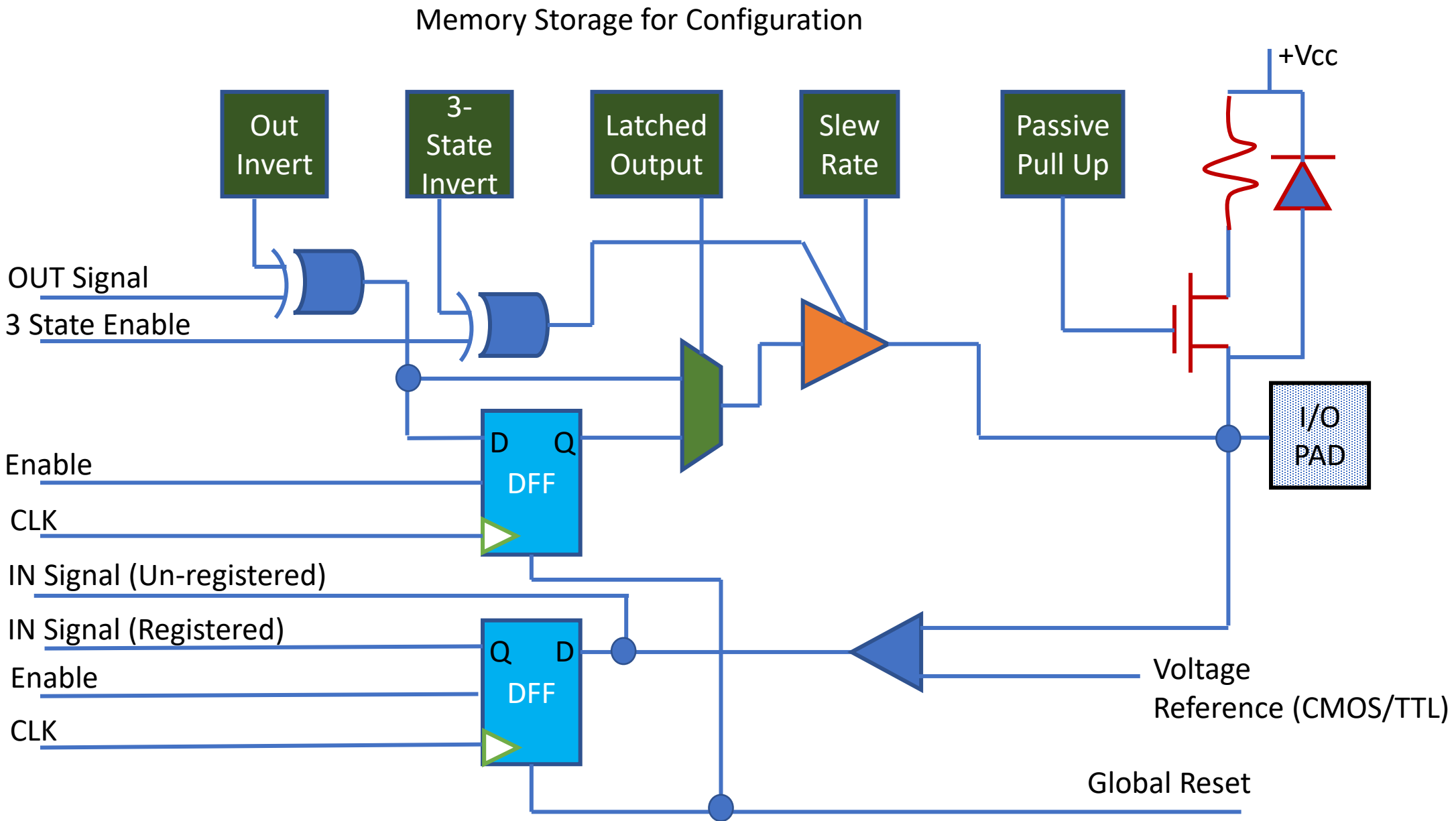


Direct Interconnect in Xilinx 4000



- Between neighboring blocks
- From CLB to CLB
- From CLB to IOB
- Fastest, short distance connections
- X: Hor. connection
- Y: Vert. connection

Programmable I/O Blocks in FPGA



Single Port Distributed RAM from LUT based CLB

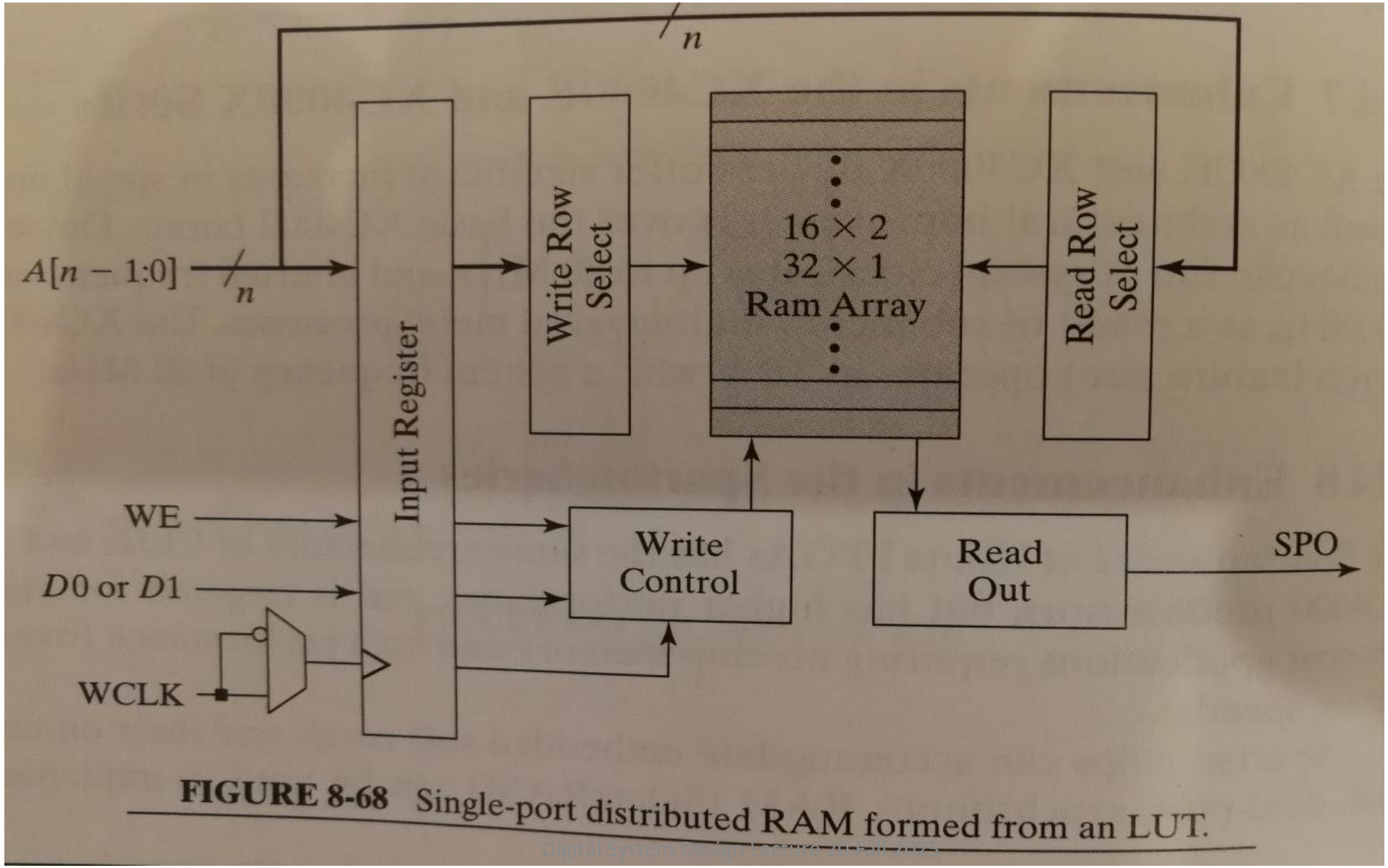


FIGURE 8-68 Single-port distributed RAM formed from an LUT.

Dual Port RAM in Xilinx Spartan FPGA

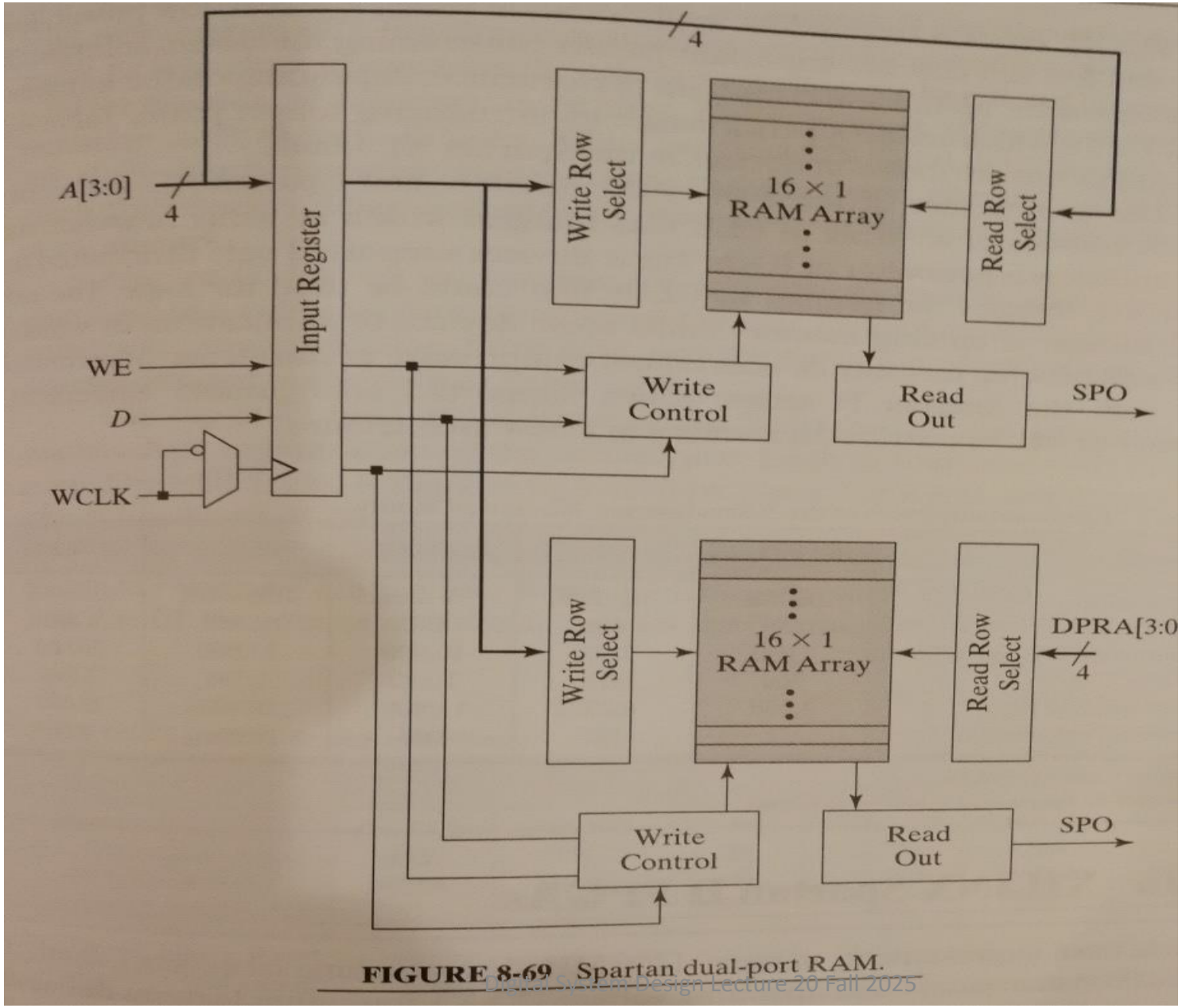
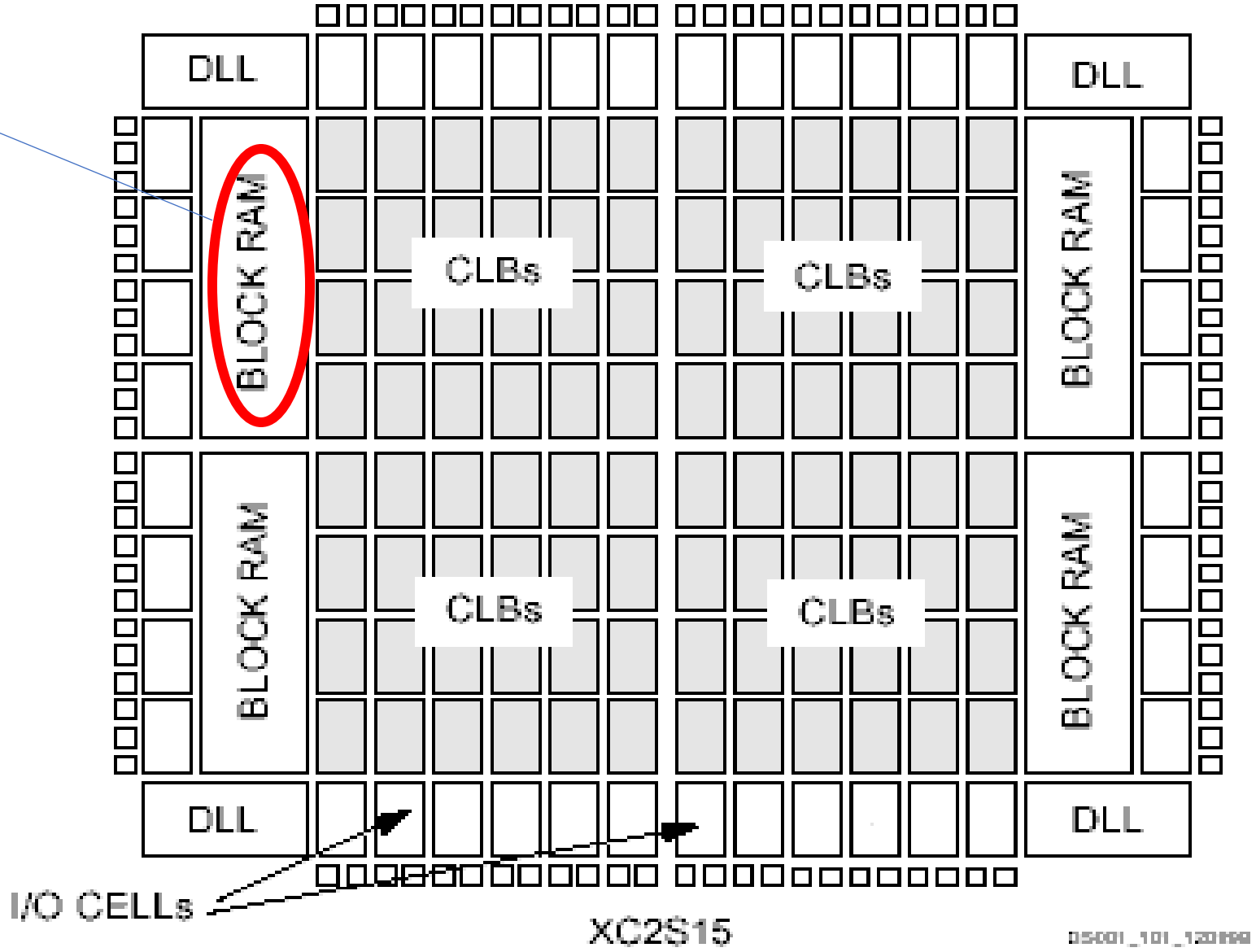


FIGURE 8-69 Spartan dual-port RAM.

Xilinx Spartan Architecture

Block RAM ?



DLL = Delay Locked Loop
For Clock Management

Digital Clock Module in Xilinx FPGA

Clock Management

- Digital Clock Managers (DCMs)
  - Clock de-skew
  - Phase shifting
  - Clock multiplication
  - Clock division
  - Frequency synthesis