Lahore University of Management Sciences

EE 421 / CS 425 – Digital System Design

(Fall 2025)

Instructor	Dr. Shahid Masud
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Secretary/TA	Will be announced on LMS
TA Office Hours	Will be announced on LMS
Course URL (if any)	LMS will be used
Support Services	LUMS offers a range of academic and other services to support students. These are mentioned below, and you are encouraged to use these in addition to in-class assistance from course staff. For a complete list of campus support services available for you click here (https://advising.lums.edu.pk/#supportservices)

Course Details	
Credit Hours	**3 (Theory) + 1 Lab** (separate enrolment required)
Core	MS EE (Electronics and Embedded Systems Stream), MS DES (Digital Embedded Systems)
Elective	BS EE / CS , MS EE Elective
Open for Student Category	Senior / MS
Closed for Student Category	Freshman / Sophomore / Junior

Course Catalog Description
This course explains how to go about designing complex, high-speed digital circuits and systems. Complete digital design-flow using modern design automation tools in description, simulation, logic synthesis and implementation technology are explored. Application of a modern hardware description language such as *SystemVerilog* to model and verify digital systems at Behavior and RTL level is studied. Advanced methods of logic minimization and state-machine design are discussed. Design and implementation of digital functional building blocks such as arithmetic circuits, datapaths, microprocessors, I/O modules, interfacing, UARTs, frequency generators, memories, encryption, etc. is included. BIST and Scan techniques for testing of digital systems are also covered. Study of architecture of modern FPGA devices is included. An introduction to contemporary testing methodology *UVM* is provided.

Course Prerequisite(s)/Co-Requisite(s)
Pre-requisites: EE 324 *OR* CS 225 *OR* CS 320/EE320 *OR* Grad Standing
Co-requisites: EE 421 Lab / CS 325 Lab

Course Offering Details (online offering may require some changes)						
Lecture(s)	Nbr of Lec(s) Per Week	2	Duration	75 min	Timings and Venue	TBA
Recitation (per week)	Nbr of Rec (s) Per Week	X	Duration			
Lab (if any) per week	Nbr of Session(s) Per Week	X	Duration			
Tutorial (per week)	Nbr of Tut(s) Per Week	X	Duration			

Course Learning Outcomes	
	The students completing EE 421 / CS 425 should be able to:
CLO1:	Describe the concepts of timing hazards and how timing and other factors influence digital system performance.
CLO2:	Analyze and synthesize complex digital circuits like advanced binary adders, integer and FP multipliers, binary dividers, DSP filters, UART, ASM charts, other digital system design case studies, etc.
CLO3:	Describe different techniques, design, and applications for testing faults in digital systems such as stuck-at faults, ALFSR, BILBO, Scrambler, SCAN test, BIST, JTAG, etc.
CLO4:	Understand the design, construction and resources available in modern programmable logic devices such as CPLD and FPGA.

Course Learning Relation to EE Program Outcomes

EE/421 CLOs	Related PLOs	Levels of Learning	Teaching Methods	CLO Attainment checked in
CLO1	PLO1	Cog-3	Instruction, Assignments	Midterm, Final, Quizzes
CLO2	PLO1	Cog-3	Instruction, Assignments	Midterm, Final, Quizzes
CLO3	PLO2	Cog-3	Instruction, Assignments	Midterm, Final, Quizzes
CLO4	PLO2	Cog-3	Instruction, Assignments	Final, Quizzes

Grading Breakup and Policy

Class quizzes: (5 – 6 quizzes, one dropped): 20%
Assignments: (1 - 2): 10%
Midterm exam: 30%
Final exam: 40%
*Note: The lab component for MS students will be included in the final overall grade of course as explained in the class!
** Lab details available separately

Examination Detail

Midterm Exam (online modalities)	Yes/No: Yes Combine Separate: NA Duration: TBD based on practical modalities Preferred Date: TBA Exam Specifications: TBA
Final Exam (online modalities)	Yes/No: Yes Combine Separate: NA Duration: TBD based on practical modalities Exam Specifications: TBA

Campus supports & Key university policies

Campus Supports

Students are strongly encouraged to meet course instructors and TA's during office hours for assistance in course-content, understand the course's expectations from enrolled students, etc. Beyond the course, students are also encouraged to use a variety of other resources. (Instructors are also encouraged to refer students to these resources when needed.) These resources include Counseling and Psychological Services/CAPS (for mental health), LUMS Medical Center/LMC (for physical health), Office of Accessibility & Inclusion/ OAI (for long-term disabilities), advising staff dedicated

to supporting and guiding students in each school, online resources (https://advising.lums.edu.pk/advising-resources), etc. To view all support services, their specific role as well as contact information click here (https://advising.lums.edu.pk/#supportservices).

Academic Honesty/Plagiarism

LUMS has zero tolerance for academic dishonesty. Students are responsible for upholding academic integrity. If unsure, refer to the student handbook and consult with instructors/teaching assistants. To check for plagiarism before essay submission, use similarity@lums.edu.pk. Consult the following resources: 1) Academic and Intellectual Integrity (http://surl.li/gpvwb), and 2) Understanding and Avoiding Plagiarism (http://surl.li/gpvwo).

LUMS Academic Accommodations/ Petitions policy

Long-term medical conditions are accommodated through the Office of Accessibility & Inclusion (OAI). Short-term emergencies that impact studies are either handled by the course instructor or Student Support Services (SSS). For more information, please see Missed Instrument or 'Petition' FAQs for students and faculty (https://rb.gy/8sj1h)

LUMS Sexual Harassment Policy

LUMS and this class are a harassment-free zone. No behavior that makes someone uncomfortable or negatively impacts the class or individual's potential will be tolerated.

To report sexual harassment experienced or observed in class, please contact me. For further support or to file a complaint, contact OAI at oai@lums.edu.pk or harassment@lums.edu.pk. You may choose to file an informal or formal complaint to put an end to the offending behavior. You can also call their Anti-Harassment helpline at 042-35608877 for advice or concerns. *For more information: Harassment, Bullying & Other Interpersonal Misconduct: Presentation (http://surl.li/gpvwt)*

Lecture / Week	Course Topics	Readings	Lab / Quiz
1 / Wk 1	Introduction to digital systems and their design flow	Ciletti	
2 / Wk 1	Review of combinational logic, logic minimization	Ciletti	
3 / Wk 2	Advanced Logic Minimization Techniques	Ciletti	
4 / Wk 2	Timing in Combinational Circuits, Hazards and Glitches	Notes	
5 / Wk 3	Review of sequential logic	Ciletti	
6 / Wk 3	Design using flip-flop and latches, State machines	Ciletti	
7 / Wk 4	State reduction, timing issues	Ciletti	
8 / Wk 4	Design of Adders and Subtractors, Carry Lookahead Adders	Ciletti	
9 / Wk 5	Serial Adders, Array Multipliers, Critical Paths	Ciletti	
10 / Wk 5	Booth and Radix-4 Encoded Signed Multipliers		
11 / Wk 6	Further *SystemVerilog* modeling, parameterization	Notes	
12 / Wk 6	Design of dividers and other arithmetic circuits	Notes	
13 / Wk 7	Circuits for Floating Point Implementation	Ciletti	
14/Wk 7	Serial Multipliers, Signed Multiplication of Fractions		
15 / Wk 7	**Midterm Exam**		
16 / Wk 8	Introducing Programmable logic, PAL, PLA, CPLD	Ciletti	
17 / Wk 8	Construction, operation, examples of FPGA and CPLD	Ciletti	
18 / Wk 9	Controller design using ASM charts	Ciletti	
19 / Wk 9	Controller Design for Sequential Multipliers and Dividers	Ciletti	
20 / Wk 10	Faults and Testability – BIST and SCAN techniques	Notes	
21 / Wk 10	Design for test – JTAG	Notes	
22 / Wk 11	LFSR, BRM, Function Generators, Design Examples	Notes	
23 / Wk 11	Parity and Error Detection, Correction Circuits	Note	
24 / Wk 11	HDL Synthesis Issues / Xilinx DSP Blocks	Notes	
25 / Wk 12	Advanced HDL / Examples of Digital Systems / UART	Notes	
26 / Wk 13	Asynchronous Sequential Design / Introduction to *UVM* test methodology	Notes	

27 / Wk 14	Digital Design Case Study / Frequency Synthesizer	Notes	
	Final Exam Week 15 or 16		

Textbook(s)/Supplementary Readings
Textbook: Michael D. Ciletti, *Advanced Digital Design with the Verilog HDL,* Prentice Hall Supplementary Reading**: (Additional Notes, articles, and slides will be provided where needed)** 1. V Taraate, *SystemVerilog for Hardware Description RTL Design and Verification*, Springer, 2020 2. Ashok B. Mehta, *Introduction to SystemVerilog,* Springer, 2021 3. Donald Thomas, *Logic Design and Verification Using SystemVerilog*, 2021 3. Brent E. Nelson, *Designing Digital Systems With SystemVerilog v2.1, Department of Electrical and Computer Engineering Brigham Young University (online available)*

Prepared by:	**Dr. Shahid Masud**
Date:	**Updated 6 August 2025**