# Lecture 13 EE 421 / C\$ 425 Digital System Design

Fall 2025
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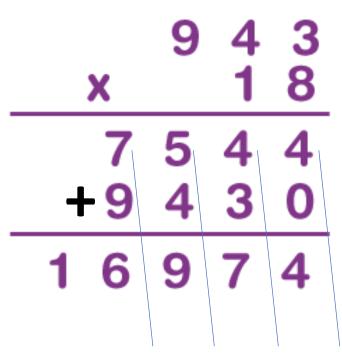
# Topics

- Binary Array Multipliers Quick Recap
- Operation of Sequential Multiplier
- Control Circuits for Multipliers
- Reducing Registers in Sequential Multipliers
- Taking care of sign in Signed Multiplication
- Fractional Binary numbers
- QUIZ 3 NEXT LECTURE



# Decimal Multiplication using Pencil and paper





Keep shifting right

Keep shifting left



# Complexity of Binary Array Multiplier

				<b>X</b> <sub>3</sub>	X <sub>2</sub>	X <sub>1</sub>	X <sub>o</sub>
				<b>Y</b> <sub>3</sub>	Y <sub>2</sub>	Y <sub>1</sub>	$\mathbf{Y}_{0}$
				$X_3Y_0$	$X_2Y_0$	$X_1Y_0$	$X_0Y_0$
			$X_3Y_1$	$X_2Y_1$	$X_1Y_1$	$X_0Y_1$	0
		$X_3Y_2$	$X_2Y_2$	$X_1Y_2$	$X_0Y_2$	0	0
	$X_3Y_3$	$X_2Y_3$	$X_1Y_3$	$X_0Y_3$	0	0	0
Cout	<b>P</b> <sub>6</sub>	<b>P</b> <sub>5</sub>	P <sub>4</sub>	P <sub>3</sub>	P <sub>2</sub>	P <sub>1</sub>	P <sub>0</sub>

How many AND gates?
How many Adders?
Identify longest Carry path?

**Complexity and Timing** 

For an n-bit x n-bit multiplier; We need:

n(n-2) full adders

n half adders

n<sup>2</sup> AND Gates

Worst Case Delay is (2n+1) C Where C is the worst adder delay



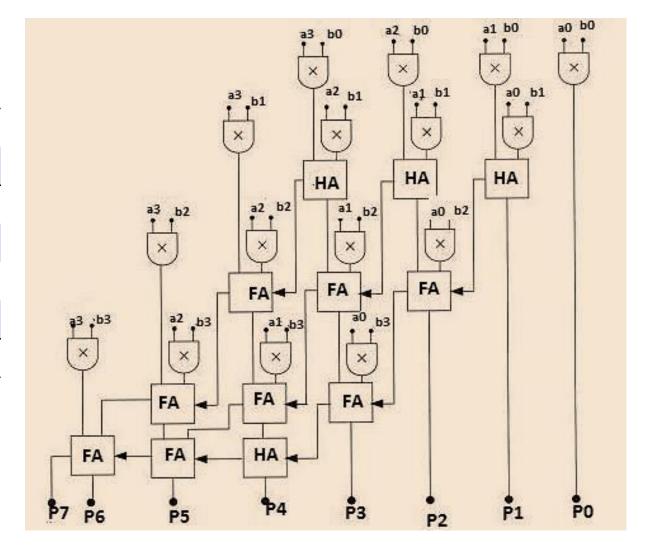
# Designing An Array Multiplier Cell

				$A_3$	A <sub>2</sub>	$A_1$	$A_0$
				B <sub>3</sub>	B <sub>2</sub>	$B_1$	$B_0$
				$A_3B_0$	$A_2B_0$	$A_1B_0$	$A_0B_0$
			$A_3B_1$	$A_2B_1$	$A_1B_1$	$A_0B_1$	0
		$A_3B_2$	$A_2B_2$	$A_1B_2$	$A_0B_2$	0	0
	$A_3B_3$	$A_2B_3$	$A_1B_3$	$A_0B_3$	0	0	0
Cout	P <sub>6</sub>	P <sub>5</sub>	P <sub>4</sub>	P <sub>3</sub>	P <sub>2</sub>	P <sub>1</sub>	$P_0$



# 4-Bit Array Multiplier connected as AND and ADD

				$A_3$	A <sub>2</sub>	$A_1$	$A_0$
				B <sub>3</sub>	B <sub>2</sub>	$B_1$	B <sub>0</sub>
				$A_3B_0$	$A_2B_0$	$A_1B_0$	$A_0B_0$
			$A_3B_1$	$A_2B_1$	$A_1B_1$	$A_0B_1$	0
		$A_3B_2$	$A_2B_2$	$A_1B_2$	$A_0B_2$	0	0
	$A_3B_3$	$A_2B_3$	$A_1B_3$	$A_0B_3$	0	0	0
Cout	P <sub>6</sub>	P <sub>5</sub>	P <sub>4</sub>	P <sub>3</sub>	P <sub>2</sub>	P <sub>1</sub>	P <sub>0</sub>



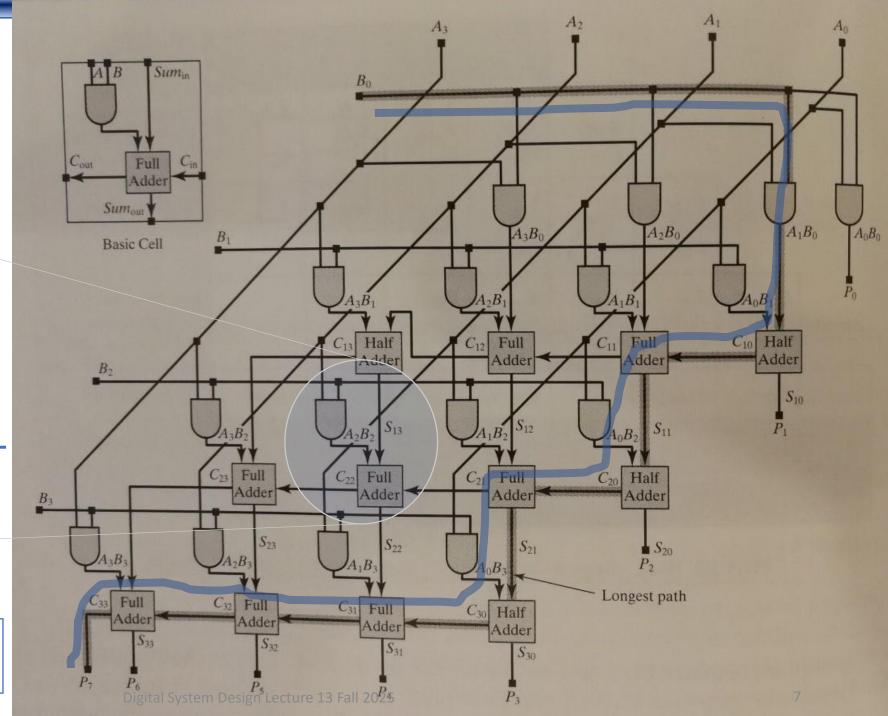


Embedded Systems Lab (EESL)

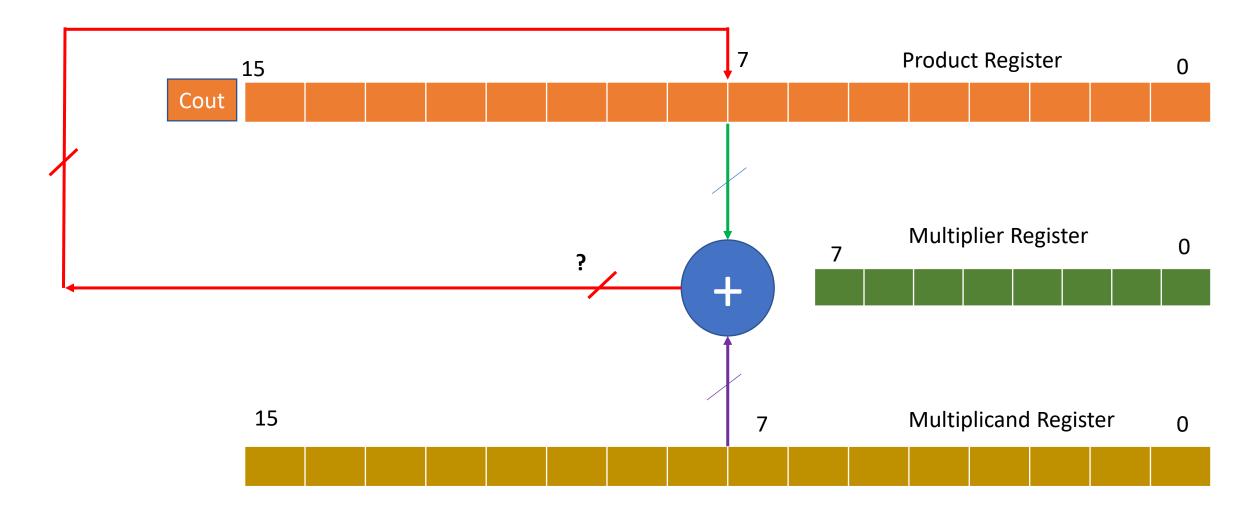
Array Multiplier Circuit Delays

**Building Block**  $B_{i}$ Sum\_in Cout Cin Full Adder Sum\_out I

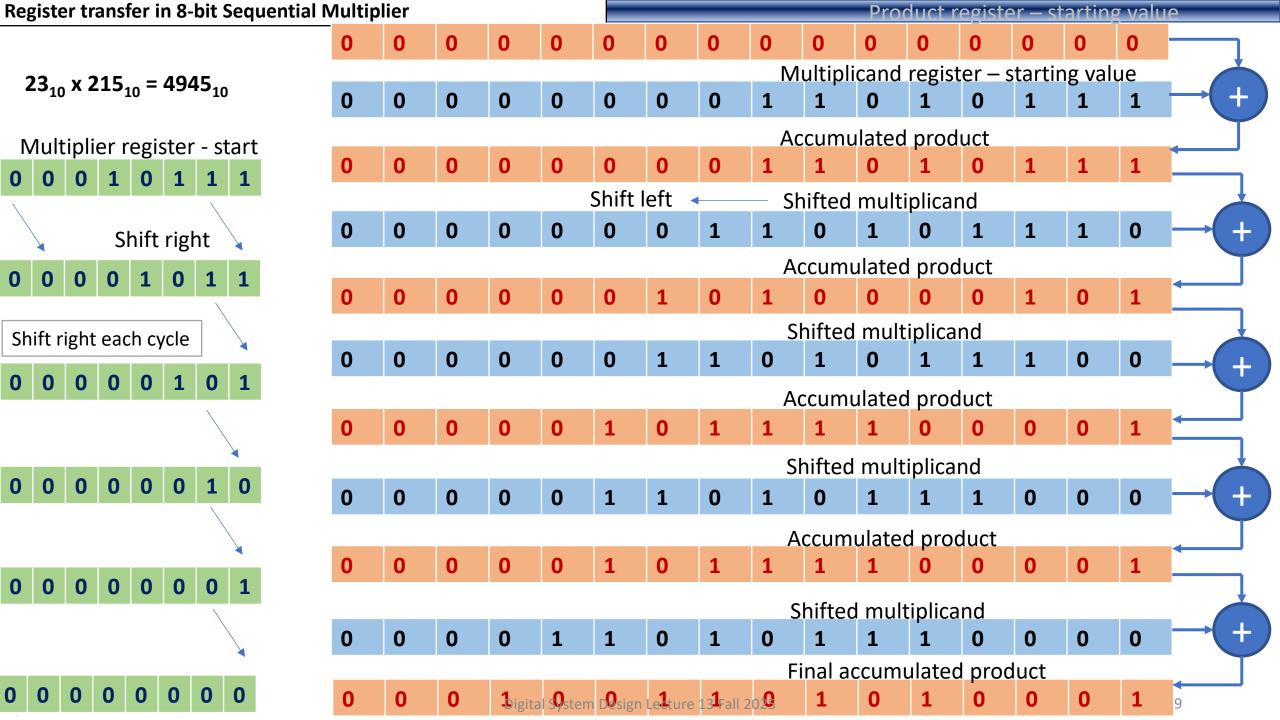
Worst case delay path is shaded
This is Critical Path
LUMS



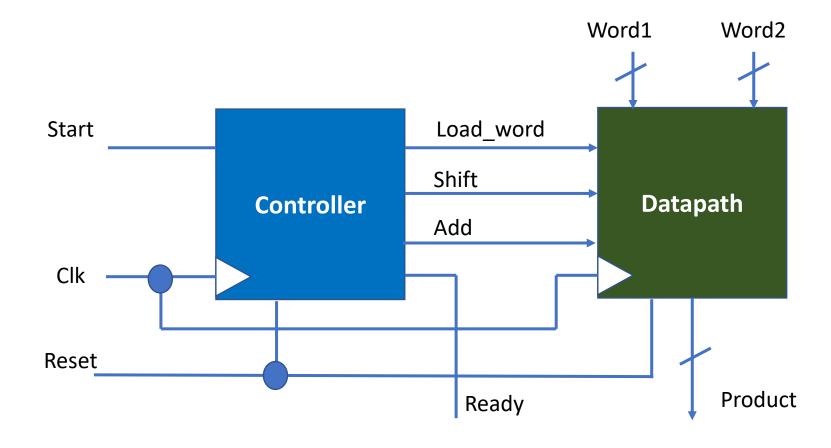
# Operation of Sequential Multiplier





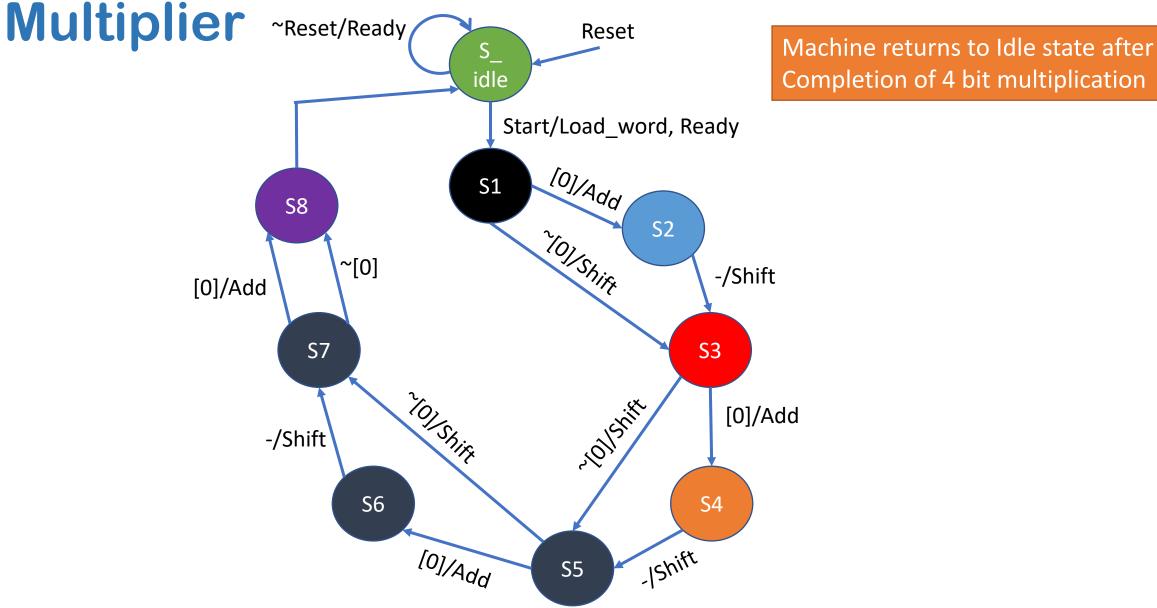


### Data Path Architecture of Sequential Mult



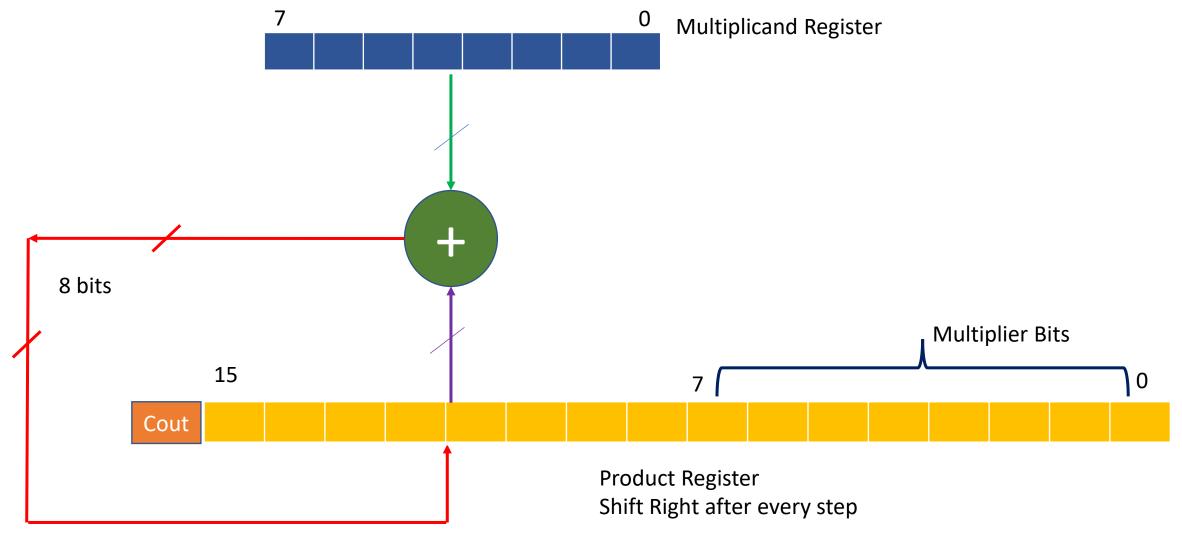


# STG for a 4 Bit Sequential Binary



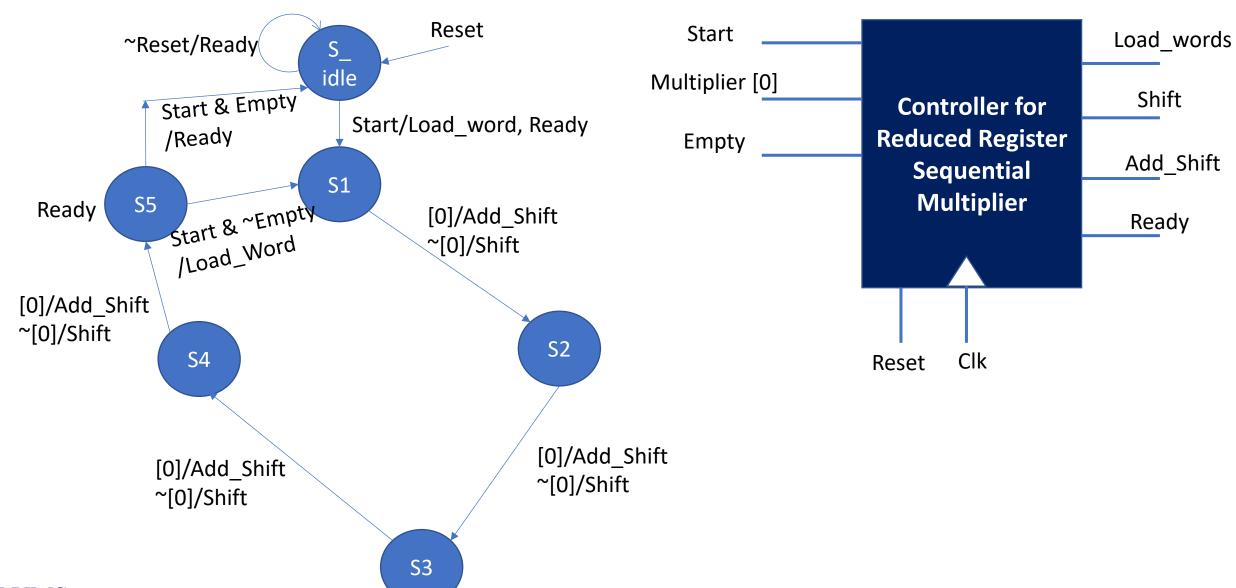


# Improvement - Sequential Multiplier with Reduced Registers





### STG of Reduced Register Sequential Multiplier





# Example of a 4-bit Serial Parallel Multiplier Product Accumulator Register (8 + 1) bits

Product Accumulator Register (8 + 1) bits Load Shift Cout Add Controller Multiplier 4 Bits Carry 4 Bit Adder M Done Start Multiplicand 4 Bits

Shift the contents To the right after Every step



# **Example continued**

				1	1	0	1	Multiplicand
			X	1	0	1	1	Multiplier
				1	1	0	1	
			1	1	0	1	( <b>X</b> )—	→ Shift Left by one
		1	0	0	1	1	1	Partial product after first step
		0	0	0	0	X	X	Another shift left
		1	0	0	1	1	1	Partial product after second step
	1	1	0	1	X	X	X	Another shift left
1	0	0	0	1	1	1	1	Partial product after final step

Answer =  $(10001111)_2 = (143)_{10}$ 



Embedded Systems Lab (EESL)

Multiplier Register
Operation Initial Conte

**Initial Contents of Accumulator** 

Multiplicand bit [0] is '1'

After Add operation

After Shift Right

Next bit M = 1 hence Add

After Add

After Shift Right

Next bit M=0, hence Skip Add

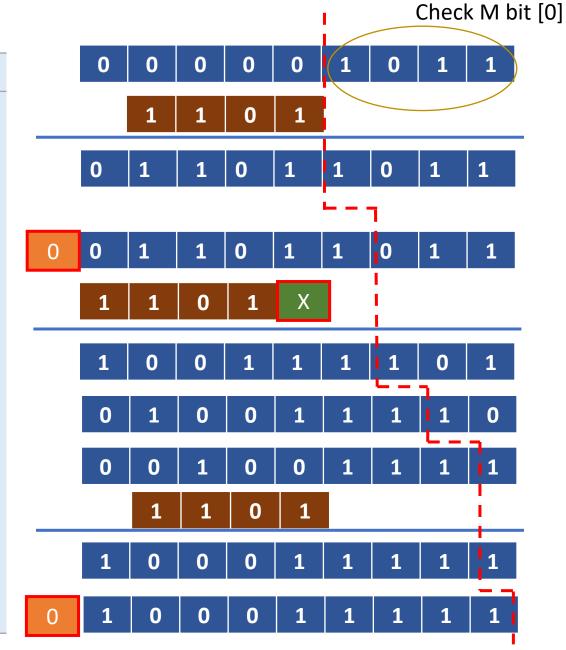
operation

After Shift Right

Next bit M=1, hence Add

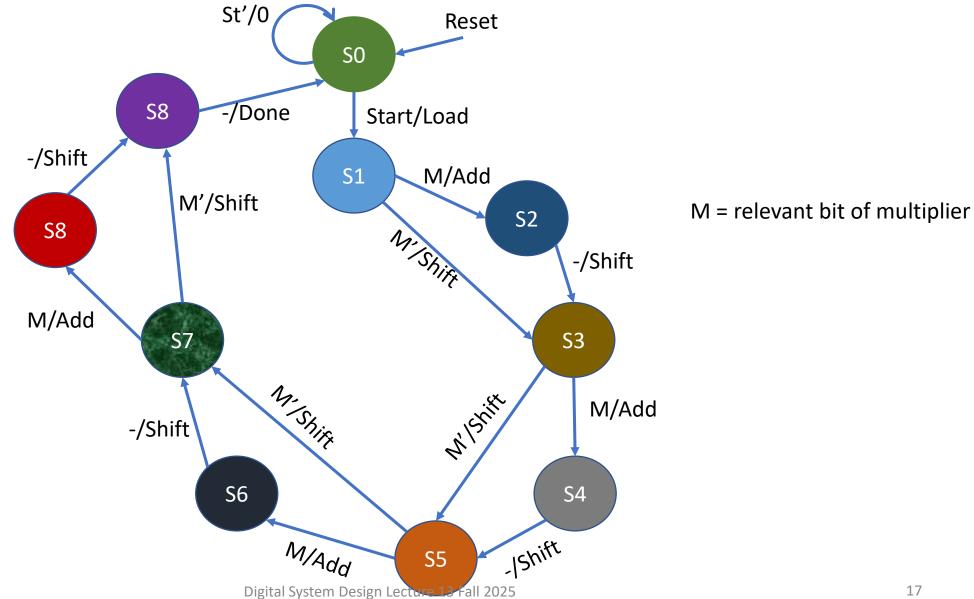
After Addition

After Shift Right, final answer



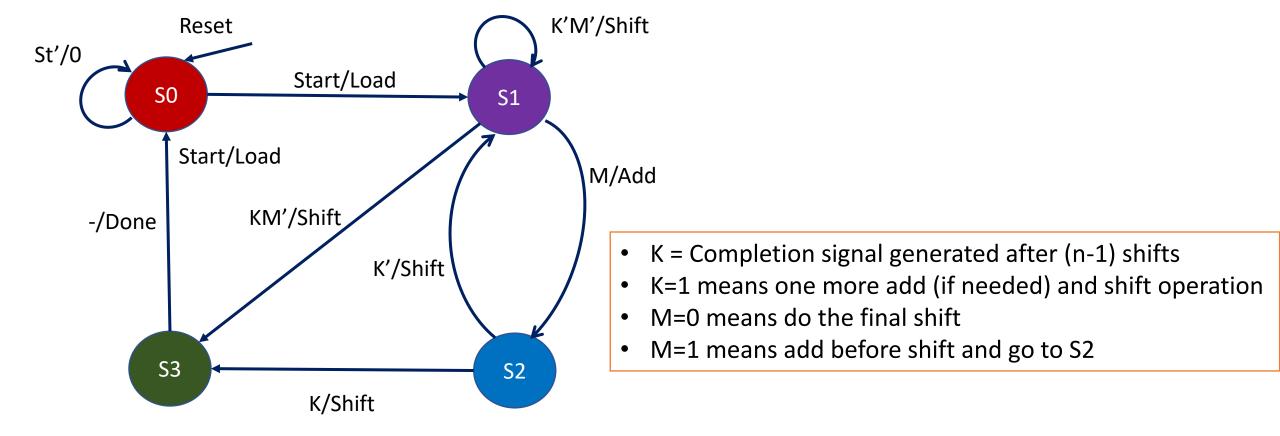


### STG Control Diagram for this Multiplier



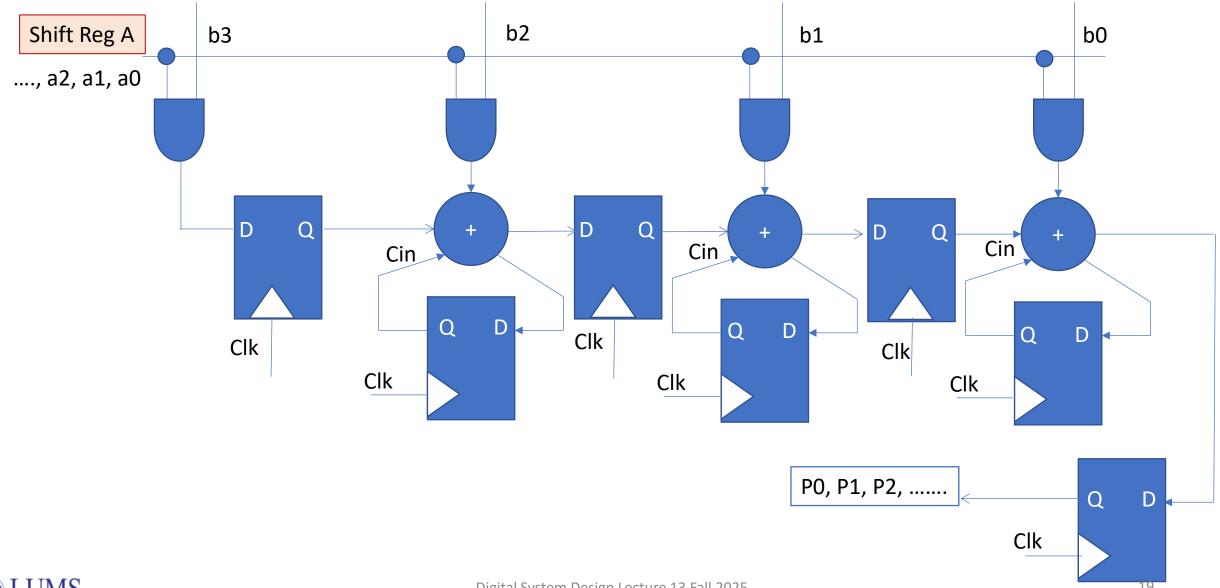


# Flexible STG for any no. of multiplicand bits





### Parallel-Serial Multiplier - Concept





## Multiplication of **Signed Binary Numbers**

Case I: Negative Multiplicand, Positive Multiplier

Example: -3<sub>10</sub> x 6<sub>10</sub>

Sign-bit of the multiplicand must be extended to the word length of the final product before Operating on the 2's Complement words.

This sign-extended multiplicand is used when forming Partial products and accumulated sums.

The result of the multiplication is the 2's Complement of the Product. The final magnitude is found by taking 2's Complement. Bit Assignment: We assign 8 bits to both numbers.

The product will thus be 16 bits.

+3 = 0000 0011

Thus 2's Complement = -3 = 1111 1101

+6 = 0000 0110

1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
							X	0	0	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	X
1	1	1	1	1	1	1	1	1	1	1	1	0	1	X	X
1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0

Remember: Sign Extension to maximum number of bits in datapath



# **Multiplication of Fractions**

#### **Convert from decimal to binary**

$$(\frac{3}{4})$$

= 0.75

 $0.75 \times 2 = 1.5$ , keep 1

 $0.5 \times 2 = 1.0$ , keep 1

 $0 \times 2 = 0 \text{ keep } 0$ 

And only zeros afterwards

$$= 2^{-1} + 2^{-2} + 0 + 0$$

= 0.1100; assigning four fractional bits



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2's Complement of Binary Fractional Nos.

- Given binary fractional number = (0.1100)
- Method 1:
- Decide on the number of total bits, eg. 5 bits; Invert all bits; add +1 to LSB
- 2's Complement = 1.0011
- + 3
- •
- = 1.0100
- Method 2:
- Look from right to left; when you Encounter first 1; invert all bits to the left
- For (0.1100), the 2's Complement = (1.0100)



### Question?

- Represent 9/16 using five fractional bits:
- Hint: 9/16 = 0.xxxxx
- Keep multiplying by 2; if answer is greater than 1, keep 1

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• Solve: 0.562 x 2 = 1.125, keep 1
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- $0.125 \times 2 = 0.25$ , keep 0
- $0.25 \times 2 = 0.5$ , keep 0
- 0.5 x 2 = 1.0, keep 1
- 0 x 2 = 0, keep 0, and same for more terms
- Answer = 0.10010 in binary

Finally, 2's Complement of "0.10010" is (look right to left) "1.01110" that is [-9/16]



### **Convert Fraction Number to Binary**

- Represent 9/16 using five fractional bits:
- Hint: 9/16 = 0.5625
- Keep multiplying by 2; if answer is greater than 1, keep 1
- Solve: 0.5625 x 2 = 1,125, keep 1
- $0.125 \times 2 = 0.25$ , keep 0
- $0.25 \times 2 = 0.5$ , keep 0
- $0.5 \times 2 = 1.0$ , keep 1
- $0 \times 2 = 0$ , keep 0, and same for more terms
- Answer = 0.10010 in binary

Finally, 2's Complement of "0.10010" is (look right to left) "1.01110" that is [-9/16]



# **Multiplication of Signed Fractions**

- Fractions are multiplied like whole numbers, but overflow is not possible
- A 4-bit fractional number is represented as minimum 5-bit fixed point number with MSB holding the sign bit in 2's Complement format
- The product of two 5-bit numbers will produce 10-bit result
- MSB will be sign-extended (bit replication) for negative multiplicand

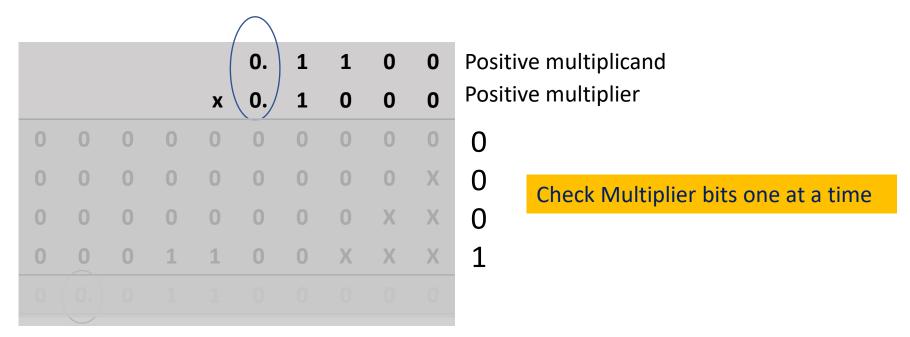


# Example 1: Positive multiplicand, positive multiplier, fraction multiplication

Show binary multiplication of  $(3/4)_{10} \times (1/2)_{10}$ Use 5-bits to represent each number

3/4 = 0.1100

1/2 = 0.1000



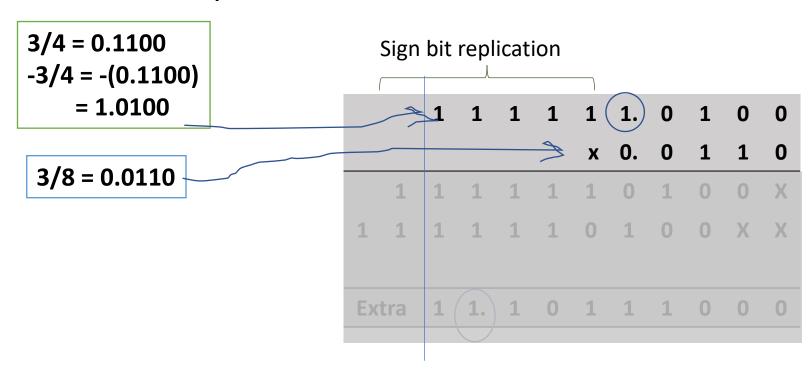
Insert decimal, count how many bits after decimal in both numbers (4 + 4 = 8 bits in both numbers)

Answer = (0.0110000000) = +(3/8)



# Example 2: Negative multiplicand, positive multiplier, fraction multiplication

Show binary multiplication of  $(-3/4)_{10} \times (3/8)_{10}$ Use 5-bits to represent each number



Negative multiplicand

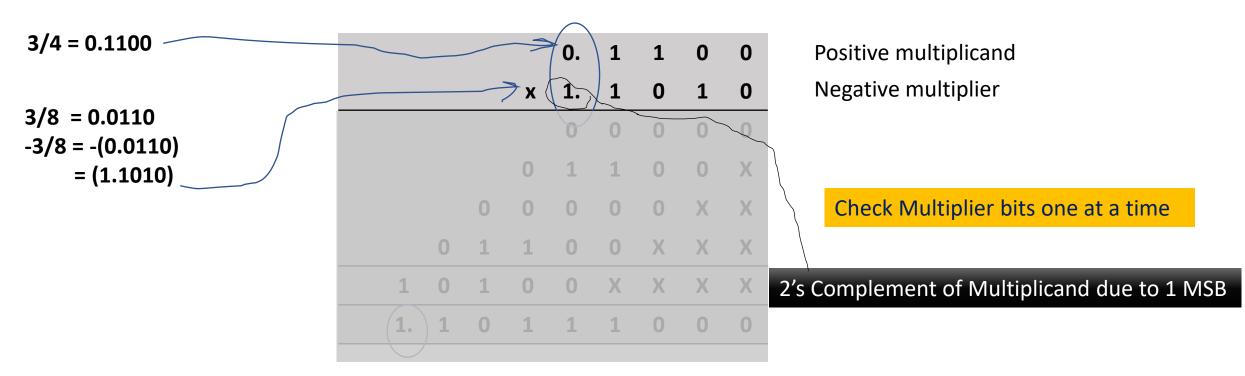
Negative multiplier
(first 0 only shift, then 1, Add multiplicand)
(next 1, Add Multiplicand, then 0 shifts only)

Insert decimal, count how many bits after decimal in both numbers (4 + 4 = 8 bits in both numbers)Answer = (11.10111000), take 2's complement = -(0.01001000) = (-9/32)



# Example 3: Positive multiplicand, negative multiplier, fraction multiplication

Show binary multiplication of  $(3/4)_{10} \times (-3/8)_{10}$ Use 5-bits to represent each number

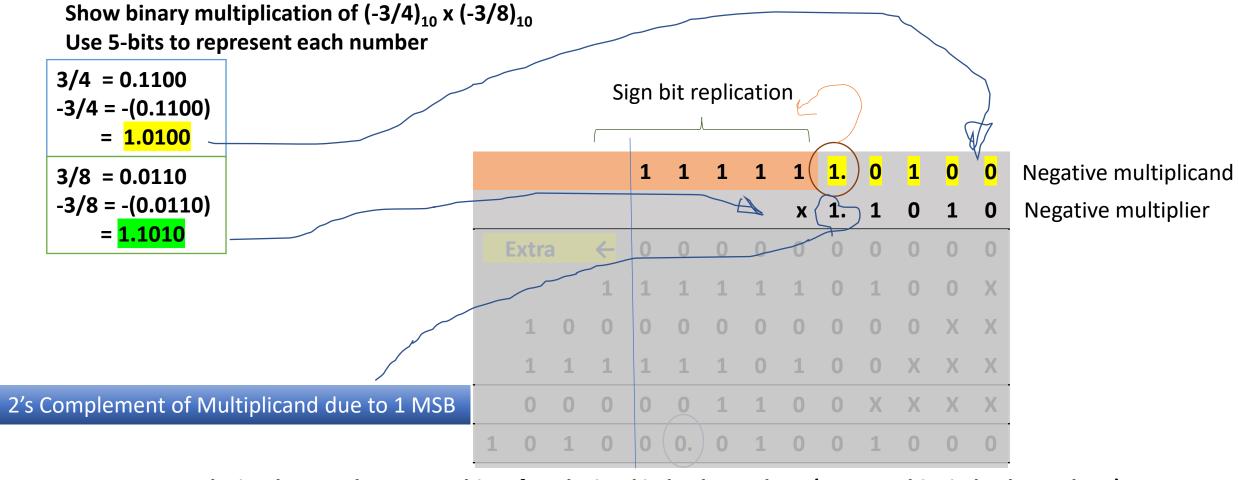


Insert decimal, count how many bits after decimal in both numbers (4 + 4 = 8 bits in both numbers)

Answer = (1.10111000), take 2's Complement = -(0.01001000) = -(9/32)



# Example 4: Negative multiplicand, negative multiplier, fraction multiplication





Insert decimal, count how many bits after decimal in both numbers (4 + 4 = 8 bits in both numbers)

### To Remember in Signed Multiplication

• When Multiplicand is Negative, do a sign extension to cover the possible bit-width of Answer

When Multiplier is Negative, there is a final 2's Complement Addition
 Step corresponding to the MSB of multiplier



# Algorithmic Improvement in Multipliers

# **Booth Encoding**

# **Booth Multiplication Process**



### **Booth Encoded Multipliers**

Object: To reduce the number of 'Add' steps required in complete multiplication cycle

→ MSB '1' shows negative number

2's Complement of 
$$7_{10} = (1 \ 0 \ 0 \ 1)_2$$

$$1 \times 2^0 = 1$$

$$0 \times 2^1 = 0$$

Allow both +ive and -ive signs to be used in conversion

$$0 \times 2^2 = 0$$

$$-1 \times 2^3 = -8$$

Decimal value of  $(1001)_2 = (-8+1) = -7 = (\underline{l} \ 0 \ 0 \ 1) \text{ or } (-1 \ 0 \ 0 \ 1)$ 

Booth's algorithm is valid for both positive and negative numbers in 2's complement format



# **Booth Recoding of a 2's Complement Number**

m <sub>i</sub>	m <sub>i-1</sub>	Booth Recoded C <sub>i</sub>	Value	Status
0				String of 0s
0	1	1	+1	End of string of 1s
1		<u>l</u>	-1 or <u>l</u>	Begin string of 1s
1	1			Midstring of 1s



# **Booth Recoding of -65<sub>10</sub>**

 $-65_{10}$  = 1 0 1 1 1 1 1 0 +65 = (01000001) 2's Complement

Append '0' on right, if LSB=1

2's Complement notation

m <sub>i</sub>	m <sub>i-1</sub>	Booth Recoded Ci
0	0	0
0	1	1
1	0	<u>l</u>
1	1	0

-65<sub>10</sub>=

Or

**Booth Recoded notation** 

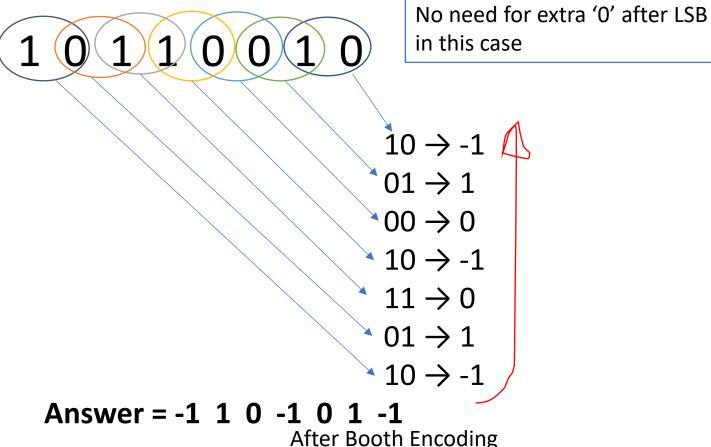
-65 = (10111111)

### Question?

Convert decimal number –78 to Booth Encoded format using 8 binary bits

+78 = 01001110 Take 2's Complement -78 = 10110010

m <sub>i</sub>	m <sub>i-1</sub>	Booth Recoded Ci
0	0	0
0	1	1
1	0	<u>l</u>
1	1	0



After Booth Encoding

