Lecture 19

EE 421 / CS 425

Digital System Design

Fall 2024

Shahid Masud

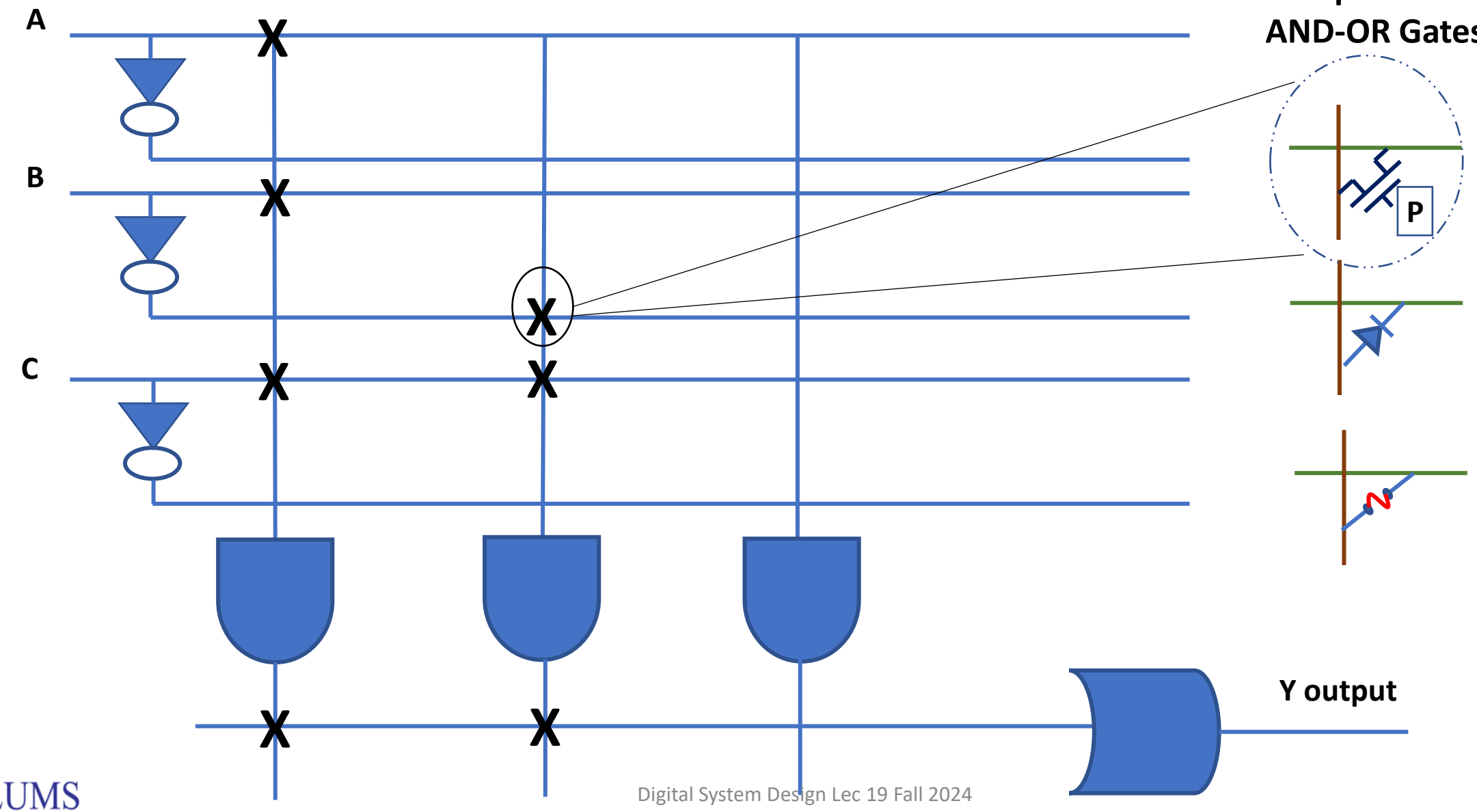
Topics

- PAL, PLA, Examples, Polarity Control Circuit in I/O
- Example of an I/O Block for SPLD
- Field Programming technology
- CPLD Architecture
- CPLD Examples from Xilinx and Altera
- Logic Expander – Shareable and Parallel
- Output Block of PLD
- FPGA Architecture

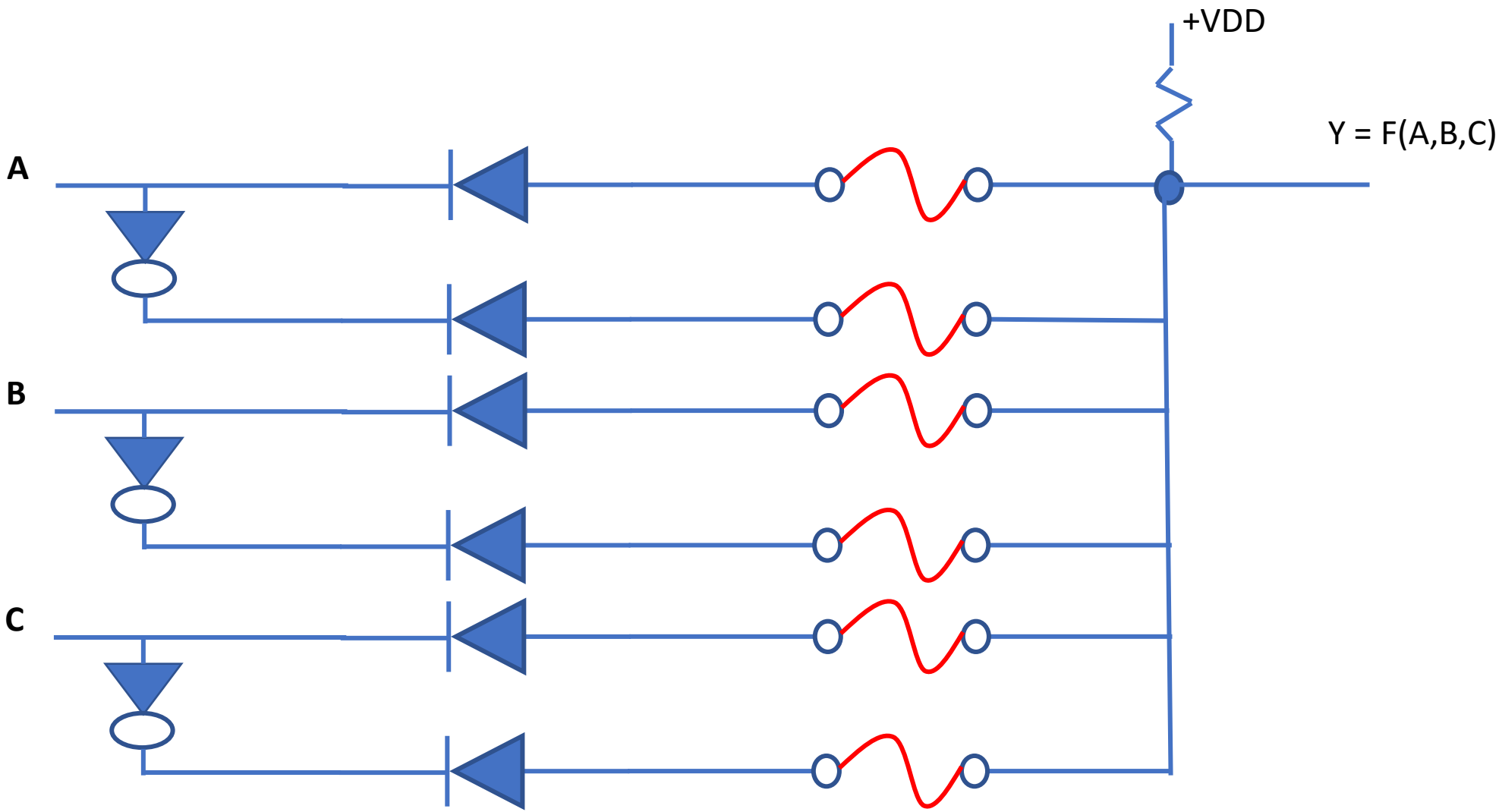
QUIZ NEXT MONDAY

AND-OR Logic Array

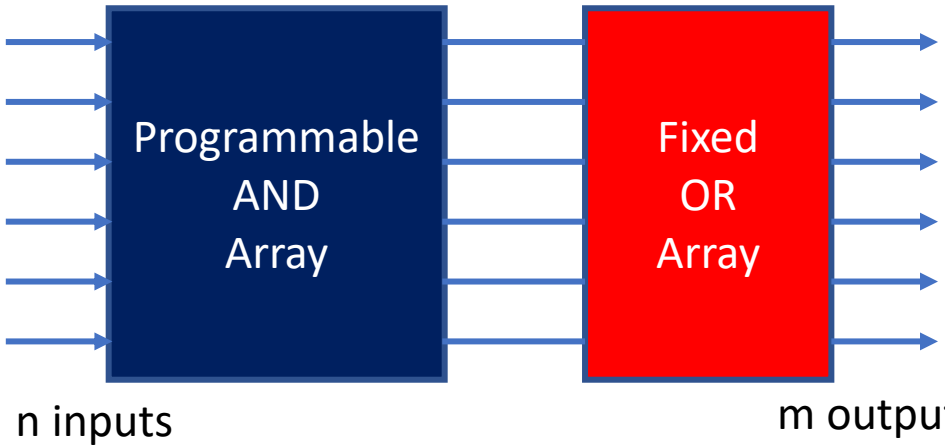
PLA = Programmable Logic Array Comprises Programmable AND-OR Gates

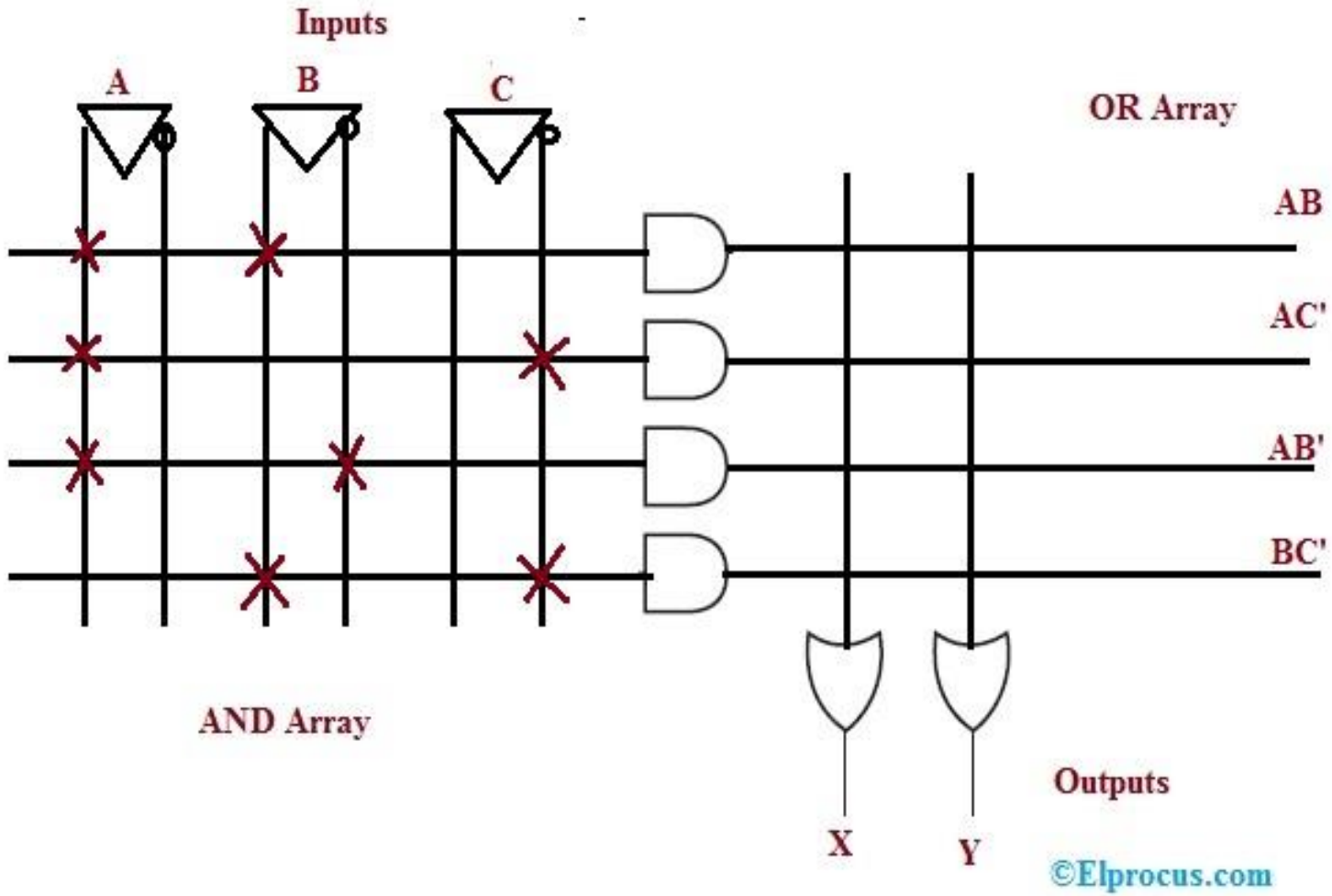


Fuse Programmable Logic Array



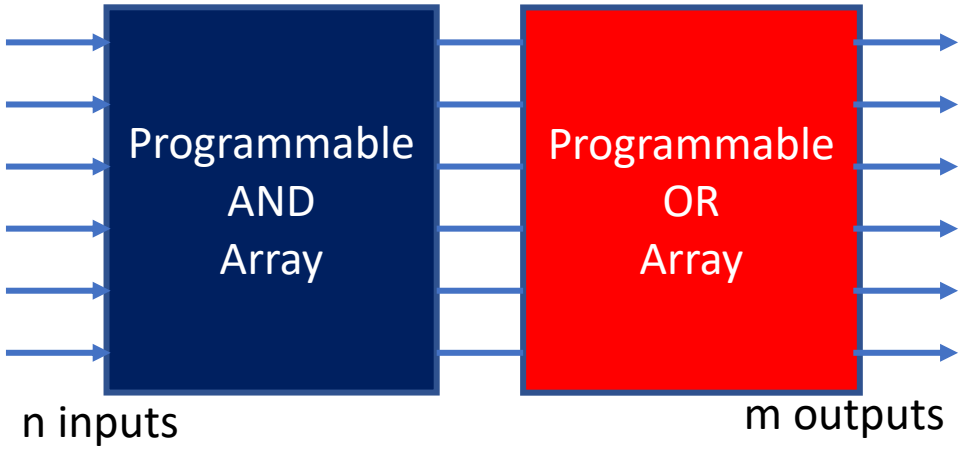
PAL – Programmable Array Logic

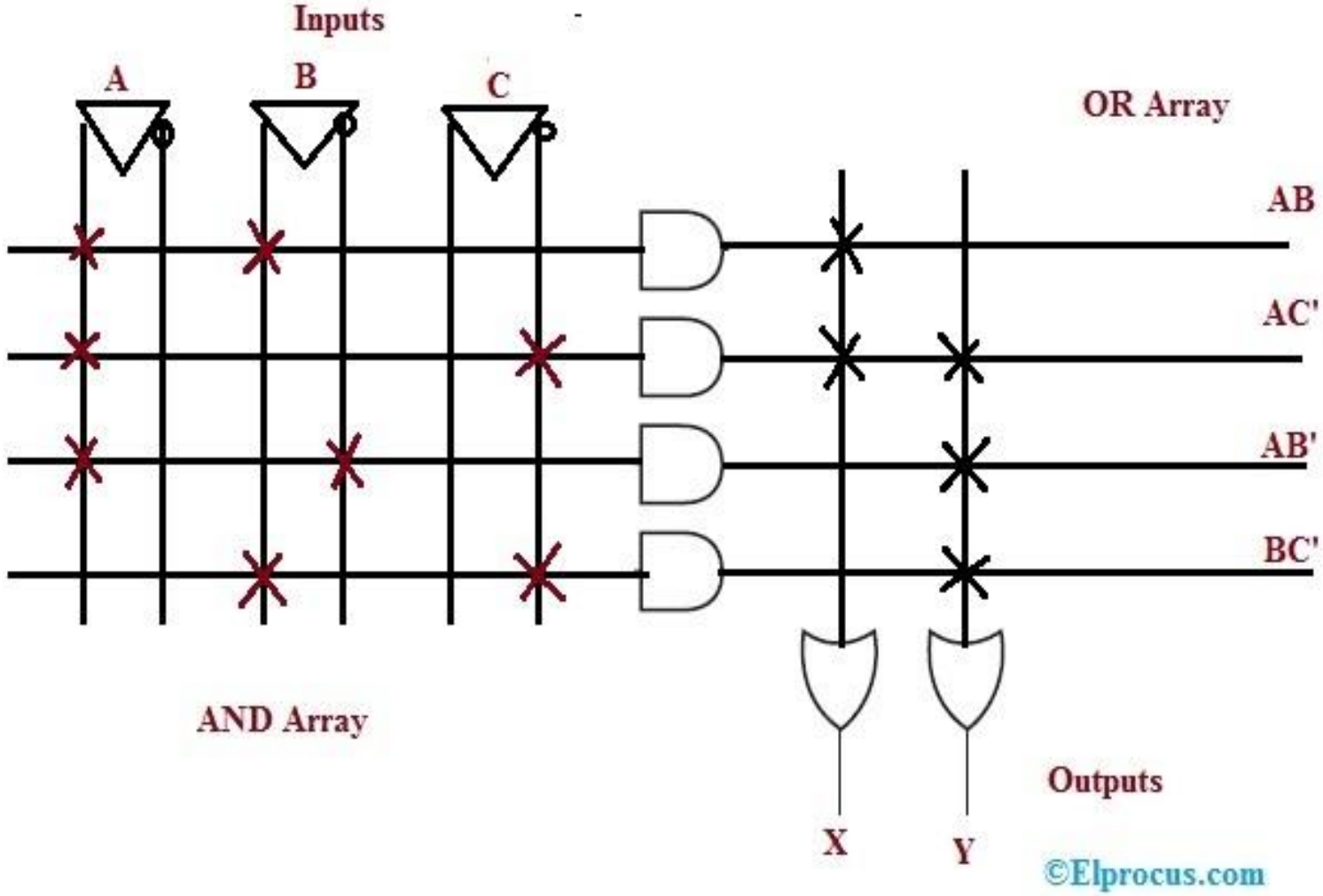




https://www.elprocus.com/what-are-pal-and-pla-design-and-differences/

PLA – Programmable Logic Array





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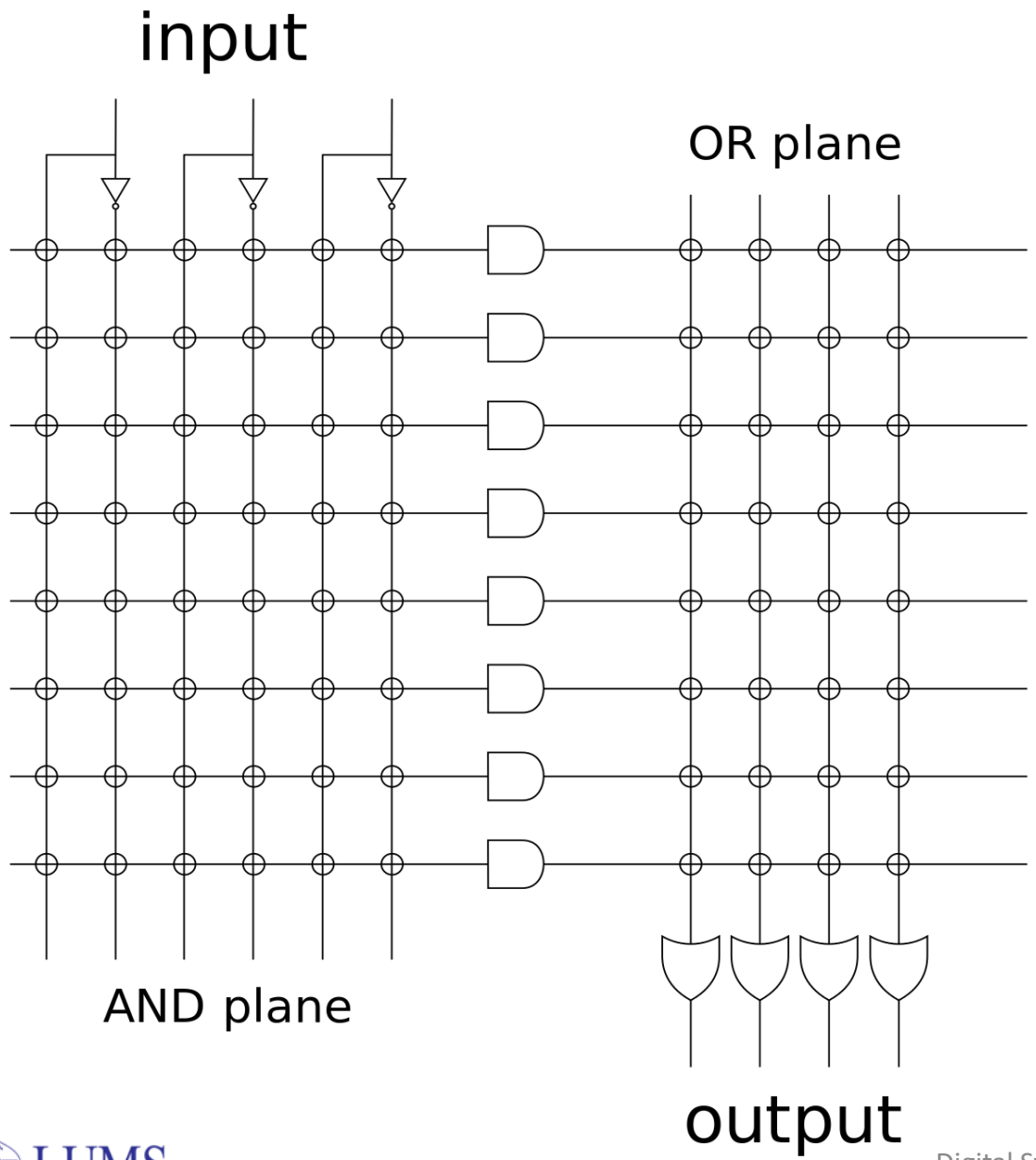
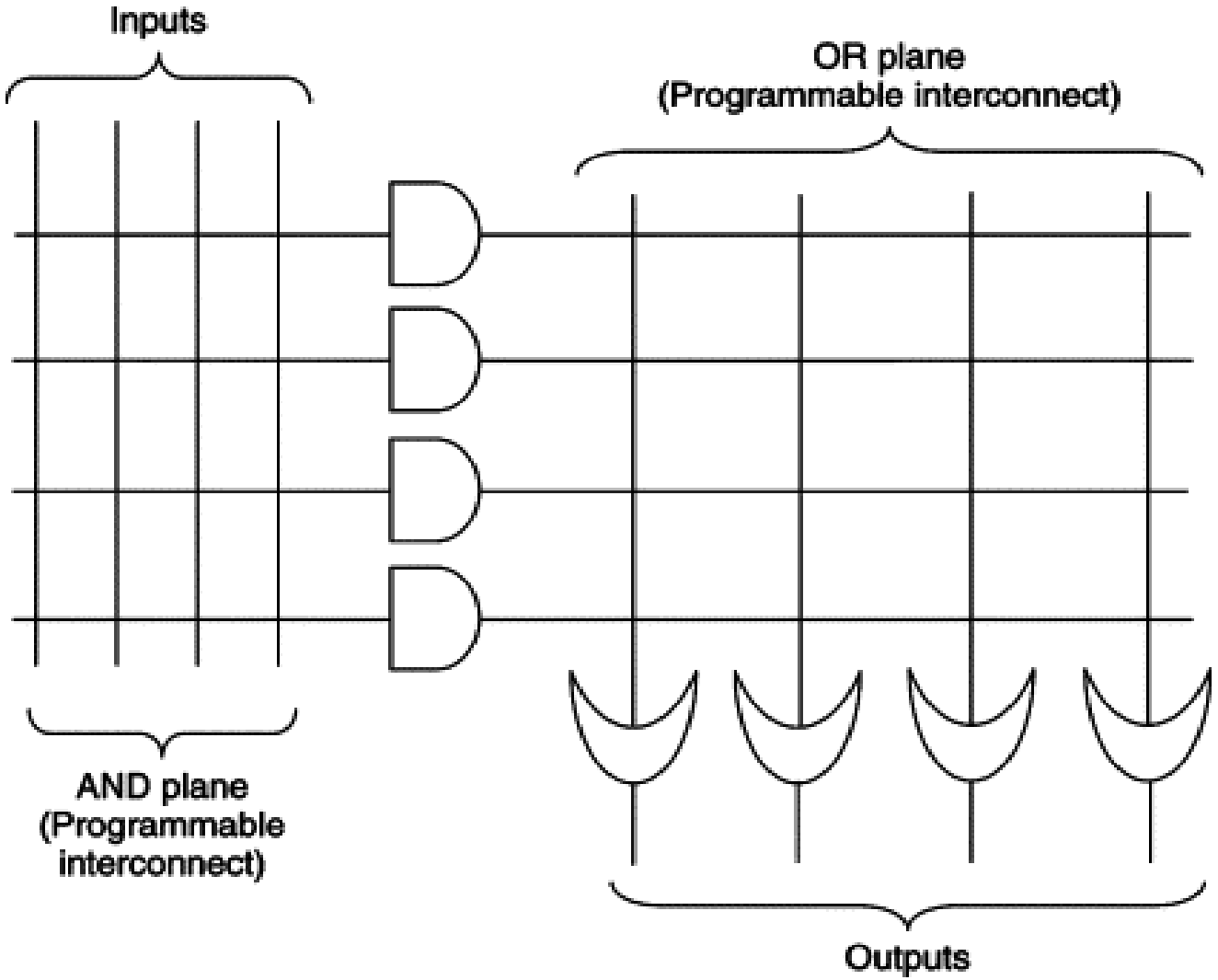
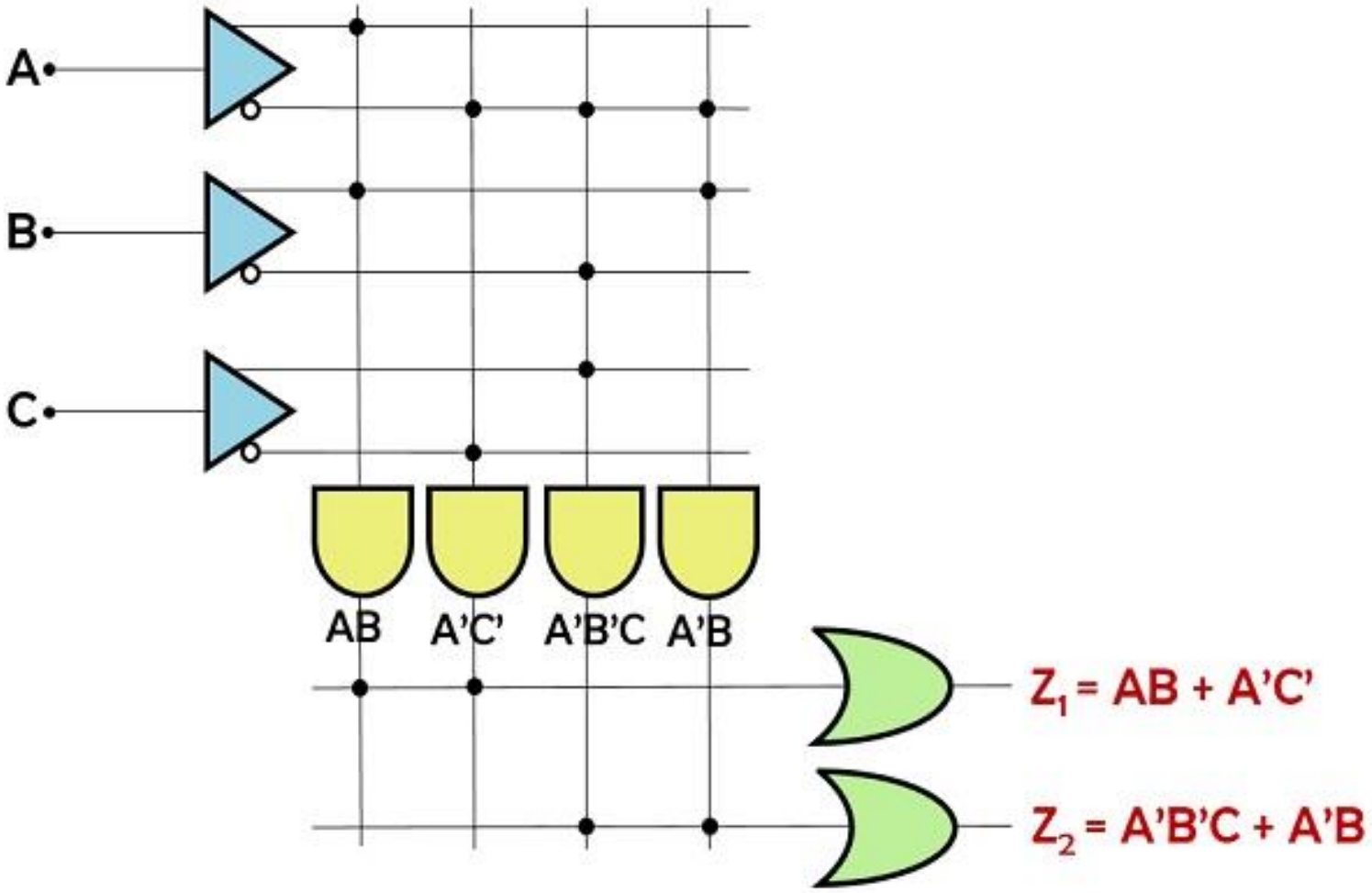
For Exercise





Example of PLA

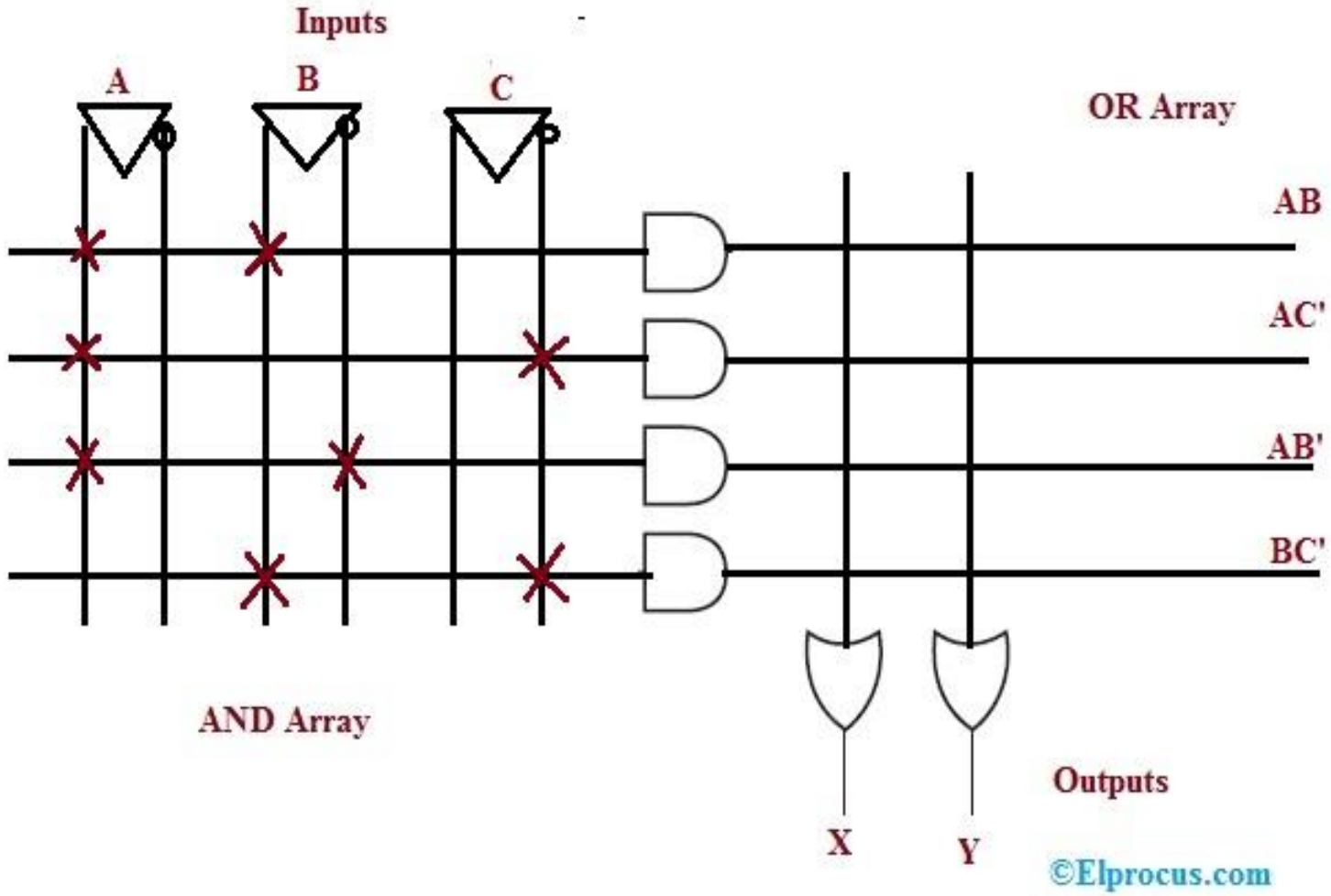


Implementation of Programmable Logic Array

Electronics Coach

https://electronicscoach.com/programmable-logic-array.html

PAL – Programmable Array Logic



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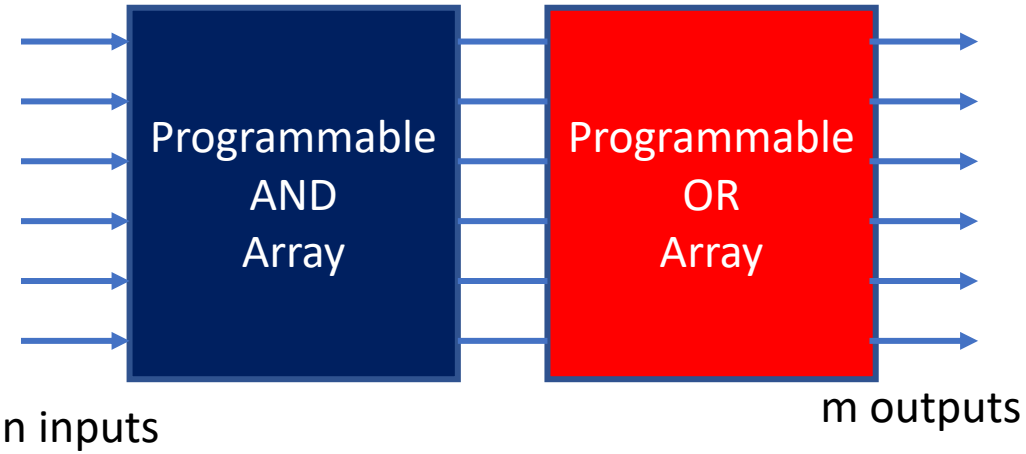
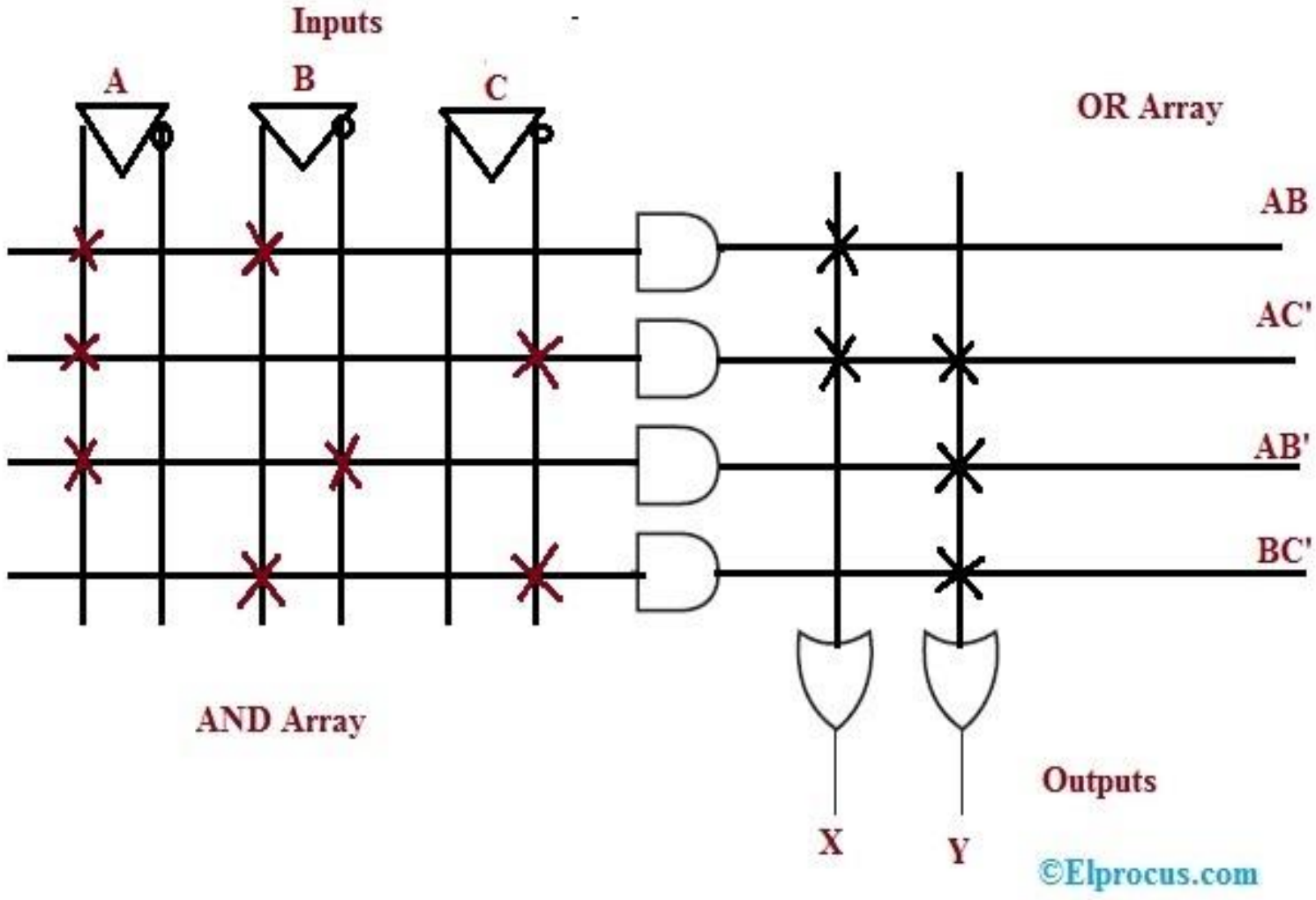
PLA – Programmable Logic Array





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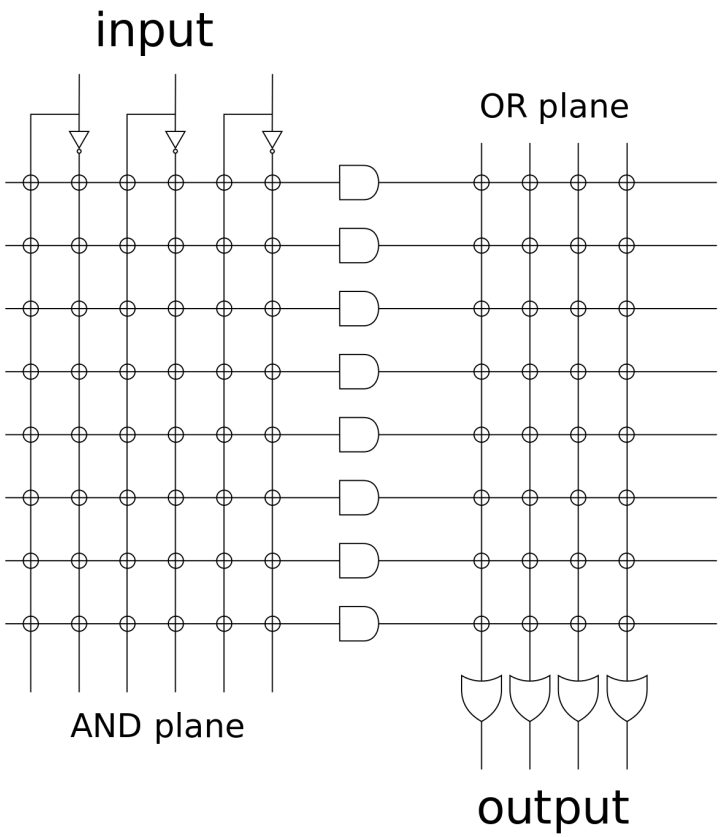
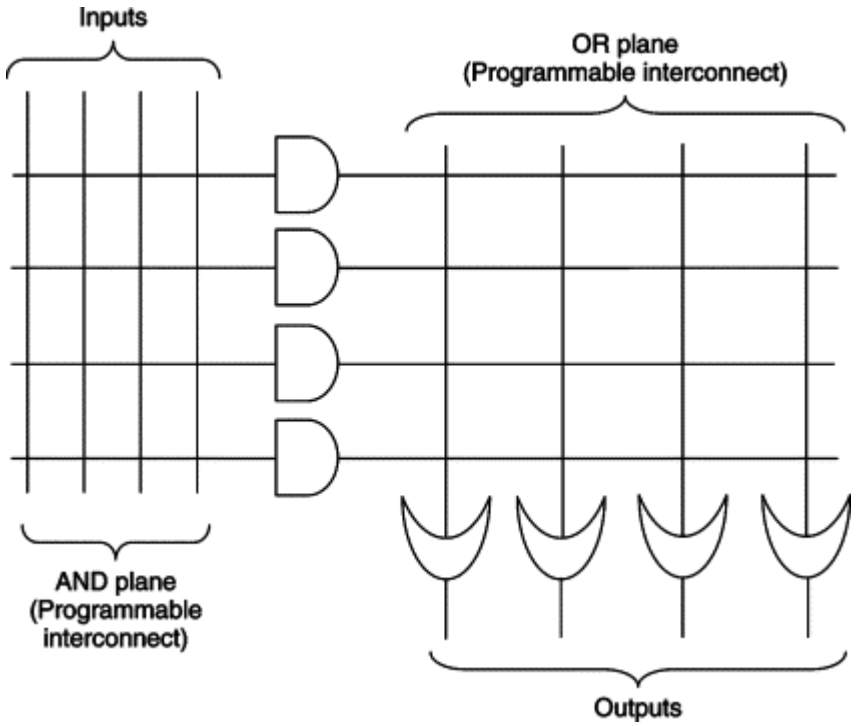
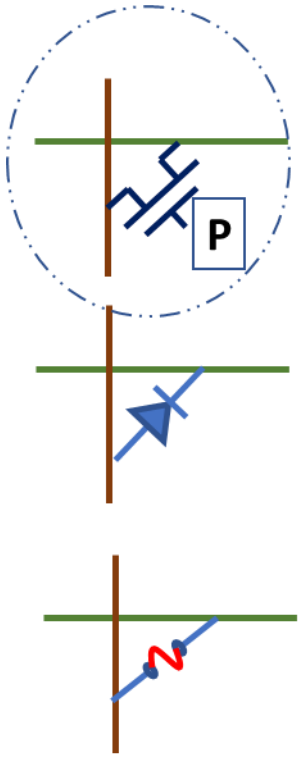
For Exercise

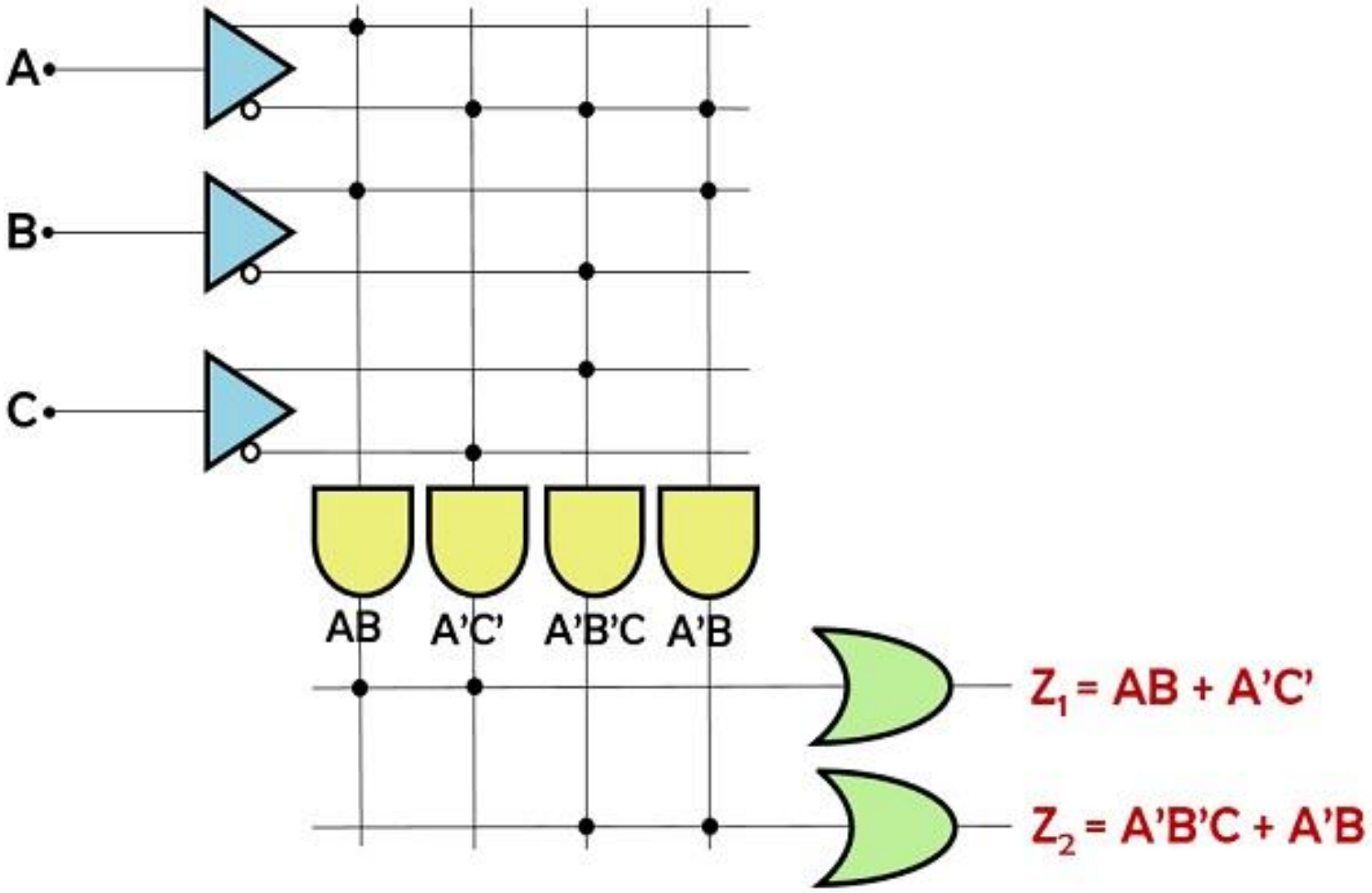






How to Configure?

Example of PLA



Implementation of Programmable Logic Array

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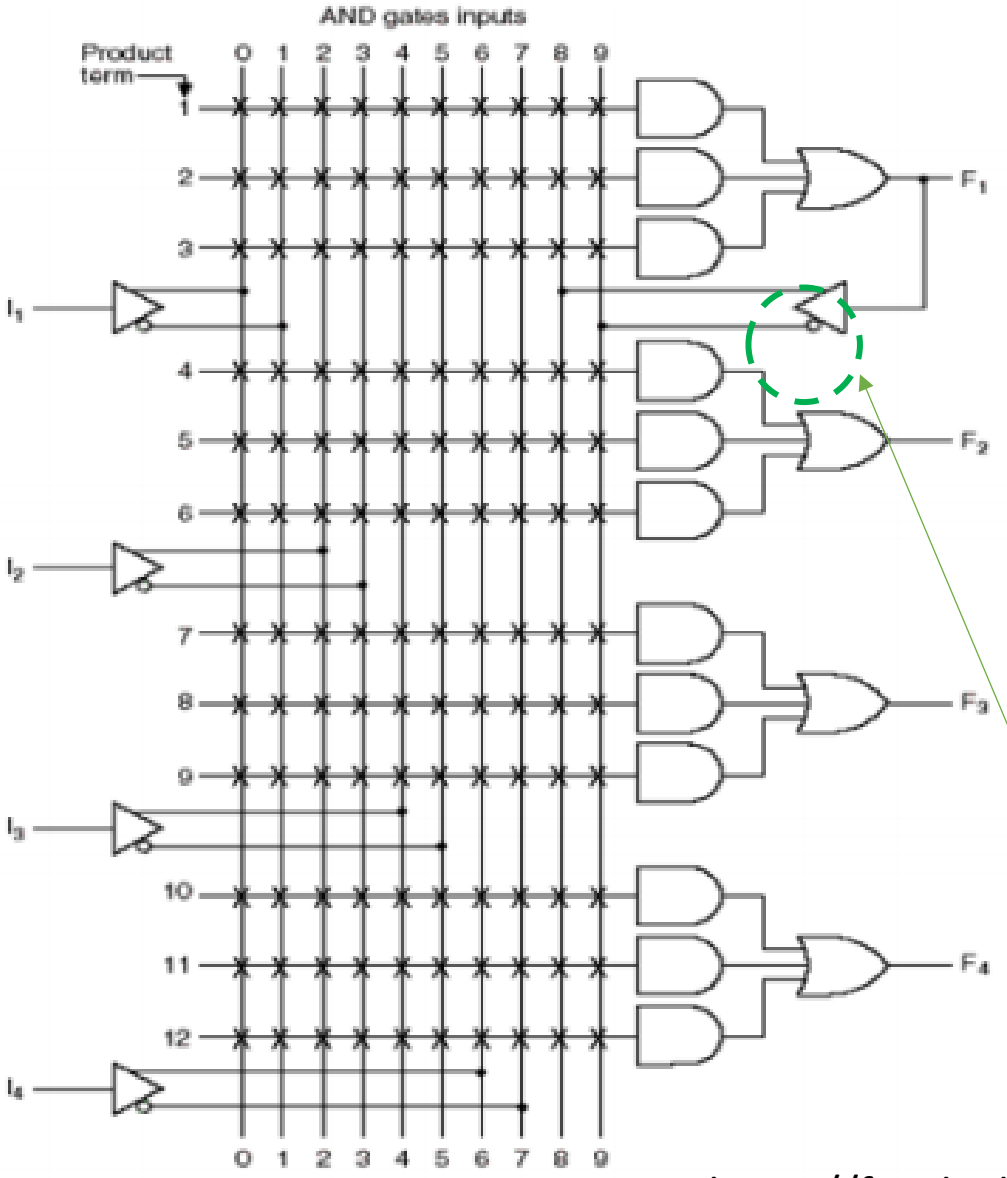
PAL – Programmable Array Logic Example



- PAL Device is a PLD with fixed OR array and a programmable AND array
- As only AND gates are programmable, PAL is easier to program

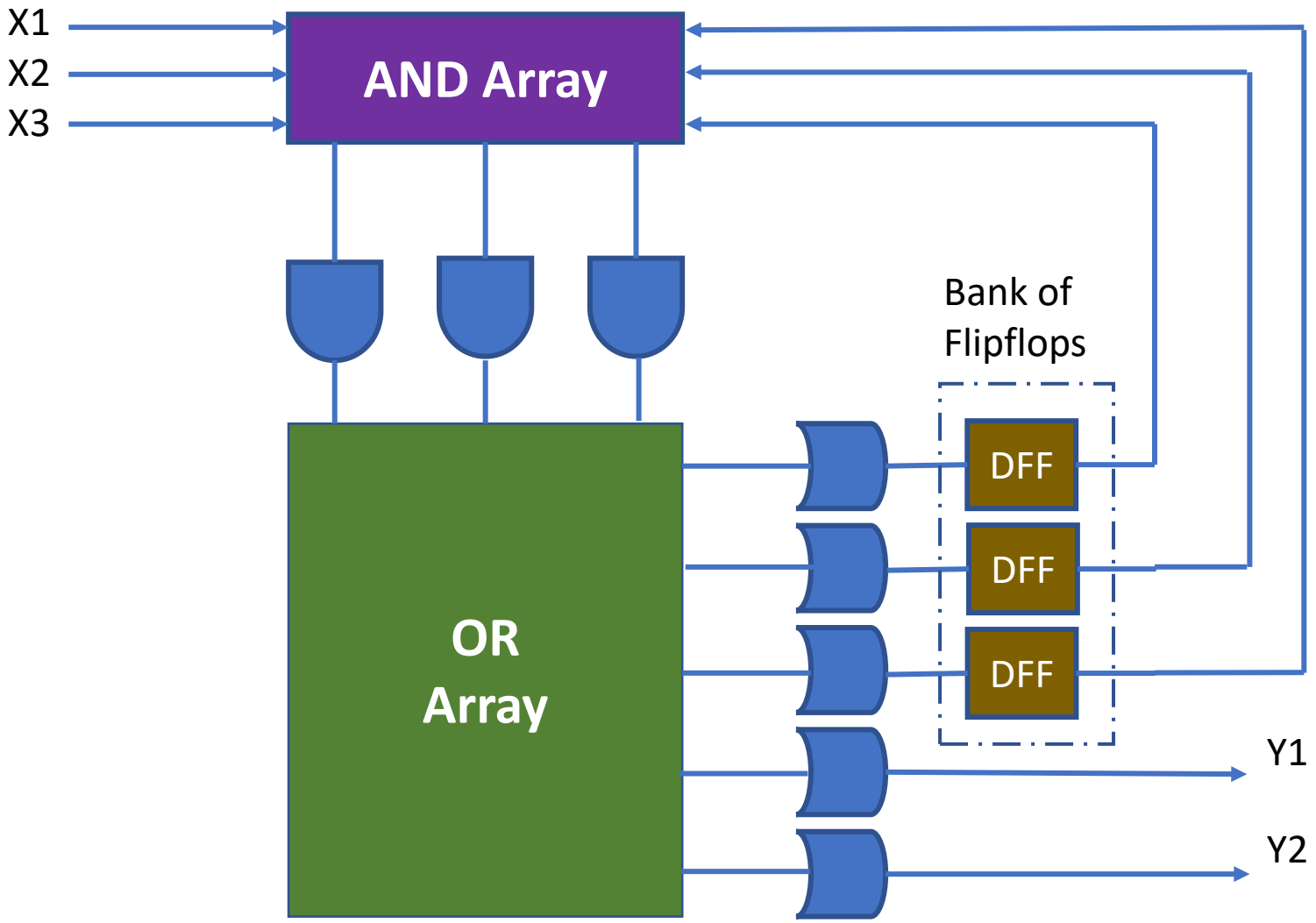
but it is less flexible compared to PLA devices

Example device:

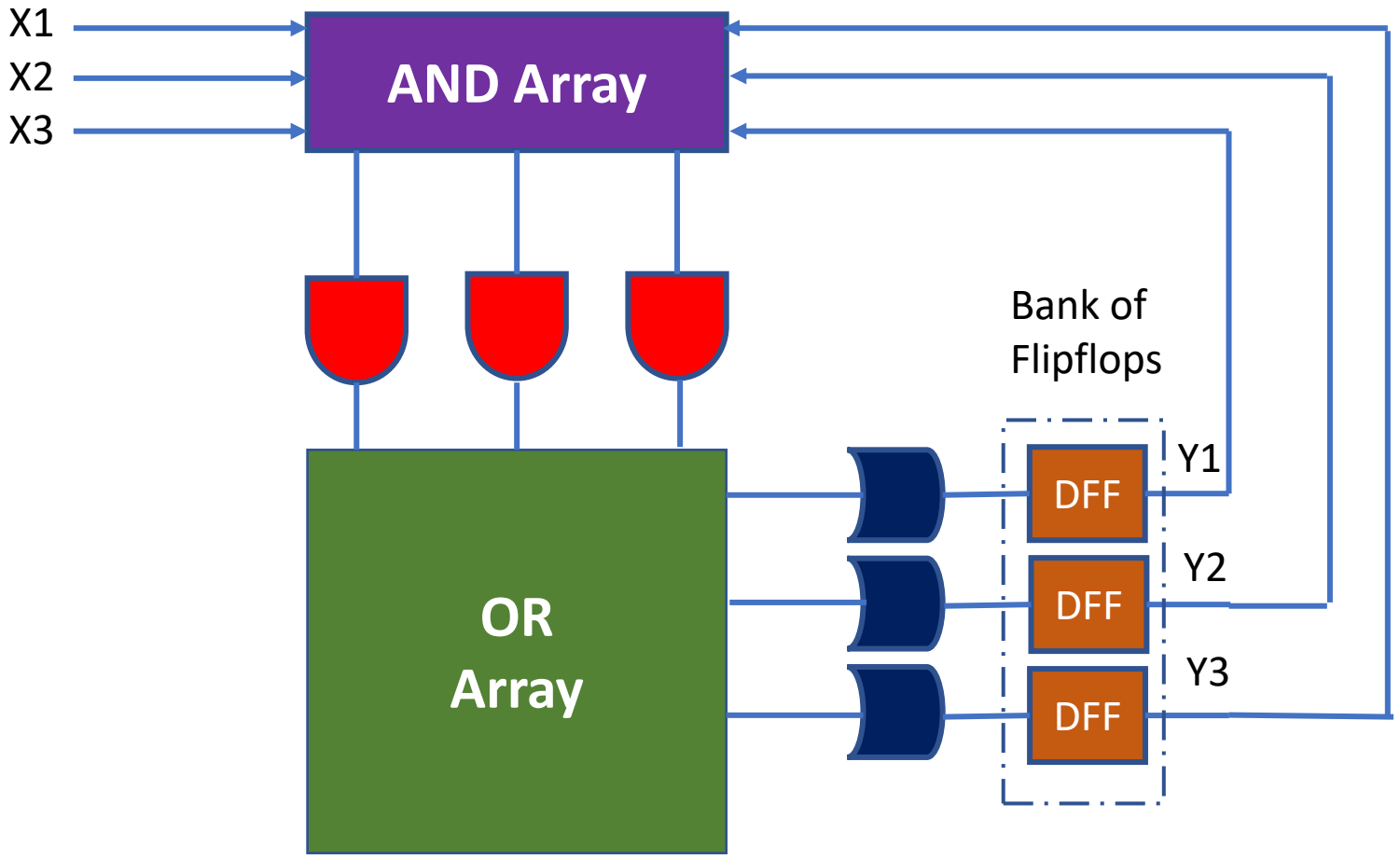
- This device has 4 inputs and 4 outputs.
- Each input has a buffer and inverter, output is from fixed OR gate
- The device has 4 sections: Each section comprises 3 wide AND-OR array, meaning three programmable AND arrays in each section
- Each AND gates has 10 programmable input connections
- One of the outputs (see F1) can be fed back to the inputs of AND gate through programmable connections

https://faculty.kfupm.edu.sa/COE/aimane/coe202/PLDs.pdf

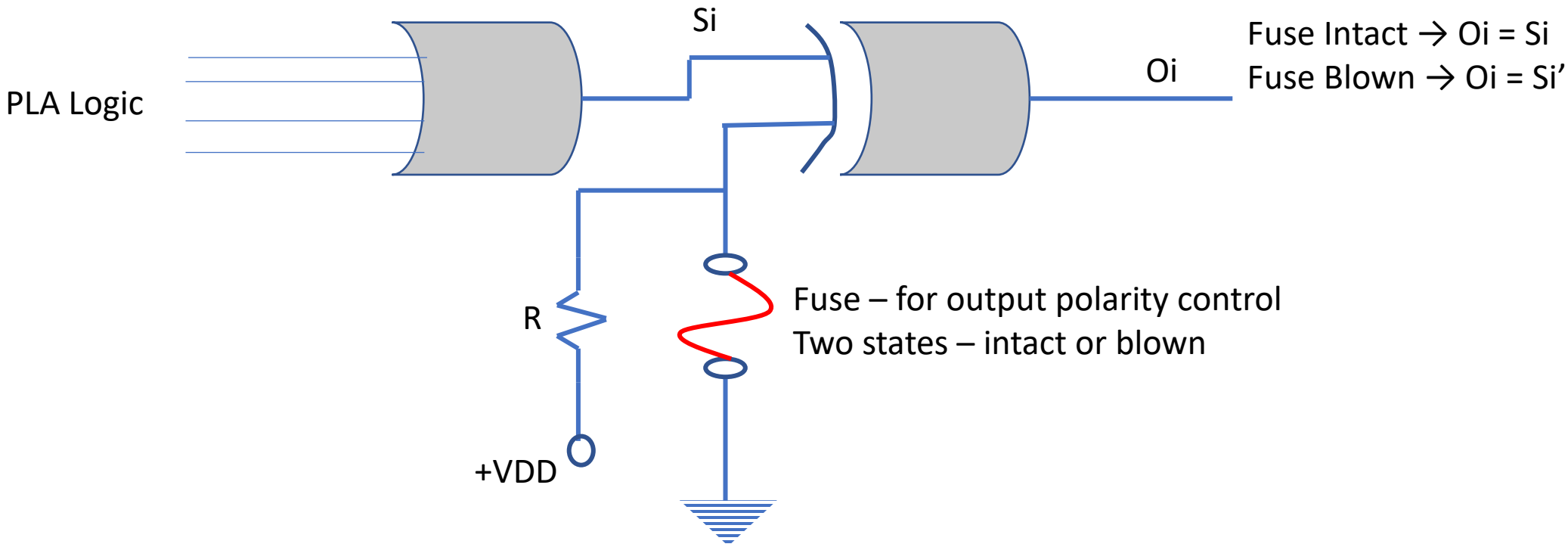
Sequential Circuits with PLD – Mealy Machine



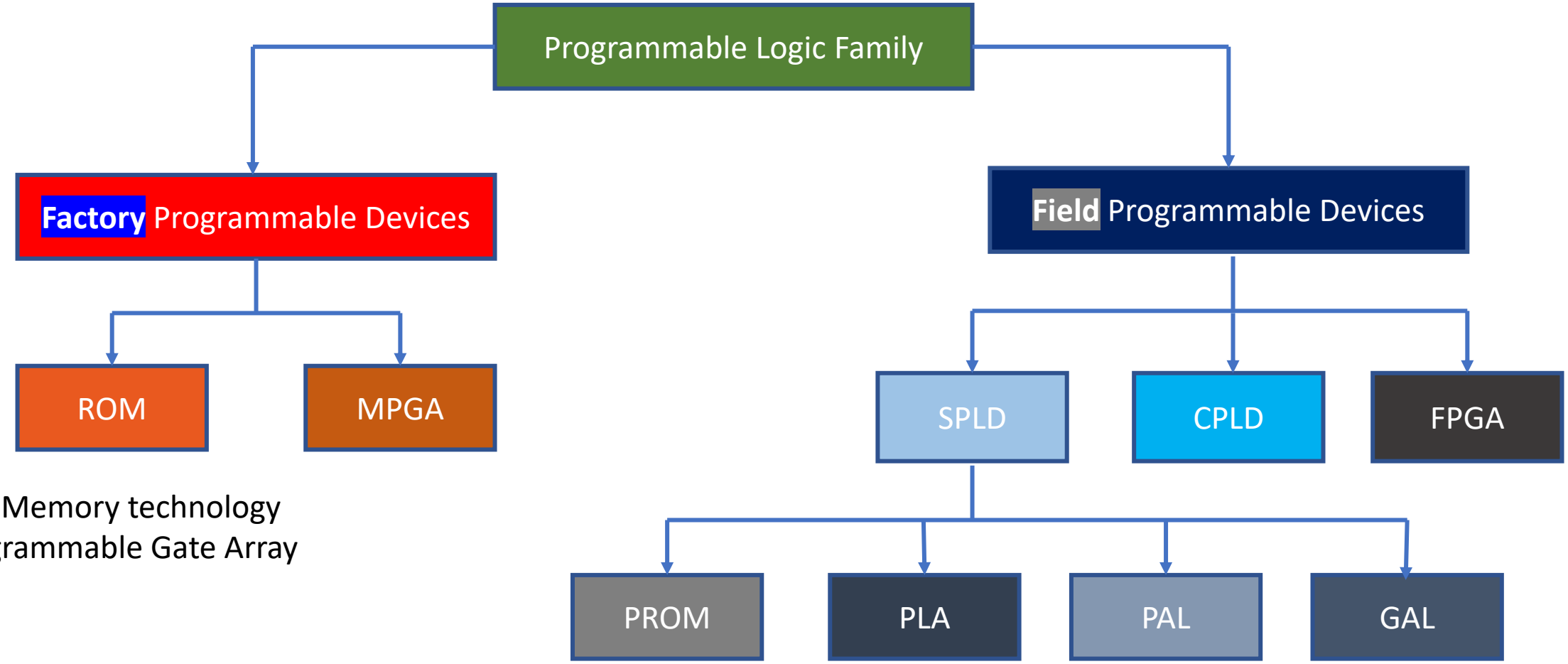
Sequential Circuits with PLD – Moore Machine



Output Polarity Control



Programmable Logic Broad Classification



Read only Memory technology
Mask Programmable Gate Array

Simple and Complex Programmable Logic Devices
Field Programmable Gate Array
Generic Array Logic (complex PAL by lattice semi), Programmable Logic Array

Programmable Hardware Devices Comparison

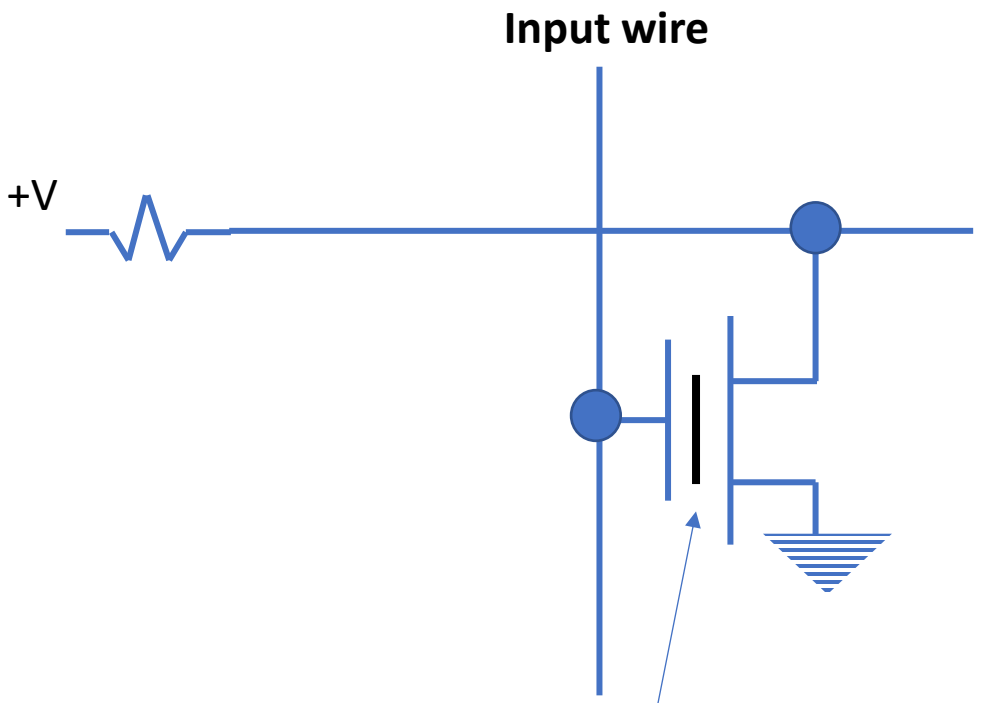
Table 3-1: *A Comparison of Programmable Devices*

	SPLD	CPLD	FPGA
Density	Low Few hundred gates	Low to Medium 500 to 12,000 gates	Medium to High 3,000 to 5,000,000 gates
Timing	Predictable	Predictable	Unpredictable
Cost	Low	Low to Medium	Medium to High
Major Vendors	Lattice Semiconductor Cypress AMD	Xilinx Altera	Xilinx Altera Lattice Semiconductor Actel
Example Device Families	**Lattice Semiconductor** GAL16LV8 GAL22V10 **Cypress** PALCE16V8 **AMD** 22V10	**Xilinx** CoolRunner XC9500 **Altera** MAX	**Xilinx** Virtex Spartan **Altera** Stratix **Lattice** Mach ECP **Actel** Accelerator

Ref: Roth & John Book

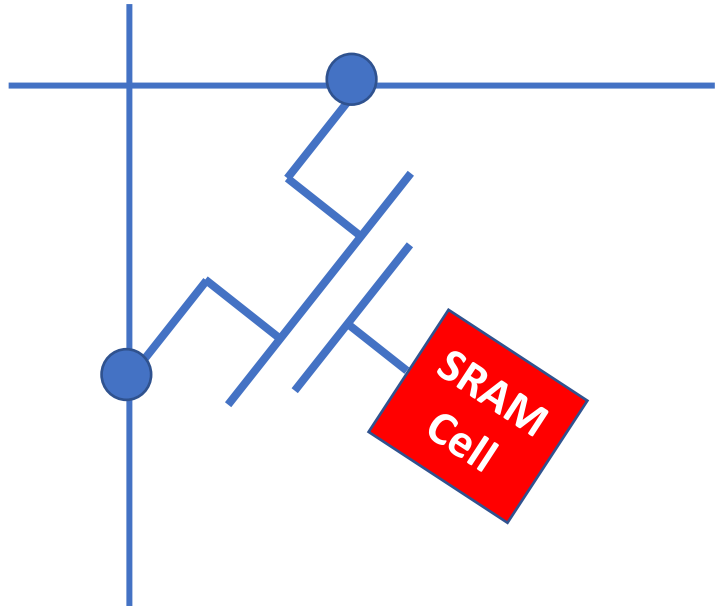
Interconnect Technology for Field Programming

EEPROM / FLASH



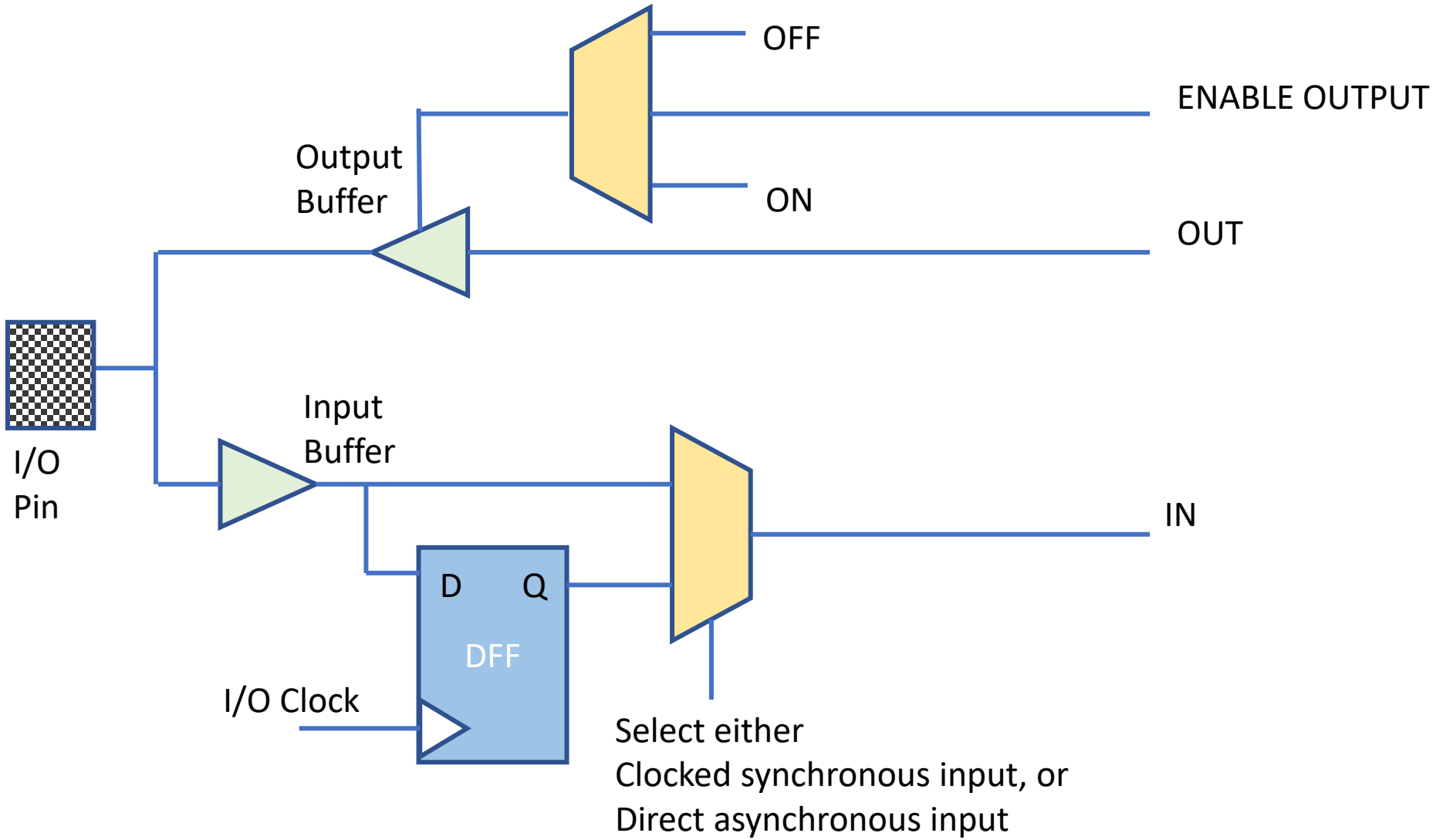
Floating Gate
Tunneling process
Used in EEPROM, USB Flash drive, etc.

SRAM



SRAM Cell is connected to Gate terminal
MOS Switch behaves as per stored value in SRAM

Concept of a Programmable I/O Block



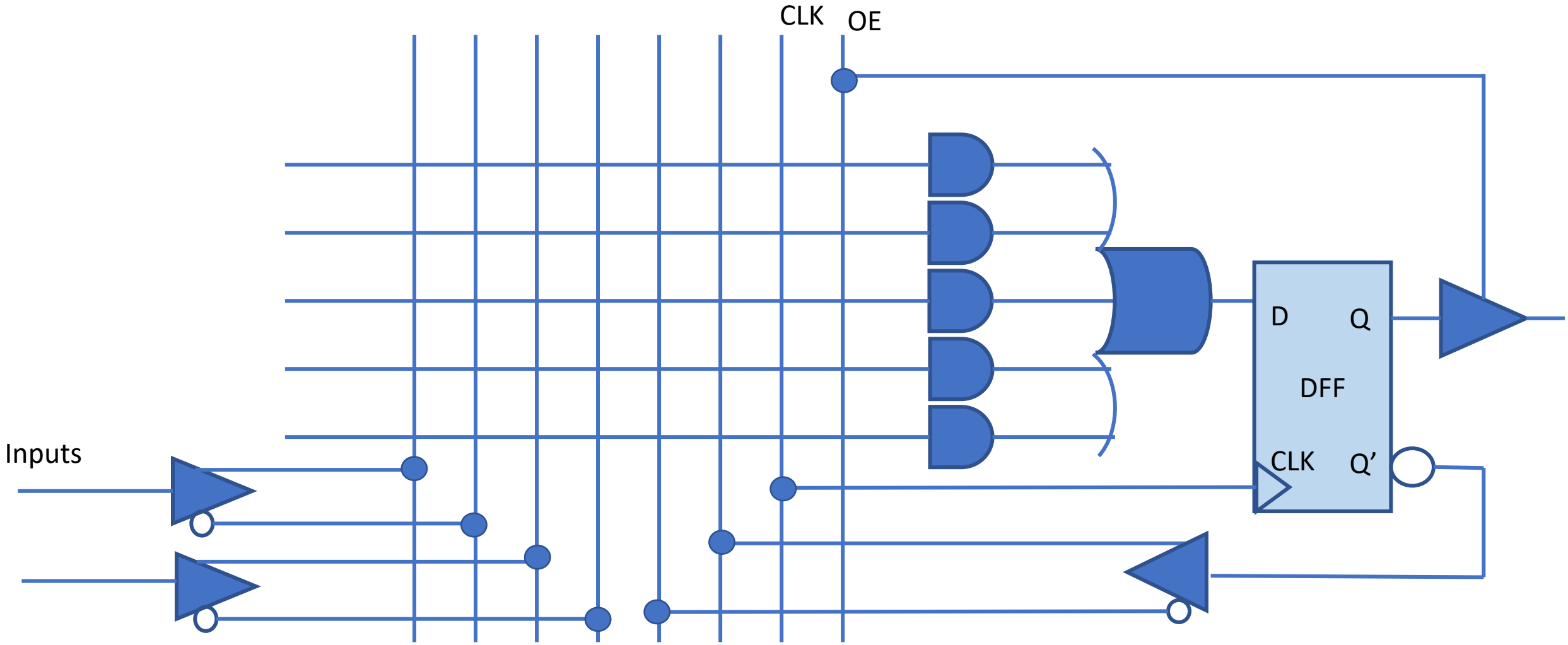
Introducing CPLD – Complex Programmable Logic Devices

Description of Basic (Registered) Macrocell

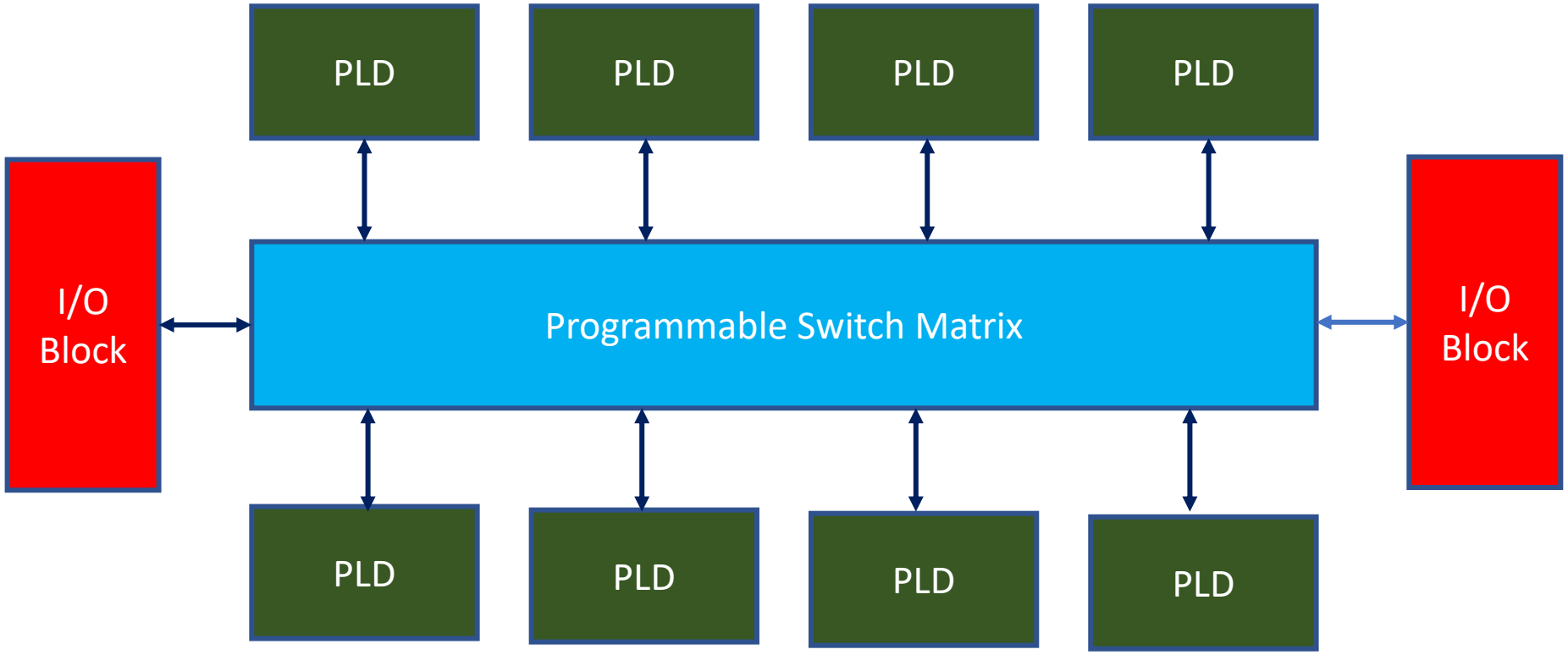
- Each section of an SPLD is called a macrocell that contains SOP combinational logic and an optional Flipflop
- A typical SPLD has from 8 to 10 macrocells within one chip
- All Flipflops are connected to common CLK input
- All three-state buffers at Flipflop output are controlled by a common OE input

Basic Macrocell Logic

PAL that includes a DFF is called a Registered PAL



Generic CPLD Configuration



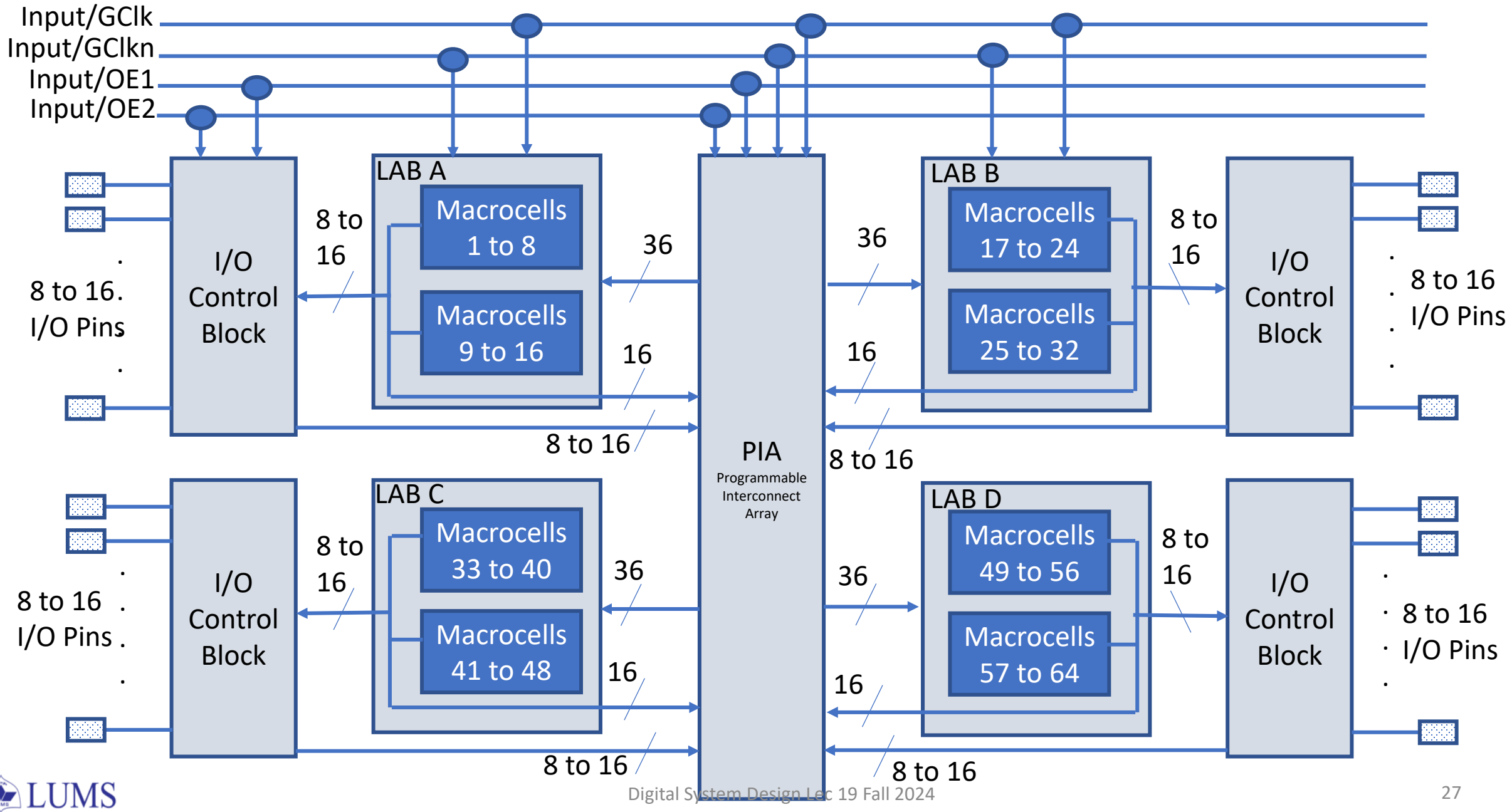
Description of CPLD

- Structured Array of PLD blocks
- Programmable On-Chip Interconnection Fabric
- Have higher number of inputs without much increase in area
- 100% connectivity between macrocells, BUT not all outputs of macrocells are connected to OUTPUT
- Wide Fan-In AND gates are used at INPUTS
- Outputs of macrocells can be routed within the chip to form more complex logic blocks
- The Interconnect Array selects signals from I/O blocks or macrocell outputs and connects them back to function block inputs
- The I/O blocks provide an interface between bidirectional physical I/O pins and the interior of the CPLD

Details of Generic CPLD Configuration

- Collection of individual PLD gate arrays on a single integrated circuit
- Each I/O pin is driven by a 3-state buffer and can be programmed to act as Input or Output pin
- Each PLD typically contains 8 to 16 macrocells
- If a macrocell has unused product terms, they can be used by nearby macrocells
- The outputs of macrocells can be routed to inputs of other macrocells to form complex multi-level logic functions
- Different manufactures offer variations in PLD design, programmable switching matrix and different types of I/O blocks

Altera 7000 Series CPLD Architecture



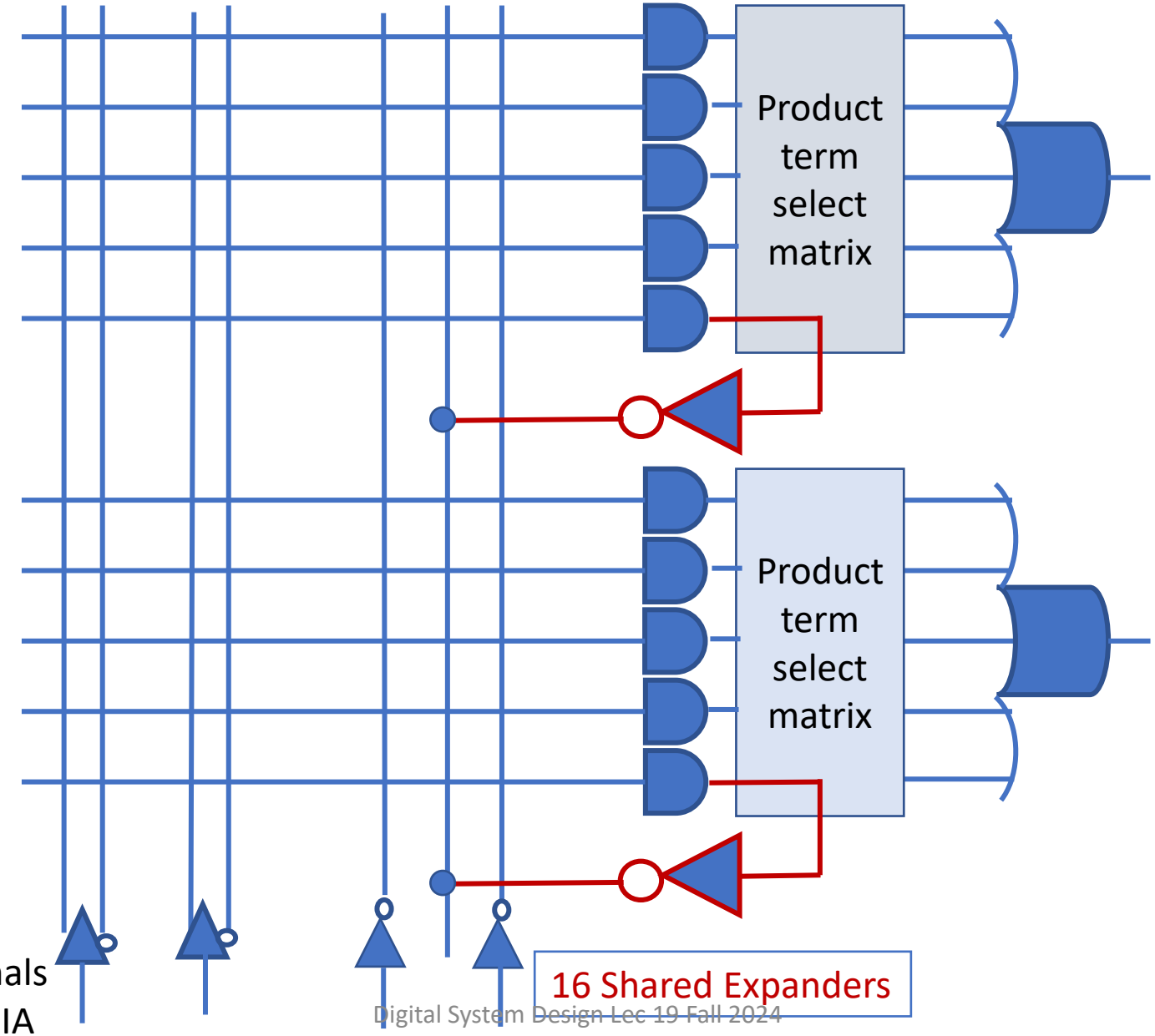
Details of Altera 7000 CPLD

- Floating gate EEPROM Configuration memory cells
- Architecture consists of an array of logic array blocks (**LAB**), programmable interconnect array (**PIA**) and an array of programmable I/O blocks
- Each LAB has 36 inputs and 16 outputs
- Each LAB consists of 16 macrocells providing both combinational and sequential logic
- PIA provides full connectivity between LAB and I/O Cells
- I/O Control block connects I/O Pins and PIA and LAB
- Global input clk (GCLK) and Global Clear (GCLR) connect to all macrocells
- Each macrocell can provide five product terms to its product-term-select matrix

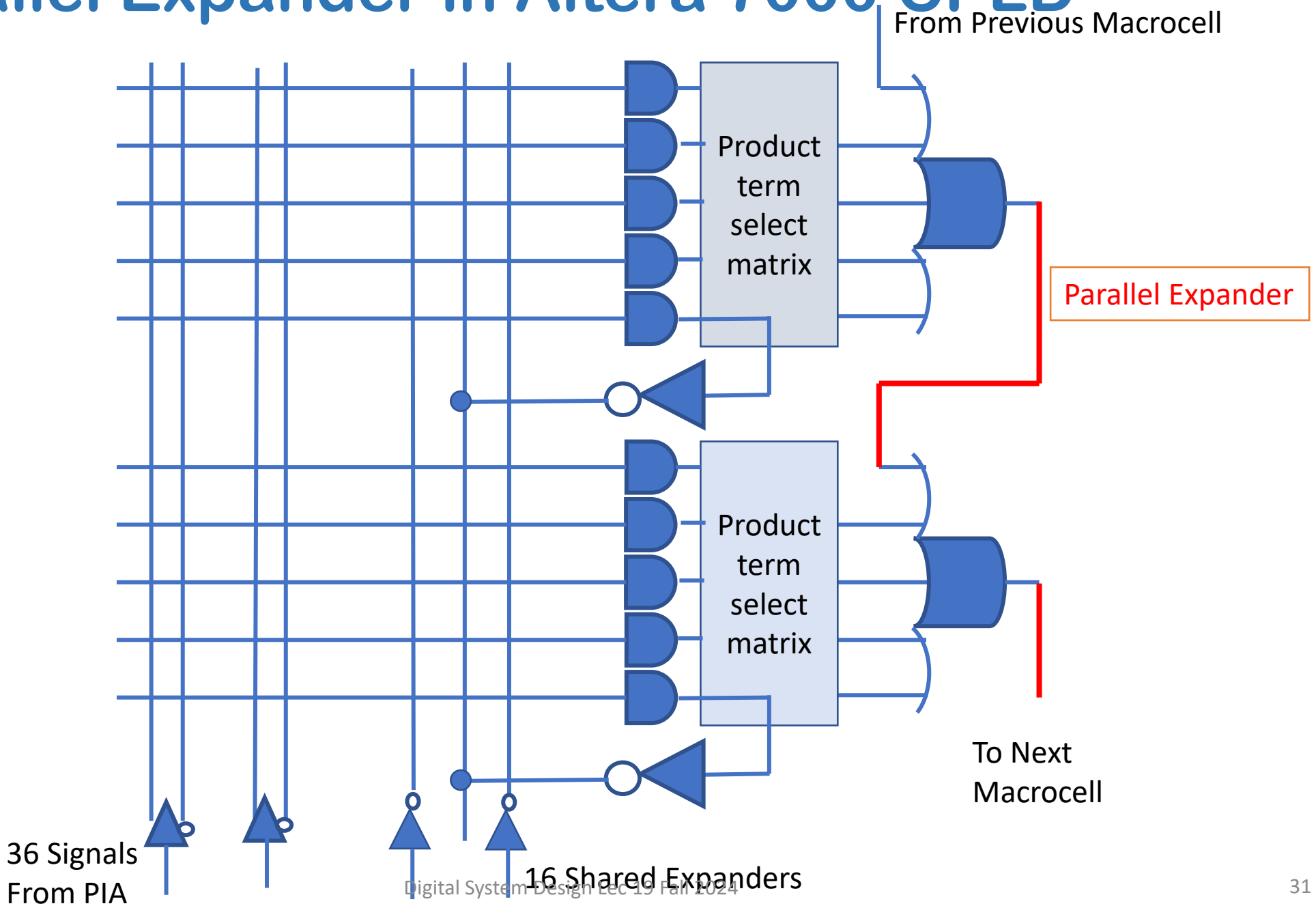
PIA and I/O

- The PIA provides full connectivity with predictable timing between LAB, dedicated inputs and I/O Pins
- The I/O Control block establishes connectivity between I/O Pins and PIA and LABs
- From 8 to 16 LAB outputs can be programmed to route through I/O Pins; and from 8 to 16 I/O Pins can be programmed to route through the I/O Control block to the PIA
- Altera architecture uses a PIA to connect LABs and I/O Pins. All signals are available throughout the device. The timing is thus predictable. The alternative is ‘Channel-Routed Architecture’ that is more denser but the timing is un-predictable as delays are routing-dependent

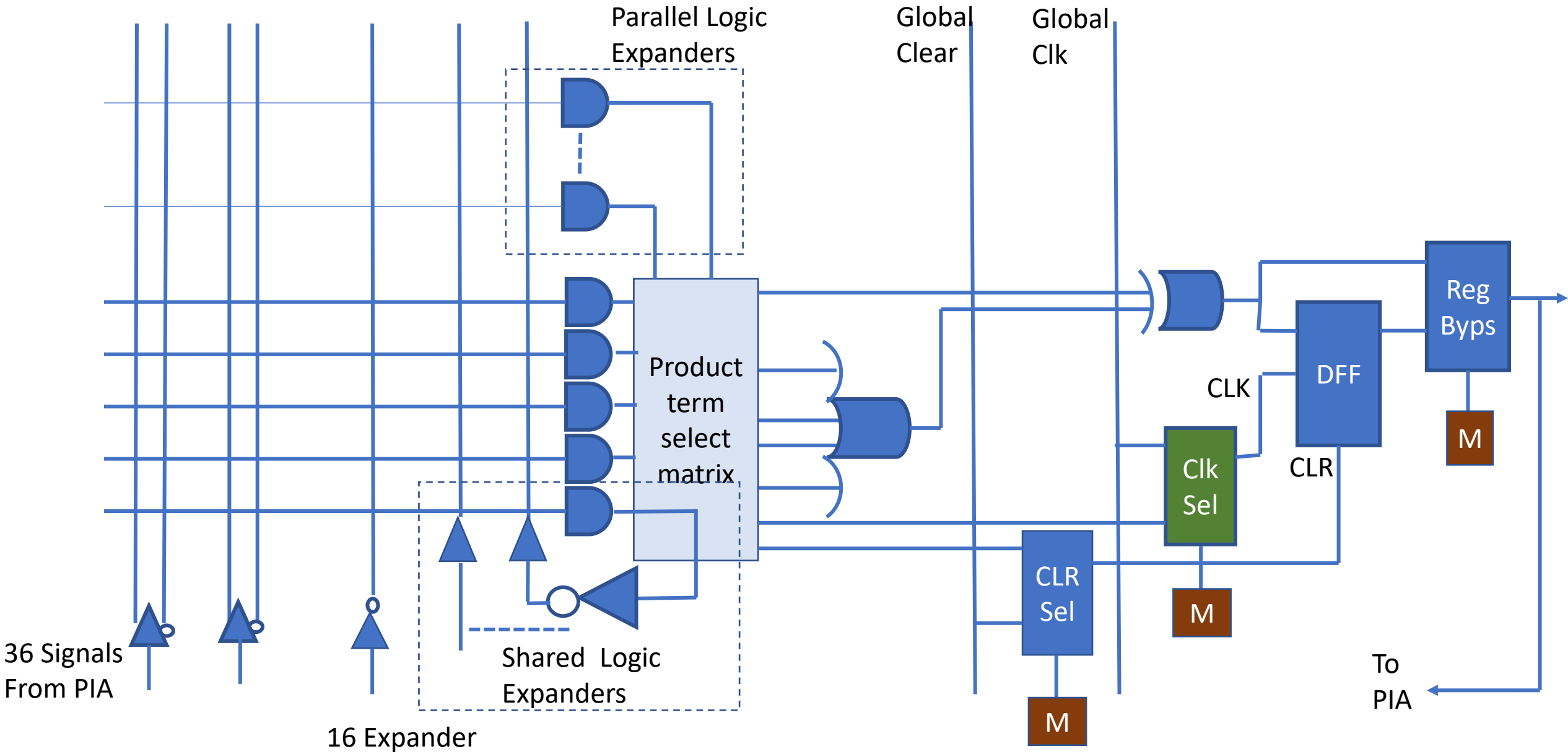
Shareable Expander in Altera 7000 CPLD



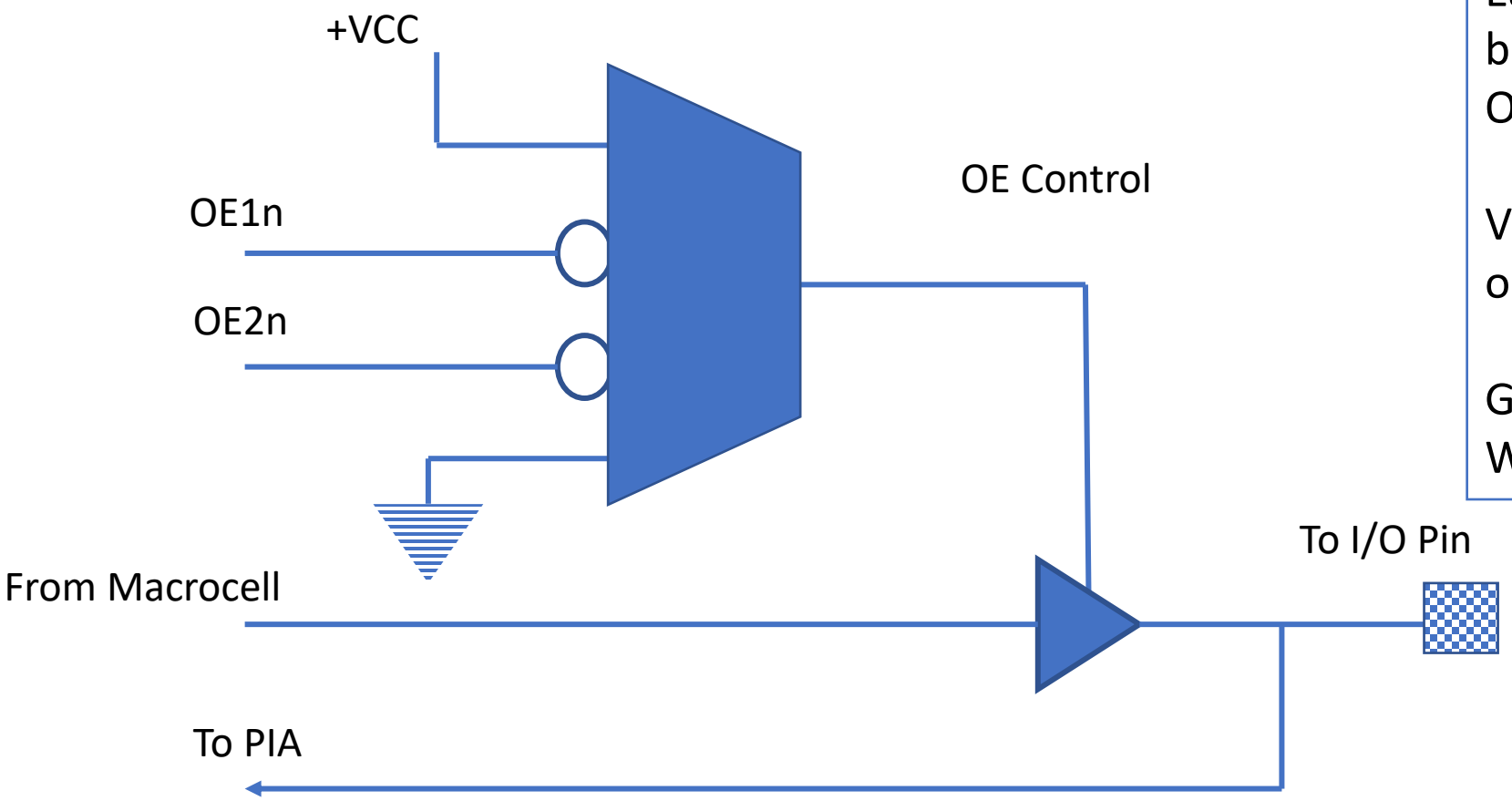
Parallel Expander in Altera 7000 CPLD



Altera 7000 Series Macrocell Architecture



Altera 7000 Series I/O Control Block

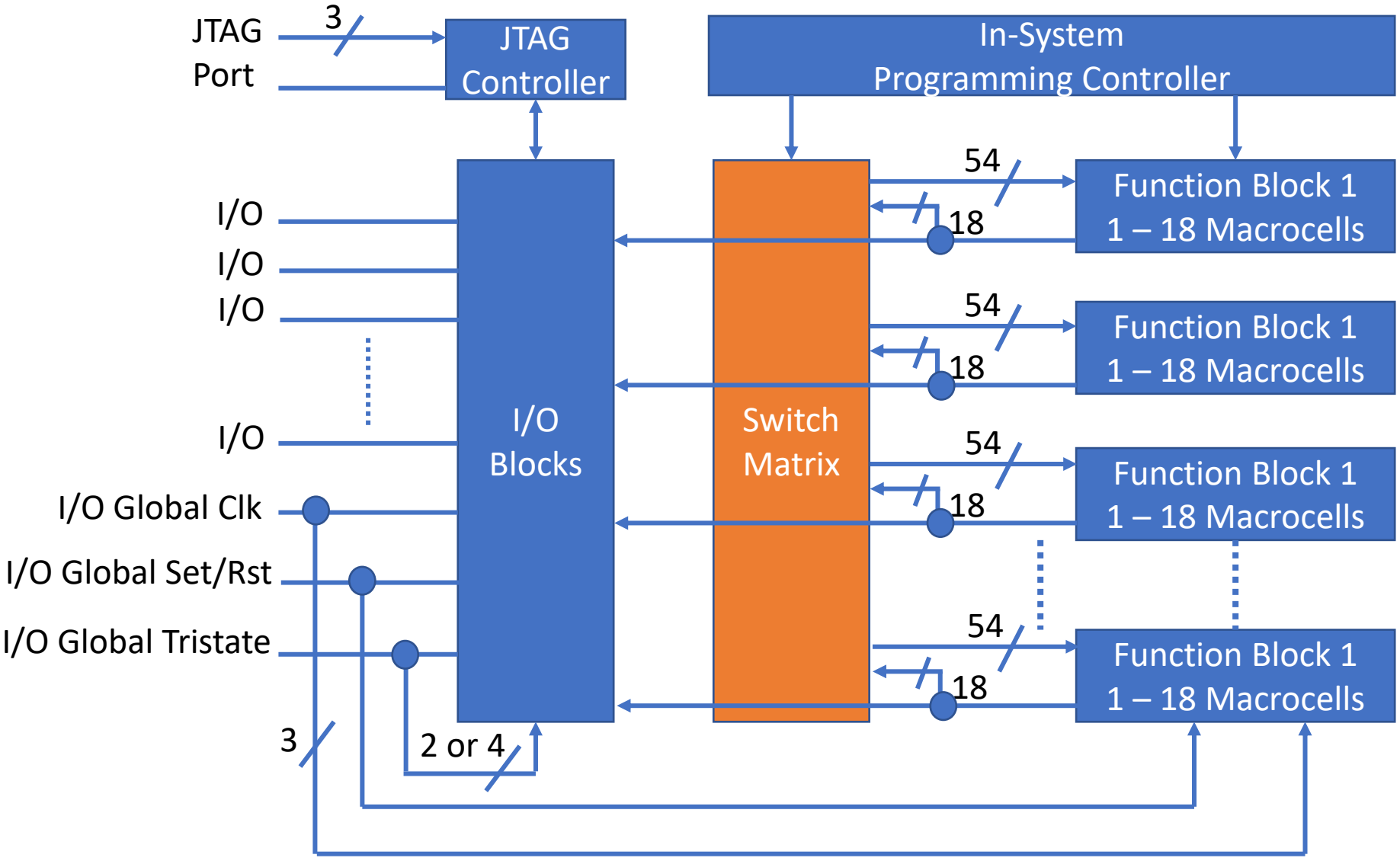


Each I/O Pin can be configured to be dedicated input pin, output pin Or bi-dir under control of OE1, OE2.

VCC will hardwire the I/O pin to output of macrocell.

GND will isolate macrocell and I/O pin Will be an input pin only.

Xilinx XC9500 CPLD Architecture



Details of Xilinx 9500 CPLD

- Flash based EEPROM Technology
- Comprises Few (4) Functional Blocks
- Each functional block contains 18 independent macrocells
- Each functional block has 54 inputs and 18 outputs
- Product-term-allocator allocates upto 90 product terms in each macrocell in a functional block to form SOP expressions
- Each macrocell can receive five direct product terms from the AND array and up to 10 more product terms can be made available from other un-committed product terms in other macrocells from same functional block
- Partial SOP terms can be combined from several macrocells
- Each macrocell can be independently configured for combinational or sequential functionality

Xilinx XC9500 Macrocell Architecture