Lecture 27

EE 421 / CS 425

Digital System Design

Fall 2024

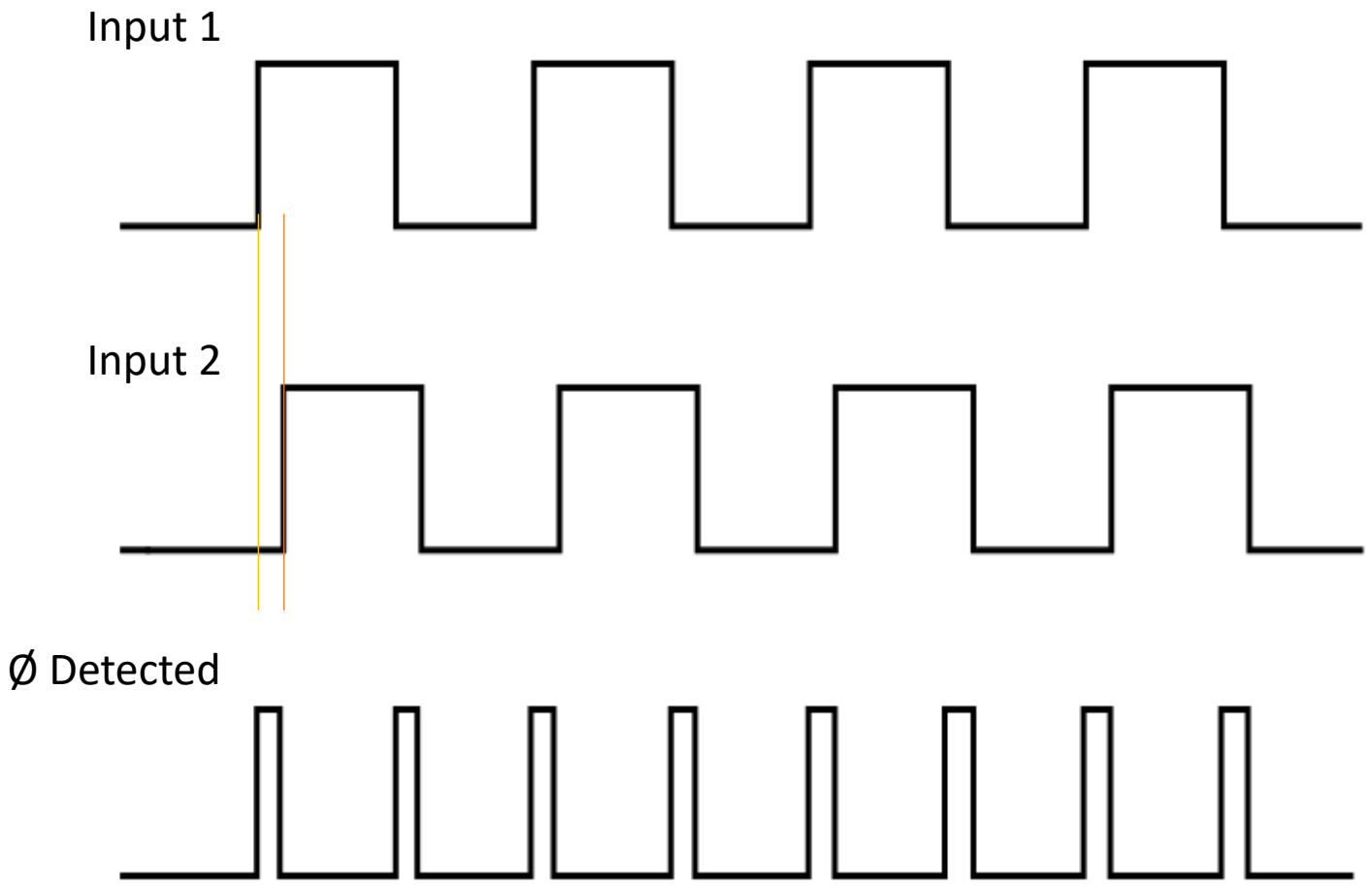
Quiz 6 next lecture

Shahid Masud

Topics

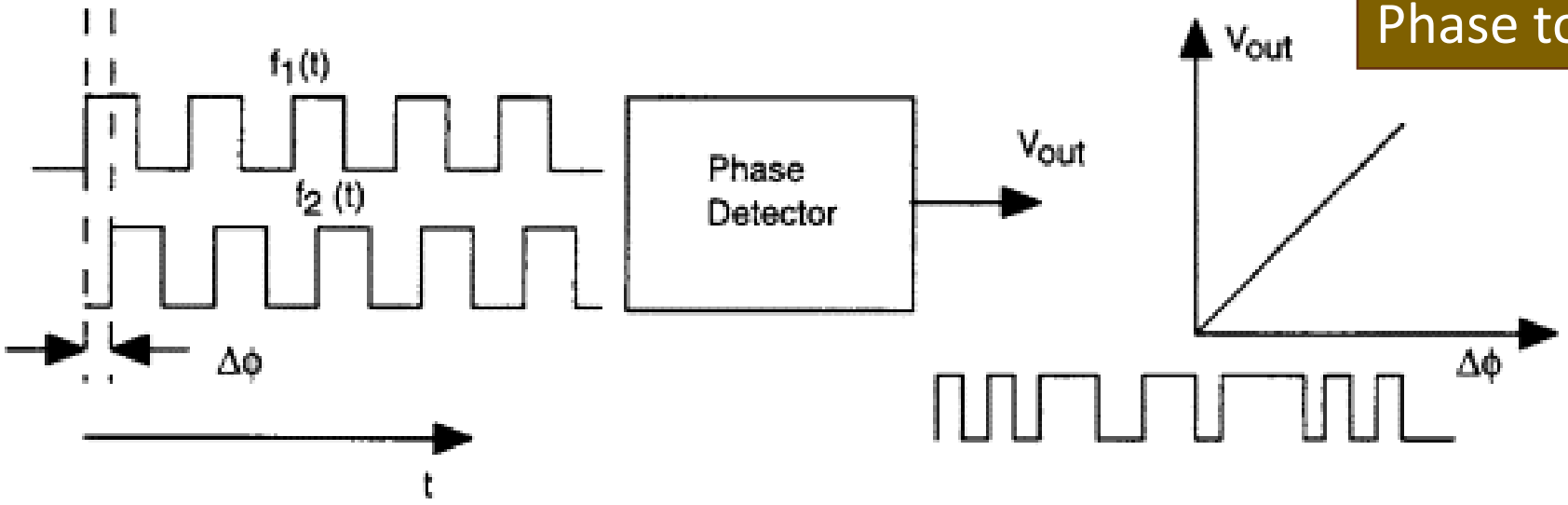
- Phase Detector, PLL, DPLL and their Applications
- Using LUT for Speech Recording and Playback
  - Sample Rate
  - Different Sound Effects
- Direct Digital Frequency Synthesis
  - Concept
  - Lookup Table Values
  - Phase Accumulator
  - DAC and Output Filter
- Asynchronous Sequential Circuits
- Types of Asynchronous Circuits:
  - Pulse mode Asynchronous Circuits
  - Fundamental Mode Asynchronous Circuits

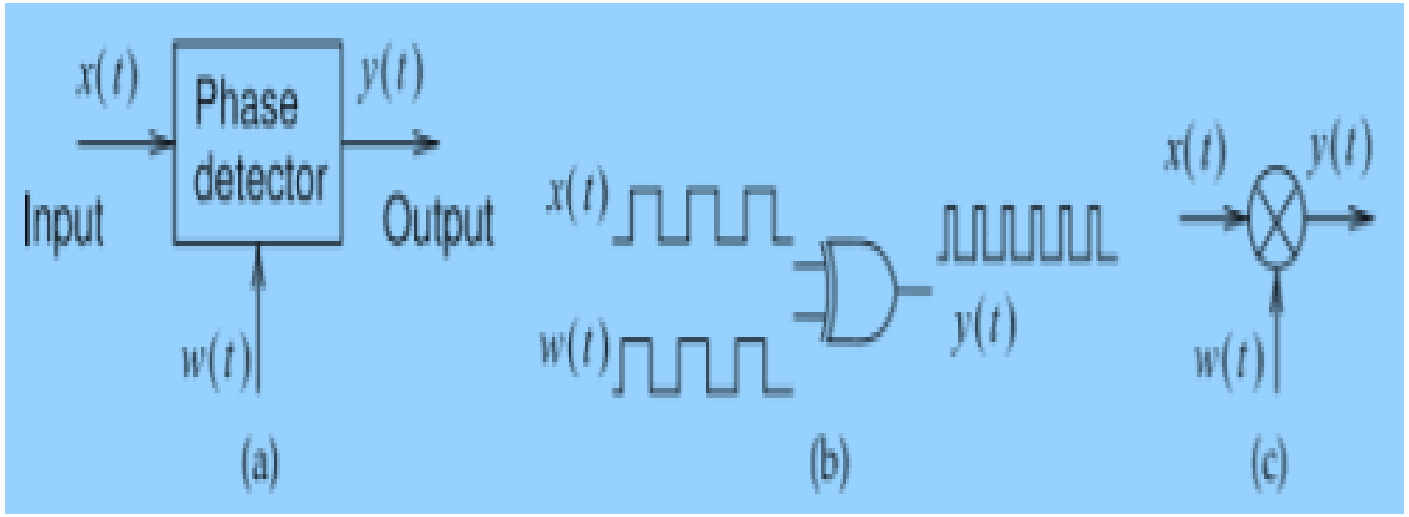
Phase Detector 1



Phase Detector 2

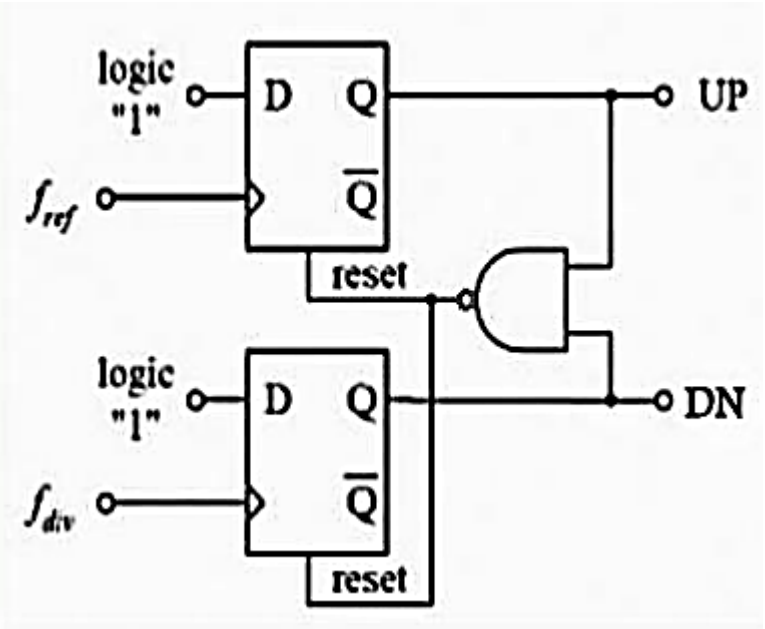
Phase to Voltage Conversion

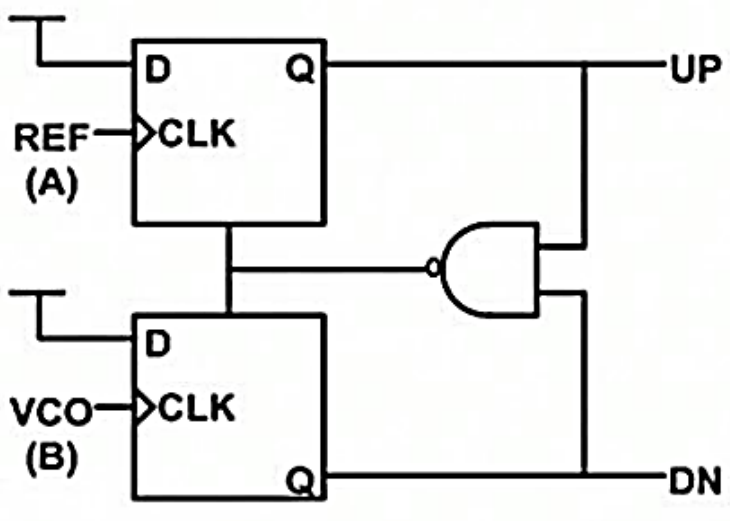


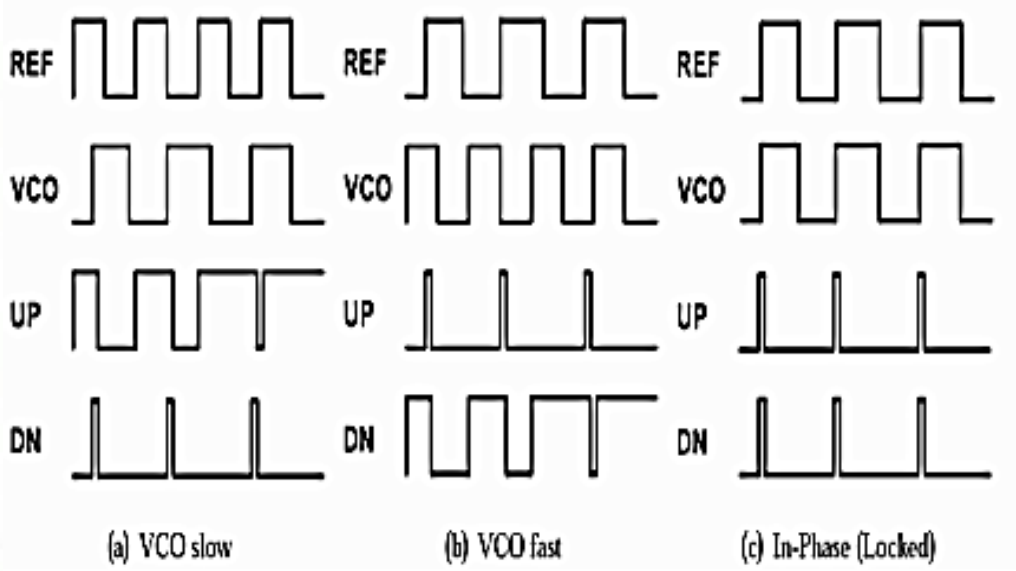


XOR based Phase Detection

Phase Detector 3







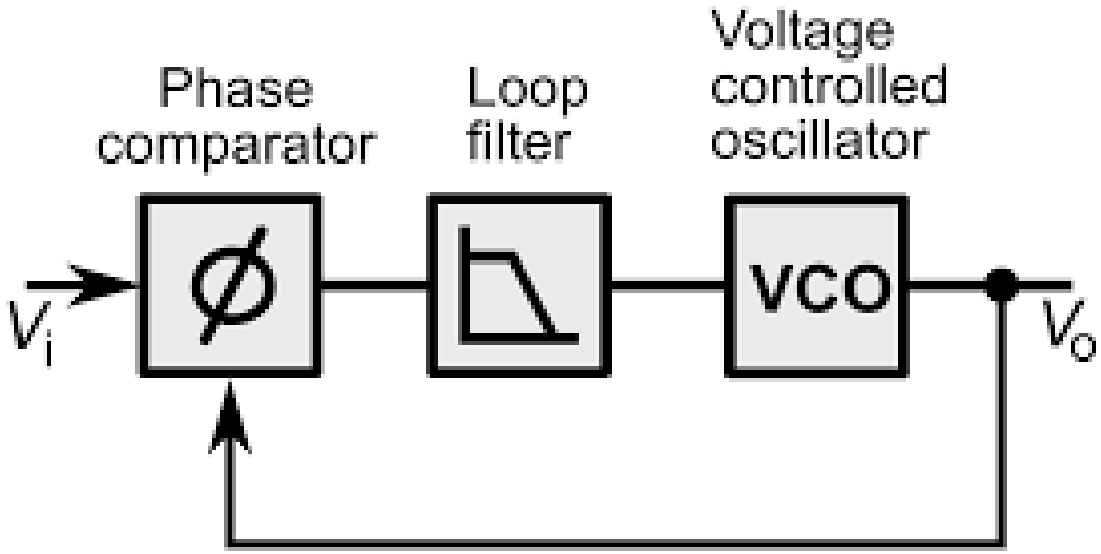
Nand Based Phase Detector and Possible Outputs

Reference: T. SUPRAJA, K. BABURAO,K. Kishore, R. Reddy, International Journal of Computer Application (2250-1797) Volume 7– No.4, July-August 2017

Phase Locked Loops PLL

Minimize Phase Error

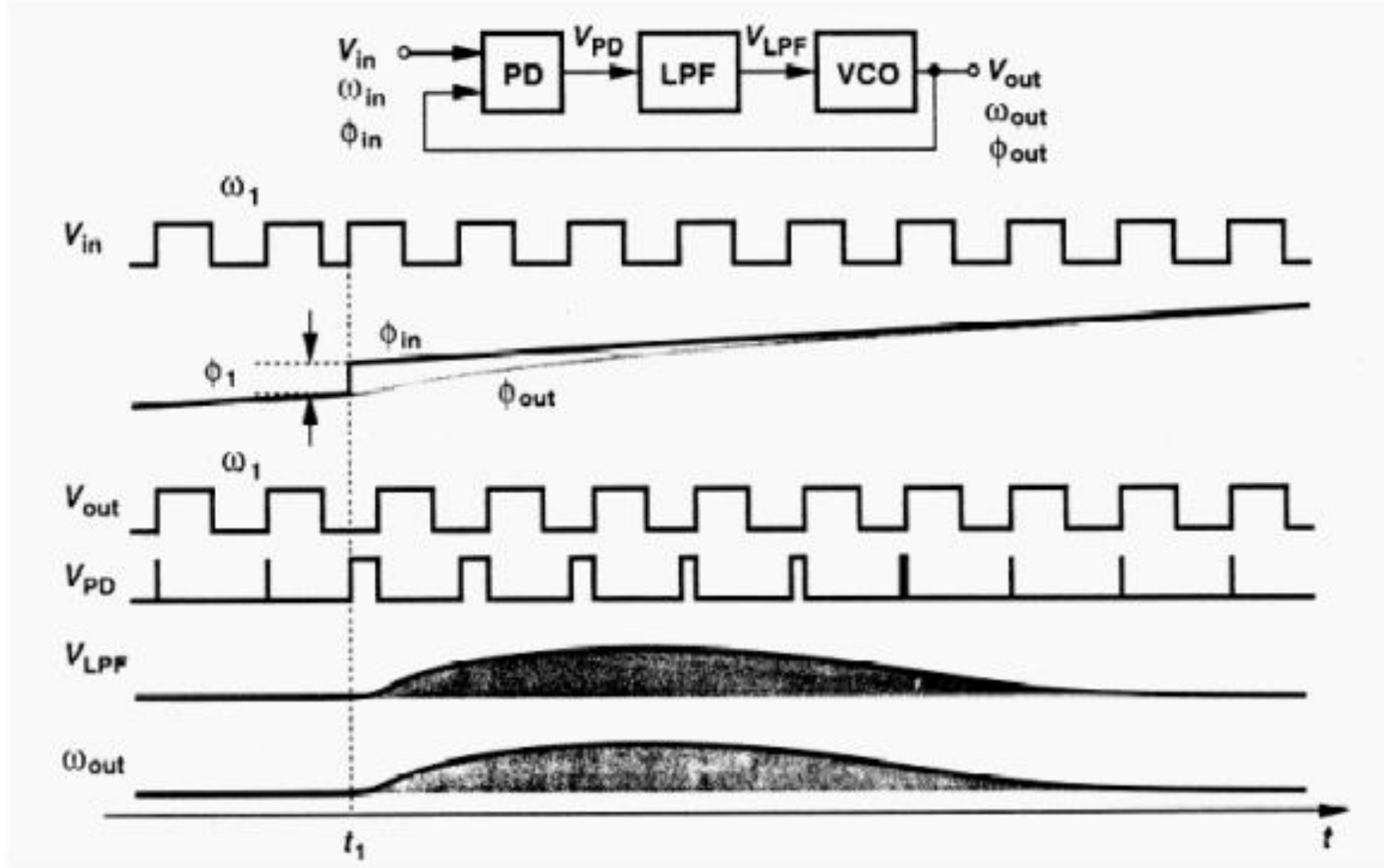
Simple Analog PLL



Three Components of PLL:

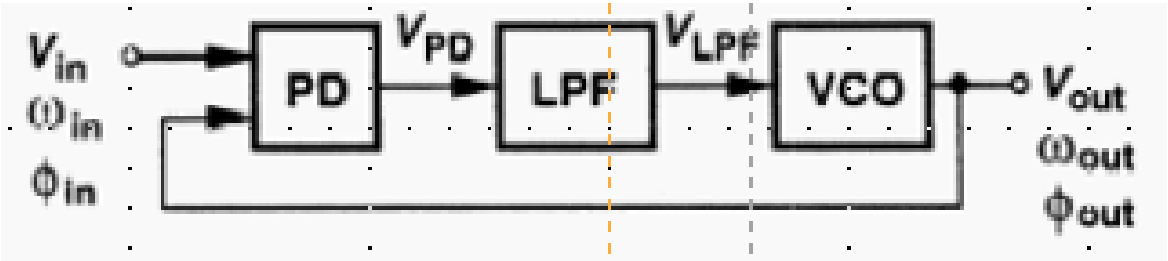
1. Phase Comparator
2. Loop Filter
3. Voltage Controlled Oscillator

PLL Operation



(Figure from B. Razavi, Ch. 15, op. cit.)

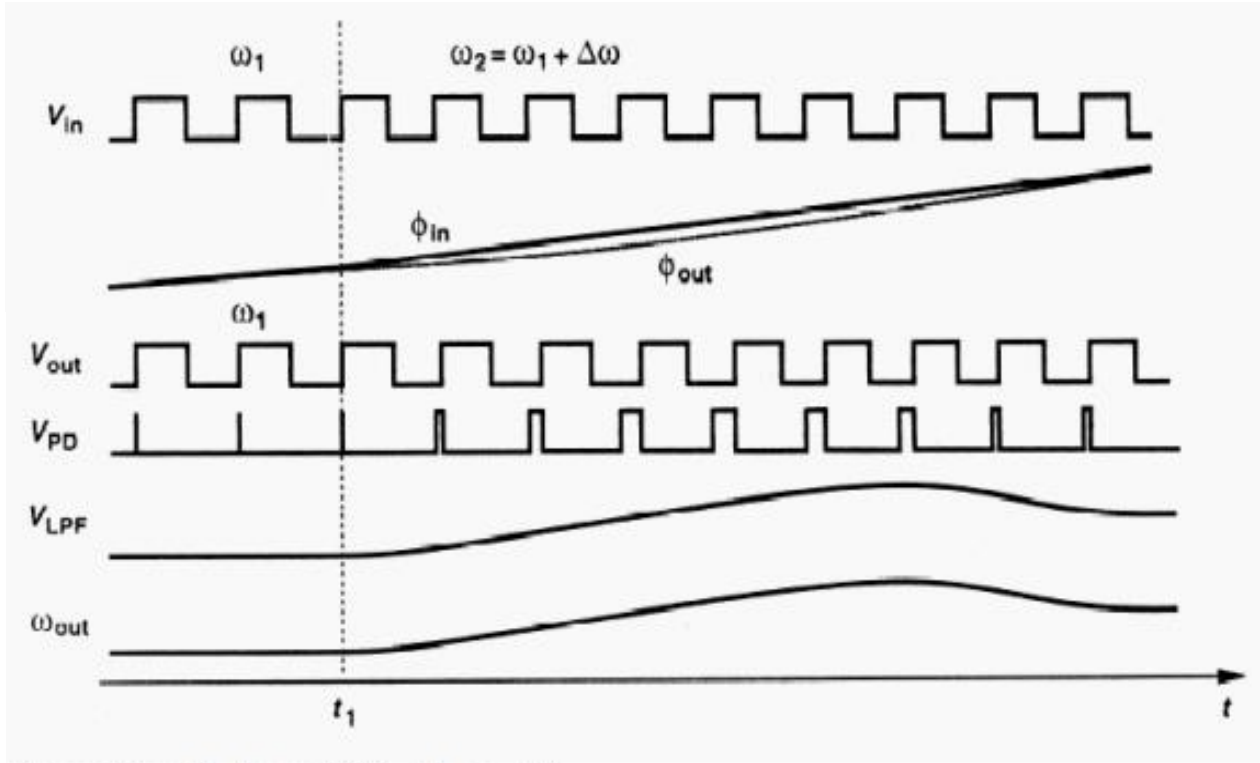
PLL Behavior with a step change in Phase



Now, let's investigate the behavior during a frequency step:

$$\omega_2 = \omega_1 + \Delta\omega$$

The frequency step will cause the phase difference to grow with time since a frequency step is a phase ramp. This in turn causes the control voltage, V_{cont}, to increase, moving the VCO frequency up to catch up with the input reference signal. In this case, we have a permanent change in ω_{out} since a higher V_{cont} is required to sustain a higher ω_{out}.



(Figure from B. Razavi, Ch. 15, op. cit.)

PLL Mechanism – for those into Maths

Following equation shows that Phase accumulated over a certain time span is the result of integration of frequency over the same time period.

Phase accumulate over time — frequency

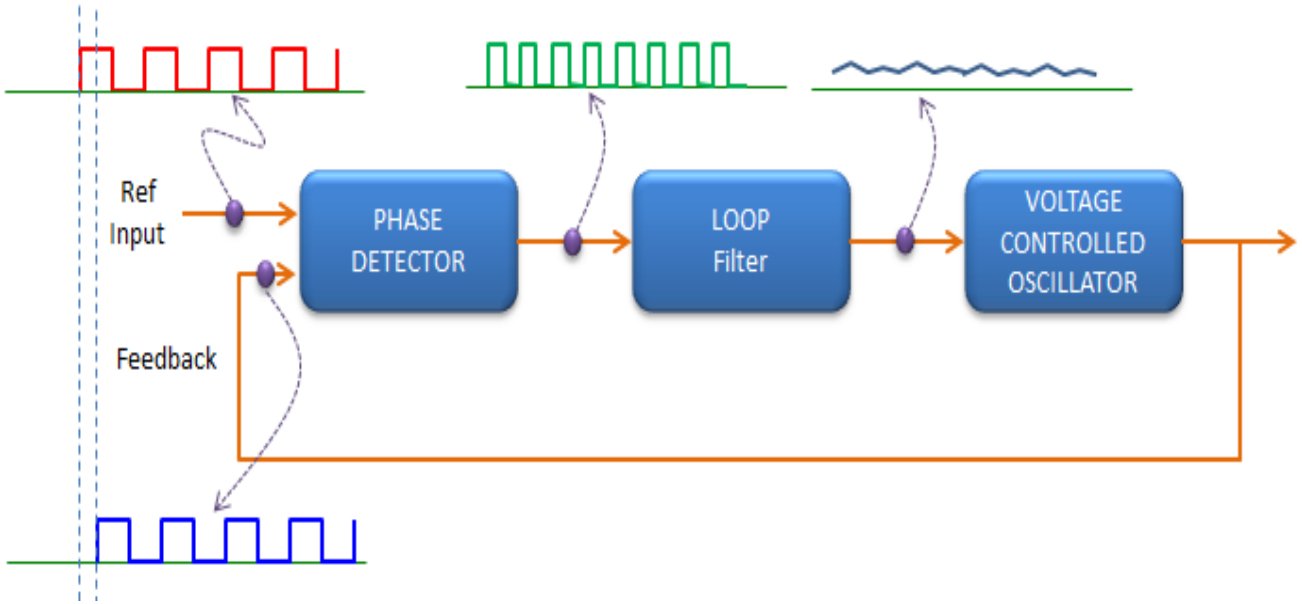
$$\Phi = \int \omega(t)dt$$

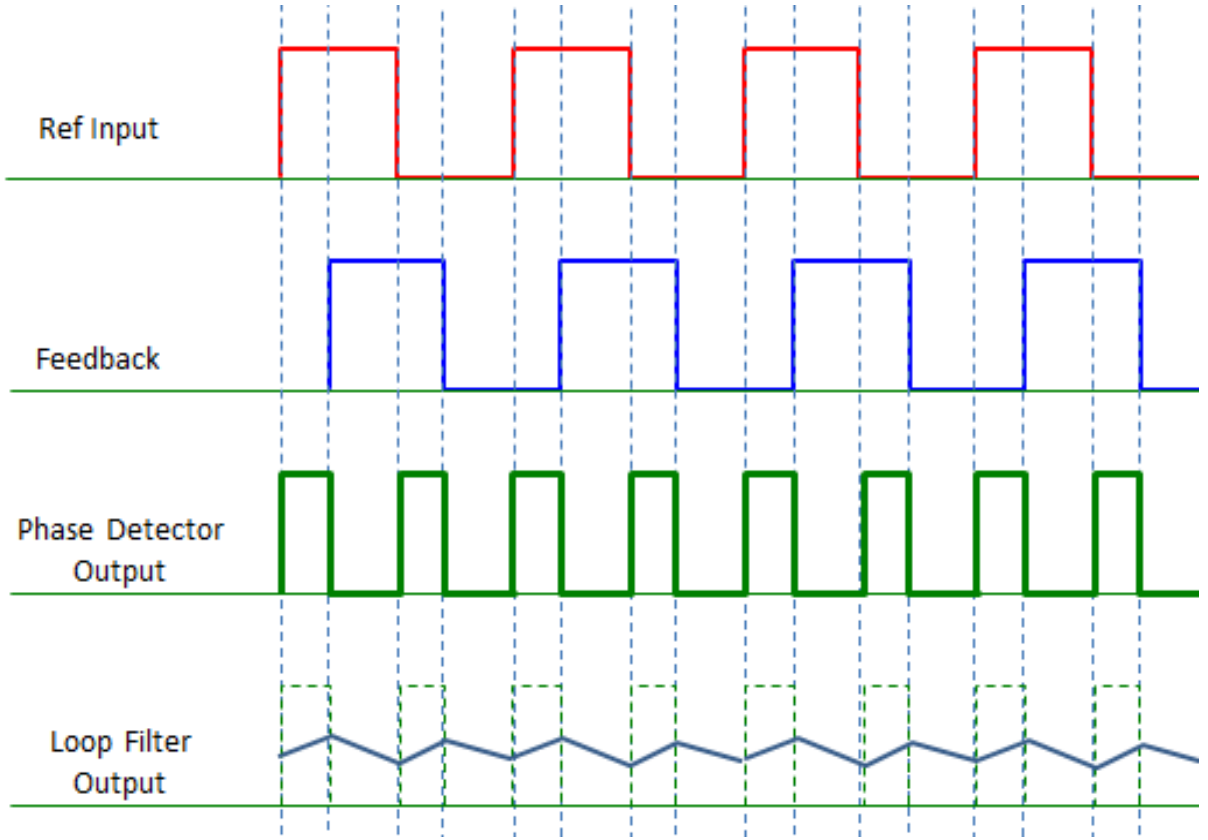
Following equation shows that phase difference between two signal (starting with the same phase) after a certain time span.

Phase difference after Δt — Frequency difference between two waves

$$\Delta\Phi = \Delta\omega \times \Delta t$$

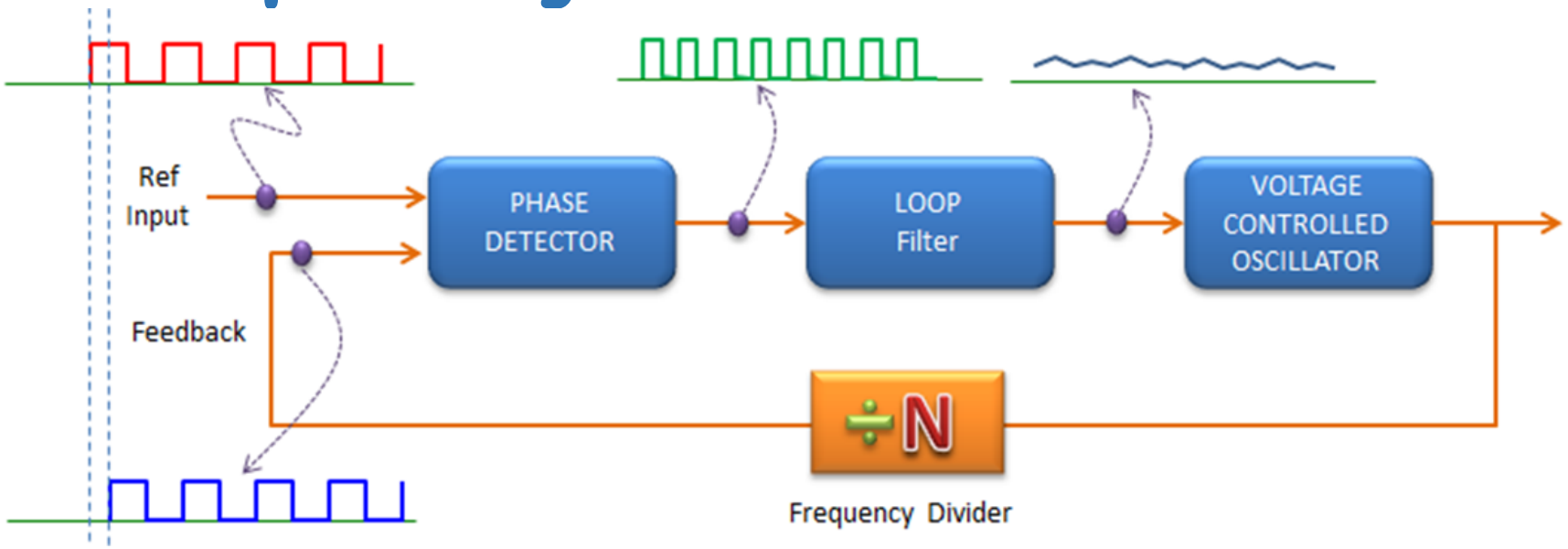
PLL Waveforms

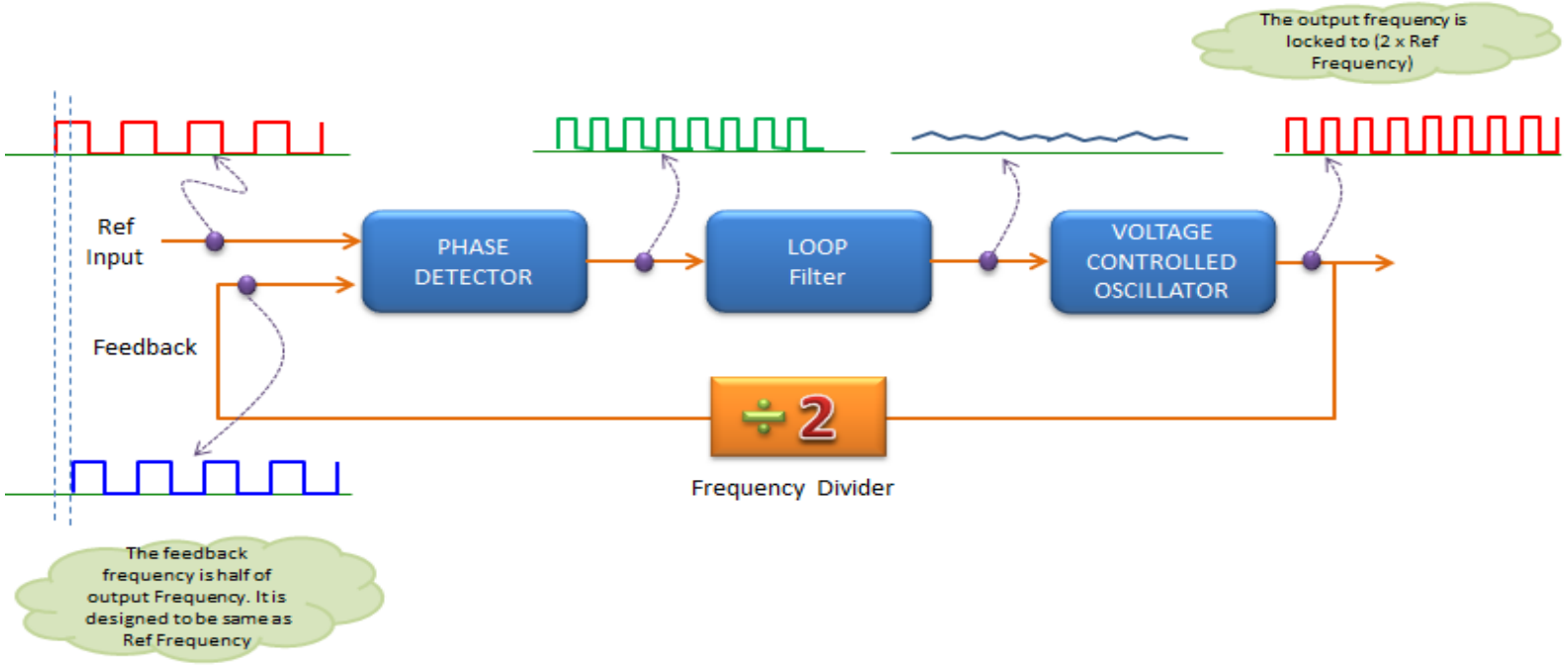




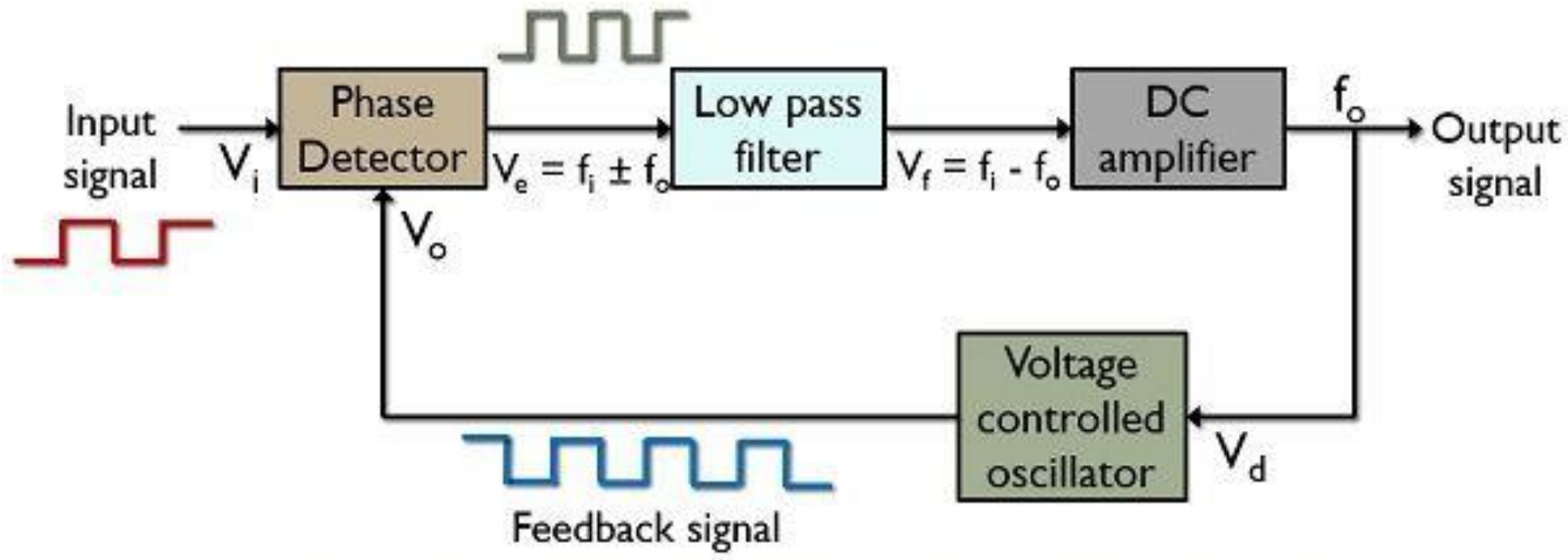
PLL with Frequency Divider

PLL with Frequency Divider





Digital PLL


Input signal
V_i
Phase Detector
$V_e = f_i \pm f_o$
Low pass filter
$V_f = f_i - f_o$
DC amplifier
f_o
Output signal
V_o
Voltage controlled oscillator
V_d
Feedback signal

DPLL Application

absence of a clock signal makes this difficult. The DPLL performs the function of generating a clock signal, which is locked or synchronized with the incoming signal. The generated clock signal of the receiver clocks the shift register and thus recovers the data. This application of a DPLL is often termed *a clock-recovery circuit* or *bit synchronization circuit*.

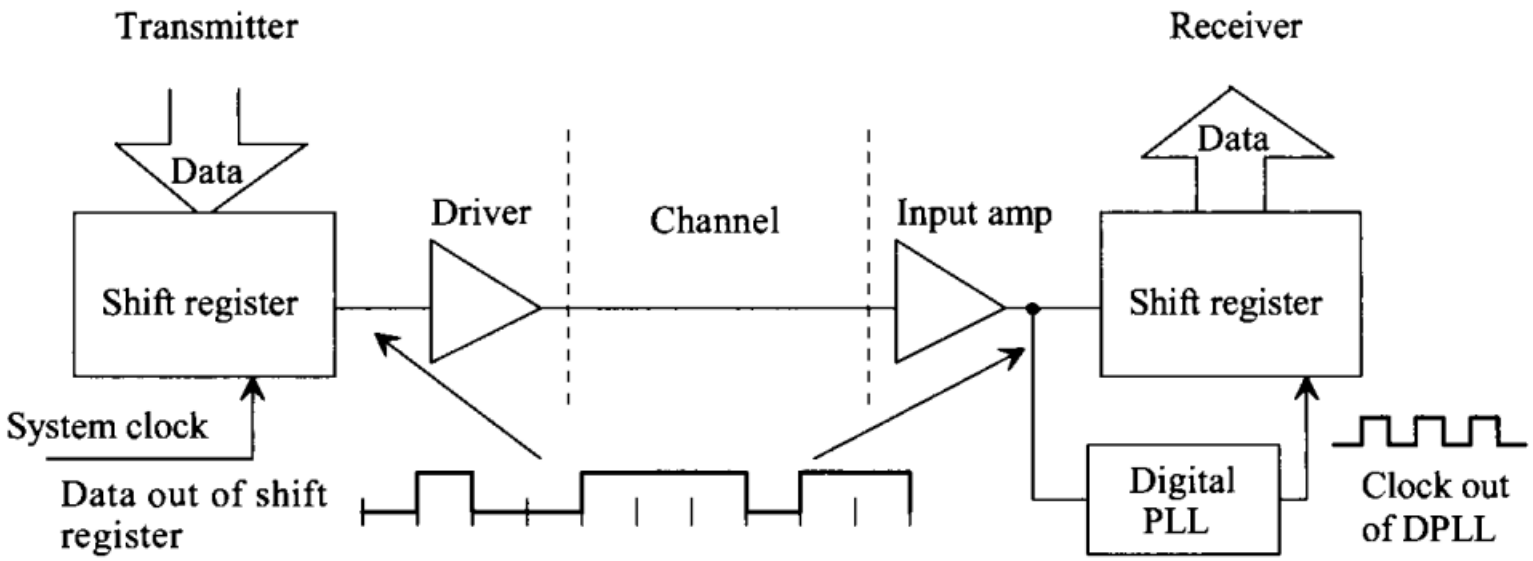


Figure 19.1 Block diagram of a communication system using a DPLL for the generation of a clock signal.

DPLL Design

A more detailed picture of the incoming data and possible clock signals out of the DPLL are shown in Fig. 19.2. The possible clock signals are labeled XOR *clock* and PFD (phase frequency detector) *clock*, corresponding to the type of phase[2] detector (PD) used. For the XOR PD, the rising edge of the clock occurs in the center of the data, while for the PFD, the rising edge occurs at the beginning of the data. The phase of the clock signal is determined by the PD used[3].

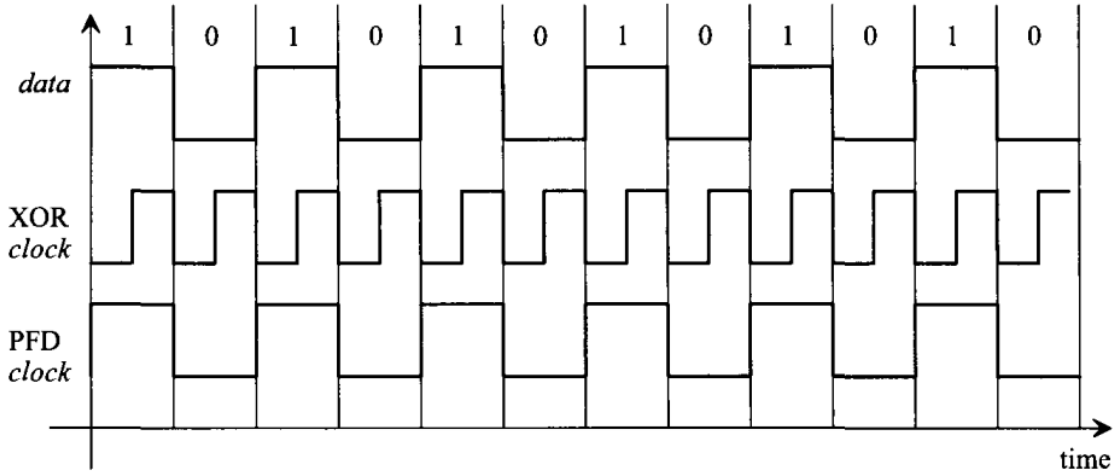


Figure 19.2 Data input to DPLL in lock and possible clock outputs using the XOR phase detector and PFD.

A block diagram of a DPLL is shown in Fig. 19.3. The PD generates an output signal proportional to the time difference between the *data in* and the divided down clock, *dclock*. This signal is filtered by a loop filter. The filtered signal, V_{inVCO}, is connected to the input of a voltage-controlled oscillator (VCO). Each one of these blocks is discussed in detail in the following sections. Once each block is understood, we will put them together and discuss the operation of the DPLL.

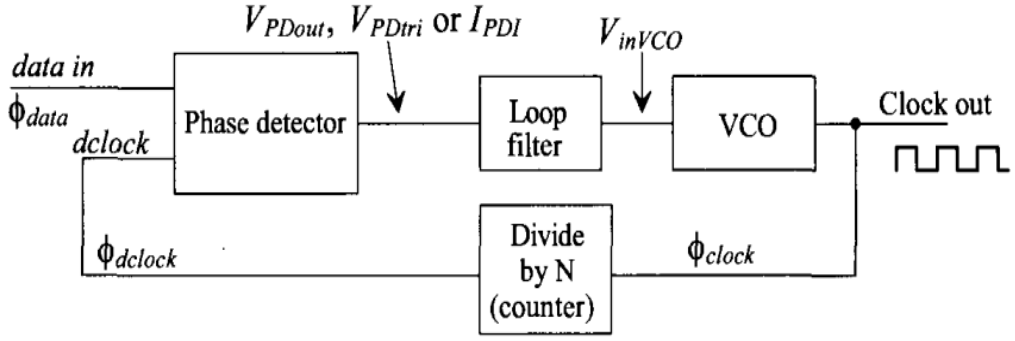


Figure 19.3 Block diagram of a digital phase-locked loop.

An Example Voltage Controlled Oscillator

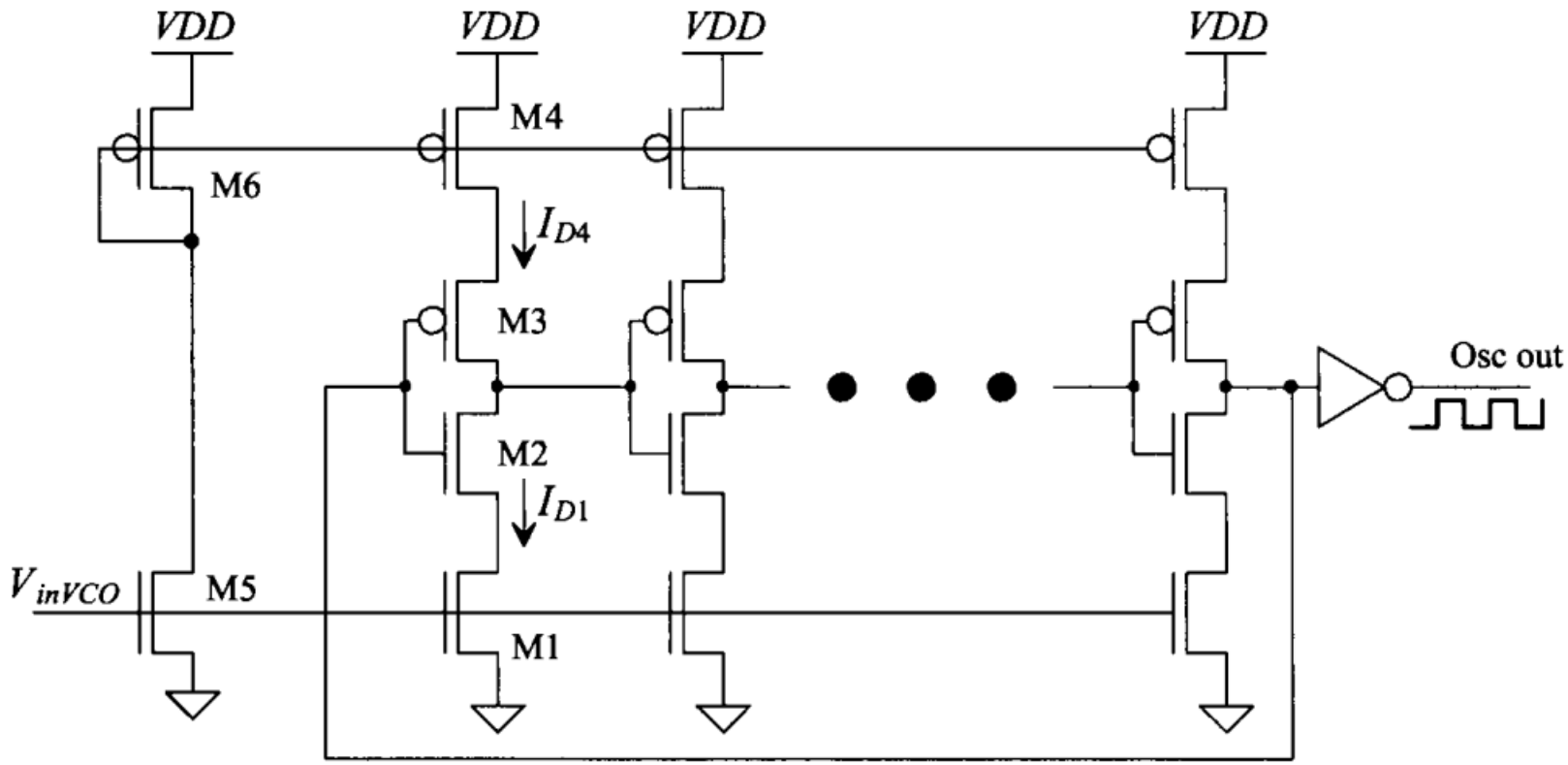


Figure 19.14 Current-starved VCO.

CD4046B PLL Chip

CD4046B PLL Technical Description

Figure 2 shows a block diagram of the CD4046B, which has been implemented on a single monolithic integrated circuit. The PLL structure consists of a low-power, linear VCO and two different phase comparators, having a common signal-input amplifier and a common comparator input. A 5.2-V Zener diode is provided for supply regulation, if necessary. The VCO can be connected either directly or through frequency dividers to the comparator input of the phase comparators. The LPF is implemented through external parts because of the radical configuration changes from application to application and because some of the components cannot be integrated. The CD4046B is available in 16-lead ceramic dual-in-line packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), 16-lead small outline package (NSR suffix) and in chip form (H suffix).

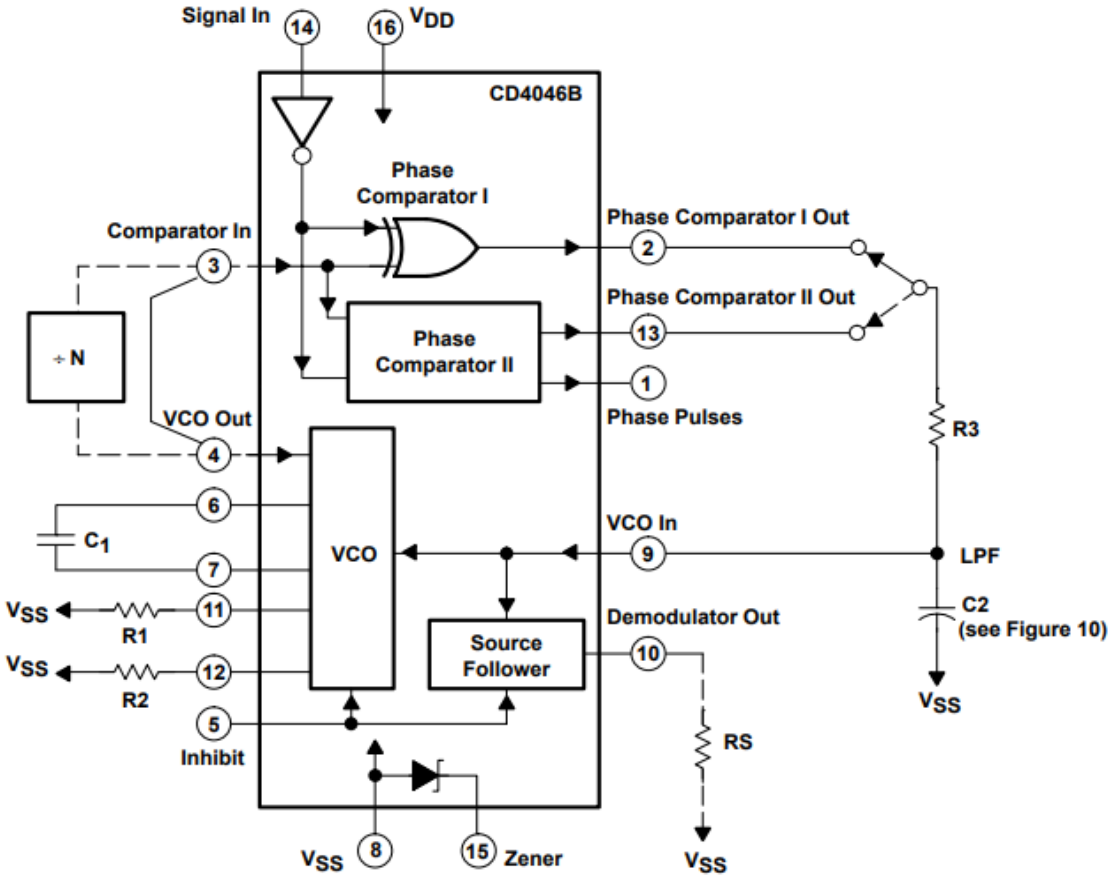
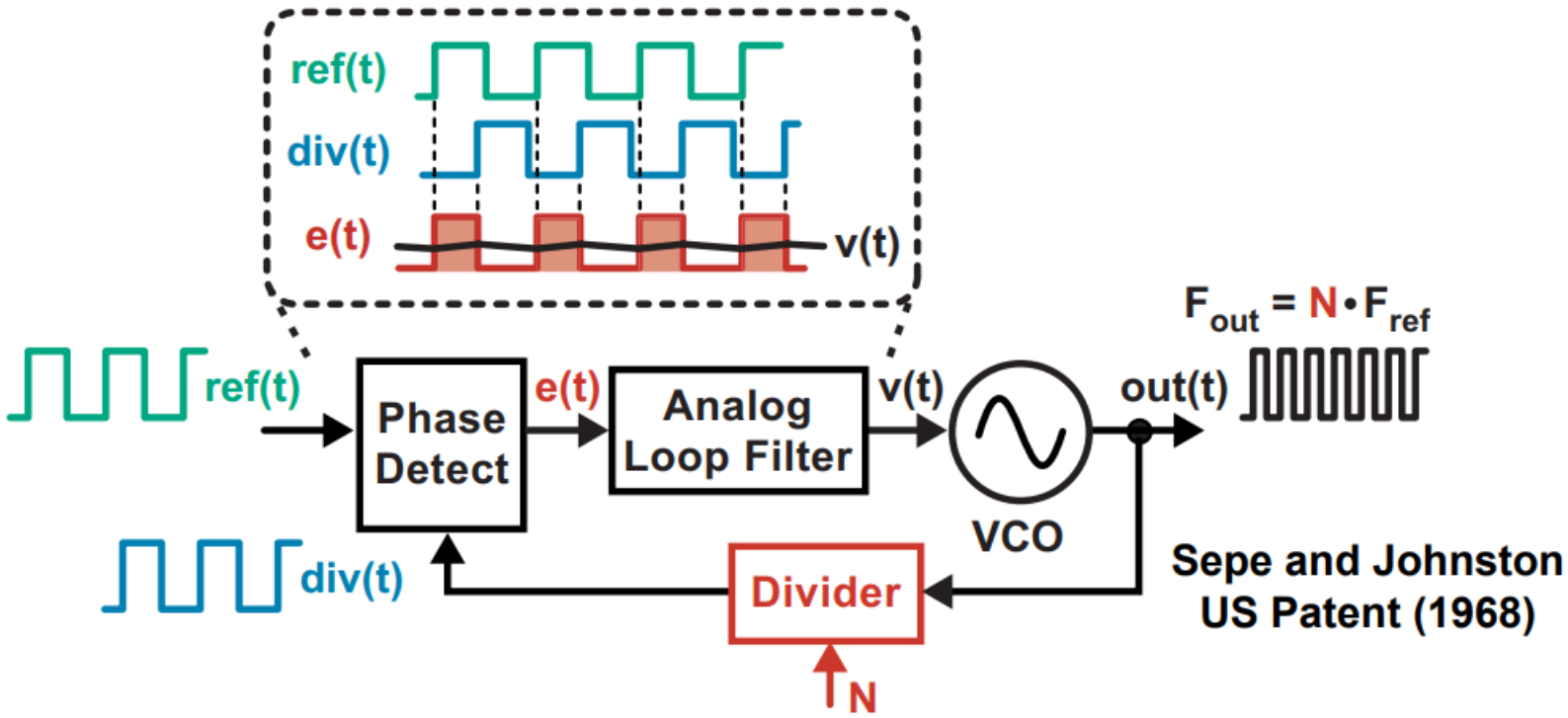


Figure 2. CD4046B Block Diagram

PLL Based Synthesizer

Integer-N Frequency Synthesizer

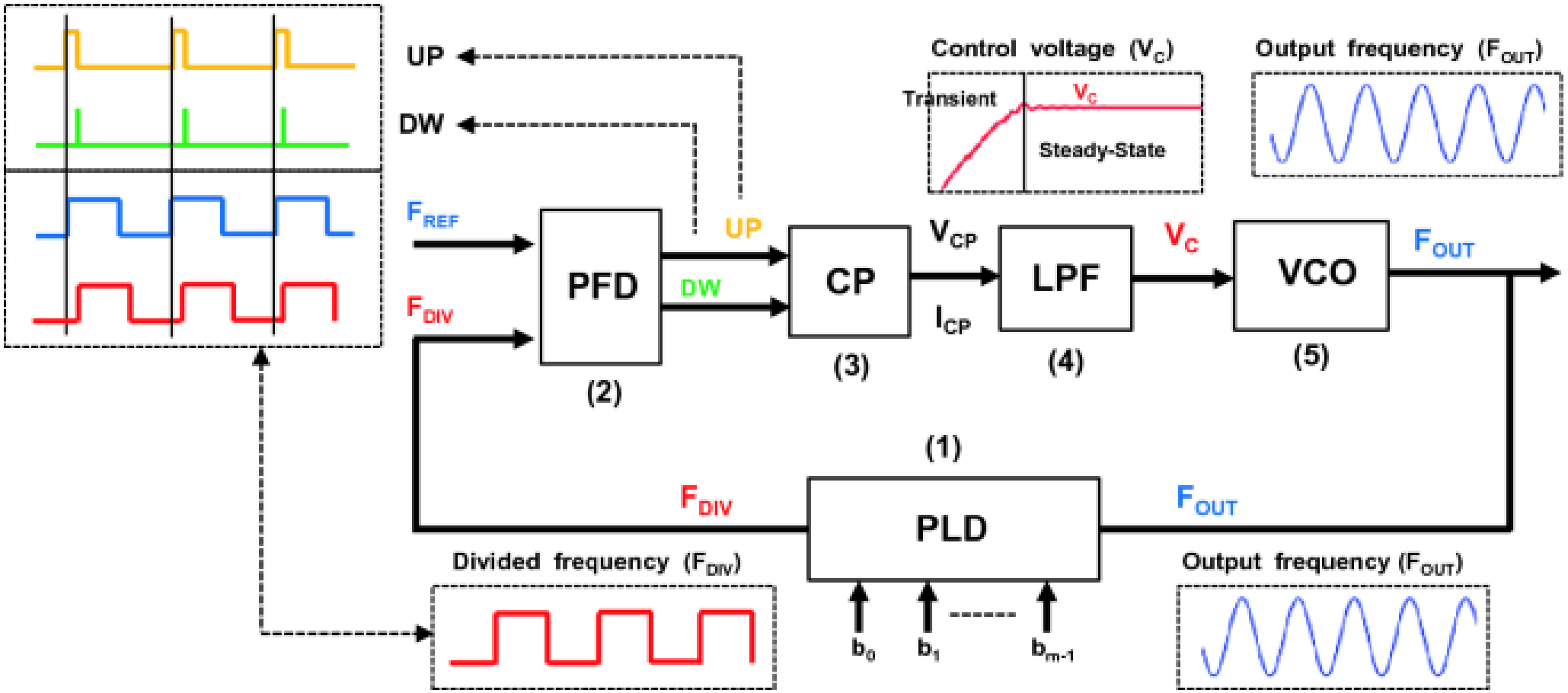
Integer-N Frequency Synthesizers



- Use digital counter structure to divide VCO frequency
  - Constraint: must divide by integer values
- Use PLL to synchronize reference and divider output

Output frequency is digitally controlled

Digital Frequency Synthesizer Waveform



Programmable Divider

CD4046B in USE

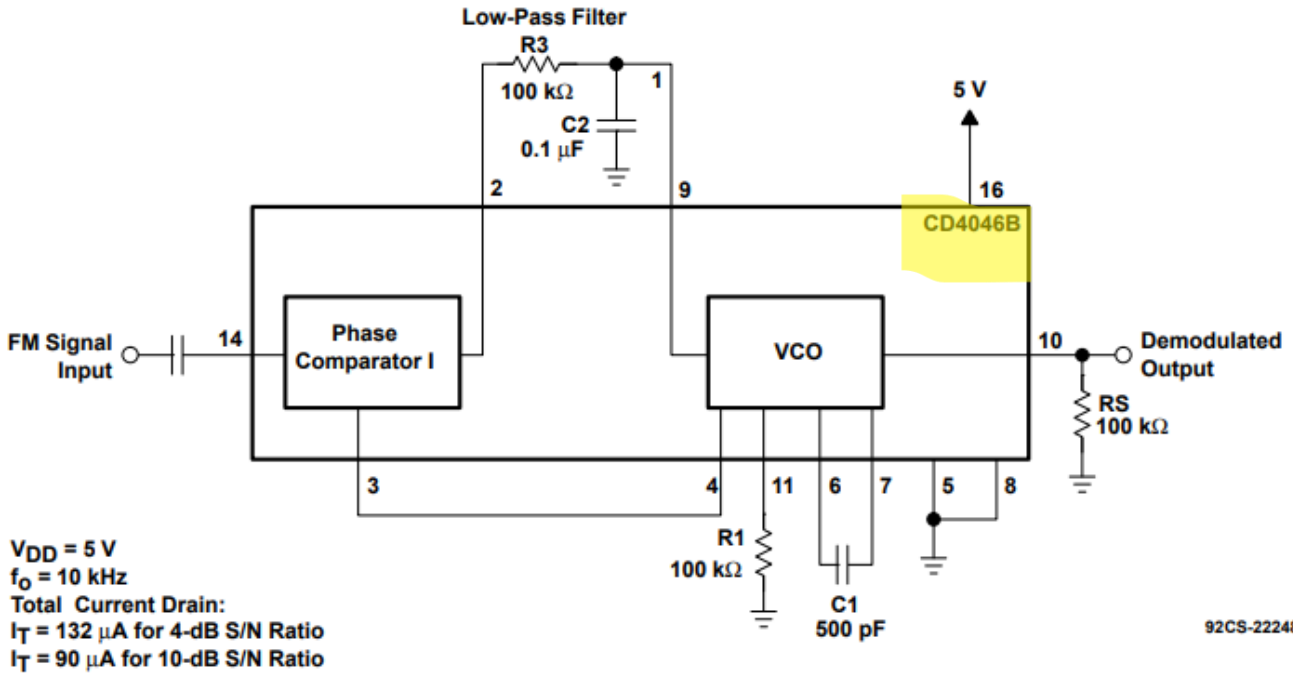


Figure 10. FM Demodulator

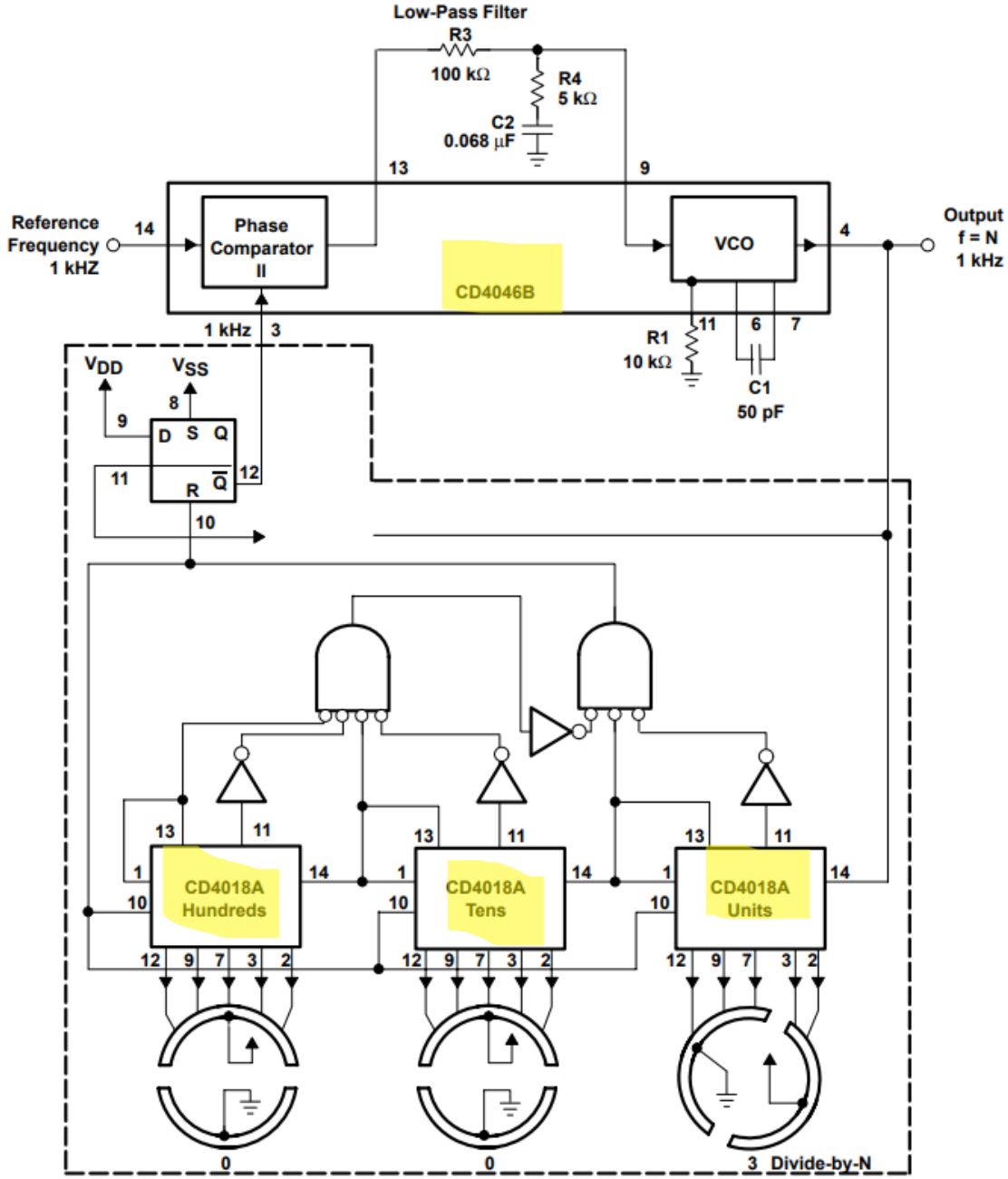
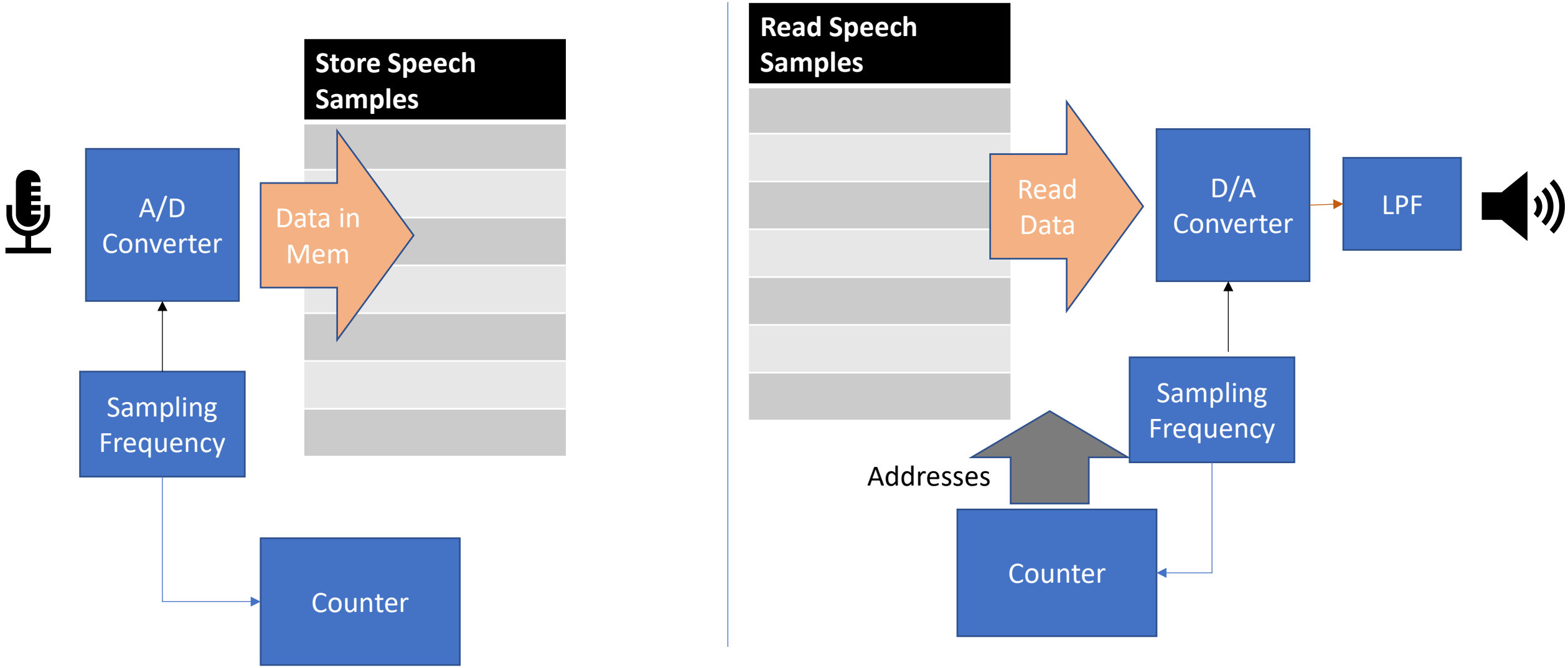


Figure 12. Low-Frequency Synthesizer With Three-Decade Programmable Divider

Speech Processing using Memory

Speech Recording on Memory



Different Recordings of Speech, Music, Effects, can be combined before playing on loud speaker
No. of stored samples depends on sampling rate and length of recording in seconds.
Counter is cyclic so the sequence will repeat after some time.

Speech Effects with Memory

- Voice Changing through changing sampling frequency at readout
- Varying amplitude through scaling of output
- Mixing sound from two memories
- Mixing memory sound with some synthesized signal
- Mixing sinusoids to generate ring tones, sirens etc.
- ….. More such ideas

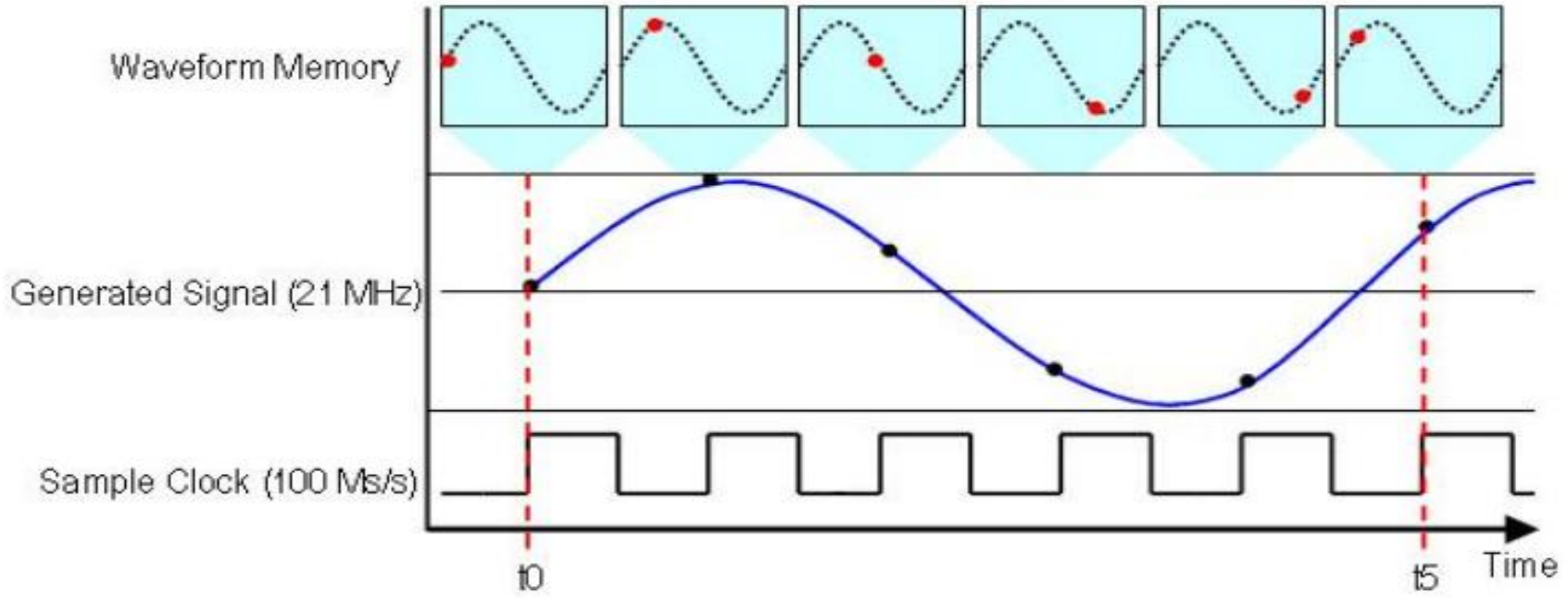
Direct Digital Synthesis

Introduction to Digital Frequency Synthesis

- DDS generates analog waveforms using digital methods, allowing it to take advantage of digital's programmability and higher levels of integration and lower cost.
- Additionally, DDS allows a nearly instantaneous change in frequency or phase, making it a primary source for advanced digital modulation techniques such as frequency shift keying (FSK) and spread spectrum, as well as the use of interference mitigation techniques such as frequency hopping.
- As a result, DDS ICs are rapidly replacing or augmenting traditional phase locked loops (PLLs) and other analog RF sources, while still offering high stability and signal purity.
- A "template" containing the signal's amplitude values for all waveform phases is stored in memory and used to recreate the signal. With DDS, signals can be synthesized directly from the template without requiring the phase-locked loops other indirect methods require.
- Different frequencies are produced by changing the rate the phase values are processed and using techniques to add, multiply and scale signals, various waveforms can be generated.
- The synthesized signals are repeatable, and the frequencies are precise. It is also used for signal generators and enables frequency sweeps.

What is DDS?

- Function Generators utilize DDS to generate periodic signals at precise frequencies by choosing samples from Memory rather than generating new samples of desired waveform.
- We can generate a waveform even though its frequency is not a direct multiple of sample rate of stored wave.
- 16384 Samples are stored in memory.
- With each clock cycle, the appropriate sample is chosen from a lookup table and then generated.
- As a result, we are able to generate signals at precise frequencies while supplying the digital-to-analog converter (DAC) with a constant 100 MHz clock.



21 MHz Sine wave Generation

Theory of DDS Operation

THEORY OF OPERATION

Sine waves are typically thought of in terms of their magnitude form a(t) = sin (ωt). However, these are nonlinear and not easy to generate except through piecewise construction. On the other hand, the angular information is linear in nature, that is, the phase angle rotates through a fixed angle for each unit of time. The angular rate depends on the frequency of the signal by the traditional rate of $\omega = 2\pi f$.

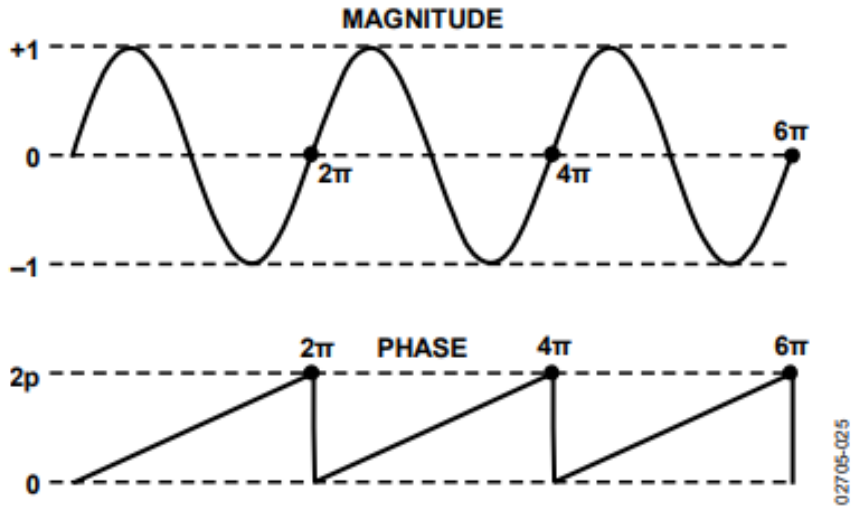


Figure 27. Sine Wave

Knowing that the phase of a sine wave is linear and given a reference interval (clock period), the phase rotation for that period can be determined.

$$\Delta Phase = \omega \Delta t$$

Solving for ω,

$$\omega = \Delta Phase / \Delta t = 2\pi f$$

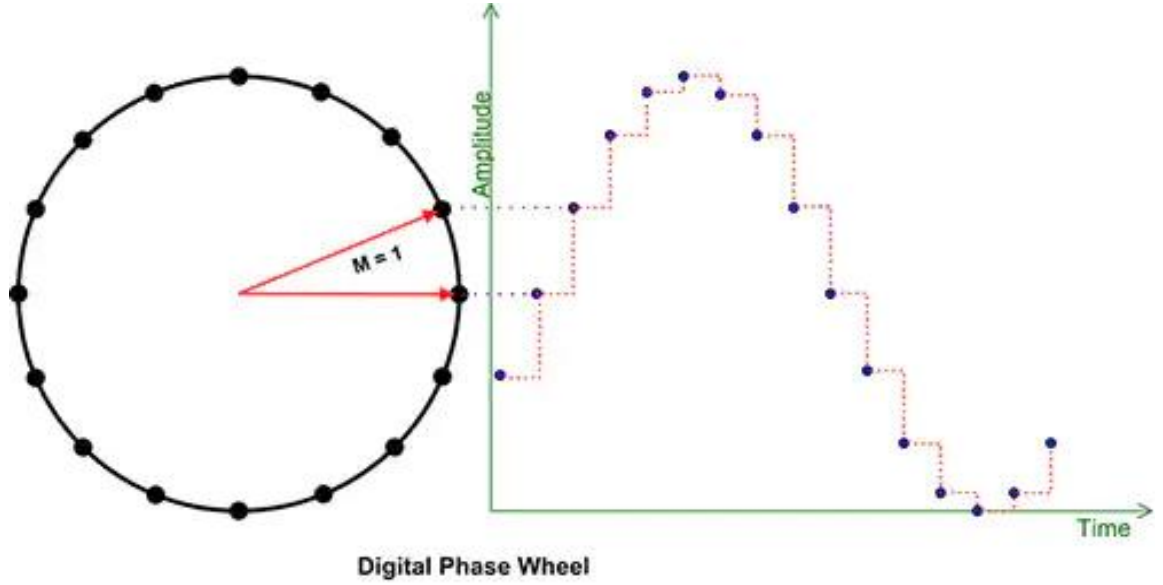
Solving for f and substituting the reference clock frequency for the reference period ($1/f_{MCLK} = \Delta t$),

$$f = \Delta Phase \times f_{MCLK}/2\pi$$

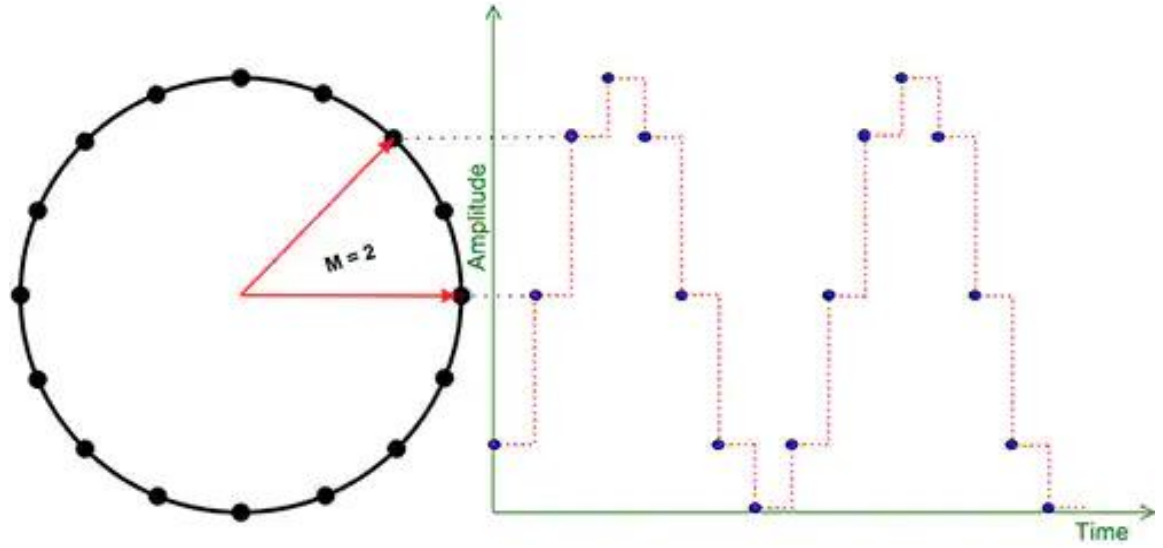
The AD9834 builds the output based on this simple equation. A simple DDS chip can implement this equation with three major subcircuits: numerically controlled oscillator + phase modulator, SIN ROM, and digital-to-analog converter (DAC). Each of these subcircuits is discussed in the Circuit Description section.

Phase Accumulator in Sinusoid

- **The phase accumulator**
- The phase accumulator is a modulo N counter that has 2^N digital states which are incremented for each system clock input pulse. The size of the increment depends on the value of the tuning word, M, applied to the accumulator adder stage. The tuning word fixes the step size of the counter increment. This will determine the frequency of the output waveform.
- The phase accumulator generally has from 24 to 48 bits; at 24 bits there are 2^{24} or 16,777,216 states. This number represents the number of phase values between 0 and 2p radians, or the achievable phase increment. For a 24-bit phase accumulator, the phase resolution is 3.74 E-7 radians. If a larger phase accumulator is used, the phase increment becomes even finer.
- One way of visualizing the operation of the phase accumulator is to look at the accumulator operation as a phase wheel.
- In the lower diagram the tuning word value is set to two. With this setting, every other state on the phase wheel is selected. The analog output now consists of two cycles, each with eight amplitudes, giving a total of sixteen states. With the tuning word set to two, the output frequency is now twice the previously obtained value.



Digital Phase Wheel



Phase Accumulator Operation

- The phase accumulator combines the reference frequency and the value in the tuning word register.
- Since the phase accumulator provides the phase value for the phase-amplitude lookup, the tuning word controls the number of values retrieved from the phase-amplitude table for a cycle.
- With a tuning word of 1, every value in the table is retrieved. A tuning word of 2 reads every other value and also causes the accumulator to clock through to zero twice as fast, with the result that the output frequency has been doubled.
- This remainder enables the DDS precision by ensuring that the lookup table will return the appropriate phase information after the phase register rolls over (once period of the waveform).

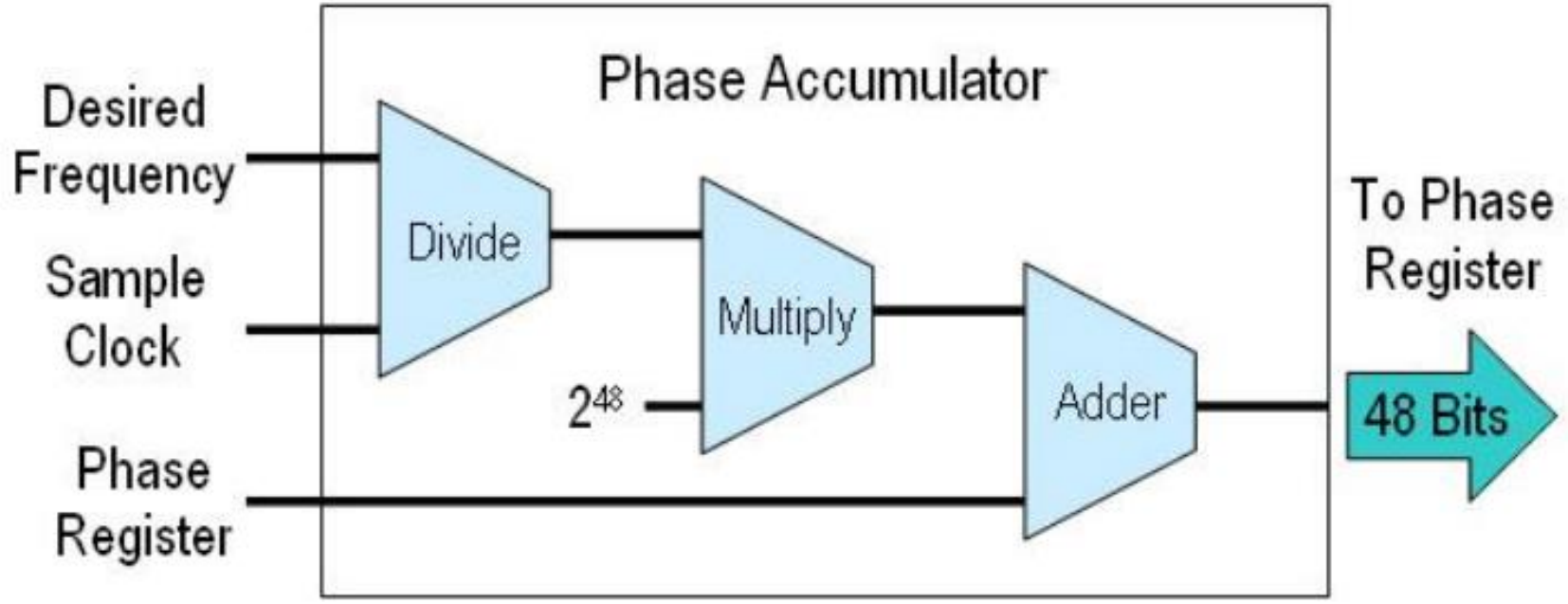


Figure 3: Computation of the Phase Register

Example Phase Accumulator

- As an example, consider a DDS designed with a phase-amplitude table of 360 entries, holding the amplitude (voltage) values for each one of the 360 degrees of a sine wave.
- The accumulator resets after 360 clock cycles. The reference frequency will be pulled from the system clock, so everything is clocked and updated at the same rate. With a tuning word of 1, the phase accumulator is incremented by 1 for every clock, and the table values are retrieved in order.
- Every 360 reference clocks, the accumulator resets and another waveform is created.
- Setting the tuning word to 2 has the result of reading every other value from the phase-amplitude table; the accumulator clocks through twice as fast and the output frequency is doubled.
- Of course, using only 360 values would produce a choppy output and the jitter would make it unusable. DDS systems typically have phase-amplitude tables with thousands of data points and 16-bit registers for the tuning register and phase accumulators.

Block Diagram of DDS

- Implementation of DDS requires a look-up table to determine the phase output signal at any point in time.
- Building blocks for DDS based waveform generation are shown below.
- Bit-widths represent a commercial chip from Analog Devices.

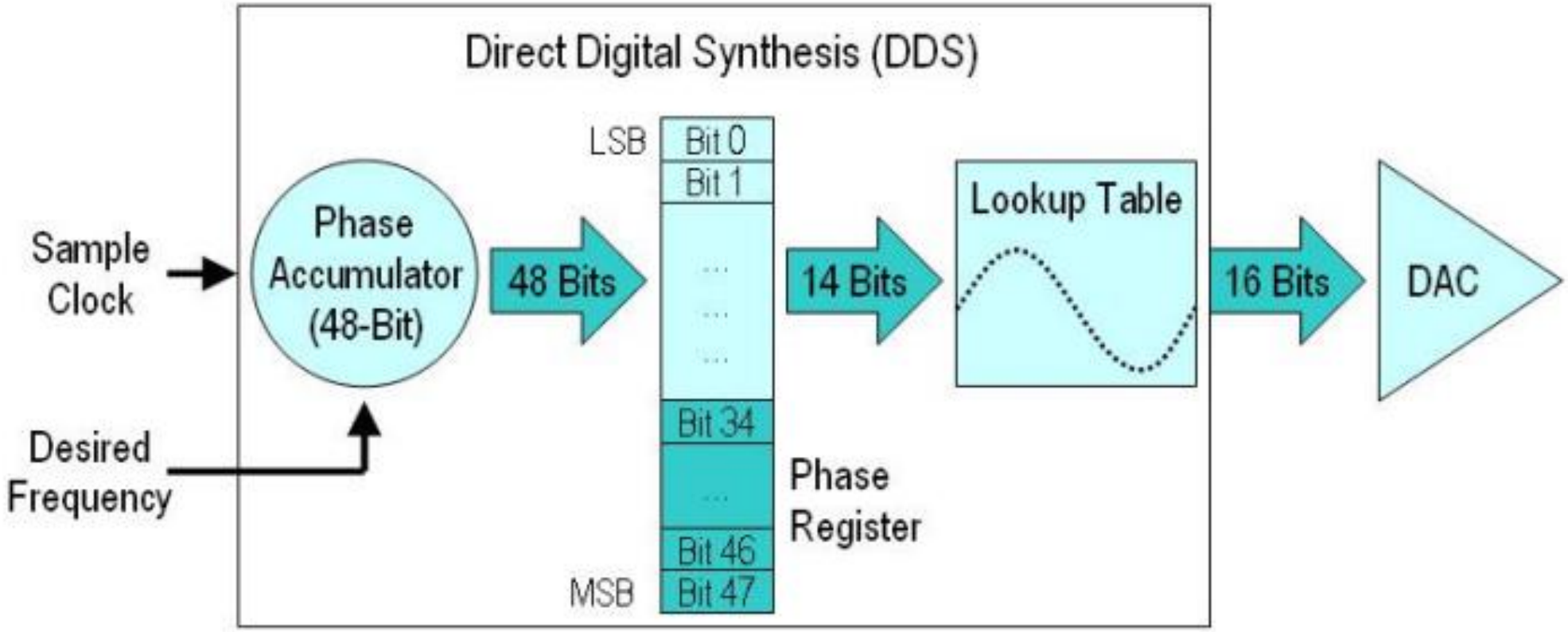
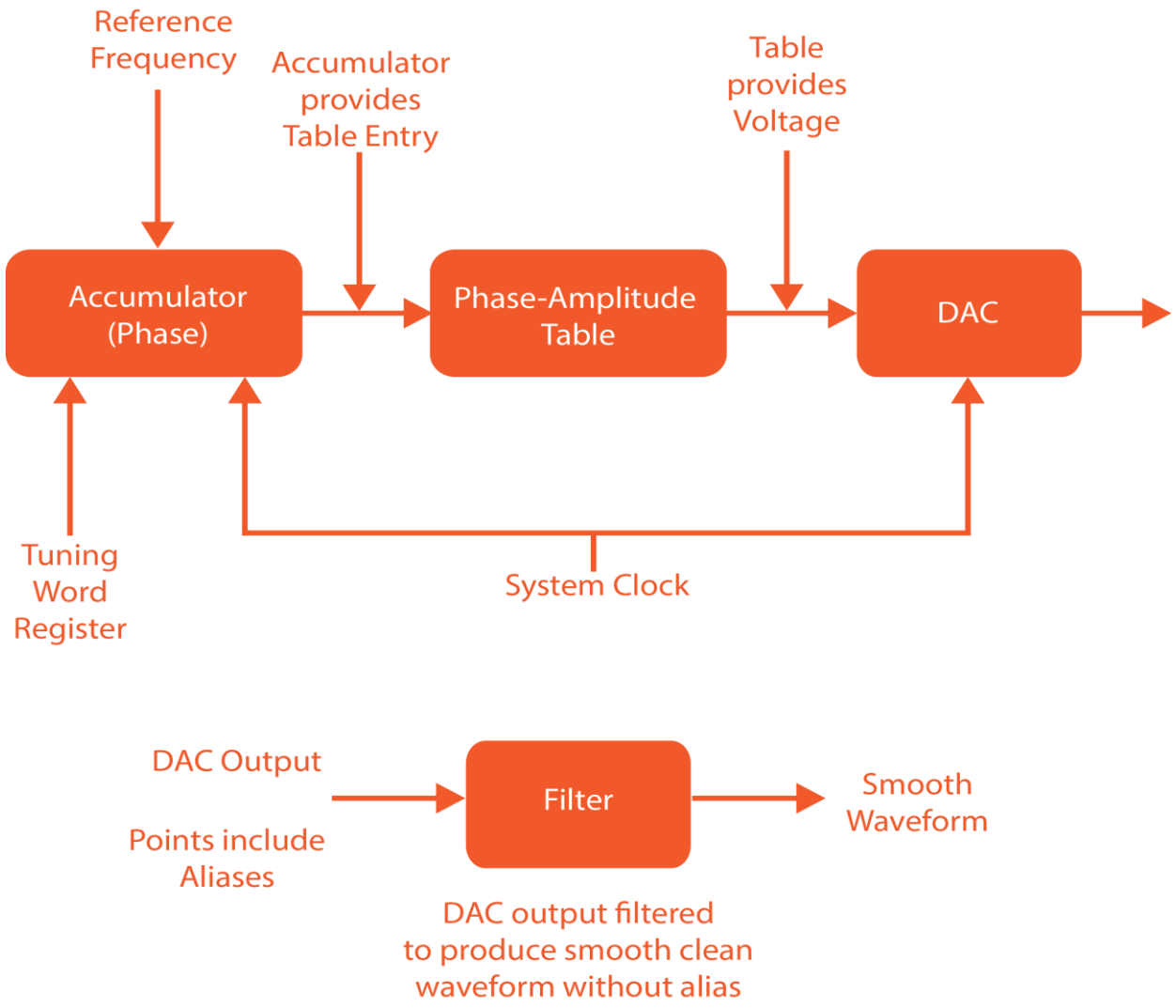


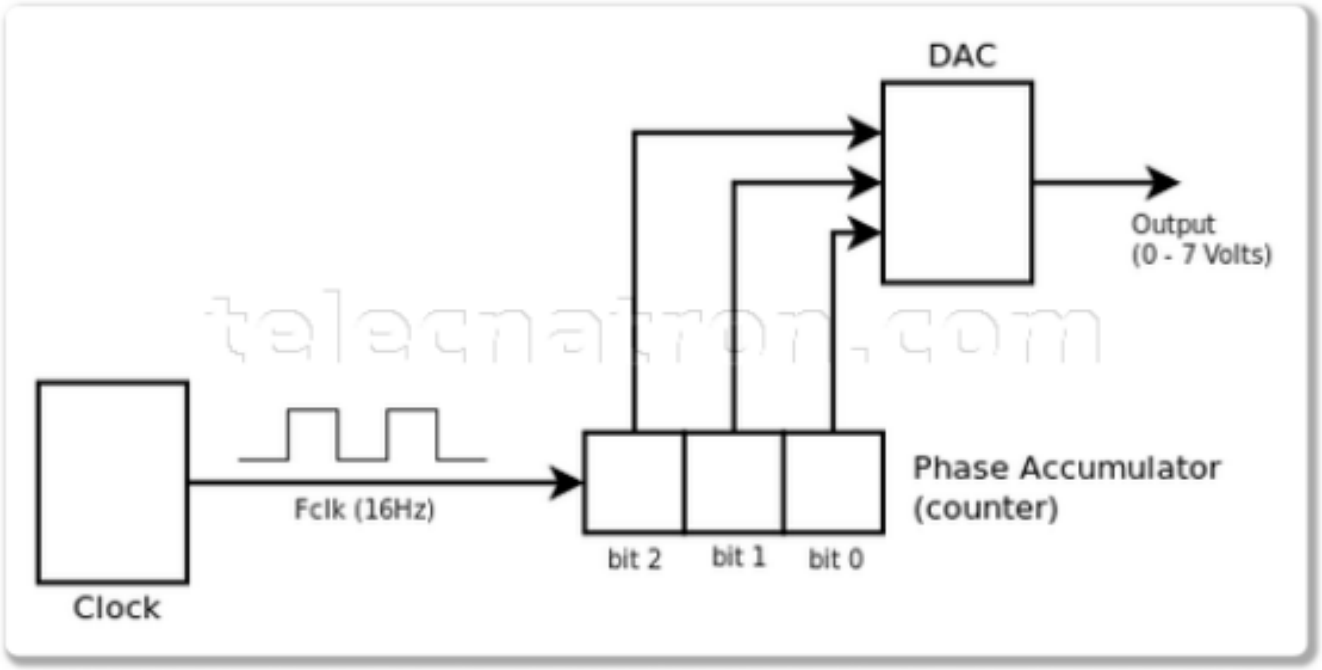
Figure 2: Direct Digital Synthesis Block Diagram

Another view of DDS Blocks



Example of Fixed Freq DDS Design

- We start with a Clock source which generates fixed frequency square wave.
- This clock is used to get output from Binary Counter.
- Output of Binary Counter is connected to Digital to Analog Converter (DAC).
- In this example, we use 16 Hz clock frequency, 3 Bit Binary Counter.
- In DDS terms, the counter is known as the ‘phase accumulator’



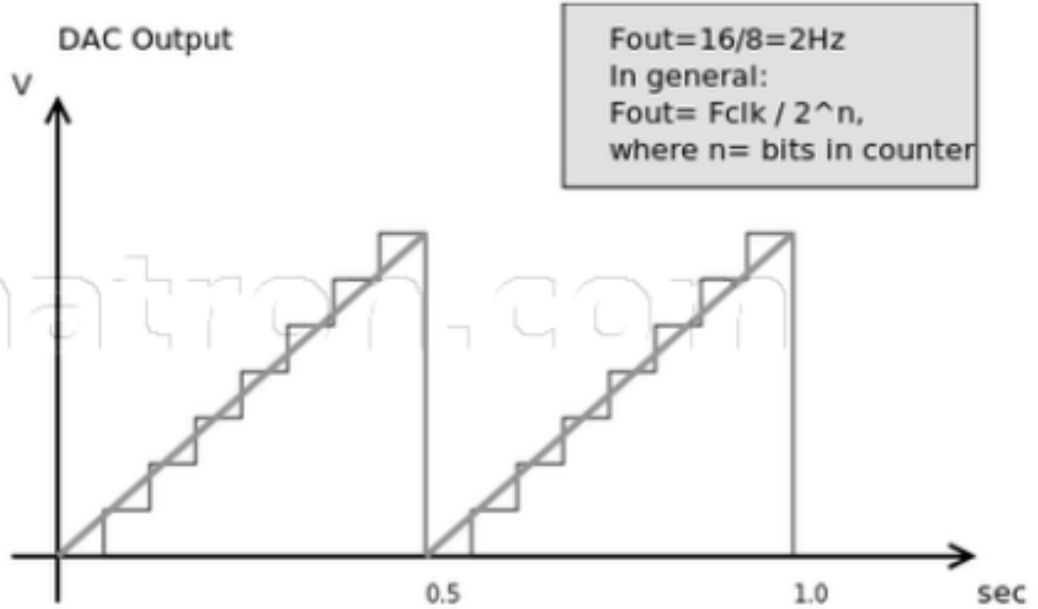
To keep things simple, we use a 16Hz clock frequency, a 3-bit counter and an DAC whose output voltage is equal to the counter's output.

In DDS terms, the counter is known as the *phase accumulator.*

Counter to DAC waveform

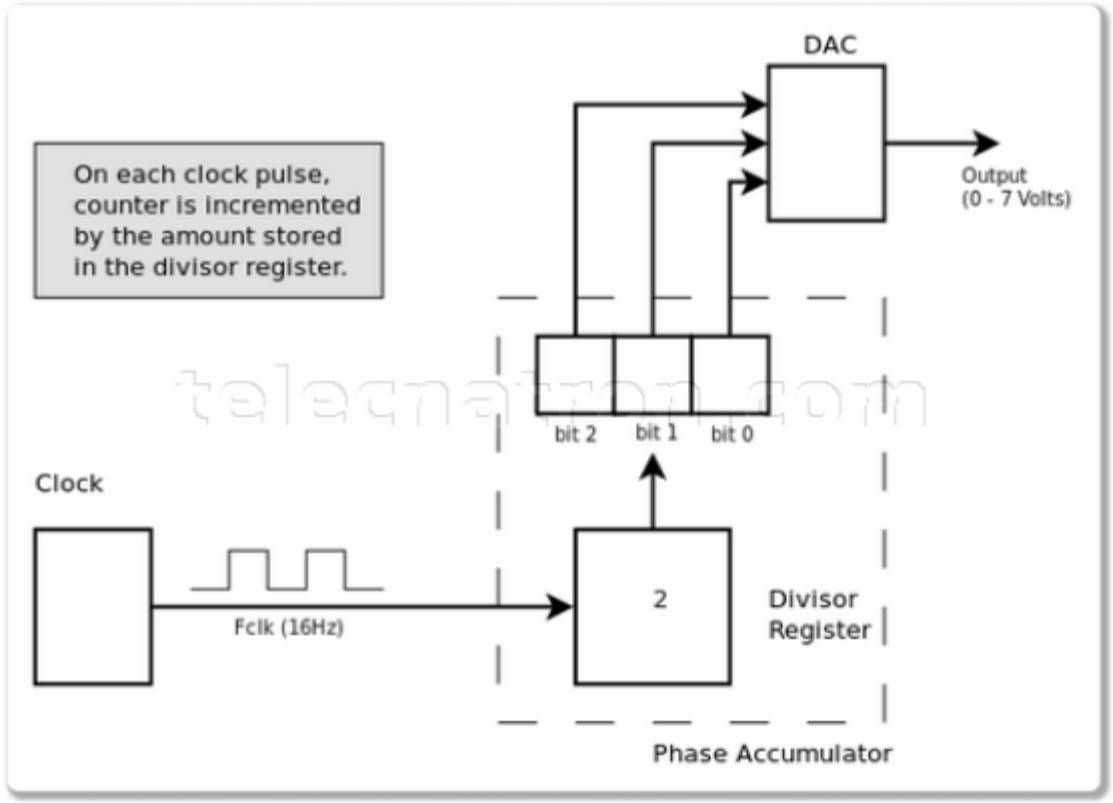
- On each clock pulse the counter counts up by one until it reaches its maximum value, when it resets and starts again from 0 on the next pulse.
- The counter has 8 discrete output values and there are 16 clock pulses per second. Hence, two complete wave cycles for a frequency of 2 Hz.
- The output frequency is determined by dividing the clock frequency by two raised to the power of the Number of bits in the counter.

counter bit	2	1	0	counter/
bit value	4	2	1	DAC output
	0	0	0	0
	0	0	1	1
	0	1	0	2
	0	1	1	3
	1	0	0	4
	1	0	1	5
	1	1	0	6
	1	1	1	7



Divisor Register in DDS

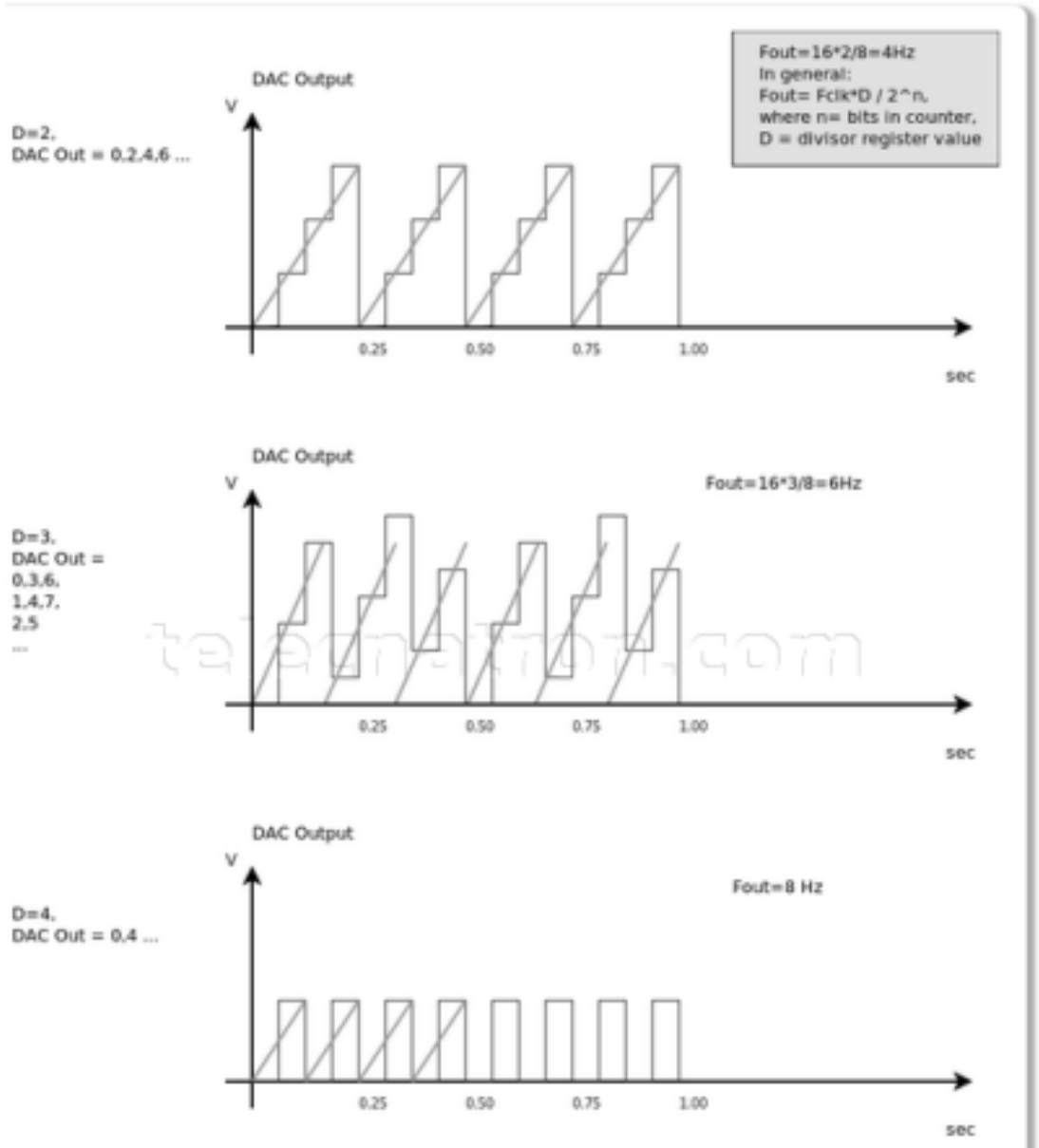
- To be able to generate other frequencies besides Fclk/2, a Divisor Register is added to the phase accumulator.
- Now, on each clock pulse, the counter is incremented by the value in the divisor register.
- Eg. With divisor register having a value of D=2, on each clock pulse, the counter is incremented by 2.
- The counter now outputs values of 0,2,4,6 before repeating. This gives a frequency of twice that in the previous case without divisor.



With the divisor register having a value of D=2, on each clock pulse the counter is incremented by two.

The counter now outputs values of 0,2,4,6 before repeating, giving a frequency of twice that in the previous step.

Waveforms with different values of Divisor



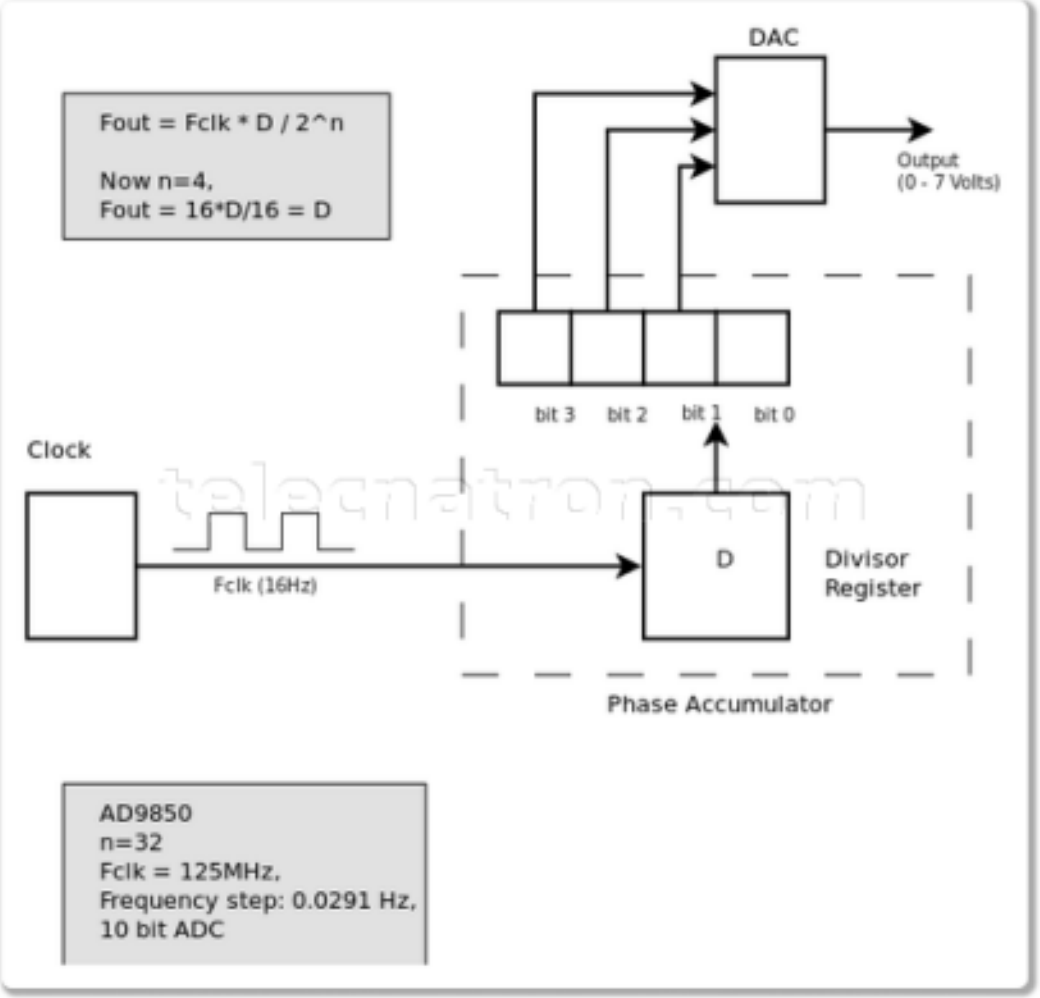
With D=3 for 6Hz, the clock frequency is no longer exactly divisible by the divisor register value and it now takes three cycles through the counter's count range before the pattern repeats. Note how the pattern of (2,5) only includes two steps whereas the others have three, but overall we still have six cycles in the one second period. In this case there is more reliance on the DAC output filter to produce a nice sawtooth wavefrom.

For D=4 there is only one step per cycle; you can see how the output waveform becomes more coarse as the frequency increases.

With D=2, we now have 4Hz. The output frequency is determined by multiplying the clock frequency by the divisor register value and dividing by two raised to the power of the number of bits in the counter.

Variable Fractional Frequencies

In the previous step, we were able to generate any frequency between zero and half of the clock frequency with a resolution of the clock frequency divided by two raised to the power of the number of bits in the counter, which, in the examples was 2Hz.



To double the resolution to 1Hz, all that needs be done is to add a bit to the counter as shown in the diagram.

The formula for calculating the output frequency remains the same but now n=4.

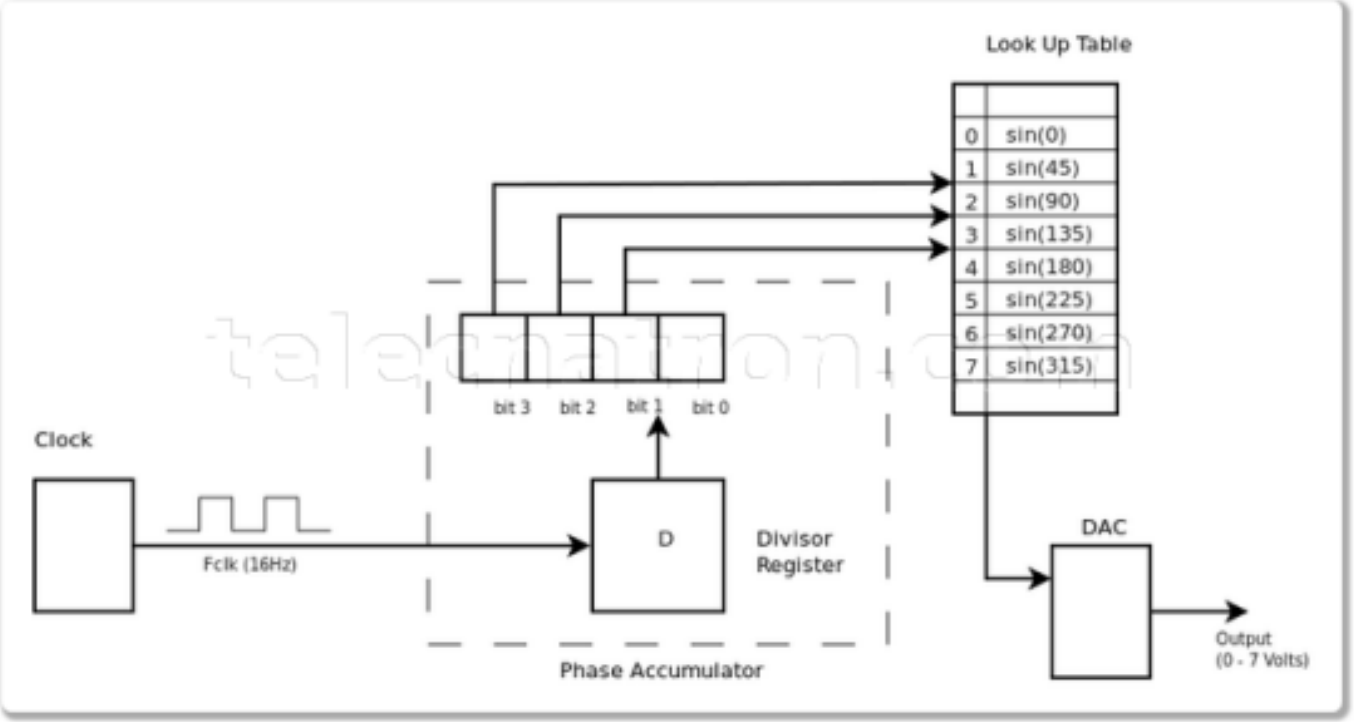
For each bit that is added to the counter, the resoluton is doubled (or should that be halved?).

A real world device such as the AD9850 has a 32 bit counter, which at its maximum clock frequency of 125MHz, has a resolution of 0.0291Hz(!) and with it's 10 bit ADC, can generate

Sinewave Synthesis

5. Step 4: Sinewave Synthesis

The final step is generate a sine wave from the DAC's sawtooth output, this is done by means of the *look up table*.



Here, the lookup table takes (LUT) takes the counter ouput and outputs the corresponding sine value. For example, with a count of 0 the LUT outpus a value of sin(0) = 1 which the DAC converts to 7 volts. With a count of 1, the LUT outpus sin(45)=0.707 and the DAC outputs 0.707 * 7 = 4.95 volts, etc and hence, after filtering, giving a close approximation to a sine wave.

Note that the look up table can contain values for any waveform, and not just a sine wave and could be used as an arbitary waveform generator.

Few Extra Slides

Operation of DDS Building Blocks

- A Phase Accumulator compares the sample clock and desired frequency to increment a phase register.
- The idea is that we can generate signals with precise frequencies by generating an appropriate sample based on the phase of that frequency at any point in time.
- In addition, by representing our waveform with 2^{14} (16,384) points, we can represent exactly 16,384 phase increments with our lookup table.
- The phase accumulator uses simple arithmetic operations to calculate the lookup table address for each generated sample.
- It does this by dividing the desired frequency by the sample clock and multiplying the result by 2^{48}. This number is based on the bit-resolution of the phase register. A 48 bit is used for maximum precision. Of these, 34 bits are used to store remainder phase and 14 bits are used to choose a sample from the lookup table.
- Thus, the phase accumulator produces a 14-bit address that corresponds to the exact phase of the signal. For example, address '0000 0000 0000 00' corresponds to 0^0.
- On the other hand, an address of '1111 1111 1111 11' corresponds to 359.978^0. Thus the signal generator can use this address to control the phase of the signal at any point in time.

Determine the Output Frequency

- The output frequency of the DDS is set by the tuning word value and increases proportionally to the value of the tuning word. The sample rate remains fixed at the system clock rate, and the time between output samples is constant.
- The output frequency depends on the tuning word increment, so as the tuning word value increases, there are fewer steps in each output cycle, thereby increasing the frequency.
- The tuning word can be increased until there are only two samples per cycle, which brings the DDS output to its Nyquist frequency, or half the system clock rate.
- The output frequency of the DDS is dependent upon the tuning word value, and the length of the accumulator.
- It is expressed by Equation:

$$f_{out} = \frac{M * f_c}{2^N}$$

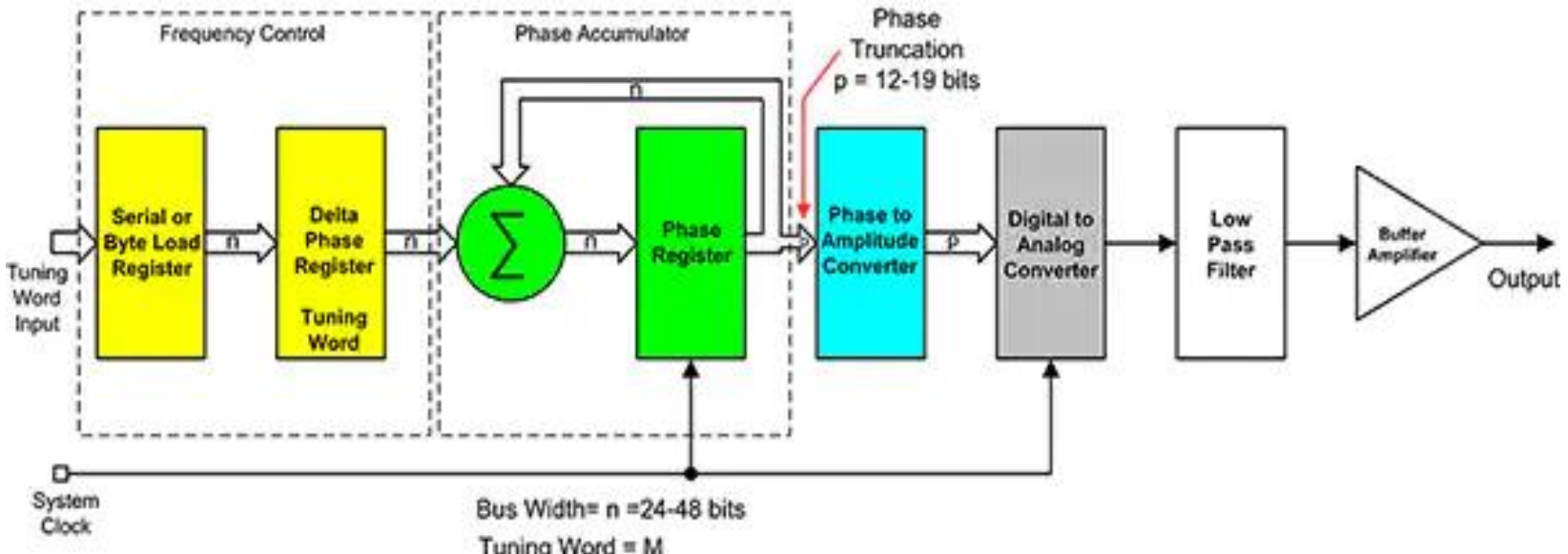
Where:

f_{out} is the DDS output frequency
M is the tuning word value
f_c is the system clock frequency
N is the length of the phase accumulator

- The output of the phase accumulator, which is the instantaneous phase of the output waveform, is used to drive the phase to amplitude converter. The phase to amplitude converter outputs a digital word, the value of which is the amplitude of the sine waveform for the input phase.
- Note that the number of bits used to drive the phase to amplitude converter is less than that used for the phase accumulator. This is referred to as **phase truncation** and is used to reduce the hardware of digital stages after the phase accumulator.

How does Digital Synthesis work?

- Digital synthesis is based on a phase accumulator which generates a series of digital states (instantaneous phase), the value of which increases linearly, forming a numeric ramp.
- This signal is made periodic and represents the instantaneous phase of the output waveform, from zero to 2p radians.
- This is the digital input to a lookup table that provides the phase to amplitude conversion which is applied to a digital-to-analog converter (DAC), producing the desired analog output after filtering.
- While the most common DDS output waveform is the sine wave; ramps, triangle waves, and square waves are also easily generated.
- Since the input to the DAC is a series of sampled values, the output has quantization steps. These steps produce spectral images at multiples of the sample rate in the frequency domain which are not desired. A low-pass filter, placed after the DAC, suppresses these unwanted spectral responses.

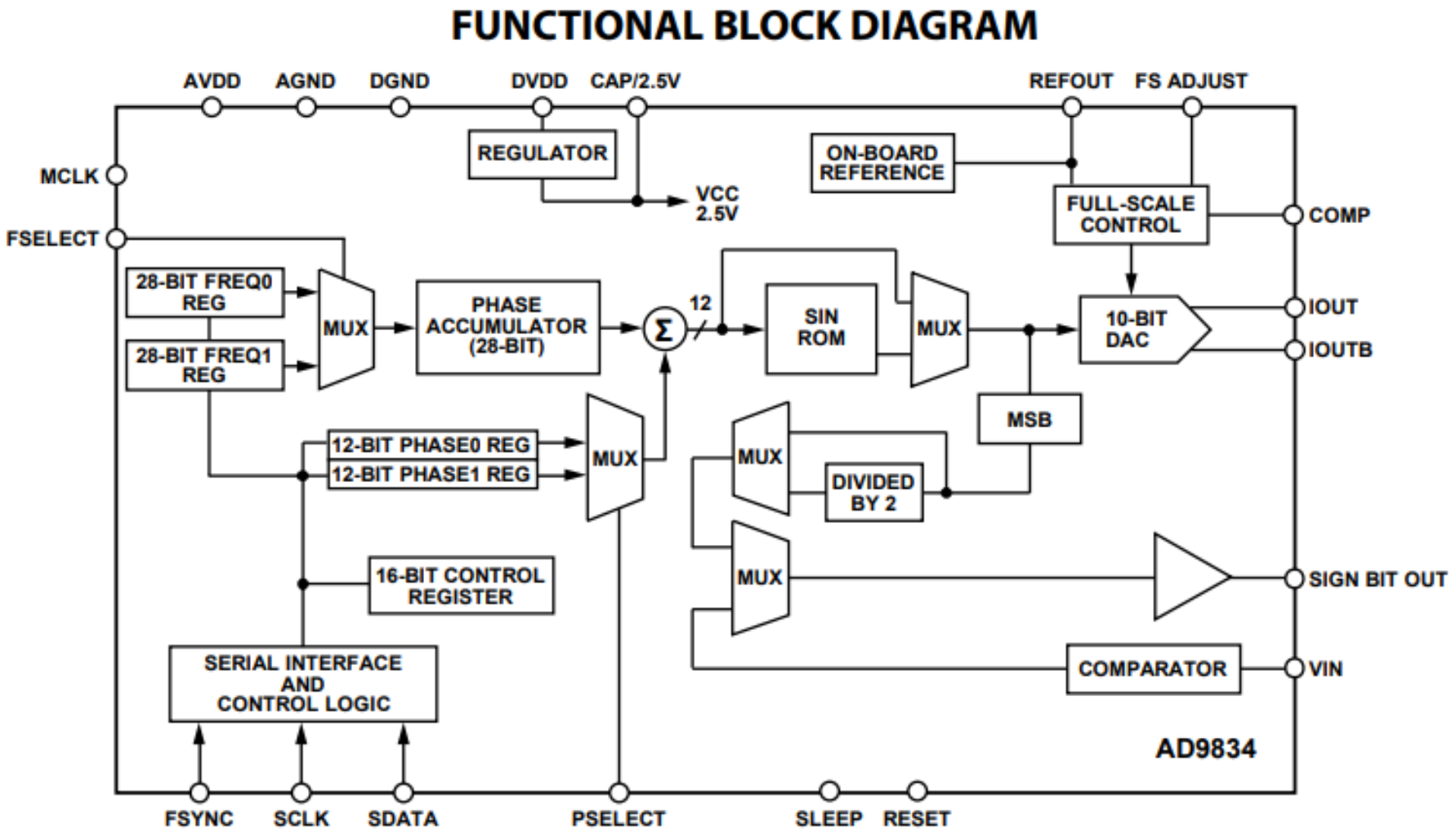


Benefits of DDS

The benefits of DDS are:

- The ability to generate arbitrary frequencies with accuracy and stability, limited only by the oscillator used to clock the phase accumulator. Crystal oscillators, depending on their specifications, can deliver tolerances of 50 parts per million to ~0.1 part per billion, making DDS extremely accurate. Analog signal generators can only deliver accuracy and stability of a few tenths of a percent unless using a high-end device.
- The frequencies provided by DDS are repeatable. Loading the tuning word register with the value corresponding to frequency F1 generates a signal at frequency F1. If the tuning register is then loaded with the value for frequency F2, the output signal is quickly changed to frequency F2. When the tuning register is reloaded with the value for F1, the exact the same frequency F1 is provided as was generated before. Analog generators can't guarantee this precision.
- High frequency resolution can be achieved with the digital techniques used in DDS. Increasing the resolution is as simple as adding more bits to the least significant end of the phase accumulator and tuning register. Analog waveform generators, which depend on mechanical components like potentiometers and variable capacitors to tune the oscillator, are limited in the resolution they can provide.

Commercial DDS Chip *AD9834 Analog Devices*



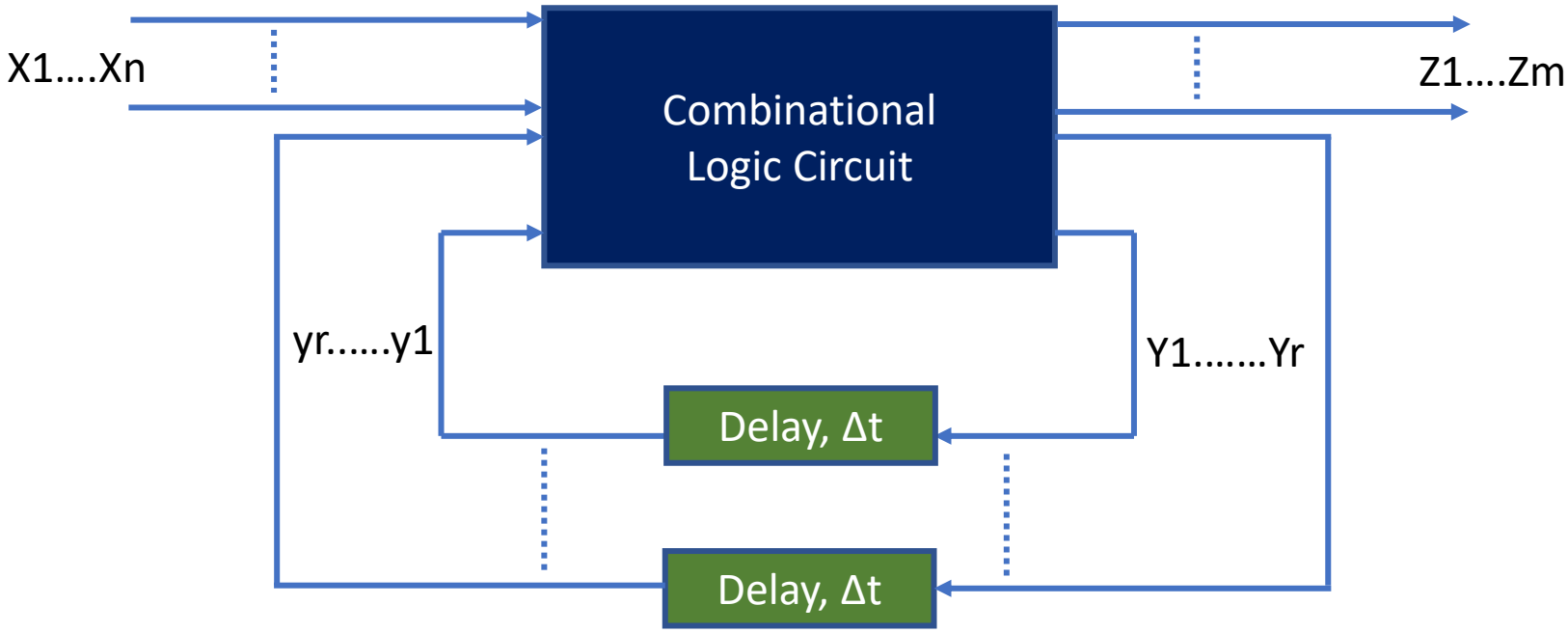
ASYNCHRONOUS SEQUENTIAL CIRCUITS

Asynchronous Sequential Circuits

- A clock is **not** utilized to synchronize state changes
- Only external inputs and current states are available to cause state changes

Fundamental Mode Asynchronous Circuits

- These circuits have level inputs and unclocked memory elements
- Uses inherent delays present in logic circuit elements
- Assume that each delay element has same delay Δt

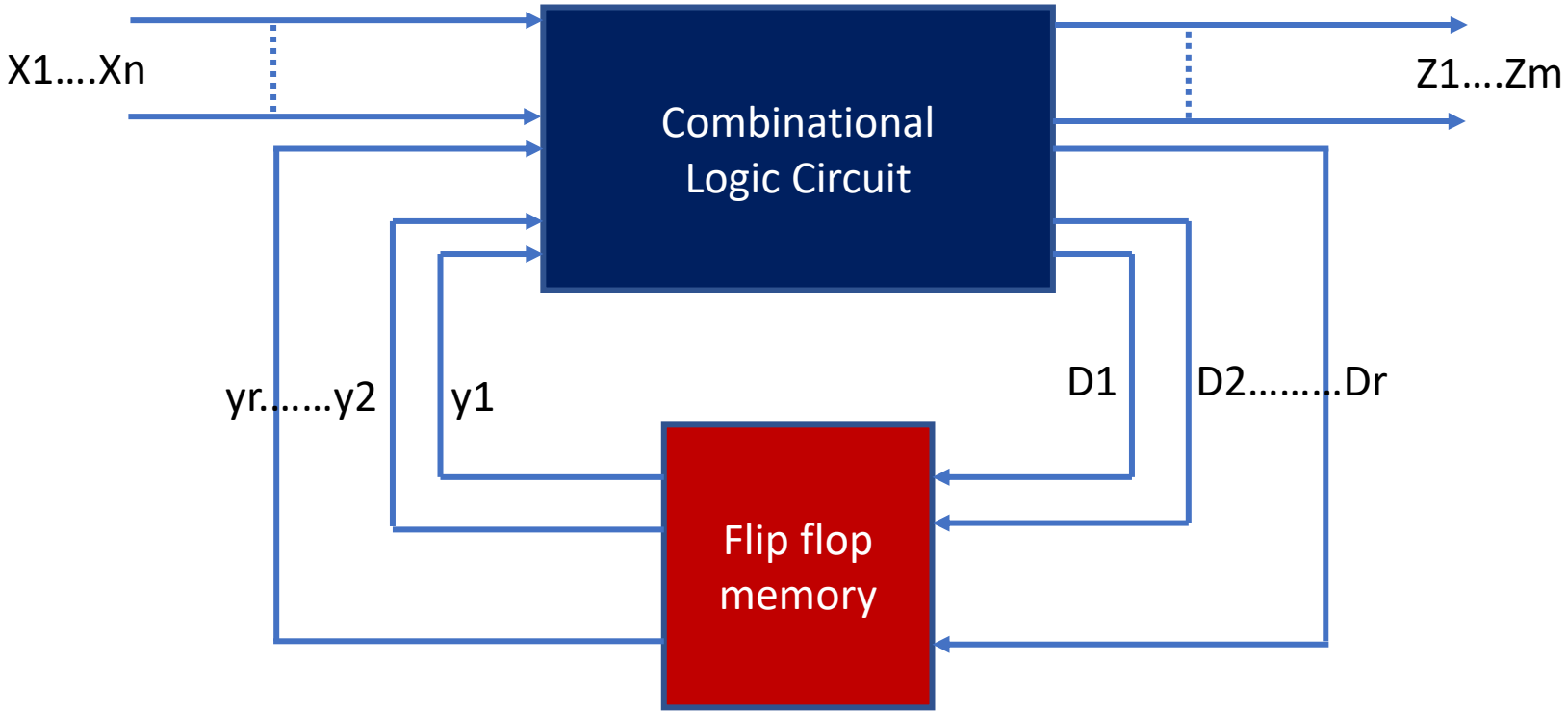


Other conditions for Fundamental Mode cct

- All delays in a circuit branch are lumped to a single Δt
- The delay is always Δt
- Inputs are restricted so that only one input variable is allowed to change value at a given instant to ensure correct behavior
- For predictable operations, input changes should be spaced in time by at least Δt; the time needed for the circuit to settle down to a stable state following an input change

Pulse Mode Asynchronous Circuits

- Pulses will not occur simultaneously on two or more input lines
- Memory element transitions are limited only by input pulses
- Input variables are used either only in uncomplemented or in the complemented forms, but not both together



Pulse Mode Asynchronous Sequential

Pulse Mode Asynchronous Circuits :

- In the pulsed mode, the input variables are allowed to be applied in the form of pulses, rather than in the form of levels.
- But the width of input pulses is a critical parameter. There are two restrictions on the width of the input pulses.
  - The first requirement is that the pulses should be long enough so that the circuit can respond to them.
  - The second requirement is that the pulses should not be too long so that they are still present after the new secondary state is reached.
- The base of calculating the minimum pulse width is the propagation delay of the excitation logic.
- The maximum pulse width is calculated based on the total propagation delay through the excitation logic and the memory.

Conditions for Pulse mode circuits

- Input pulses should be spaced in time by at least the response time of the slowest memory element
- No memory element will be in process of changing state when a new input pulse arrives