Lecture 5
EE 421 / CS 425
Digital System Design

Fall 2024

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QUIZ 1 TODAY

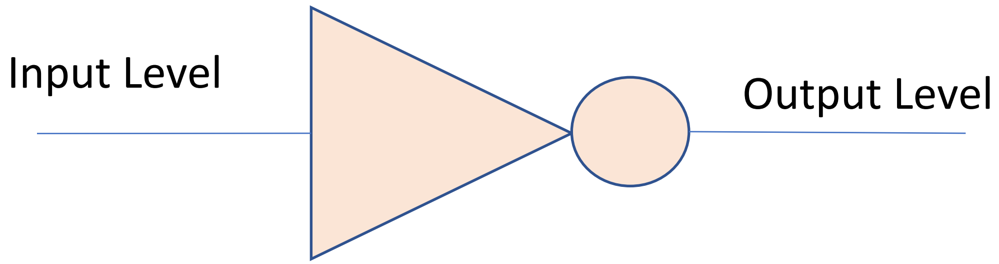
Topics

- Pulse Circuits
- Timing Related Effects in Combinational Circuits
- Glitches
- Hazards
- Identify and Remove Glitches and Hazards (May do in next lecture)
- QUIZ 1 Today

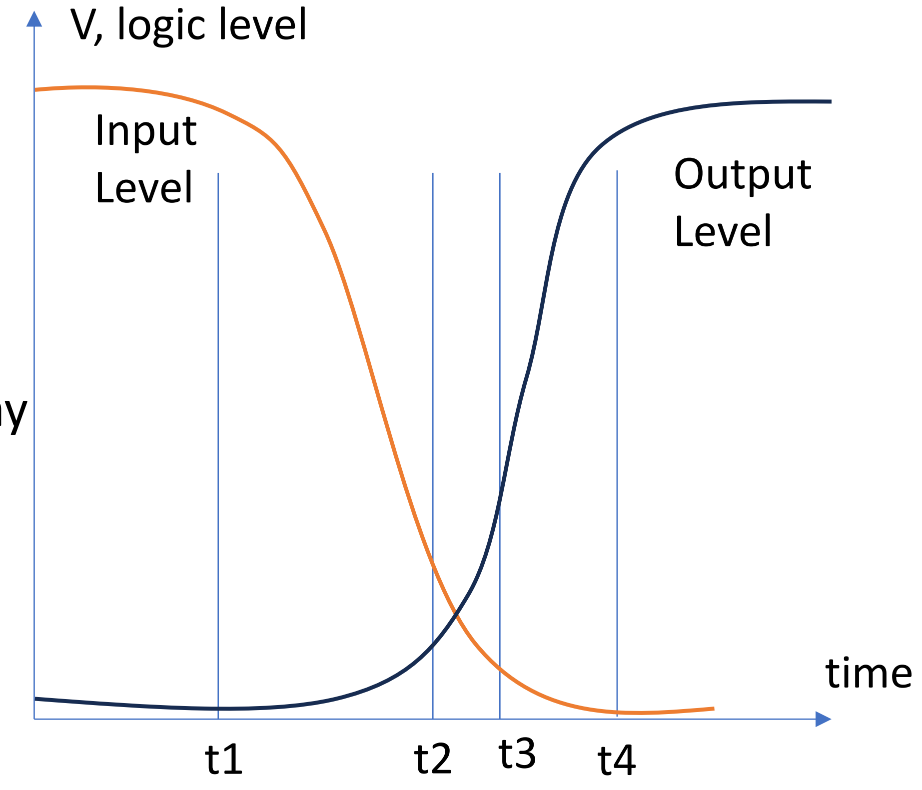
Timing Waveforms

Every physical circuit has some processing delay; once the input has settled, **the correct output appears after some time**.

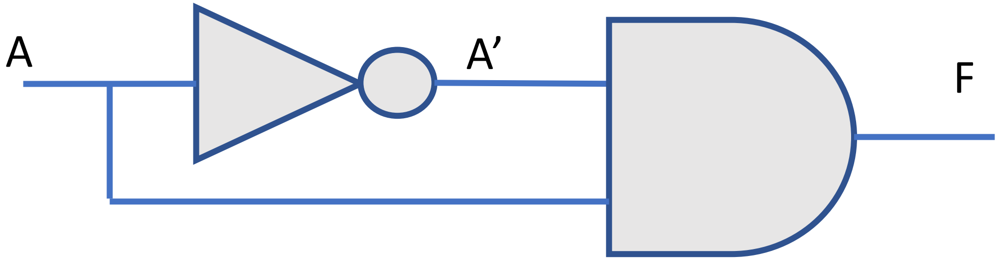
Propagation delay from a gate is defined by:
tplh = time delay in output going from low to high
tphl = time delay in output going from high to low

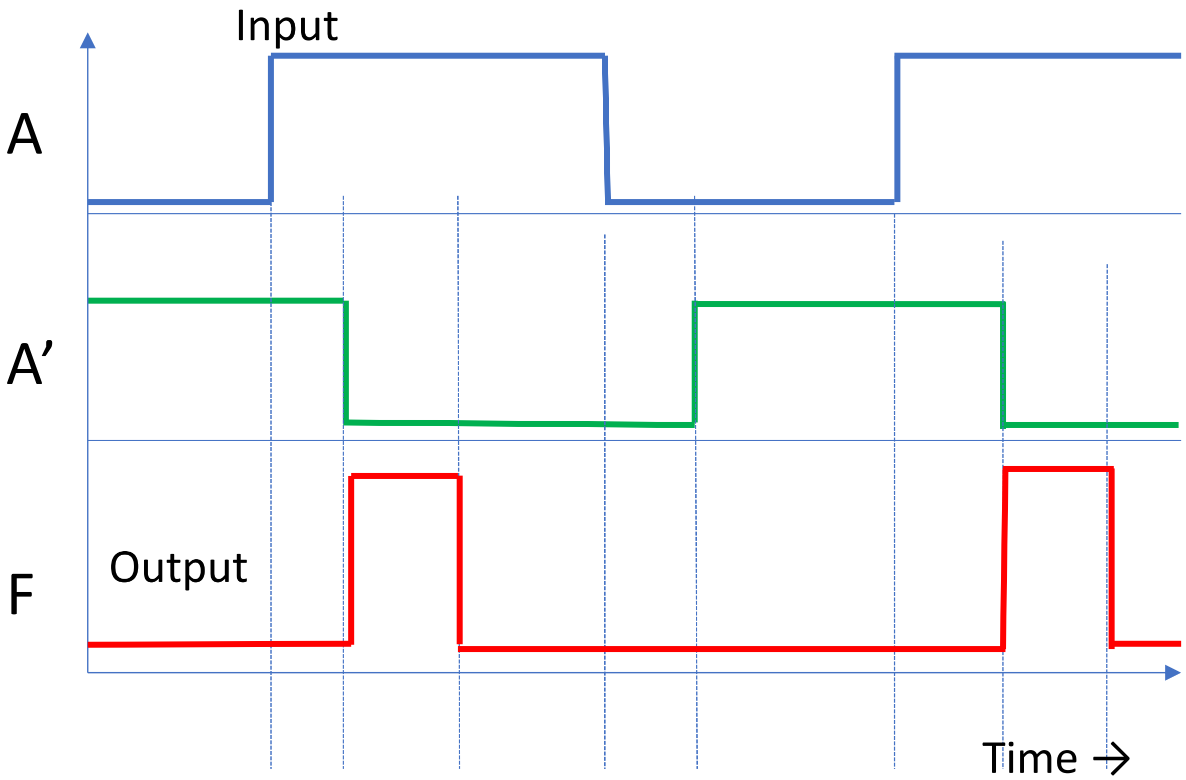


Inverter Circuit Delay



A simple pulse circuit

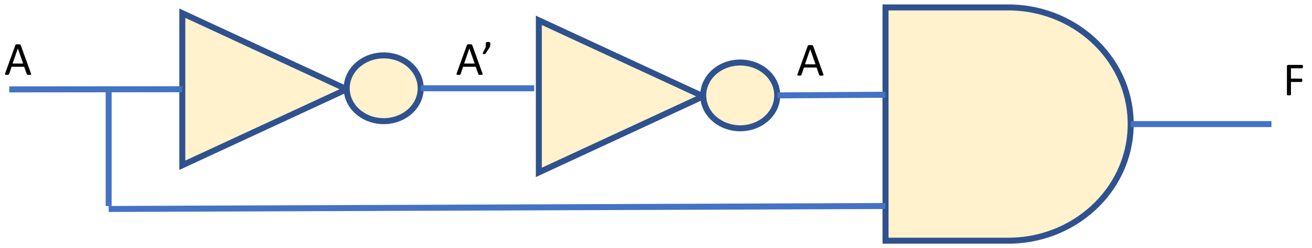




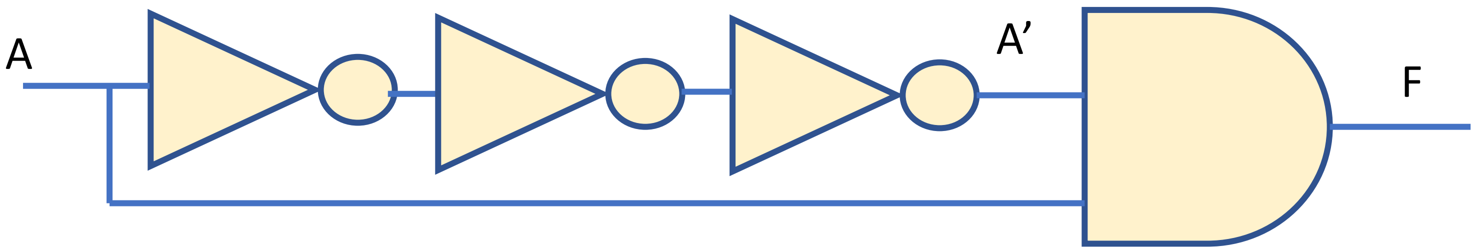
Question: What will be the Output if there are two inverters in series?

Question: What will be the Output if there are three inverters in series?

Two and Three Inverters in simple pulse circuit

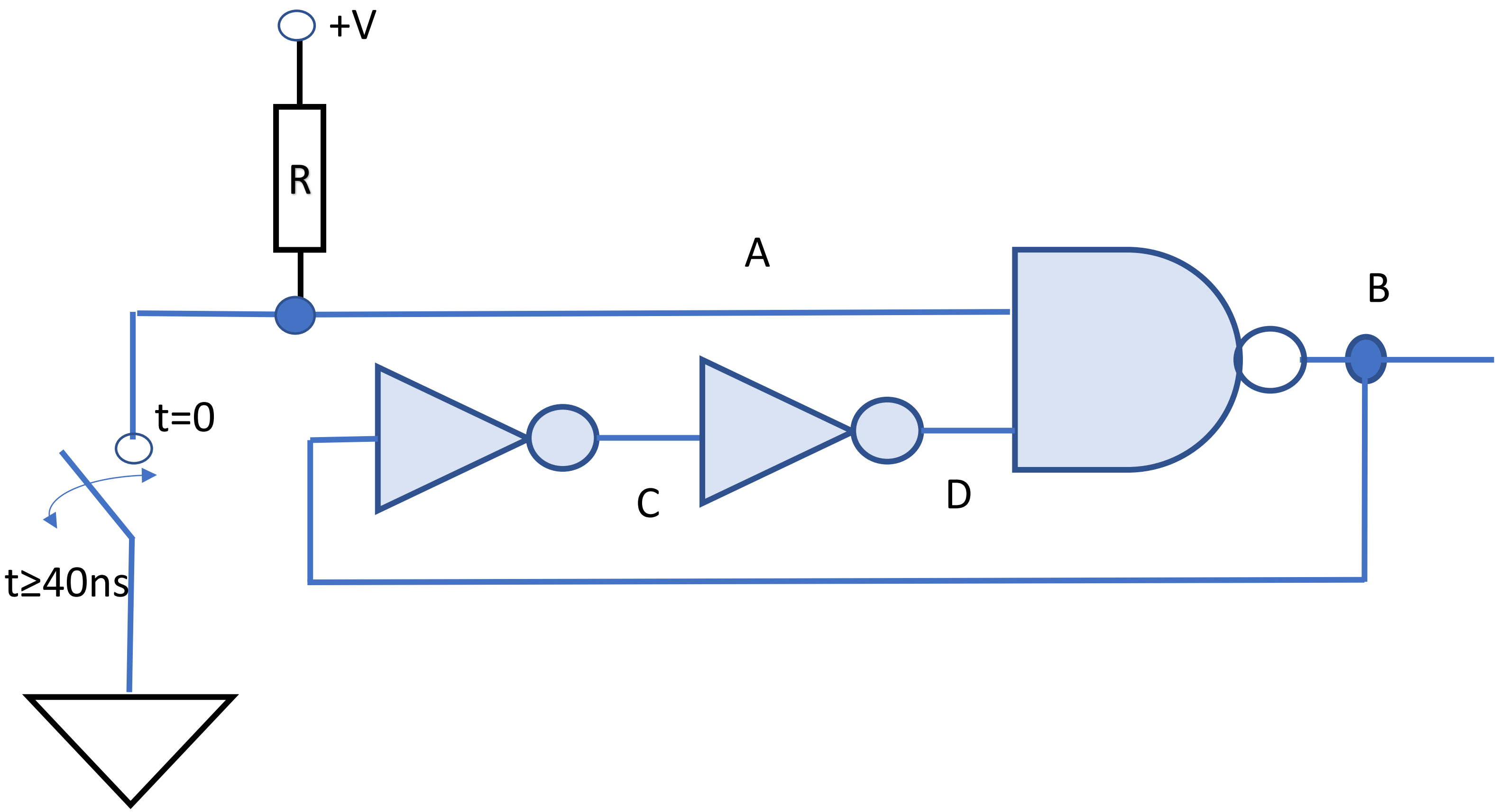


For even number of Inverters:
Check input A transitions from
0 to 1 and from 1 to 0
Pulse behaviour is not observed
(Hint: Check whether F is like A?)



For Odd number of Inverters:
At 0 to 1 transitions at A, a pulse will appear at F. The pulse width is proportional to number of inverters as their propagation delay adds up

A Pulse Shaper Circuit



Case 1:

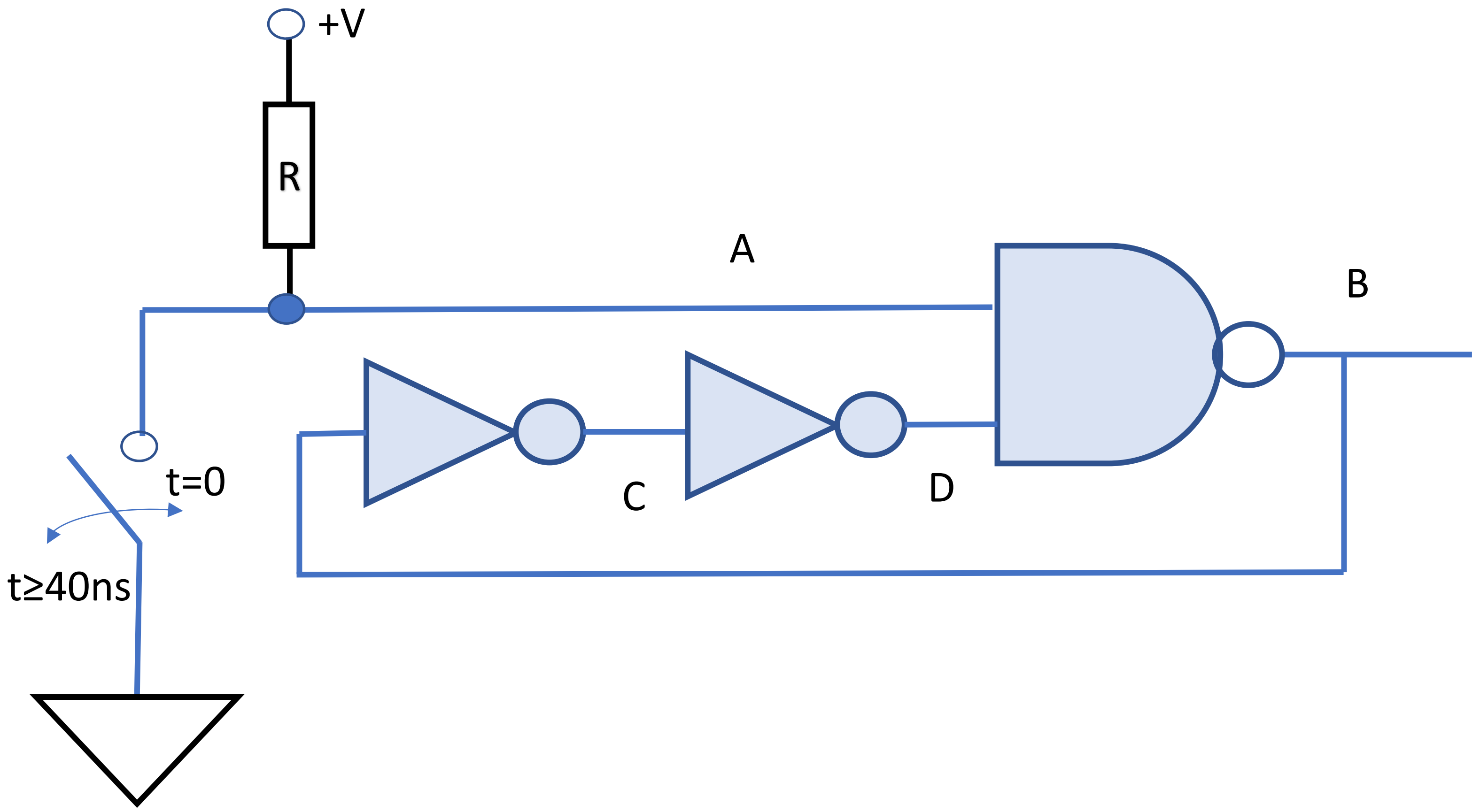
Assume propagation delay of gates as 10ns

Switch is closed at **t=0ns**, thus:

A goes to ‘0’ at time t=0ns
B goes to ‘1’ at time t=10ns
C goes to ‘0’ at time t=20ns
D goes to ‘1’ at time t=30ns

Since D=‘1’, A=‘0’, hence:
Output B=‘0’ always for A=‘0’ in steady state

Pulse Shaper Circuit – Case 2



Case 2:

Assume propagation delay of gates as 10ns

Output B was in steady state = '0' while Switch was closed at t=0

Now Switch is opened at t=40ns

So A goes to '1' at t=40ns

B goes to '0' after 10ns at t=50ns

C goes to '1' at t = 60ns

D goes to '0' at t = 70ns

Now D='0' and A='1', hence B='1' at t=80ns

C goes to '0' at t=90ns

D goes to '1' at t=100ns

Since A ='1' and D='1' so B='0' at t=110ns

The cycle will start repeating automatically

We get an **OSCILLATOR**

Time Period of this oscillator is determined by propagation delay of gates

Same behavior can be obtained from a NOR gate circuit with some changes

Glitches and Hazards

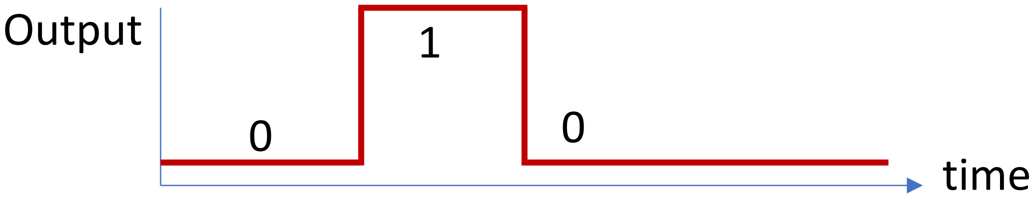
Glitch: An Unwanted Pulse at the Output of a Combinational Logic Circuit. Glitch is dependent upon Inputs and how the circuit is configured

Hazard: A Combinational Logic Circuit with a potential to produce Glitches is called a Hazard.

Possible Reasons:

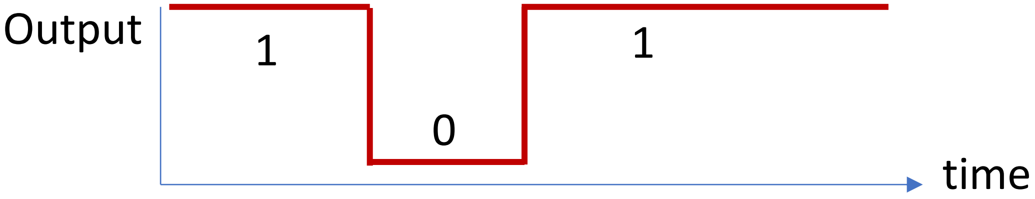
1. Using Un-Stable Input Signals
2. Not Considering Propagation Delays in high-speed designs
3. Using Asynchronous Inputs

Kinds of Hazards



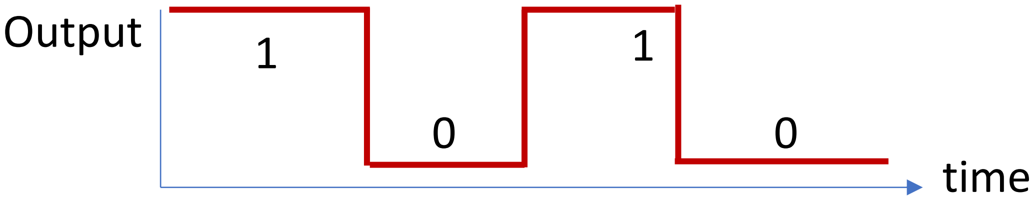
Input Changes cause output to change from ‘0’ to ‘1’ to ‘0’

STATIC ZERO HAZARD



Input Changes cause output to change from ‘1’ to ‘0’ to ‘1’

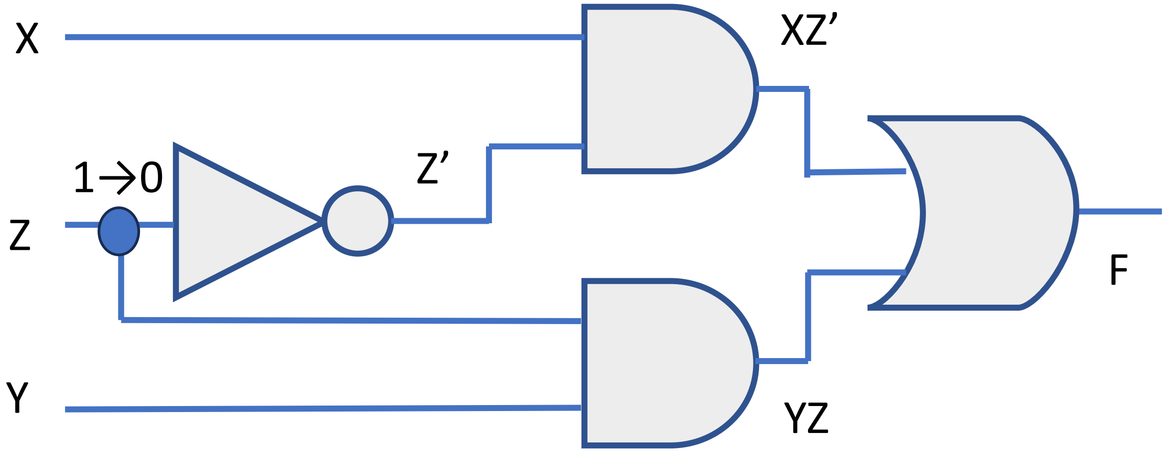
STATIC ONE HAZARD

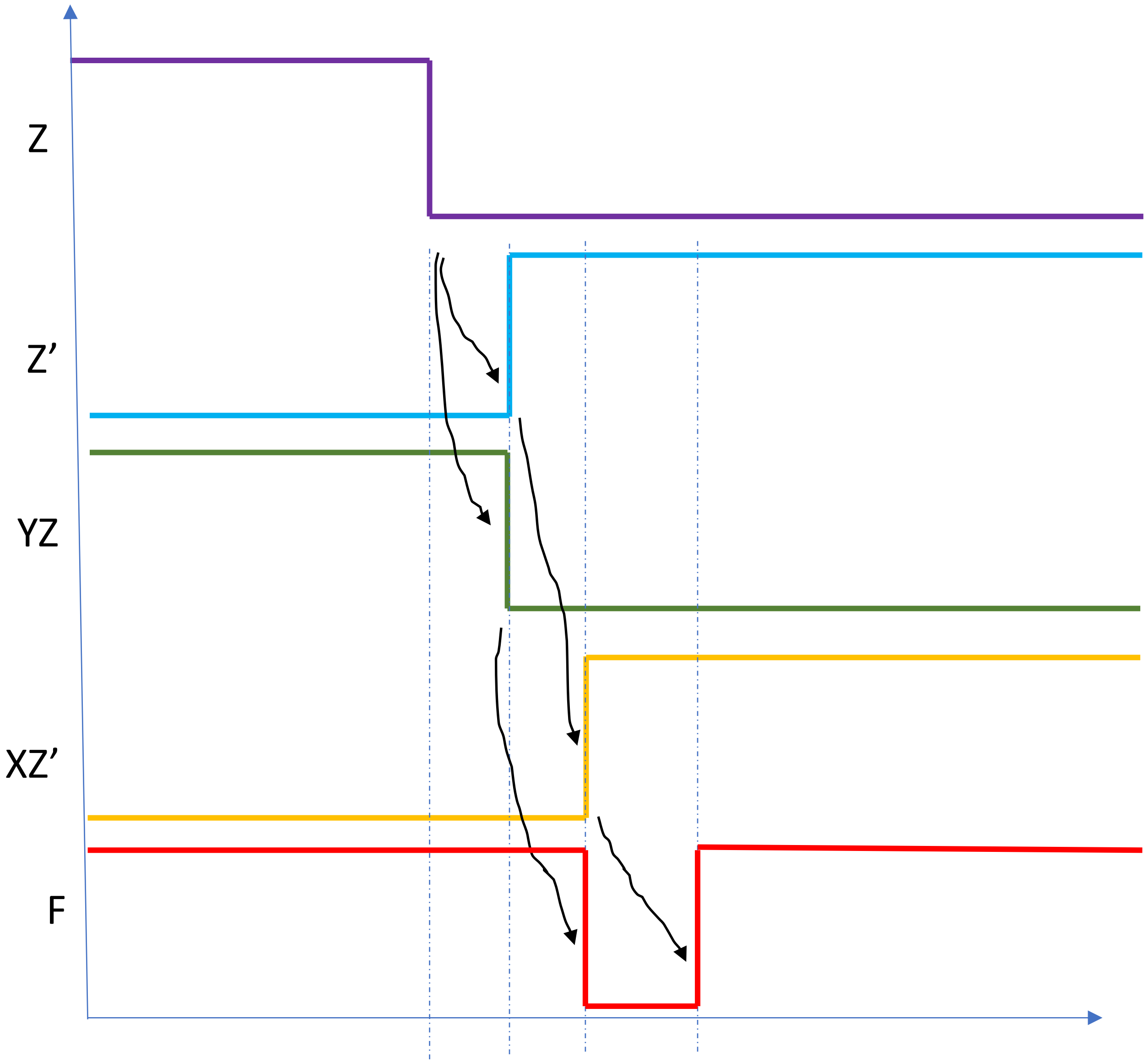


Input Changes cause two or more changes from ‘1’ to ‘0’ to ‘1’ to ‘0’, Or changes from ‘0’ to ‘1’ to ‘0’ to ‘1’

DYNAMIC HAZARD

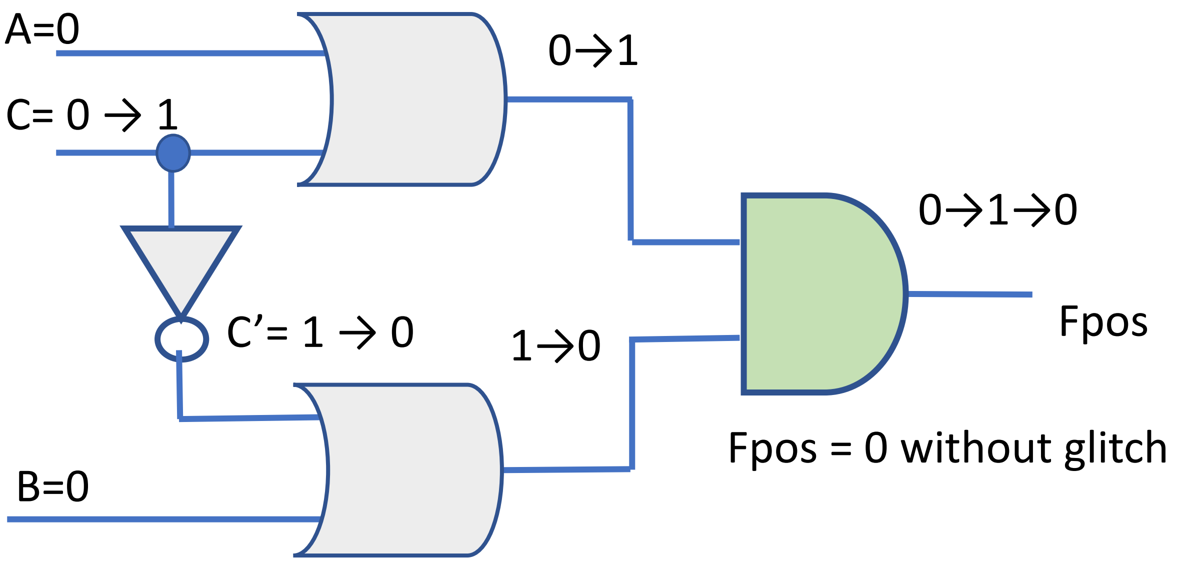
Circuit with Static 1 Hazard

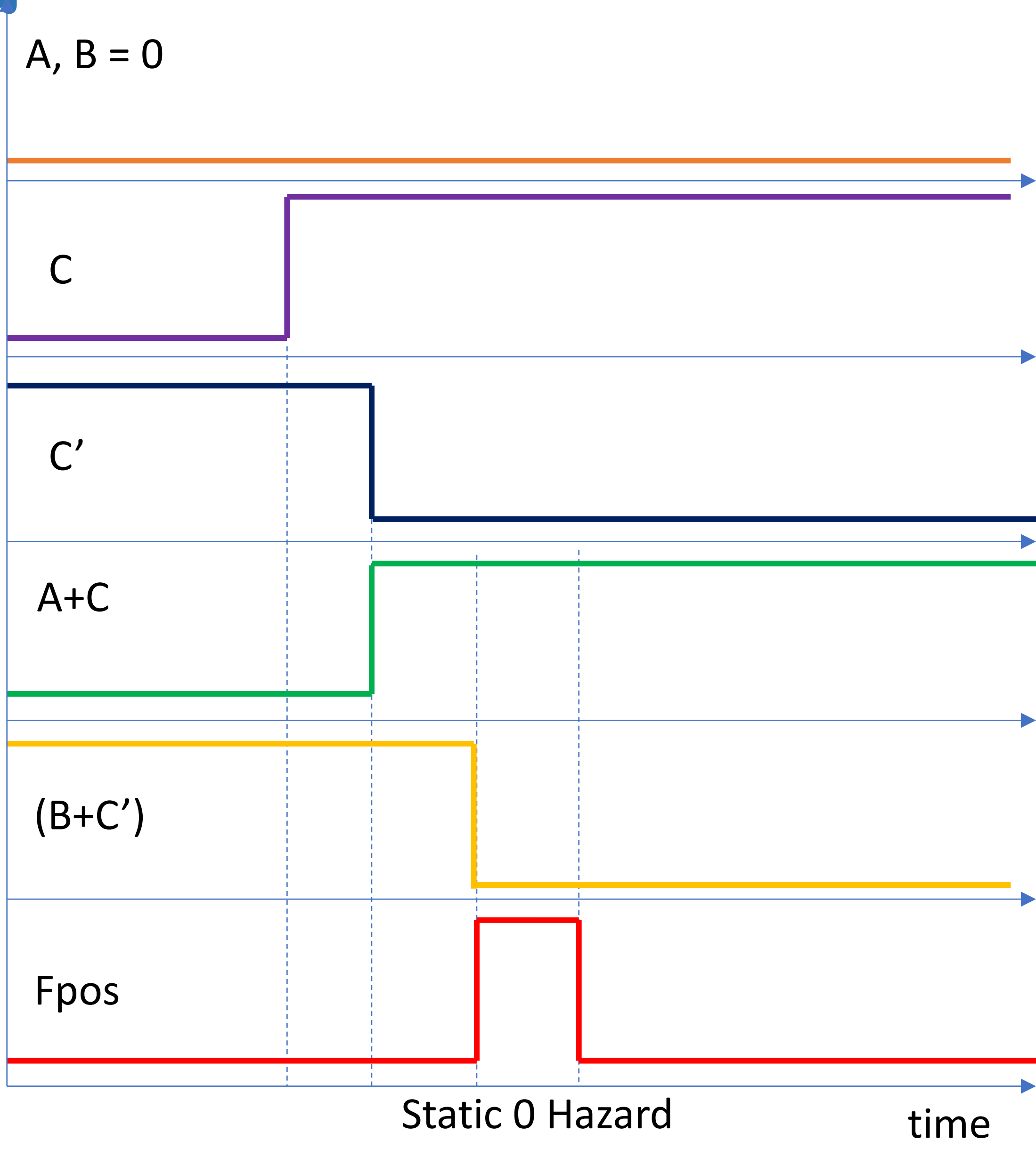




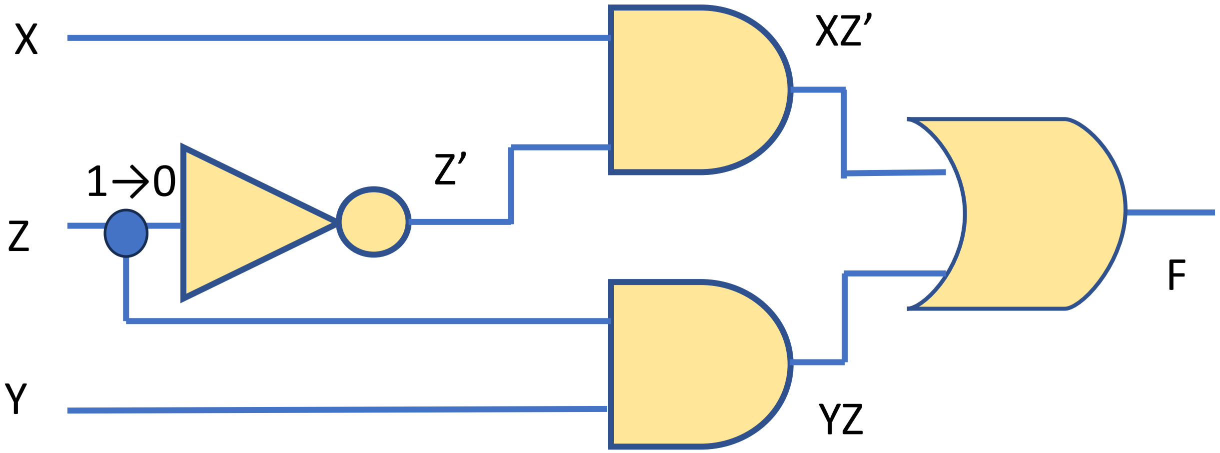
Static 1 Hazard Observed

Example of Static 0 Hazard





K Maps to Identify Hazards



XZ’

Z, XY	00	01	11	10
0	0	0	1	1
1	0	1	1	0

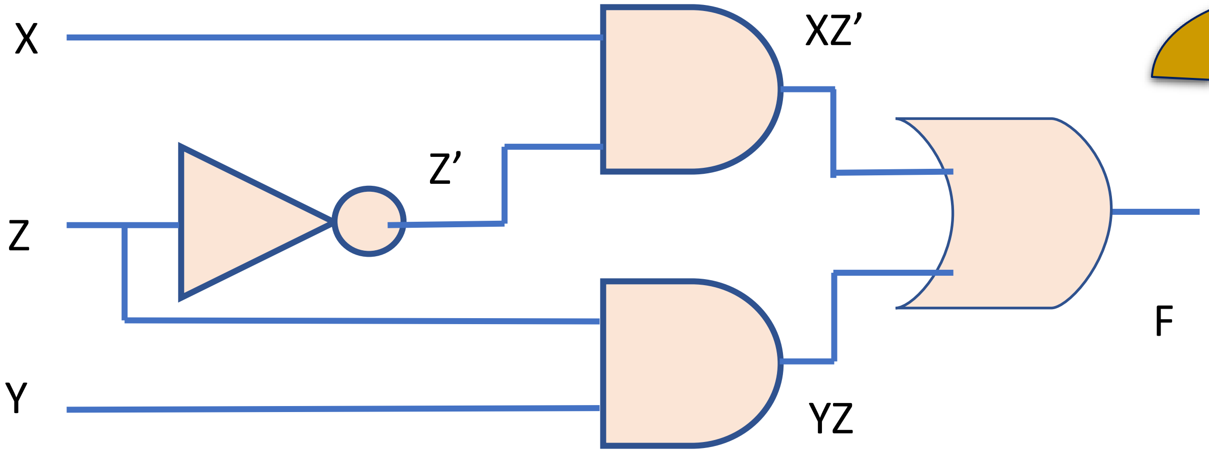
YZ

F=XZ’ + YZ

How to Know about Hazards?

- A properly designed two level SOP (AND-OR) circuit has no Static-0 Hazard
- This type of SOP circuits can have Static-1 Hazards
- Look at the K-Map again and we notice that there is no single product term that covers the inputs XYZ=111 and XYZ=110. Thus glitch to 0 is possible if the AND gate covering the other combination goes to 1.
- To Eliminate Such Hazards:
- Include an extra product term (AND gate) to cover the hazard input. This is where the adjacent 1s exist in K-Maps but are not covered. This is called ‘Adding a Consensus Term’

Hazard Free two level SOP Circuit



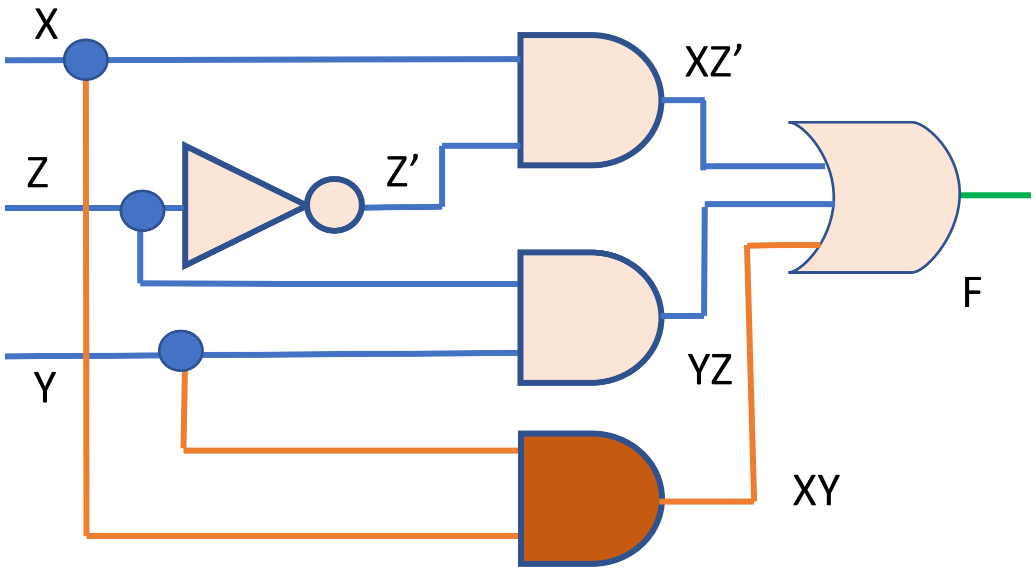
Z, XY	00	01	11	10
0	0	0	1	1
1	0	1	1	0

XZ'

YZ

Consensus Term XY

F including Consensus Term = XY + YZ + XZ'



Final Hazard Free Circuit
Including Extra Consensus Circuit

The Adjacent 1s in K-Map are now Covered

Using K-Map to Identify Static 1 Hazard in 4 input variables

AB, CD	00	01	11	10
00	0	1	1	0
01	1	1	0	0
11	1	1	1	1
10	0	0	1	1

Given K-Map with Minimal Grouping

Identify the Hazards

Adjacent 1s that are not in the same group

K-Map Groups to Eliminate Static 1 Hazard

XY'Z'

YZ, WX	00	01	10	11
00	0	1	1	0
01	1	1	0	0
11	1	1	1	1
10	0	0	1	1

W'Z

WY

W'XY'

WXZ'

AB, CD	00	01	10	11
00	0	1	1	0
01	1	1	0	0
11	1	1	1	1
10	0	0	1	1

YZ

Minimal Expression:

F=XY'Z' + W'Z + WY

Hazard Free Expression:

F=XY'Z' + W'Z + WY + W'XY' + YZ + WXZ'

K-Map Grouping to Eliminate Static 0 Hazard

POS = Grouping of Zeros

AB, CD	00	01	10	11
00	1	1	0	0
01	1	1	1	1
11	0	0	1	1
10	0	0	0	0

(B + C’)

(A’ + C)

Minimal Mapping without Hazard Consideration

F=(A’ + C) (B + C’)

AB, CD	00	01	10	11
00	1	1	0	0
01	1	1	1	1
11	0	0	1	1
10	0	0	0	0

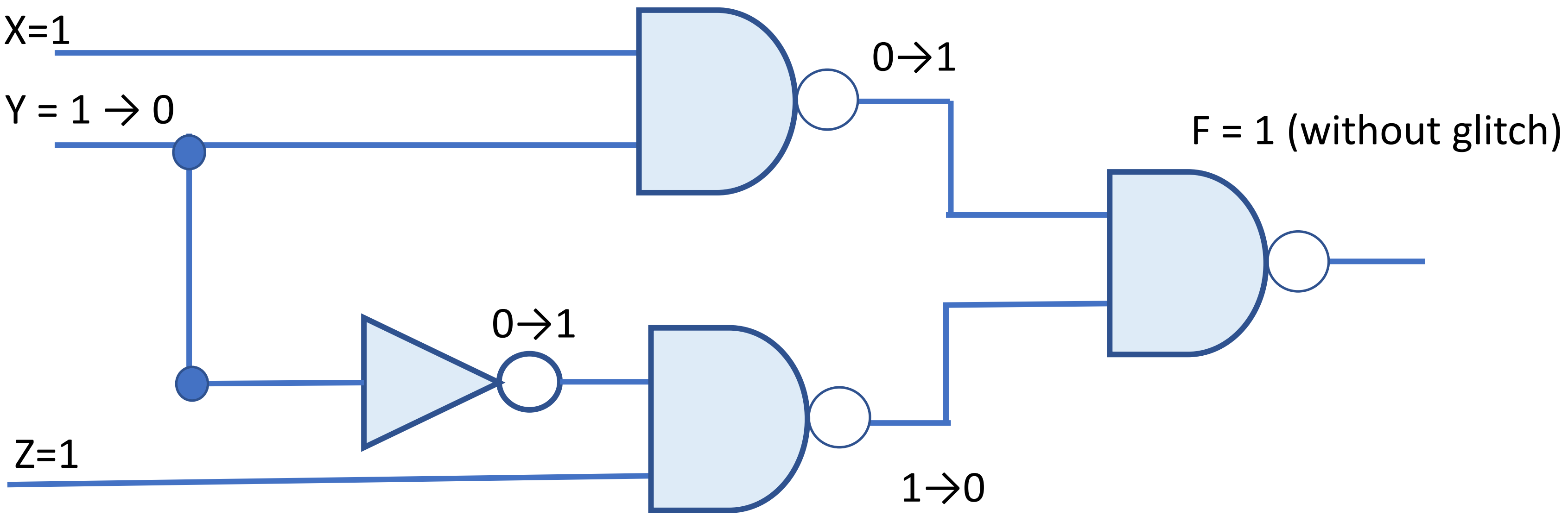
(A’+B)

Additional Cover for Static 0 Hazard prevention

F=(A’ + C) (B + C’) (A’ + B)

Now free from Static 0 Hazard

Example of Static 0 Hazard



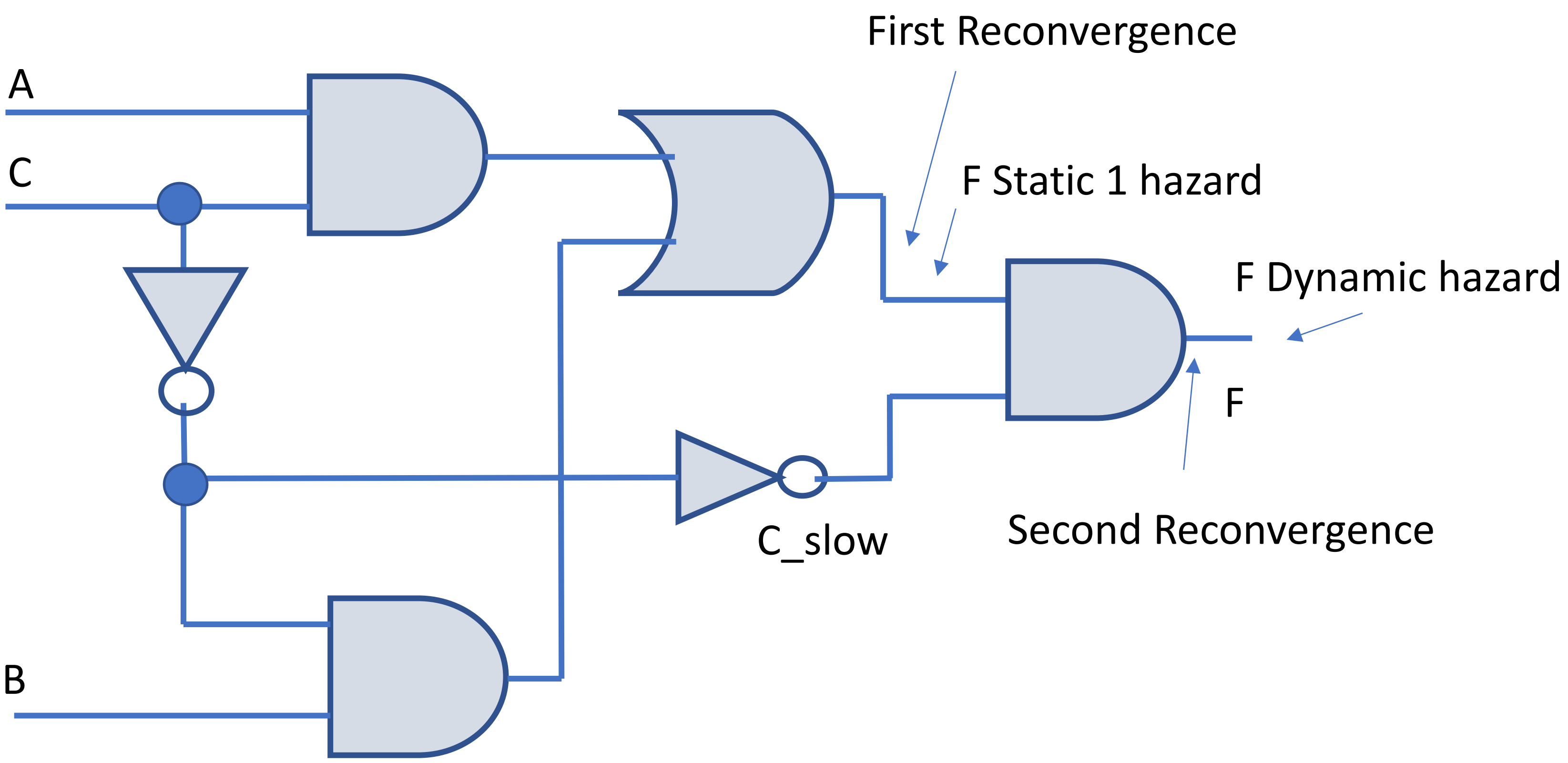
F=(X+Y').(Y+Z)

When Y changes from 1 to 0, both inputs of Nand Gate F may be equal to 1, Causing the output to momentarily go to 0 when it should have stayed at 1.

Dynamic Hazards

- Dynamic Hazard is the possibility of an output changing more than once as the result of a single input transition.
- These can occur if there are multiple paths with different delays from the input to the output
- Dynamic Hazards do not occur in properly designed two level AND-OR or OR-AND Circuits.
- Thus remove all Static-1 and Static-0 Hazards in the two-level SOP or POS design and the possibility of Dynamic Hazards is minimized.

Circuit containing Dynamic Hazard



Try changing
ABC from 110 to 111

Solution: Make K Map and add redundant cover for C

Redundant Circuit to remove Dynamic Hazard