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EE 421L / CS 425 – Digital System Design **Laboratory**

(Fall 2024)

Instructor	Dr. Shahid Masud
Room No. (Labs)	Lab 9-2C1 Lifts Area, Level 2, SSE Building
Office Hours	Mon, Tue, 10 am – 11:00 am
Email	smasud@lums.edu.pk;
Telephone	8199
Secretary/TA	TBA
TA Office Hours	TBA
Course URL (if any)	LMS will be used
Support Services	LUMS offers a range of academic and other services to support students. These are mentioned below, and you are encouraged to use these in addition to in-class assistance from course staff. For a complete list of campus support services available for you click here (https://advising.lums.edu.pk/#supportservices)

Course Details	
Credit Hours	1 (Co-Requisite lab course with EE 421 / CS 425 Digital System Design)
Core	MS EE (Electronics and Embedded Systems Stream), MS DES (Digital Embedded Systems)
Elective	BS EE / CS, MS EE / CS
Open for Student Category	Senior / MS
Closed for Student Category	Freshman / Sophomore / Junior

Course Prerequisite(s)/Co-Requisite(s)
Pre-requisites: EE 324 OR CS 225 OR CS 320/EE320 OR GRAD Standing **Co-requisites: EE 421/CS 325 (Theory)**

Course Catalog Description
This lab course is designed to supplement the theory course EE421 / CS 425: Digital System Design. The students will learn how to design, simulate, synthesize, and implement concepts and analysis methods introduced in EE 421 using modern EDA tools (E.g. Xilinx ISE and Questa / ModelSim) and Xilinx FPGA boards. Basic understanding of hardware descriptive language (HDL) i.e., *SystemVerilog* will be very useful in successful completion of this course. The following topics are covered: Application of *SystemVerilog* to model digital systems at gate, dataflow, and behavioral level. Usage of FPGA in the laboratory exercises as a vehicle to understand complete design flow of an integrated circuit (IC). Design and implementation of digital system building blocks such as arithmetic circuits, data paths, FSM controllers, I/O modules/interfacing, UARTs, frequency generators, memories, etc. is included. Design project involving original design and implementation of any problem in the field of communication, health sector, computer architecture, energy sector, etc. on FPGA boards will be completed. An introduction to *UVM* testing methodology is included.

Course Offering Details						
Lecture(s)	Nbr of Lec(s) Per Week	X	Duration	X	Timings and Venue	X
Recitation (per week)	Nbr of Rec(s) Per Week	X	Duration			
Lab (if any) per week	Nbr of Session(s) Per Week	1	Duration	3:00 Hrs.		
Tutorial (per week)	Nbr of Tut(s) Per Week	X	Duration			

Course Teaching Methodology (Please mention following details in plain text)
• Teaching Methodology: This course will be offered in In-Person setting. • Lecture details: 100% On-Campus interaction as per University's COVID-related SOPs or other restrictions.

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Assessed Course Learning Outcomes	
EE421L	The students should be able to:
CLO1:	Describe, Simulate and debug combinational and sequential digital systems using *SystemVerilog* hardware description language.
CLO2:	Understand EDA tools and design flow for simulation and FPGA design of digital systems.
CLO3:	Implementation, Synthesis and testing of digital systems on FPGA platforms.

Course Learning Relation to EE Program Outcomes

EE/421 CLOs	Related PLOs	Levels of Learning	Teaching Methods	CLO Attainment Assessed in
CLO1	PLO1	Cog-3	Instruction, Lab Manual	Lab Task / Midterm
CLO2	PLO3	Cog-4	Instruction, Lab Manual	Lab Task / Lab Project
CLO3	PLO1	Psy-3	Instruction, Lab Manual	Lab Task

Grading Breakup and Policy

- **Lab Completion (10 to 11 Labs): 50%**
  - Lab Attendance (1% each lab)
  - TA grades the Task Completion (2% each lab)
  - Submitting Reports and Observations, as required (2% each lab)
- **Lab Projects (1 to 2): 30% (Breakup as below)**
  - ***SystemVerilog* coding and testbench**
  - **Simulation**
  - **Synthesis**
  - **FPGA prototyping**
  - **Project report**
  - **Presentation**
- **Lab Midterm Exam: 20%**

*Note: The lab component for MS students will be included in the final grade of theory as explained in the theory class!

Campus supports & Key university policies

Campus Supports

Students are strongly encouraged to meet course instructors and TA's during office hours for assistance in course-content, understand the course's expectations from enrolled students, etc. Beyond the course, students are also encouraged to use a variety of other resources. (Instructors are also encouraged to refer students to these resources when needed.) These resources include Counseling and Psychological Services/CAPS (for mental health), LUMS Medical Center/LMC (for physical health), Office of Accessibility & Inclusion/ OAI (for long-term disabilities), advising staff dedicated to supporting and guiding students in each school, online resources (https://advising.lums.edu.pk/advising-resources), etc. To view all support services, their specific role as well as contact information click here (https://advising.lums.edu.pk/#supportservices).

Academic Honesty/Plagiarism

LUMS has zero tolerance for academic dishonesty. Students are responsible for upholding academic integrity. If unsure, refer to the student handbook and consult with instructors/teaching assistants. To check for plagiarism before essay submission, use similarity@lums.edu.pk. Consult the following resources: 1) Academic and Intellectual Integrity (http://surl.li/gpvwb), and 2) Understanding and Avoiding Plagiarism (http://surl.li/gpvwo).

LUMS Academic Accommodations/ Petitions policy

Long-term medical conditions are accommodated through the Office of Accessibility & Inclusion (OAI). Short-term emergencies that impact studies are either handled by the course instructor or Student Support Services (SSS). For more information, please see Missed Instrument or 'Petition' FAQs for students and faculty (https://rb.gy/8sj1h)

LUMS Sexual Harassment Policy

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LUMS and this class are a harassment-free zone. No behavior that makes someone uncomfortable or negatively impacts the class or individual's potential will be tolerated.

To report sexual harassment experienced or observed in class, please contact me. For further support or to file a complaint, contact OAI at oai@lums.edu.pk or harassment@lums.edu.pk. You may choose to file an informal or formal complaint to put an end to the offending behavior. You can also call their Anti-Harassment helpline at 042-35608877 for advice or concerns. *For more information: Harassment, Bullying & Other Interpersonal Misconduct: Presentation (http://surl.li/gpvwt)*

COURSE OVERVIEW			
Lab/Week	**Topics**	**Readings**	Related CLO
1.	Structural and Modular *SystemVerilog* coding, Data types, Ports, Instantiation*	Lab Manuals / Books	CLO1/CLO2
2.	Module definition and testbench in *SystemVerilog,* coding using Questa / Modelsim*		
3.	Gate Level and Hierarchical design, high level constructs, enum, generate		
4.	Use of assign, delays, classes, structs, arithmetic and logic operators		
5.	RTL and FSM design in *SystemVerilog*, coding and simulation		
6.	Behaviour modelling, always, loops, conditions, case		
7.	*SystemVerilog* features and Design Examples, ALU, random data, memory arrays		
8.	**Lab Mid Exam – SystemVerilog Simulation**		
9.	Xilinx Synthesis - FPGA implementation of design 1	Lab Manuals / Books	CLO3/CLO4
10.	Xilinx Synthesis - FPGA implementation of design 2		
11.	Optimize logic design (speed, area), placement and routing		
12.	Design Exercise and further FPGA experiments		
13.	Other *SystemVerilog* and *UVM* Concepts, simulation and synthesis		
14.	**Design Project**		
15.			
16.	**Due – Final Report/Presentation and Submission of Project**		
	***Each lab includes cases studies and examples**		

Textbook(s)/Supplementary Readings

Textbook:

1. V Taraate, *SystemVerilog for Hardware Description RTL Design and Verification*, Springer, 2020
2. Ashok B. Mehta, *Introduction to SystemVerilog*, Springer, 2021
3. Donald Thomas, *Logic Design and Verification using SystemVerilog*, Printed by Amazon.com, 2016

Examination Detail	
Midterm Exam	Yes/No: Yes Combine Separate: NA Duration: 120 - 150 minutes Preferred Date: TBA Exam Specifications: TBA
Final Exam	Yes/No: NO Combine Separate: NA Duration: NA Exam Specifications: NA

Prepared by:	**Dr. Shahid Masud**
Date:	**Updated: 6 September 2024**