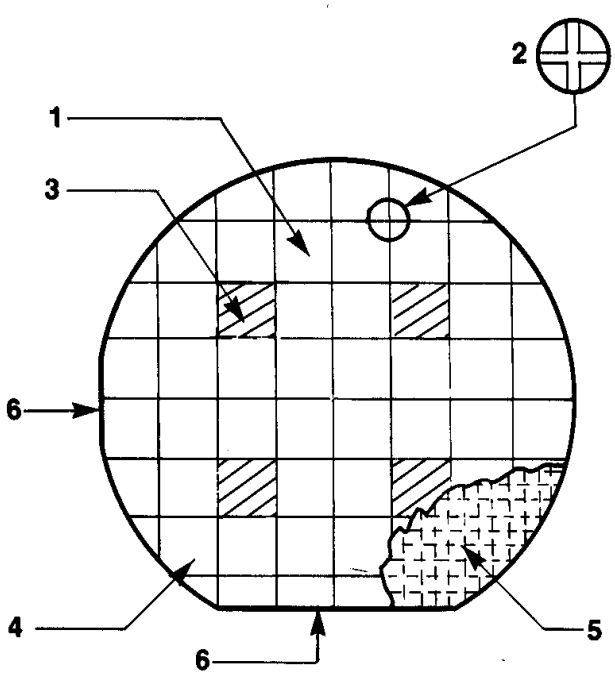
6. CMOS Technology

CMOS Technology

- Basic Fabrication Operations
- Steps for Fabricating a NMOS Transistor
- LOCOS Process
- n-Well CMOS Technology
- Layout Design Rules
- CMOS Inverter Layout Design
- Circuit Extraction, Electrical Process Parameters
- Layout Tool Demonstration
- Appendix: MOSIS, EUROPRACTICE

Wafer Terminology

1. Chip = Die = Microchip = Bar
2. Scribe Lines
3. Engineering Test Die
4. Edge Die
5. Crystal Planes
6. Wafer Flats



Basic Wafer Fabrication Operations

The number of steps in IC fabrication flow depends upon the technology process and the complexity of the circuit

Example:

CMOS n-Well process - 30 major steps, and each major step may involve up to 15 substeps

Only **three basic operations** are performed on the wafer:

- Layering
- Patterning
- Doping

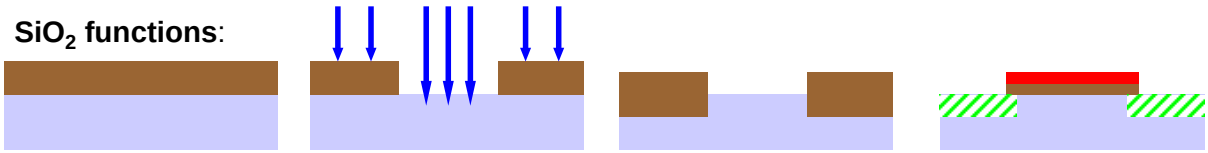
Layering

Grow or deposit thin layers of different materials on the wafer surface

Layers	Technique			
	Thermal oxidation	**ChemicalVapor Deposition (CVD)**	**Evaporation**	**Sputtering**
Insulators	Silicon Dioxide (SiO2)	Silicon Dioxide (SiO2) Silicon Nitrides (Si3N4)		Silicon Dioxide (SiO2) Silicon Monoxide (SiO)
Semiconductors		Epitaxial Silicon Poly Silicon		
Conductors		Dopedpolysilicon Metals Al/SiAlloys Silicides	Metals Alloys	Metals Alloys

Layering - Thermal Oxidation

SiO_2 functions:



Surface passivation | Diffusion barrier | Field oxide | MOS Gate oxide

Natural oxide: silicon will readily grow an oxide (5-10nm) if exposed to oxygen in the air!

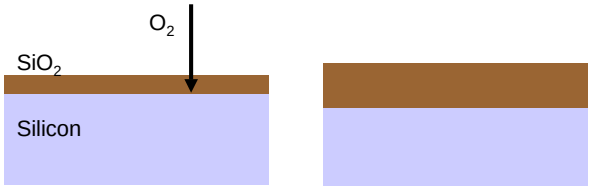
The range for useful oxide thickness: 25nm (MOS gates) - 1500nm (field oxide)

Dry oxidation

$Si + O_2 \rightarrow SiO_2$ (900-1200°C)

700nm oxide: 10hours (1200°C)

Good oxide quality: gate oxide



Wet oxidation (water vapor or steam)

$Si + H_2O \rightarrow SiO_2 + 2H_2$ (900-1200°C)

700nm oxide: 0.65hours (1200°C)

Poor oxide quality: field oxide

Layering - Chemical Vapor Deposition (CVD)

Deposited materials:

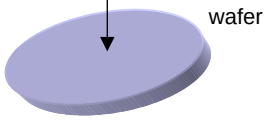
- **Insulators & Dielectrics**: SiO_2, Si_3N_4, Phosphorus Silicate Glass (PSG), Doped Oxide
- **Semiconductors**: Si
- **Conductors**: Al, Cu, Ni, Au, Pt, Ti, W, Mo, Cr, Silicides (WSi_2, $MoSi_2$), doped polysilicon

Basic CVD processing:

- a gas containing an atom(s) of the material to be deposited reacts with another gas liberating the desired material
- the freed material (atom or molecular form) “deposits” on the substrate
- the unwanted products of the chemical reaction leave the reaction chamber

Example: CVD of silicon from silicon tetrachloride

$$SiCl_4 + 2H_2 \rightarrow Si + 4HCl\uparrow$$

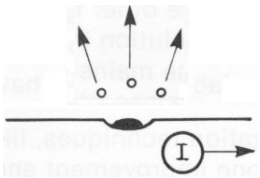


Layering - Evaporation

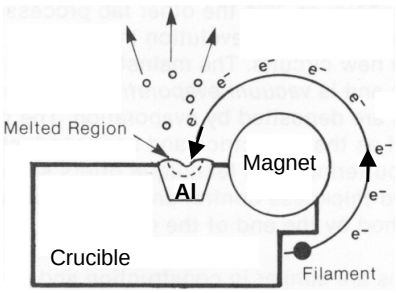
Used to deposit **conductive layers** (**metallization**): Al, Al/Si, Al/Cu, Au, Mo, Pt

When temperature is raised high enough, atoms of solid material (Al) will melt and “evaporate” into the atmosphere and deposit on to the wafer

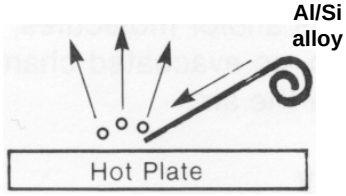
External energy needed to evaporate the metal are provided by:



1.A current flowing through a filament

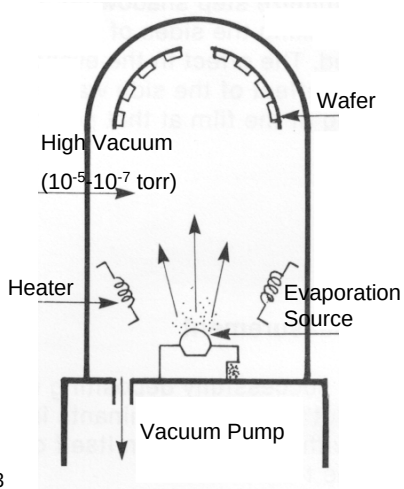


3.Electron beam



2.Flash system

The evaporation take place into an evacuated chamber; otherwise Al would combine with oxygen in air to form Al_2O_3



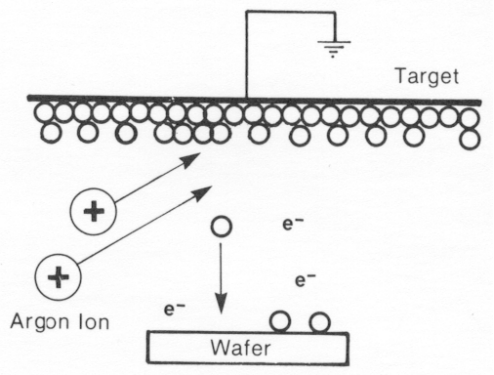
Layering - Sputtering

Used to deposit **thin metal/alloys** films and **insulators**: Al, Ti, Mo, Al/Si, Al/Cu, SiO_2

Sputtering process:

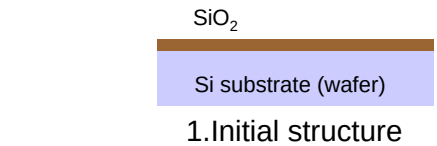
- ionized argon atoms (+) are introduced into an evacuated chamber
- the target (Al) is maintained at negative potential
- the argon ions accelerated towards the negative charge
- following the impact some of the target material atoms tear off
- the liberated material settles on everything in the chamber, including the wafers

The material to be sputtered does not have to be heated



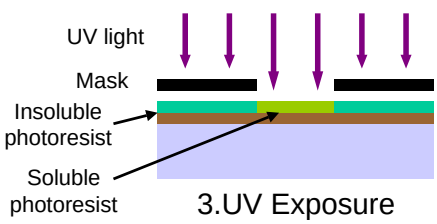
Patterning

- Patterning = Lithography = Masking
- Selective removal of the top layer(s) on the wafers
- Ex.: Process steps required for patterning SiO_2

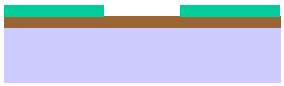


1.Initial structure

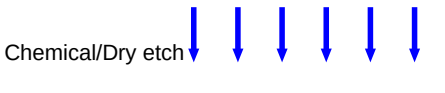
2.Photoresist deposition



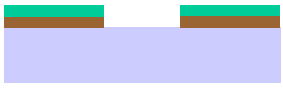
3.UV Exposure



4.Soluble photoresist etching



5.SiO_2 etching

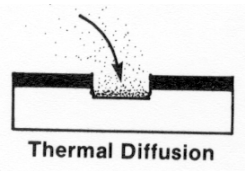


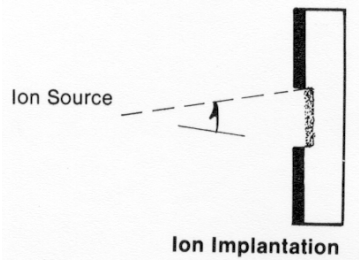
5.SiO_2 etching (end)

6.Photoresist etching

Doping

- Change conductivity type and resistivity on selected regions of wafer
- Doping takes place to the wafer through the holes patterned in the surface layer
- **Two techniques** are used:
  - Thermal diffusion
  - Ion implantation

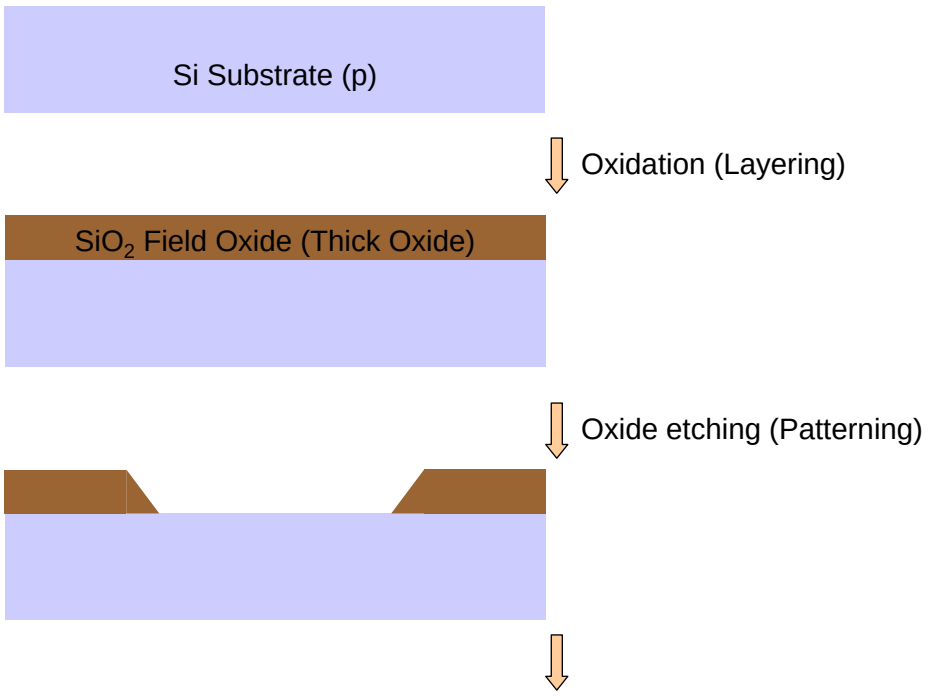




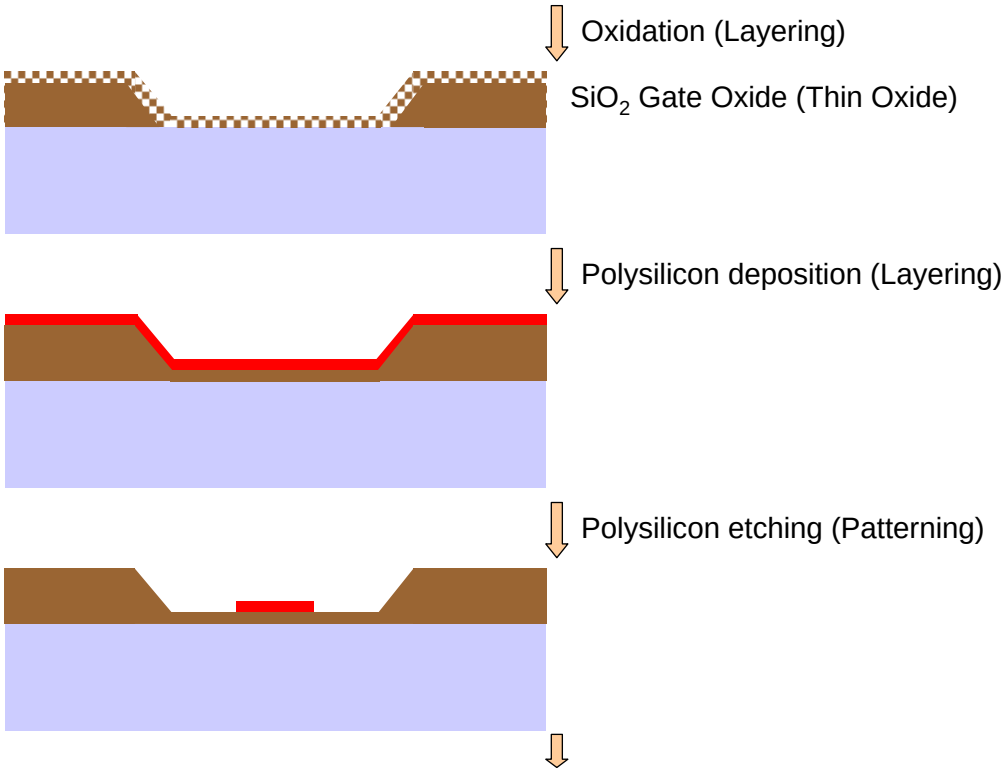
Thermal diffusion:
- heat the wafer to the vicinity of 1000°C
- expose the wafer to vapors containing the desired dopant
- the dopant atoms diffuse into the wafer surface creating a p/n region

Ion implantation:
- room temperature
- dopant atoms are accelerated to a high speed and “shot” into the wafer surface
- an annealing (heating) step is necessary to reorder the crystal structure damaged by implant

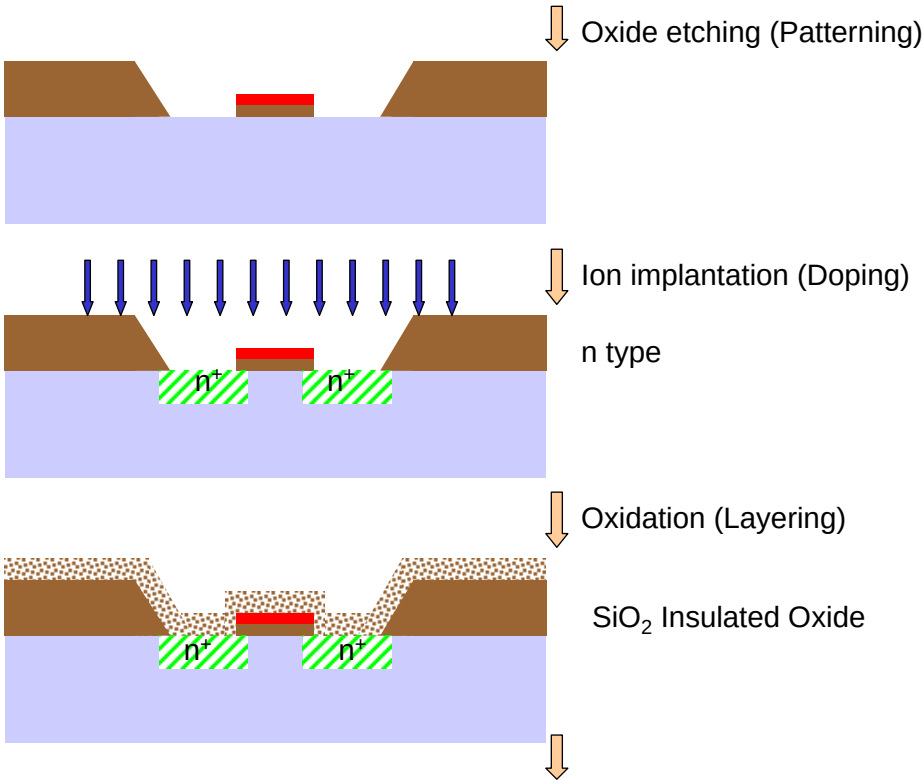
NMOS Transistor Fabrication - process flow (1)



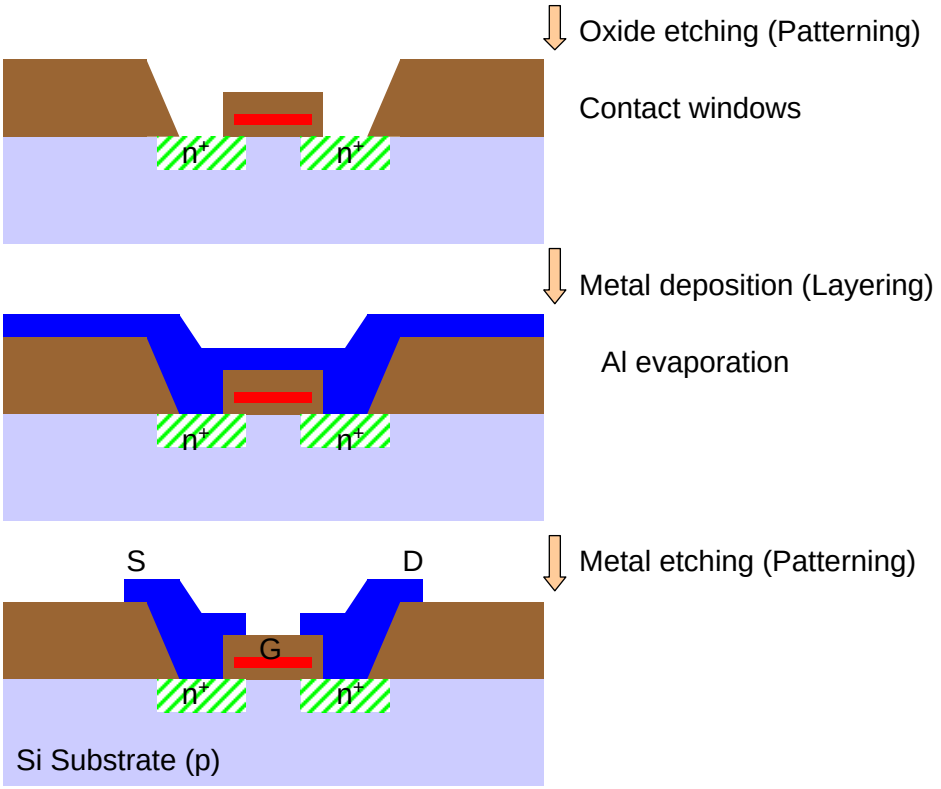
NMOS Transistor Fabrication - process flow (2)



NMOS Transistor Fabrication - process flow (3)



NMOS Transistor Fabrication - process flow (4)



Device Isolation Techniques

MOS transistors must be **electrically isolated** from each other in order to:

- prevent unwanted conduction paths between devices
- avoid creation of inversion layers outside the channel regions
- reduce the leakage currents

Each device is created in dedicated regions - **active areas**

Each active area is surrounded by a field oxide barrier using few techniques:

A) **Etched field-oxide isolation**

1) grow a field oxide over the entire surface of the chip

2) pattern the oxide and define active areas

Drawbacks: -large oxide steps at the boundaries between active areas and field regions!

-cracking of polysilicon/metal subsequent deposited layers!

Not used!

B) **Local Oxidation of Silicon (LOCOS)**

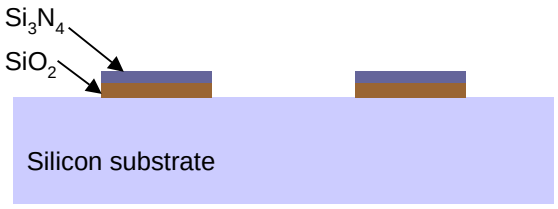
Local Oxidation of Silicon (LOCOS) (1)

More planar surface topology

Selectively growing the field oxide in certain regions - process flow:

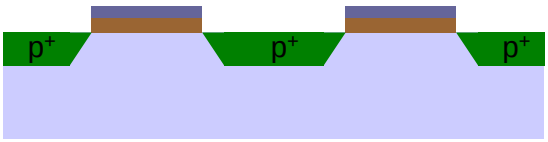
1) grow a thin pad oxide (SiO_2) on the silicon surface

2) define active area : deposition and patterning a silicon nitride (Si_3N_4) layer



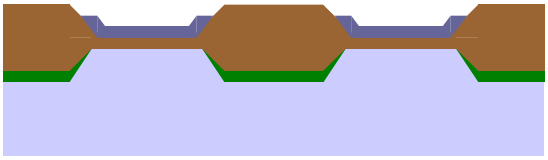
The thin pad oxide - protect the silicon surface from stress caused by nitride

3) channel stop implant: p-type regions that surround the transistors



Local Oxidation of Silicon (LOCOS) (2)

4) Grow a thick field oxide

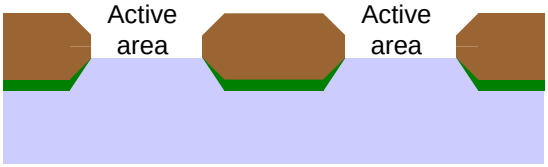


Field oxide is partially recessed into the surface (oxidation consume some of the silicon)

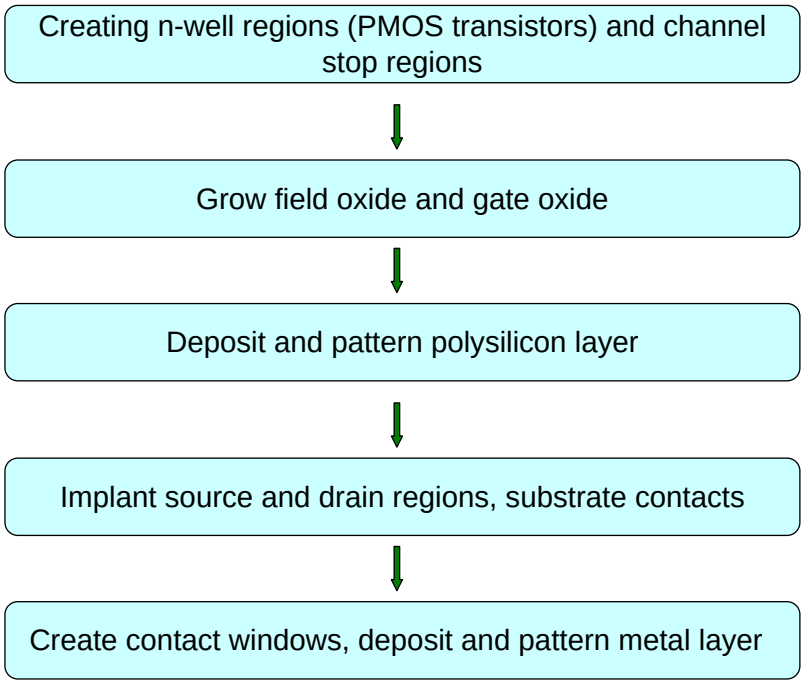
Field oxides forms a **lateral extension** under the nitride layer - **bird`s beak region**

Bird's beak region **limits device scaling** and **device density** in VLSI circuits!

5) Etch the nitride layer and the thin oxide pad layer

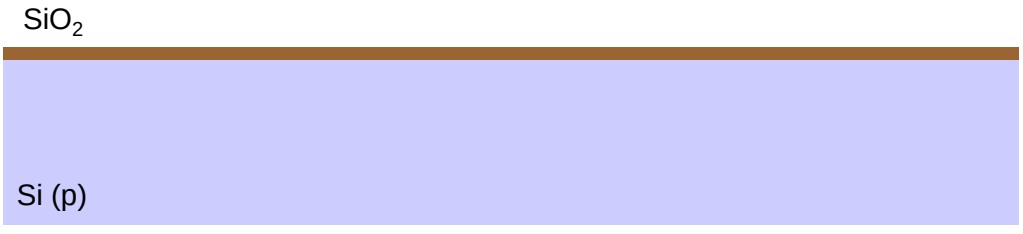


n-Well CMOS Technology - simplified process sequence



n-Well CMOS Technology - Inverter Example

- Process starts with a moderately doped (10^{15} cm^{-3}) p-type substrate (wafer)
- An initial oxide layer is grown on the entire surface (barrier oxide)

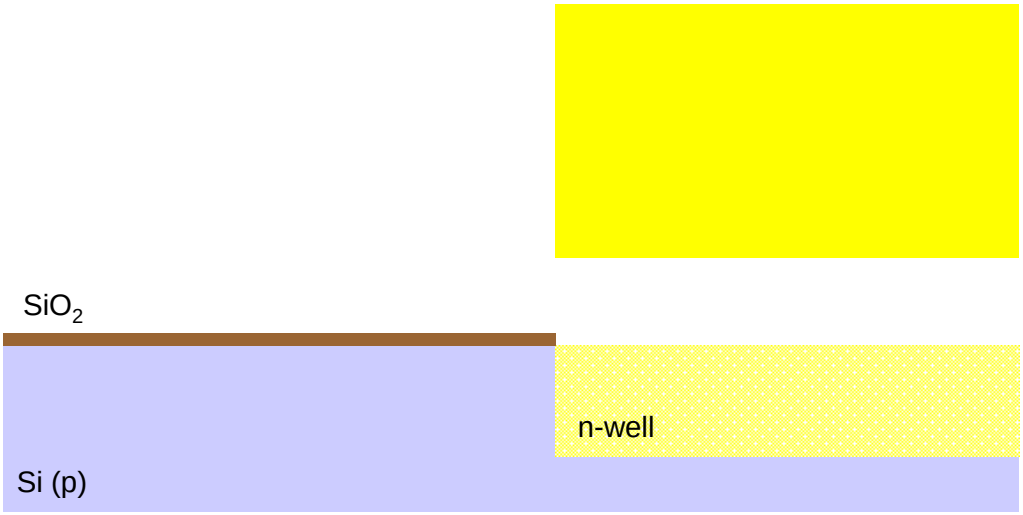


1. **n-Well mask** - defines the n-Well regions

• Pattern the oxide

• Implant n-type impurity atoms (phosphorus) - $10^{16}cm^{-3}$

• Drive-in the impurities (vertical but also lateral redistribution - **limits the density**)



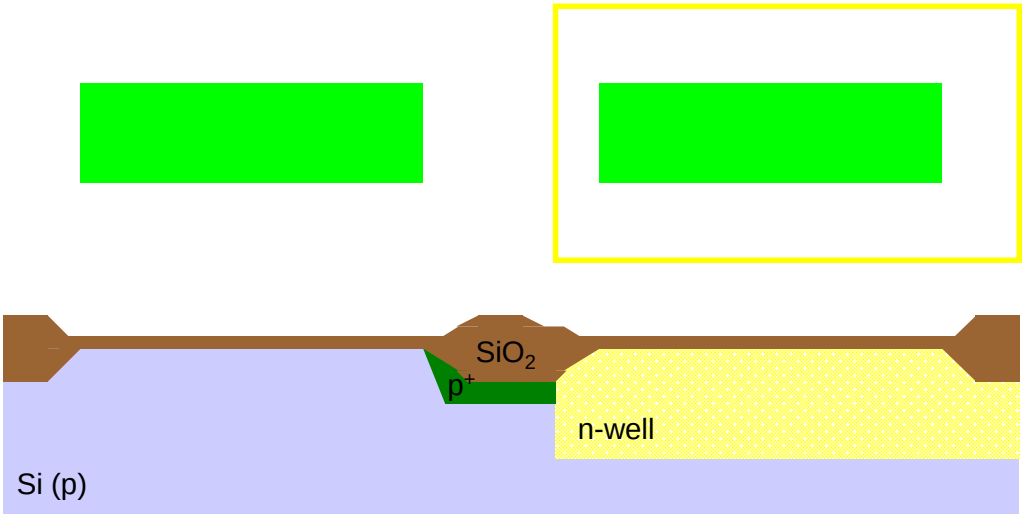
2. **Active area mask** - define the regions in which MOS devices will be created

• LOCOS process to isolate NMOS and PMOS transistors

  • lateral penetration of bird's beak region ~ oxide thickness

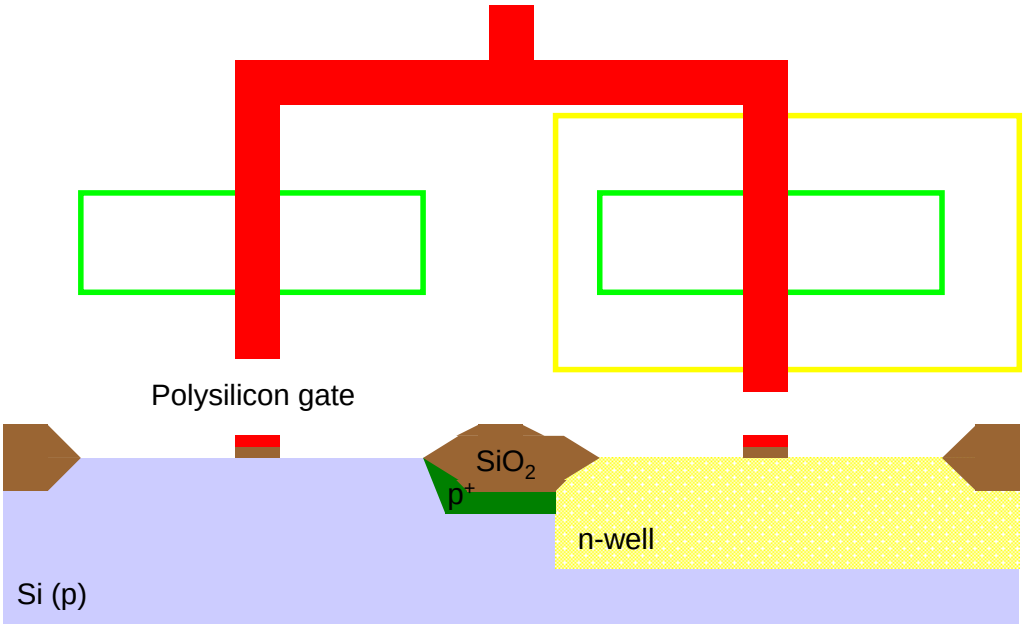
  • channel stop p^+ implants (boron)

• Grow gate oxide (dry oxidation) - only in the open area of active region



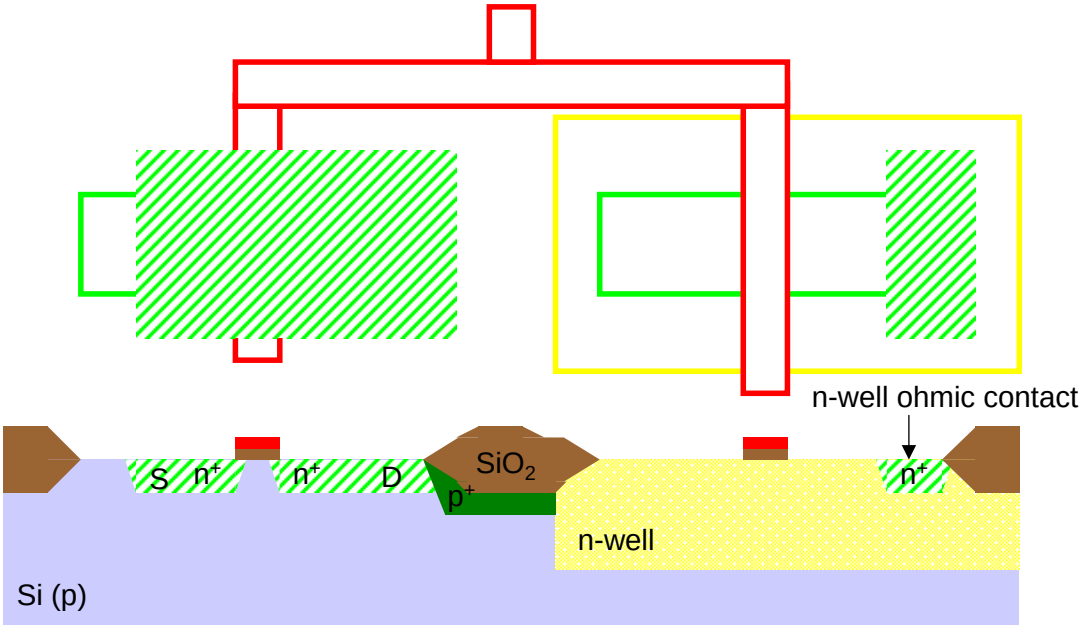
3. **Polysilicon mask** - define the gates of the MOS transistors

- Polysilicon is deposited over the entire wafer (CVD process) and doped (typically n-type)
- Pattern the polysilicon in the dry (plasma) etching process
- Etch the gate oxide



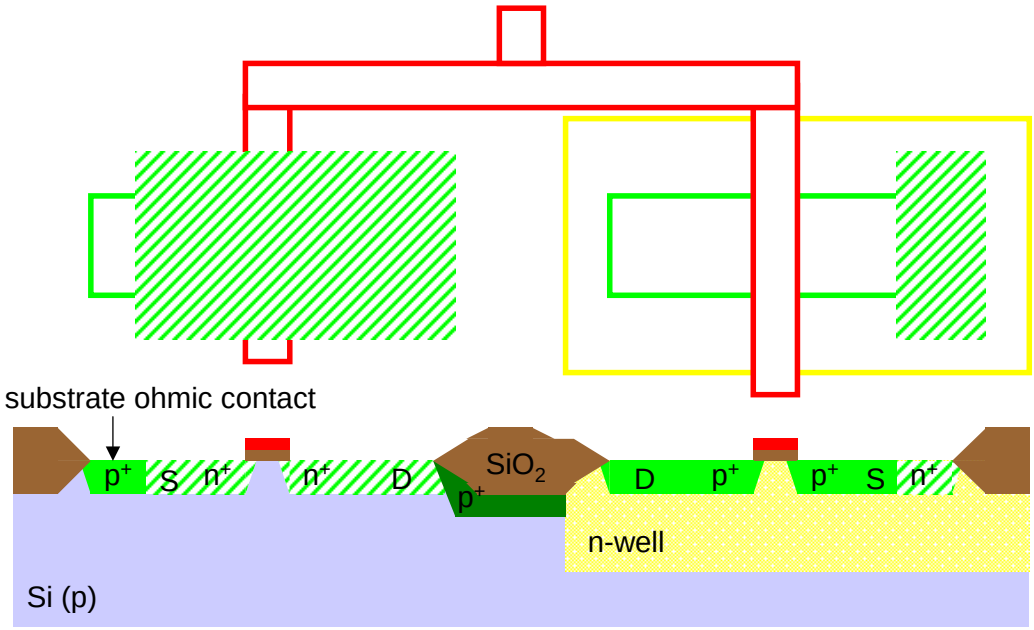
4. **n-Select mask** - define the n^+ source/drain regions of NMOS transistors

- Define an ohmic contact to the n-well
- Implant n-type impurity atoms (arsenic)
- Polisilicon layer protects transistor channel regions from the arsenic dopant

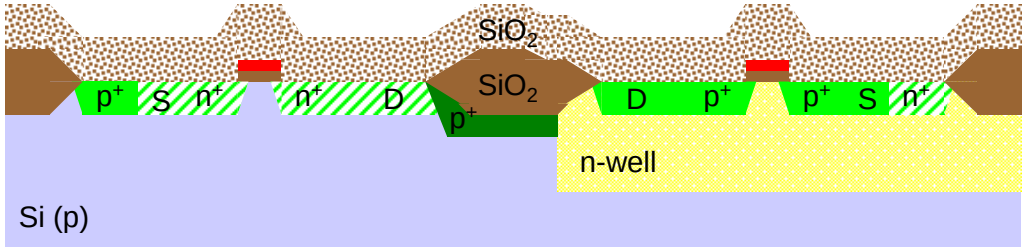


5. **Complement of the n-select mask** - define the p^+ source/drain regions of PMOS transistors

- Define the ohmic contacts to the substrate
- Implant p-type impurity atoms (boron)
- Polisilicon layer protects transistor channel regions from the boron dopant

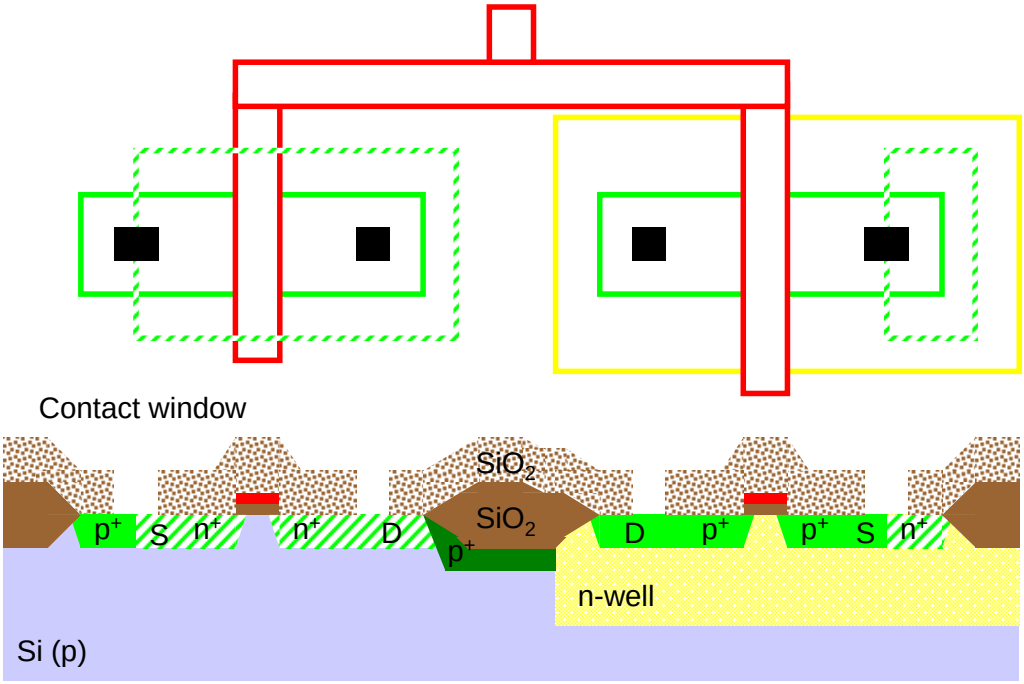


- In the n-well two p^+ and one n^+ regions are created
- After source/drain implantation a short thermal process is performed (annealing):
  - moderate temperature
  - drive the impurities deeper into the substrate
  - repair some of the crystal structure damage
  - lateral diffusion under the gate: overlap capacitances
- Next the SiO_2 **insulated layer** is deposited over the entire wafer area using a CVD technique
- The surface becomes nonplanar: impact on the metal deposition step



6. **Contact mask** - define the contact cuts in the insulating layer

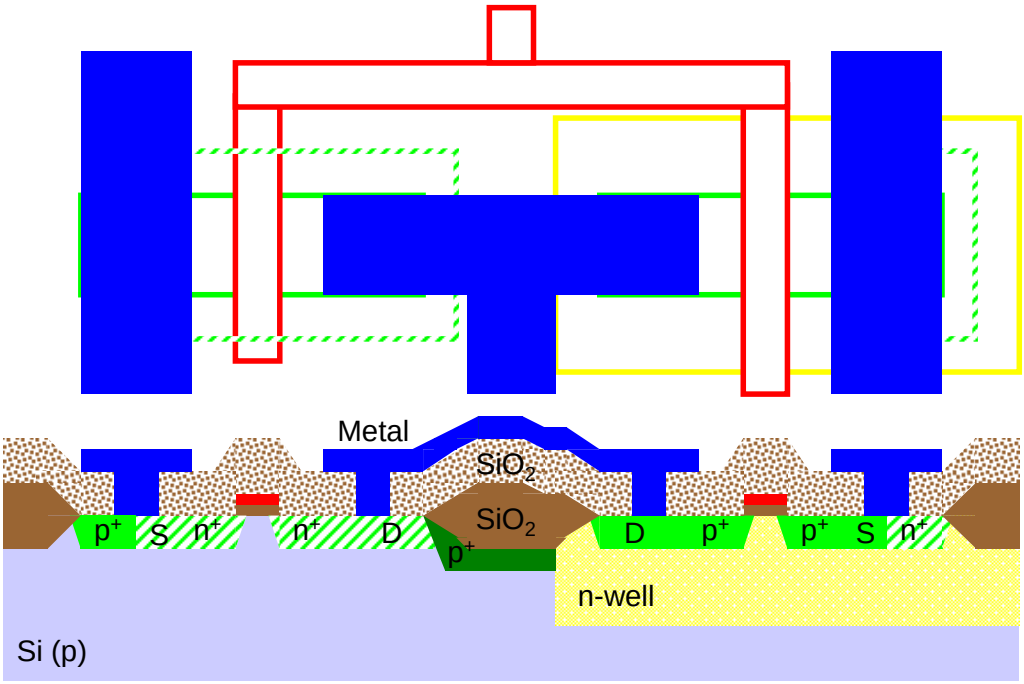
• Contacts to polysilicon must be made outside the gate region (avoid metal spikes through the poly and the thin gate oxide)



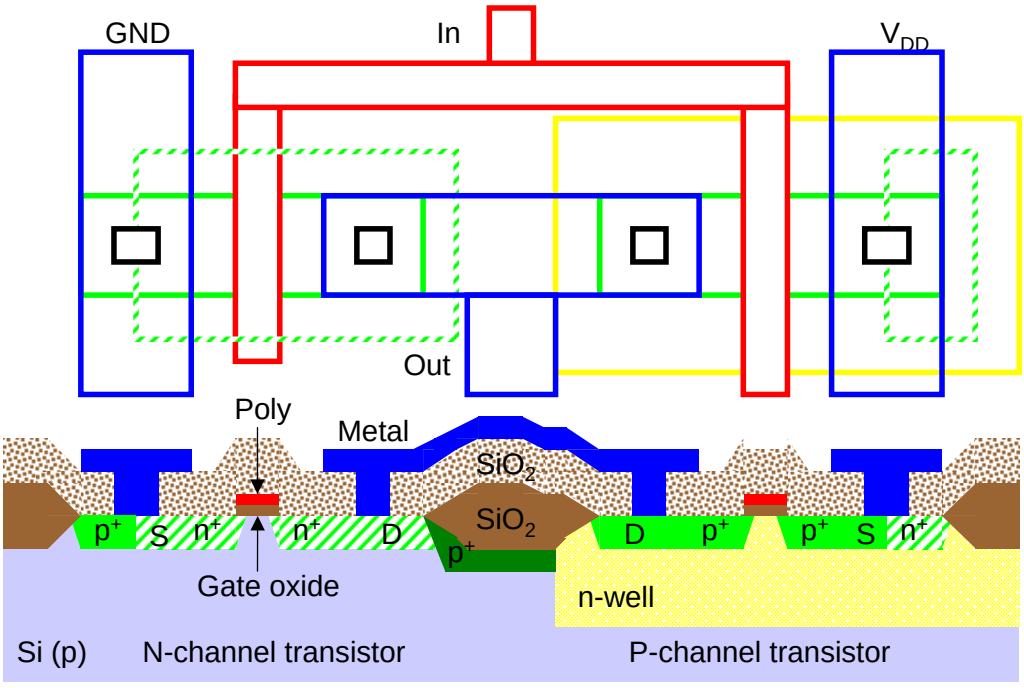
7. **Metallization mask** - define the interconnection pattern

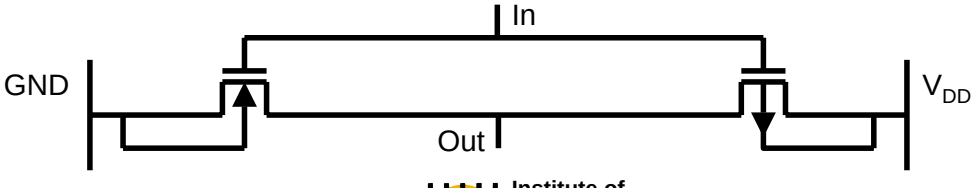
• Aluminum is deposited over the entire wafer (evaporation) and selectively etched

• The step coverage in this process is most critical (nonplanarity of the wafer surface)



- The final step: the entire surface is passivated (overglass layer)
- Protect the surface from contaminants and scratches
- Than opening are etched to the bond pads to allow for wire bonding





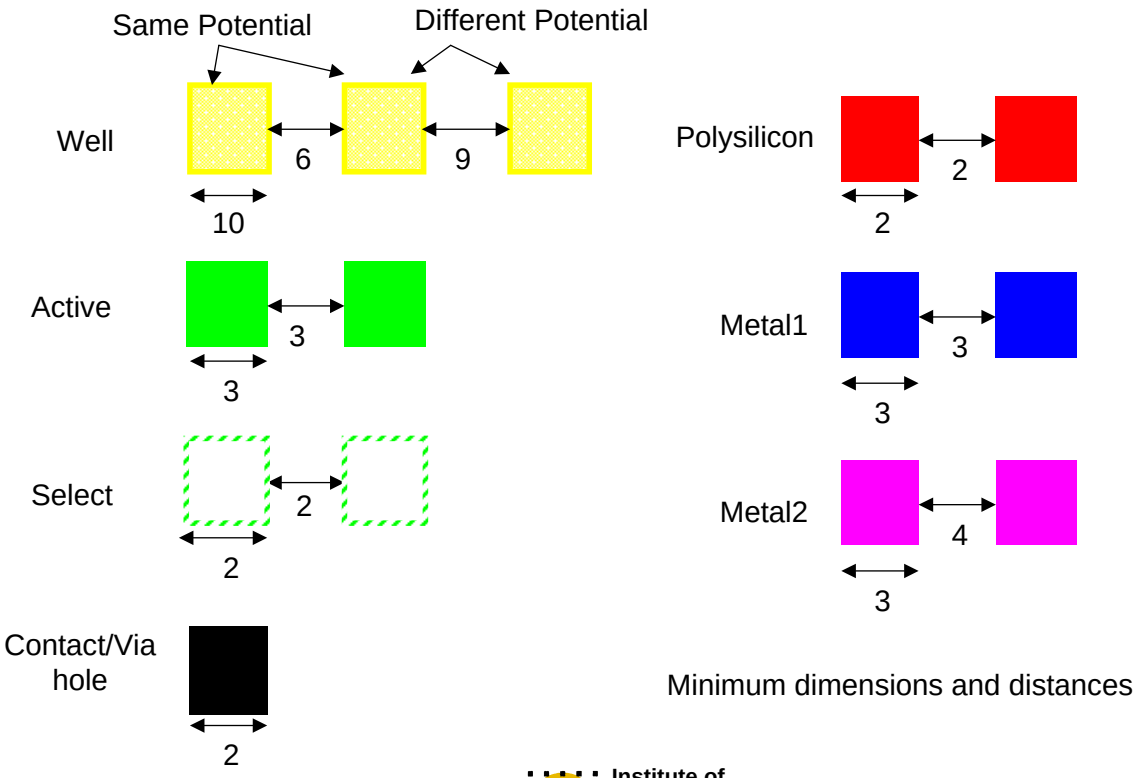
Design Rules

- Interface between designer and process engineer
- Guidelines for constructing process masks
- Unit dimension: minimum line width
- **Scalable design rules** - lambda (λ) parameter:
  - define all rules as a function of a single parameter λ
  - scaling of the minimum dimension: change the value of λ - **linear scaling**!
  - linear scaling is only possible over a limited range of dimensions (1-3μm)
  - are conservative: they have to represent the worst case rules for the whole set
  - for small projects are a flexible and versatile design methodology
- **Micron rules** - absolute dimensions:
  - can exploit the features of a given process to a maximum degree
  - scaling and porting designs between technologies is more demanding: manually or using advanced CAD tools!
- Ex.: Scalable CMOS design rules

CMOS Process Layers

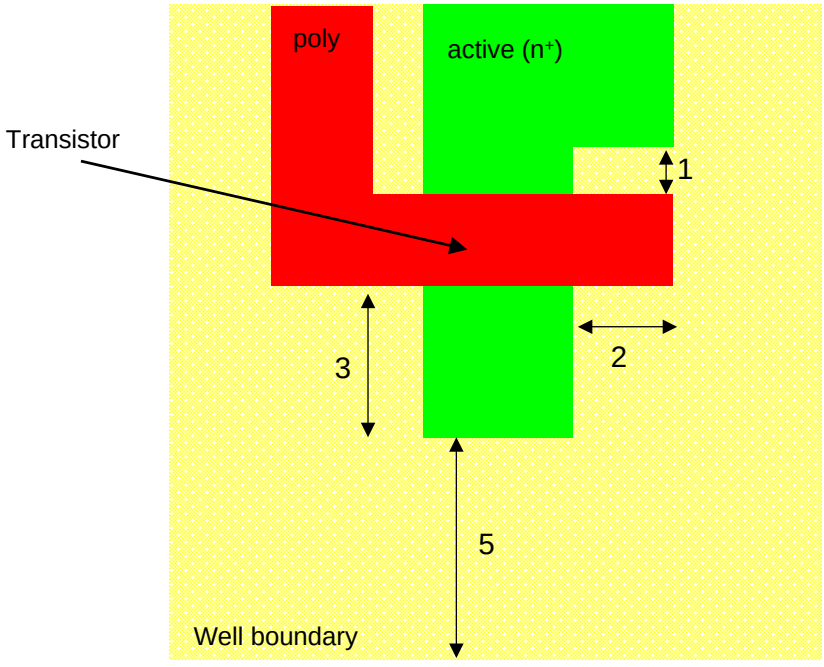
Layer	Color	Representation
Well (p,n)	Yellow	
Active Area (n^+,p^+)	Green	
Select (p^+,n^+)	Green	
Polysilicon	Red	
Metal1	Blue	
Metal2	Magenta	
Contact To Poly	Black	
Contact To Diffusion	Black	
Via	Black	

Intra-Layer Design Rules (λ)

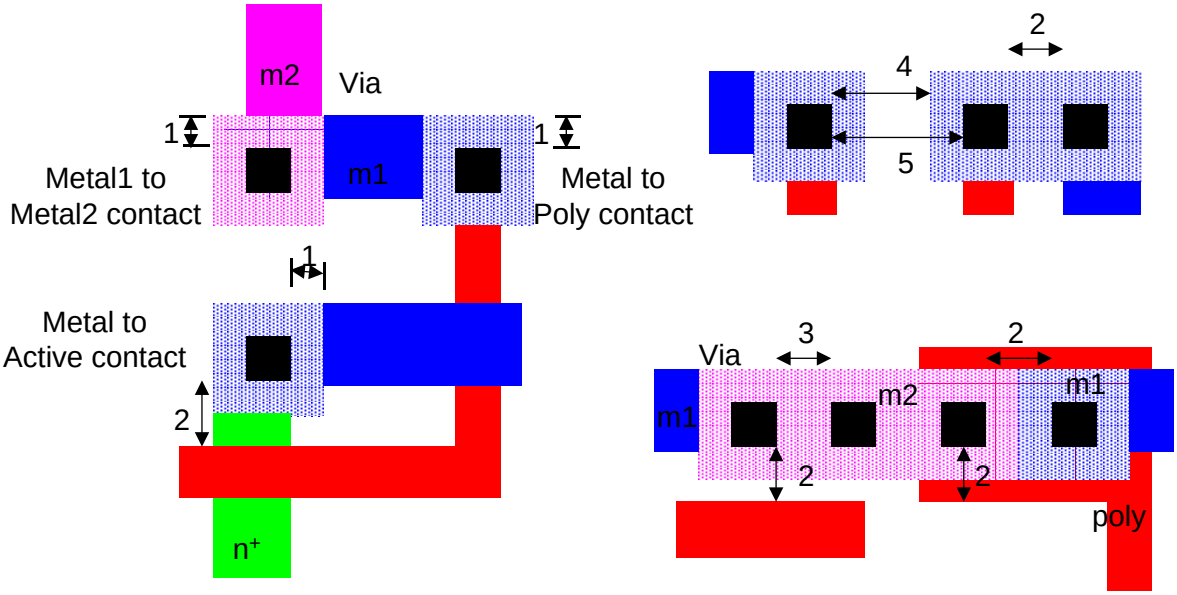


Minimum dimensions and distances

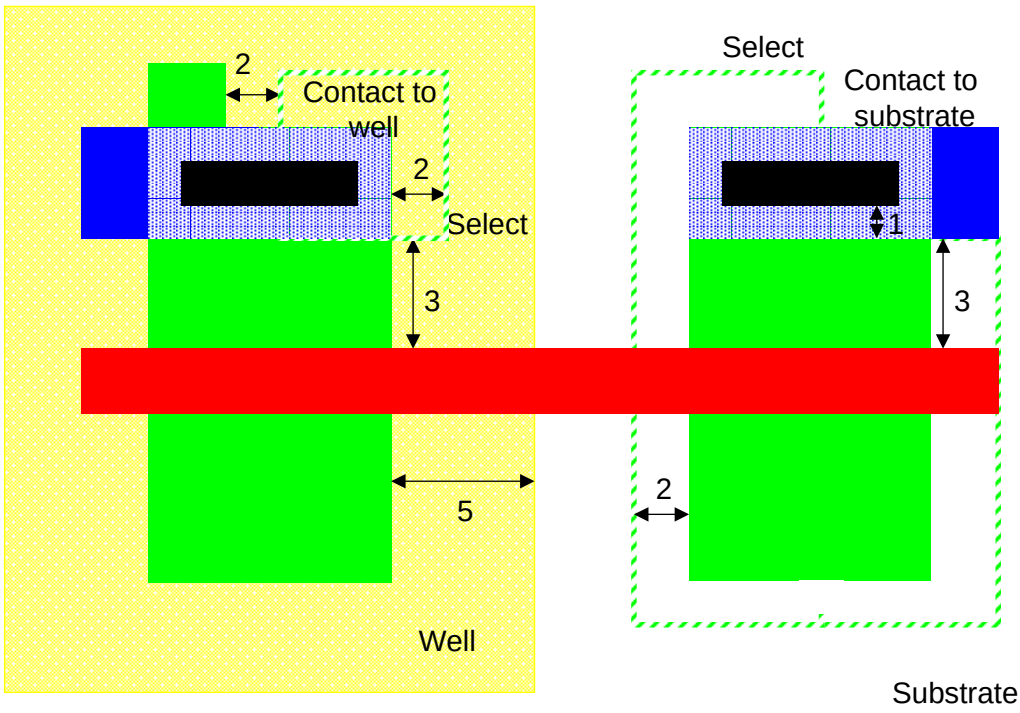
Inter-Layer Design Rules - Transistor Layout (λ)



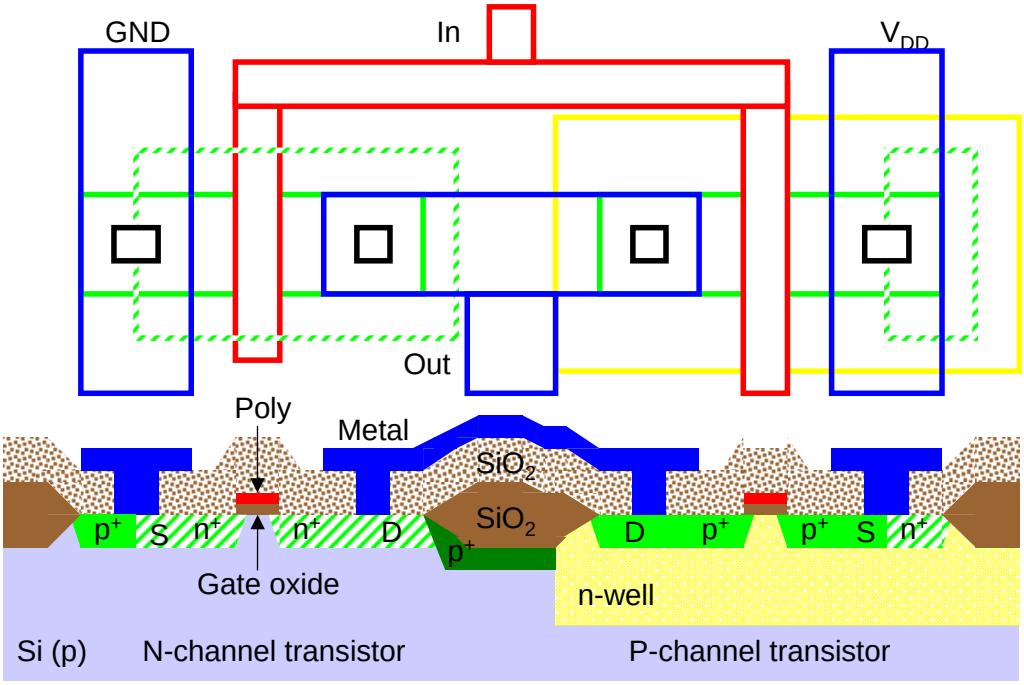
Inter-Layer Design Rules - Contact and Via (λ)



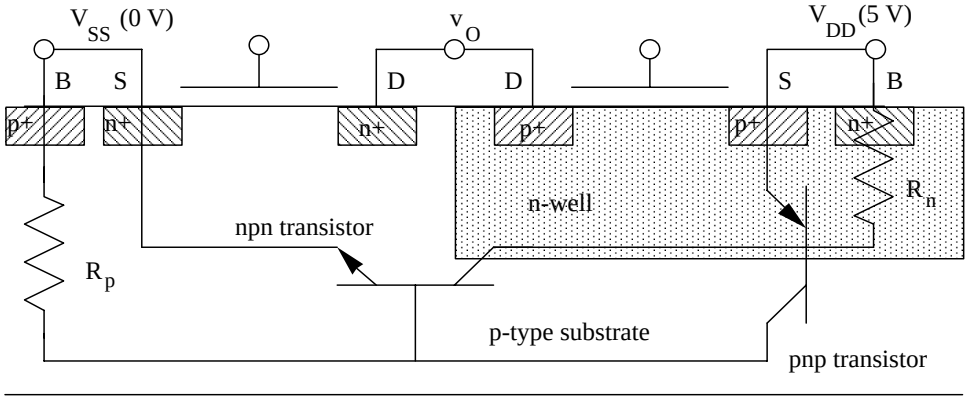
Select Layer (λ)



CMOS Inverter Layout



CMOS Latchup



- The parasitic bipolar transistors can destroy the CMOS circuitry
- The bipolar devices are normallly inactive
- The collector of each bipolar transistor is connected to the base of the other in a positive feedback structure
- The latchup effect can occur when:
    1. Both bipolar transistors conduct
    2. Product of gains of the 2 transistors in the feedback loop exceeds unity ($\beta_P\beta_N > 1$)