VLSI Design EE 523
Spring 2025

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Lecture 12

Topics for lecture 12

- RC model of CMOS gates
- Elmore Delay Model
- Calculate tpdr and tpdh of unit inverter
- Calculate tpdr and tpdh of Nand gate using Elmore
- Introduce Logical Effort LE
- How does W and L of CMOS transistors effect timing
- **Quiz 2 was held**

RC Equivalent Circuits for MOSFET

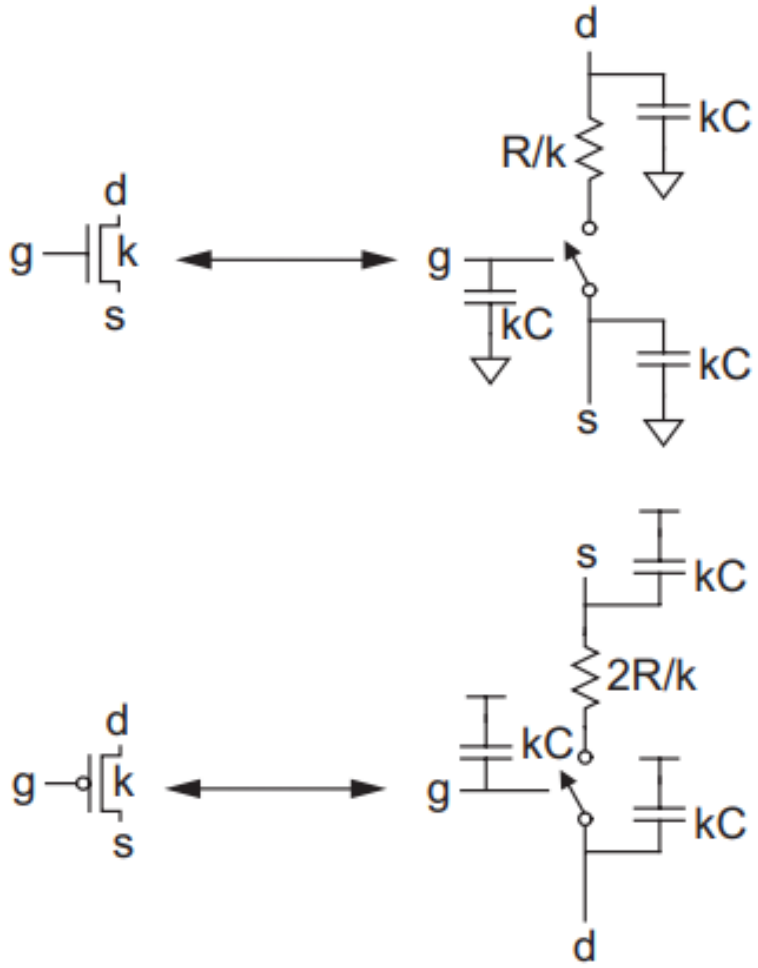


FIGURE 4.5
Equivalent circuits for transistors

RC Model of Inverter

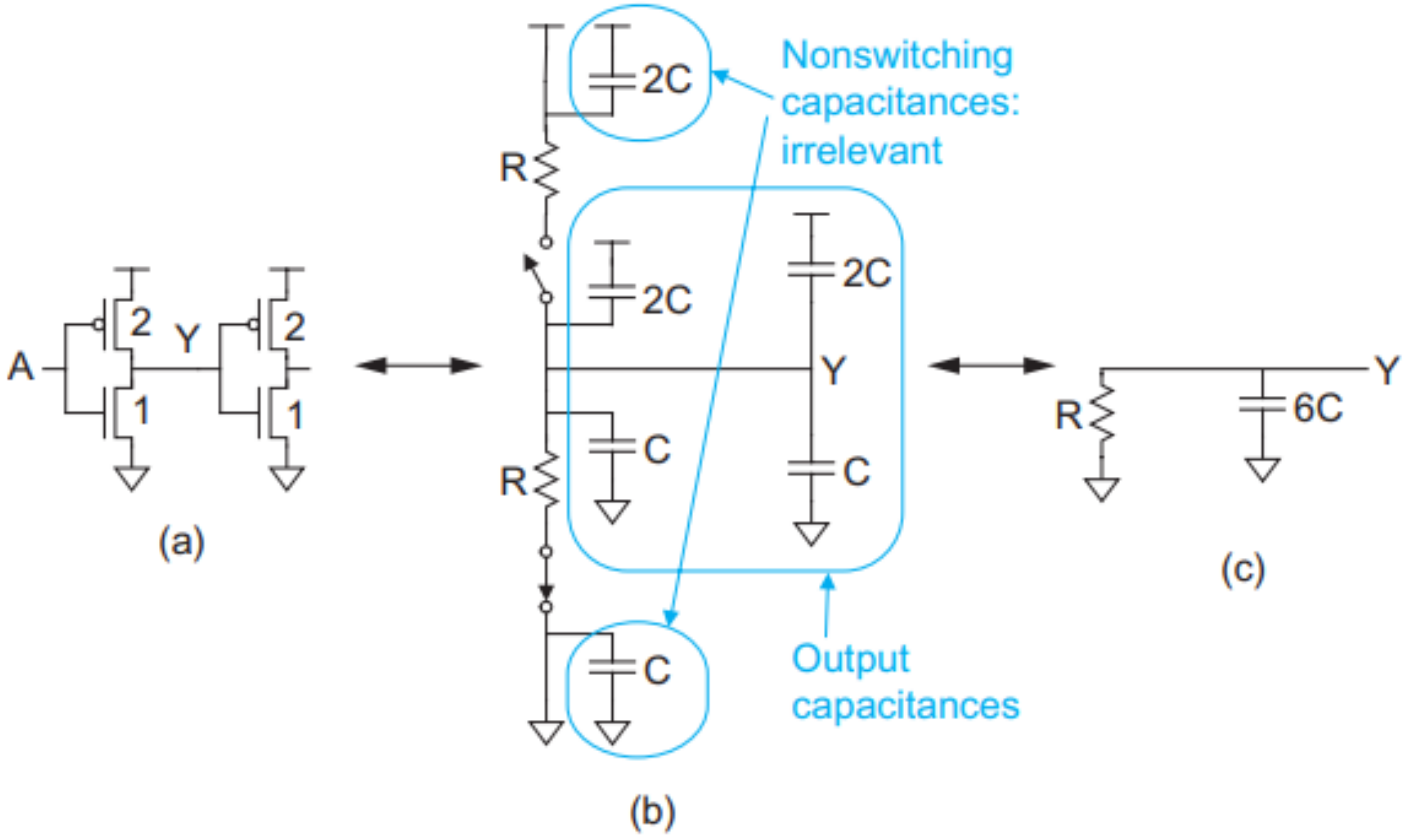


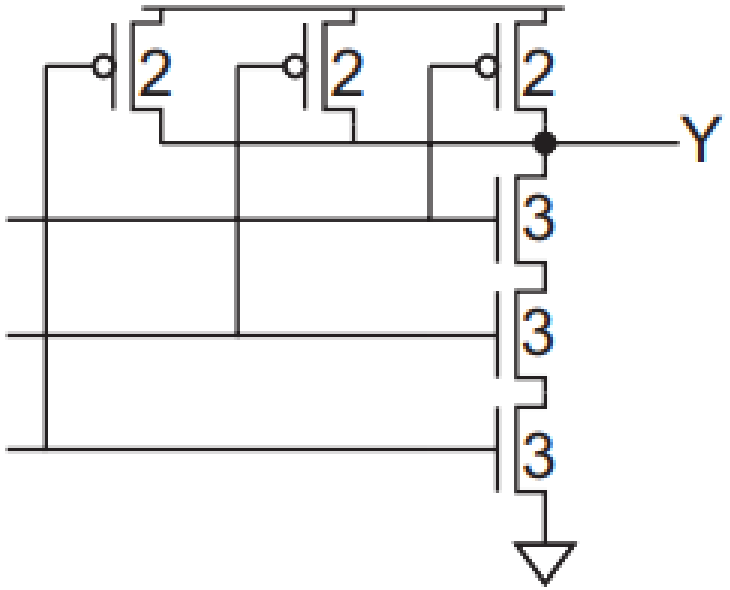
FIGURE 4.6 Equivalent circuit for an inverter

Annotating Sizes of MOSFETs

Example 4.2

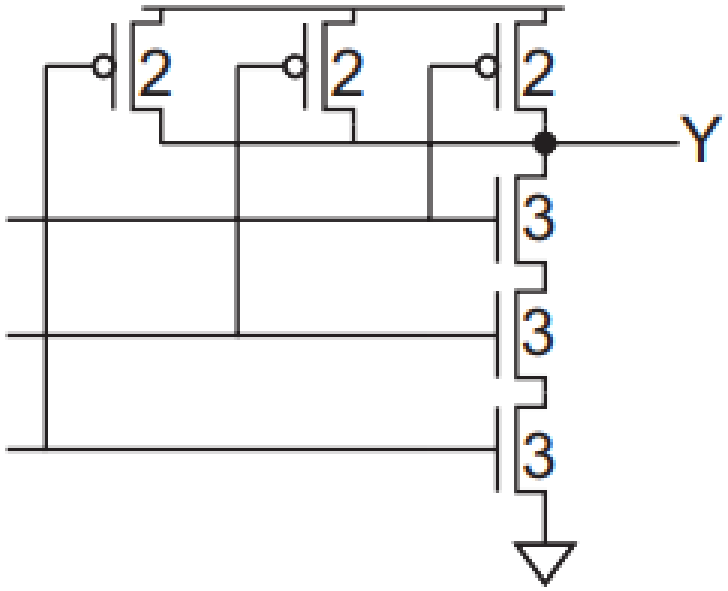
Sketch a 3-input NAND gate with transistor widths chosen to achieve effective rise and fall resistance equal to that of a unit inverter (R). Annotate the gate with its gate and diffusion capacitances. Assume all diffusion nodes are contacted. Then sketch equivalent circuits for the falling output transition and for the worst-case rising output transition.

Look at Sizes of NMOS and PMOS

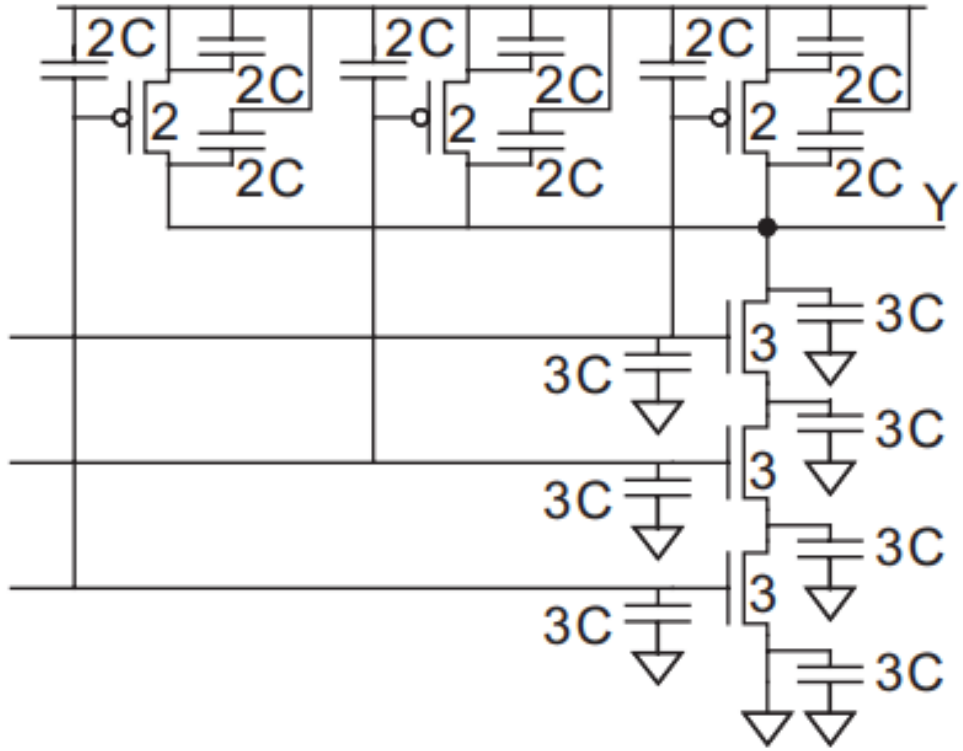


(a)

From Sizes to Distributed Capacitances

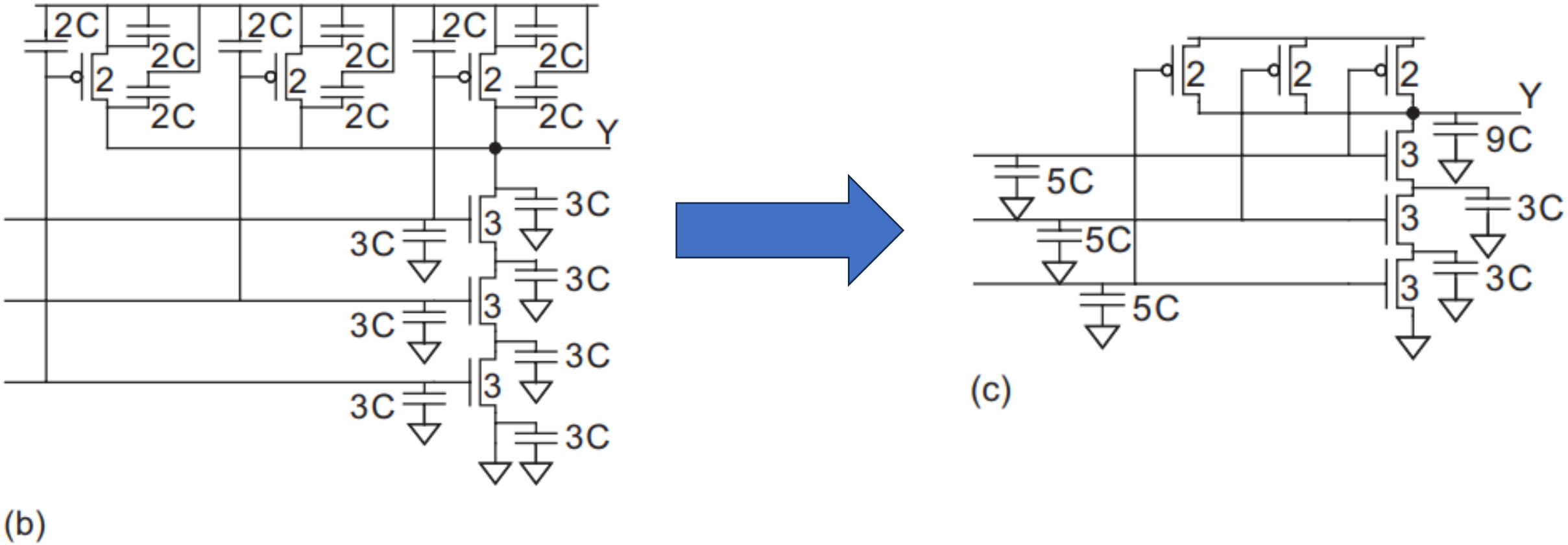


(a)

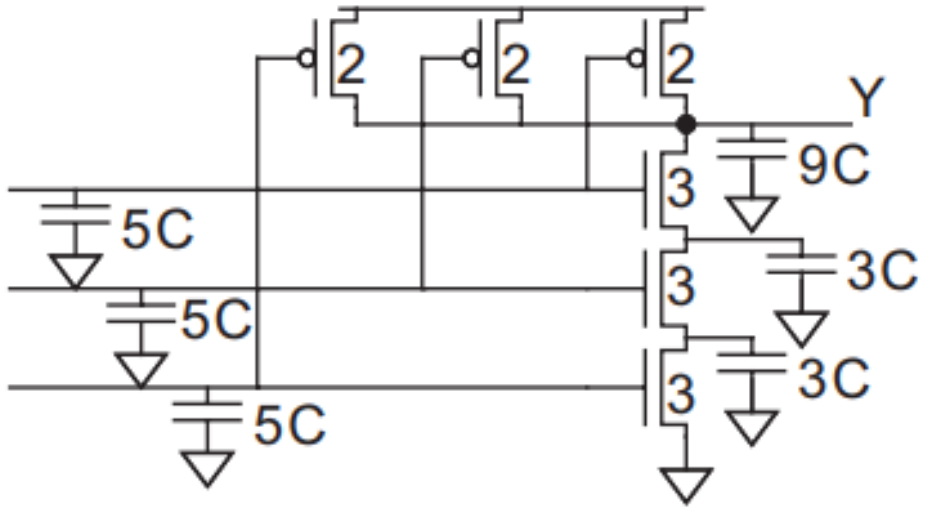


(b)

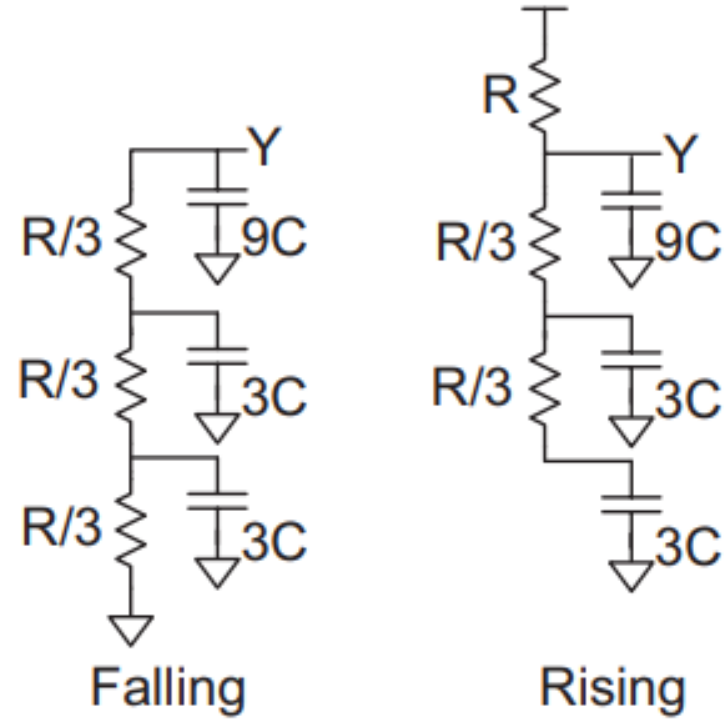
Distributed Capacitance to Lumped Capacitance



Lumped Capacitance to RC Model



(c)



(d) (e)

FIGURE 4.7 Equivalent circuits for a 3-input NAND gate

Real-world 74HC00

The 74HC00 quad two-input NAND gate comprises four identical circuits like the one shown in Figure 9.22. This circuit is double buffered by two inverters. Although the two inverters do not alter the overall logic function of the circuit, they do provide voltage gain (thus sharpening the voltage transfer characteristic) and current gain (thus allowing the use of smaller input transistors, with reduced input capacitance).

Table 9.3 summarizes the basic characteristics of 74HC high-speed CMOS gates. The range of supply voltages is much tighter than for the 4000 series.

TABLE 9.3

Basic Characteristics of High-Speed CMOS[a]

74HC series CMOS	
Gate material	Polysilicon
Gate length	3 µm
Oxide thickness	60 nm
Supply voltage	4.5 to 5.5 V
Propagation delay (C_L = 15 pF)	10 ns

[a] 74HCxx series.

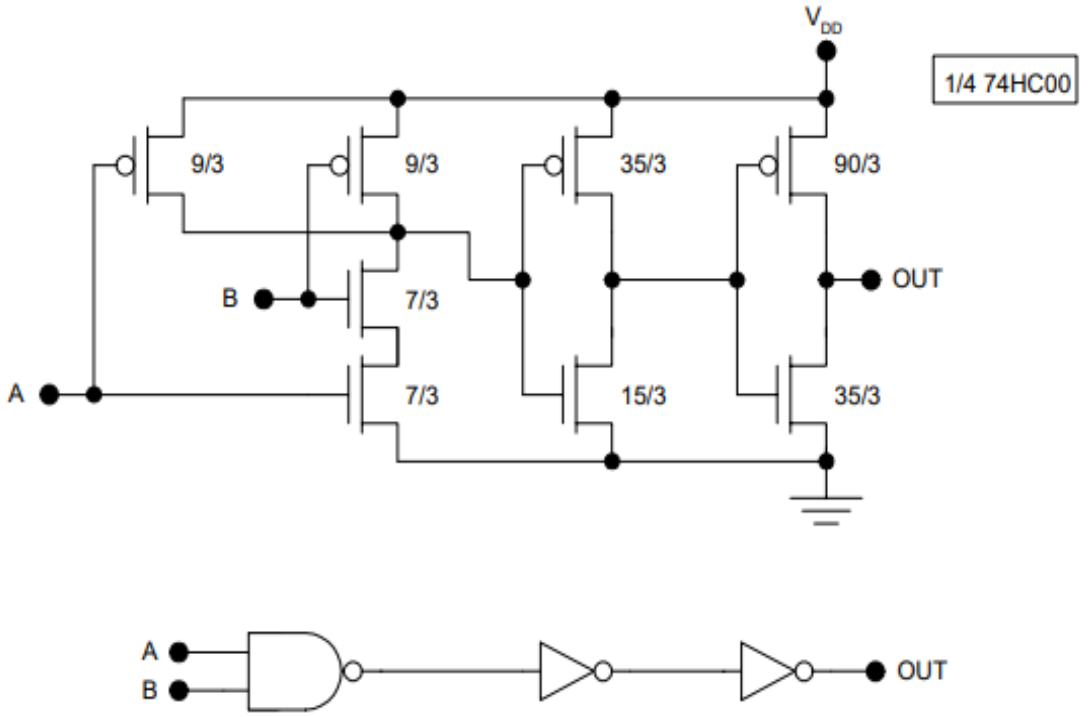
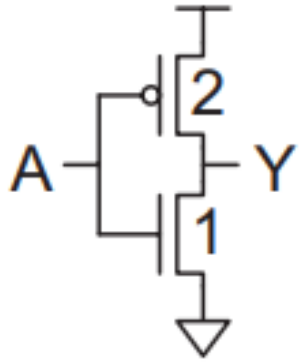


FIGURE 9.22
74HC high-speed CMOS NAND2 gate (1/4 of the 74HC00 quad two-input NAND gate).

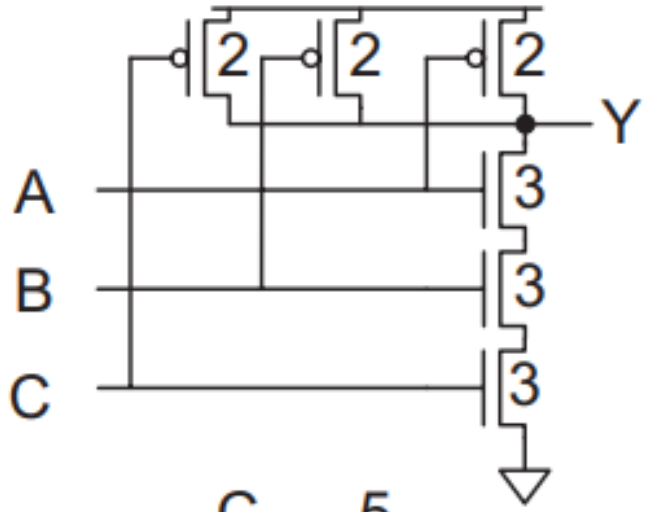
Logical Effert - Definition

4.4.1 Logical Effort

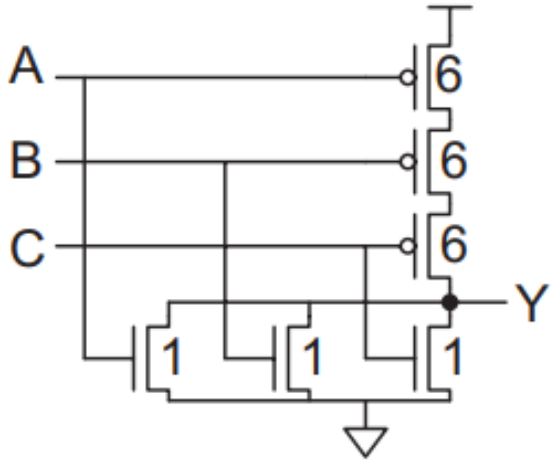
Logical effort of a gate is defined as *the ratio of the input capacitance of the gate to the input capacitance of an inverter that can deliver the same output current*. Equivalently, logical effort indicates how much worse a gate is at producing output current as compared to an inverter, given that each input of the gate may only present as much input capacitance as the inverter.



(a) $C_{in} = 3$, $g = 3/3$



(b) $C_{in} = 5$, $g = 5/3$



(c) $C_{in} = 7$, $g = 7/3$

Logical Effort of Common Gates

TABLE 4.2 Logical effort of common gates

Gate Type	Number of Inputs				
	1	2	3	4	*n*
inverter	1				
NAND		4/3	5/3	6/3	$(n+2)/3$
NOR		5/3	7/3	9/3	$(2n+1)/3$
tristate, multiplexer	2	2	2	2	2
XOR, XNOR		4, 4	6, 12, 6	8, 16, 16, 8	

Parasitic Delay

4.4.2 Parasitic Delay

The parasitic delay of a gate is the delay of the gate when it drives zero load. It can be estimated with RC delay models. A crude method good for hand calculations is to count only diffusion capacitance on the output node. For example, consider the gates in Figure 4.22, assuming each transistor on the output node has its own drain diffusion contact. Transistor widths were chosen to give a resistance of R in each gate. The inverter has three units of diffusion capacitance on the output, so the parasitic delay is $3RC = \tau$. In other words,

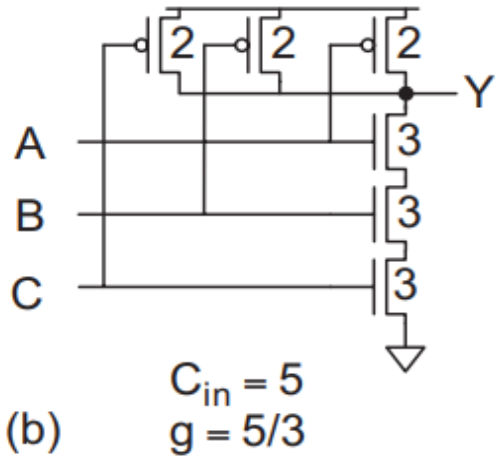


TABLE 4.3 Parasitic delay of common gates

Gate Type	Number of Inputs				
	1	2	3	4	*n*
inverter	1				
NAND		2	3	4	*n*
NOR		2	3	4	*n*
tristate, multiplexer	2	4	6	8	2*n*

Elmore Delay (no branches)

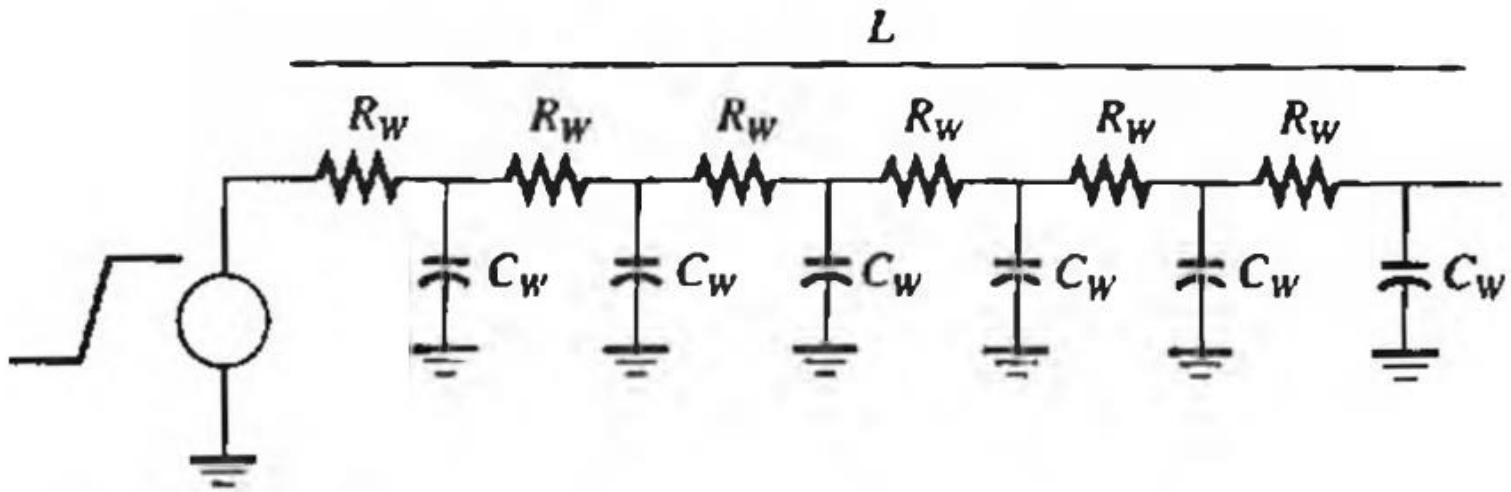


Figure 10.4
Distributed *RC* line as a lumped *RC* ladder.

For a general network, we can compute the Elmore delay as

$$\tau_i = \sum_k (C_k \times R_{ik}) \qquad (10.6)$$

Elmore Delay example

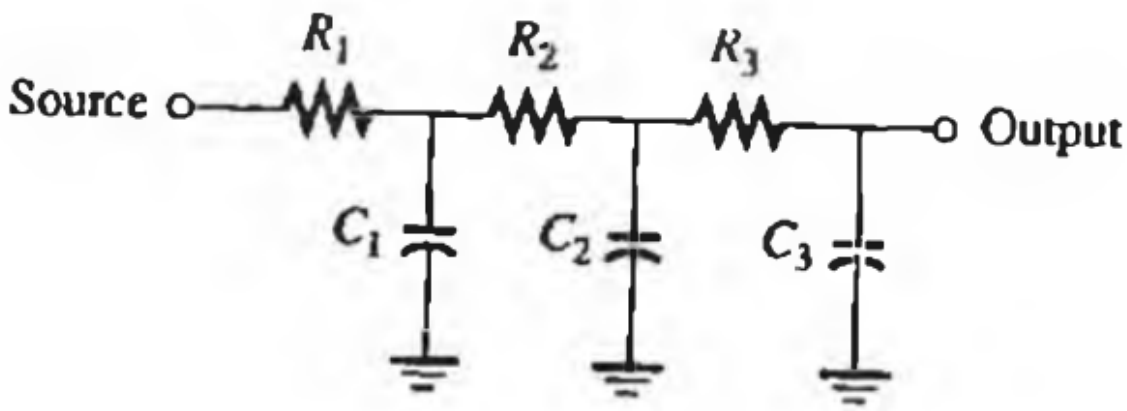


Figure 10.6
RC ladder for Elmore delay calculation.

To further illustrate this procedure, consider the circuit in Figure 10.6. It has an Elmore delay of

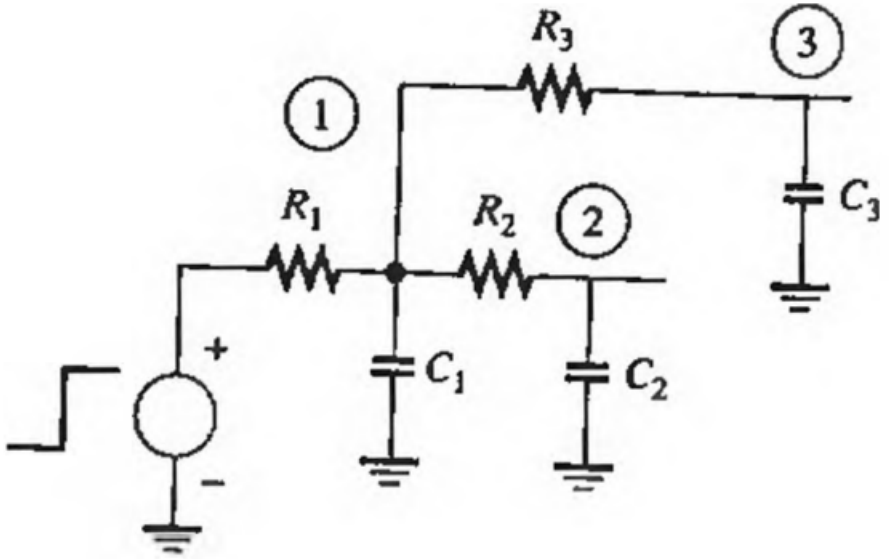
$$\tau = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3$$

Elmore Delay with Branches

Elmore Delay of a Simple *RC* Tree

Problem:

Compute the Elmore delay from the input to nodes 1, 2, and 3 in the following *RC* tree. The Elmore delay is not accurate for internal nodes such as node 1. However, we are not usually interested in the delay from the input to an internal node in *RC* trees. In any case, write the expression for the time constant due to Elmore for each node.



Solution:

$$\tau_1 = R_1C_1 + R_1C_2 + R_1C_3$$

$$\tau_2 = C_1R_1 + C_3R_1 + C_2(R_1 + R_2)$$

$$\tau_3 = C_1R_1 + C_2R_1 + C_3(R_1 + R_3)$$

Reading and Book

- Textbook can be downloaded online “CMOS VLSI Design by Weste and Harris, 4th Edition”
- Readings from Chapter 4