# VLSI Design EE 523
# Spring 2025

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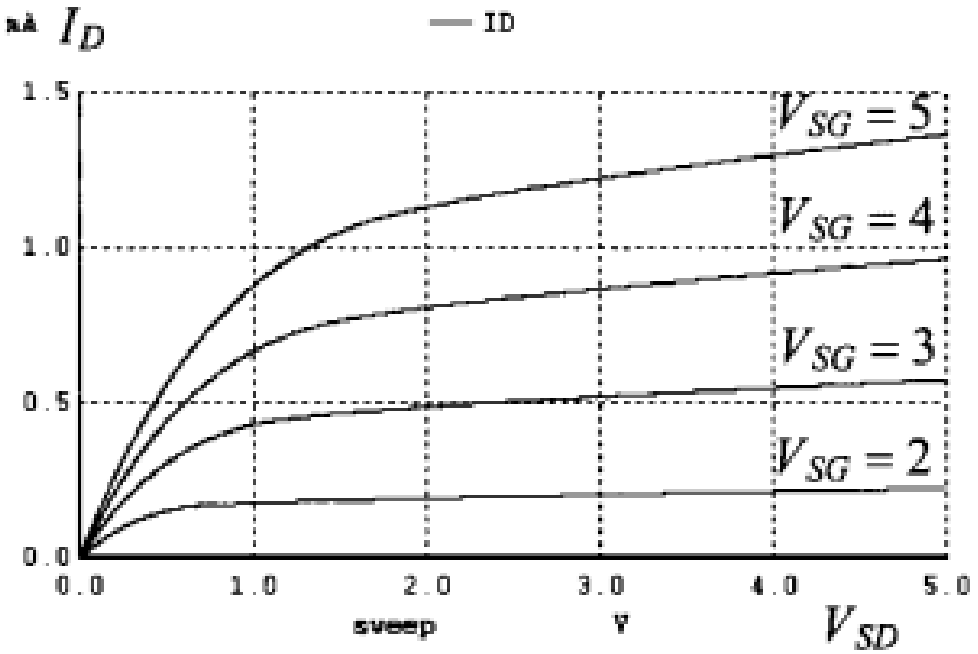
**Lecture 9**

# Topics for lecture 9

- CMOS characteristics – Non-Ideal effects
  - Velocity Saturation and Mobility Degradation
  - Subthreshold Conduction
  - Tunnelling
  - Temperature and Geometry Effects
  - Junction Leakage
  - Body Effect – Equation
  - Channel Length Modulation - Equation
- **Transfer characteristics of CMOS Inverter**
- **Regions of MOS operation in an Inverter**
- **Noise Margin** of CMOS Inverter
- Quiz next week

# PMOS VDS vs ID plot



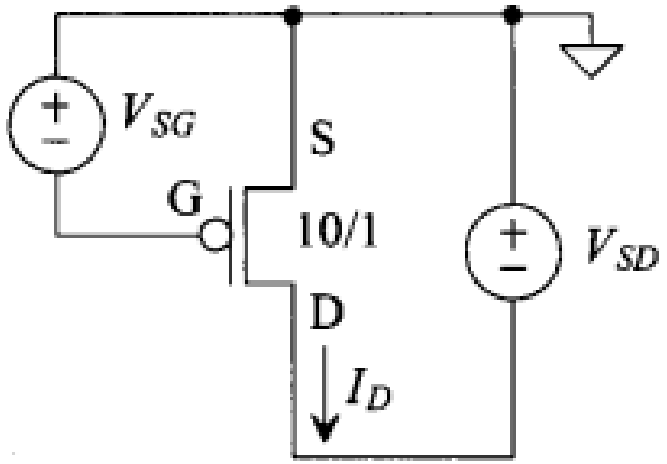




**Figure 6.12** Characterisitics of a long-channel PMOS device.

# Body Effect - Pictorially

To qualitatively understand the origin of the body effect, consider the MOSFET cross-sectional view seen in Fig. 6.15. As the source potential rises above the bulk (substrate) potential (represented by $V_{SB}$ in the figure), electrons are attracted towards the positive terminal of $V_{SB}$ from the MOSFET's channel. To keep the surface inverted, a larger $V_{GS}$ must be applied to the MOSFET. Thus the effect of the body stealing charge from the channel is an increase in the MOSFET's threshold voltage.

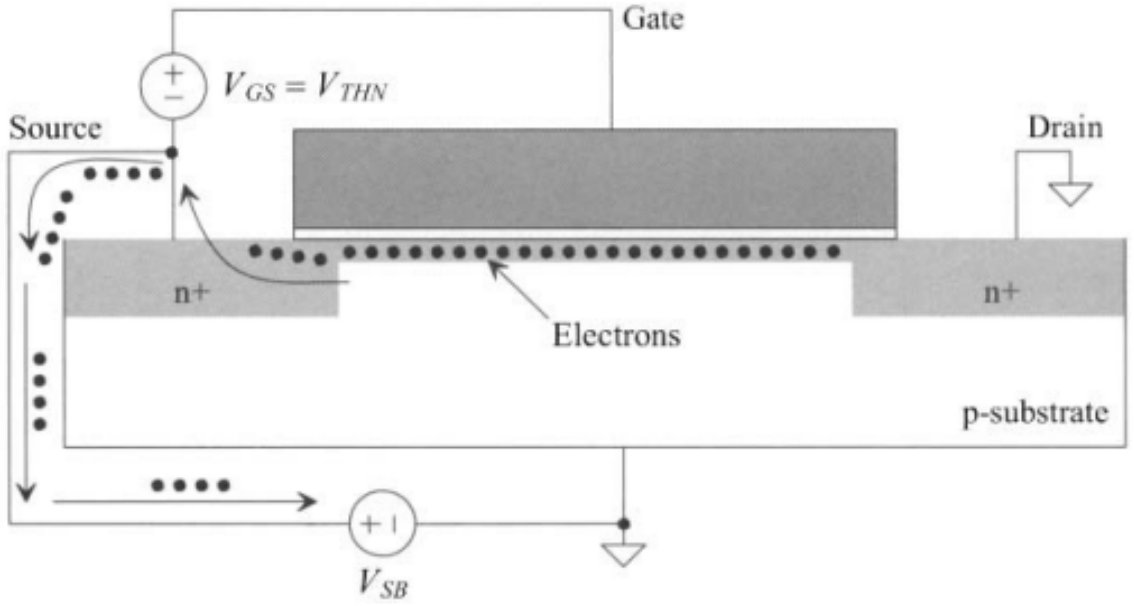



**Figure 6.15** Qualitative description of body effect.

# CMOS Inverter as Switch

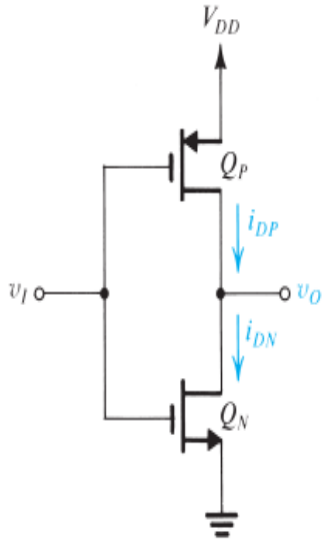



**Figure 14.22** The CMOS inverter.

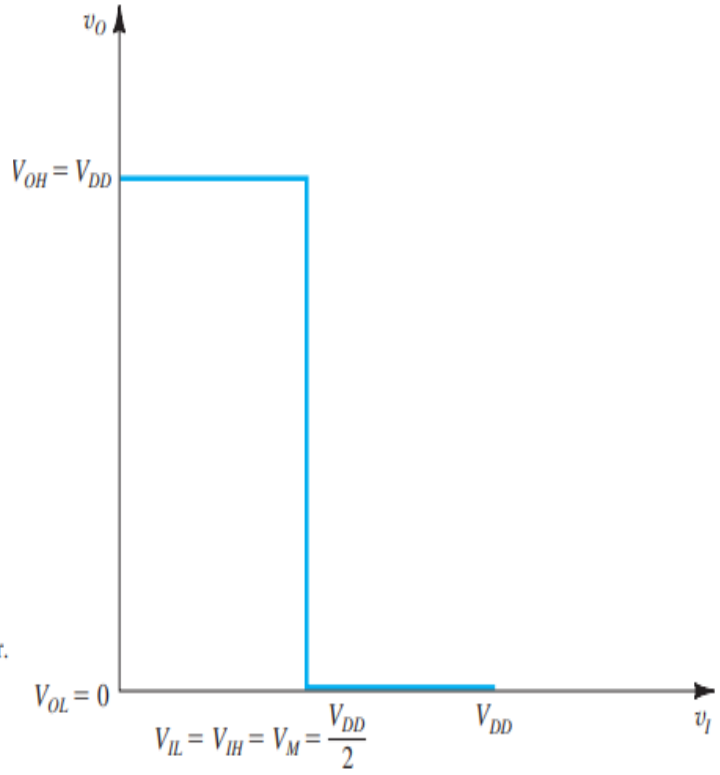



**Figure 14.16** The VTC of an ideal inverter.

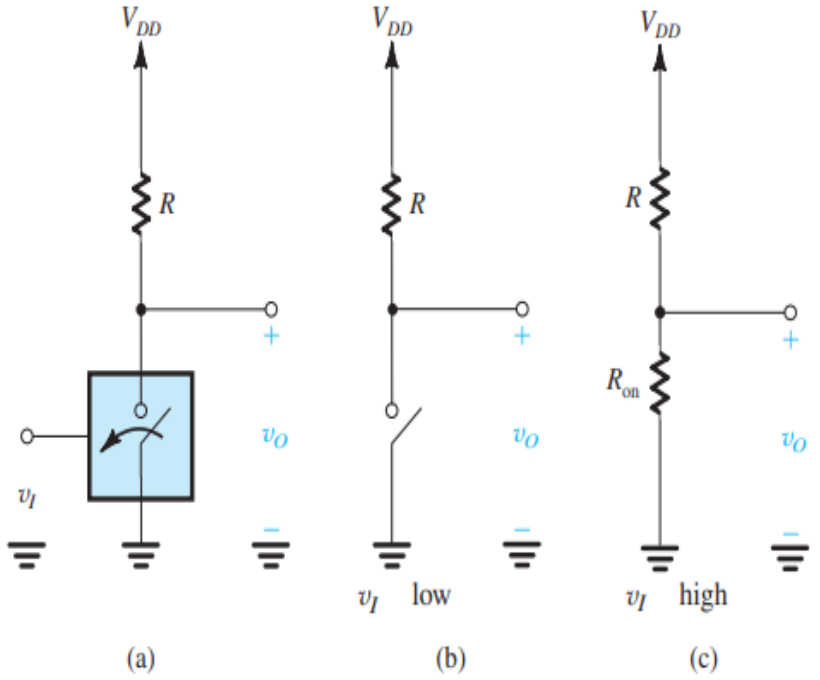



**Figure 14.17** **(a)** The simplest implementation of a logic inverter using a voltage-controlled switch; **(b)** equivalent circuit when $v_I$ is low; **(c)** equivalent circuit when $v_I$ is high. Note that the switch is assumed to close when $v_I$ is high.

# Basic Inverter Operation – Vout vs Vin

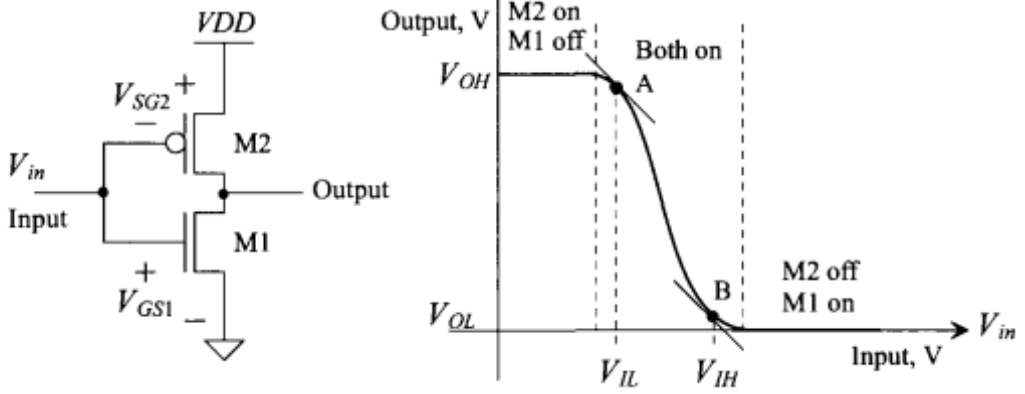



**Figure 11.2** The CMOS inverter transfer characteristics.

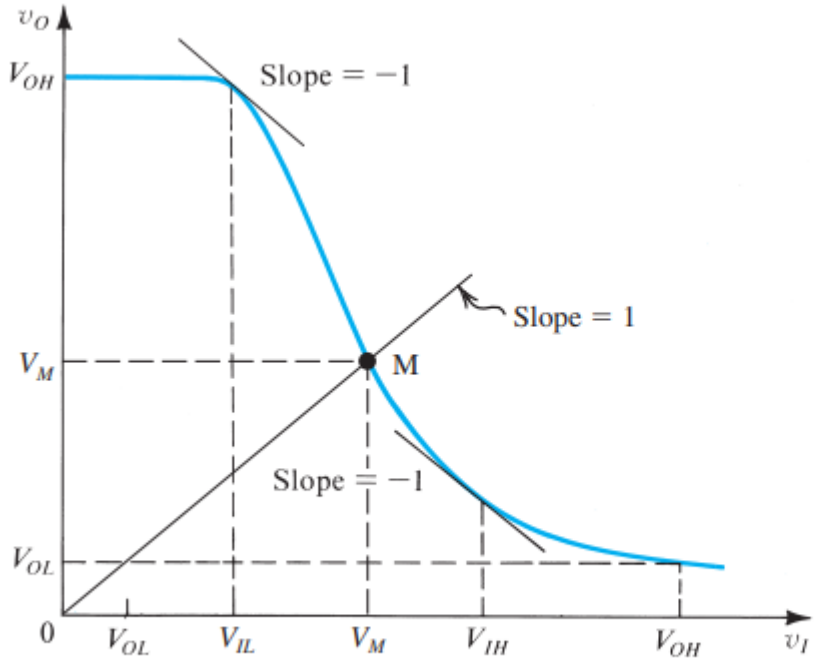



**Figure 14.15** Typical voltage-transfer characteristic (VTC) of a logic inverter, illustrating the definition of the critical points.

The maximum output "high" voltage is labeled $V_{OH}$ and the minimum output "low" voltage, $V_{OL}$. Points A and B on this curve are defined by the slope of the transfer curves equaling –1. Input voltages less than or equal to the voltage $V_{IL}$, defined by point A, are considered a logic low on the input of the inverter. Input voltages greater than or equal to the voltage $V_{IH}$, defined by point B, are considered a logic high on the input of the inverter. Input voltages between $V_{IL}$ and $V_{IH}$ do not define a valid logic voltage level. Ideally, the difference in $V_{IL}$ and $V_{IH}$ is zero; however, this is never the case in real logic circuits.

# Noise Margin Definitions

$$NM_L = V_{IL} - V_{OL} \tag{2.58}$$

The value of $NM_H$ is the difference between the minimum HIGH output voltage of the driving gate and the minimum HIGH input voltage recognized by the receiving gate. Thus,

$$NM_H = V_{OH} - V_{IH} \tag{2.59}$$

where

$V_{IH}$ = minimum HIGH input voltage
$V_{IL}$ = maximum LOW input voltage
$V_{OH}$ = minimum HIGH output voltage
$V_{OL}$ = maximum LOW output voltage

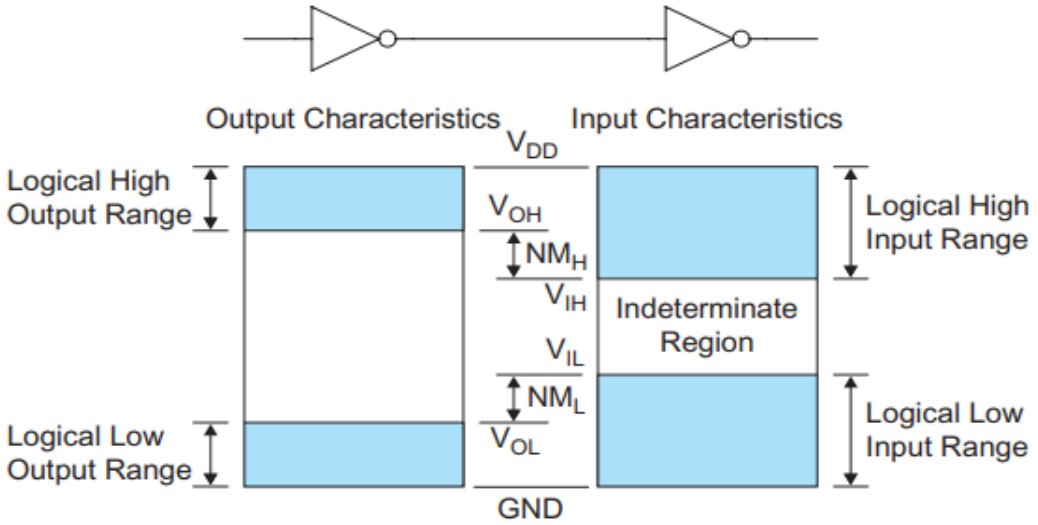



**FIGURE 2.29** Noise margin definitions

# Voltage and Current Plotted together for Inverter

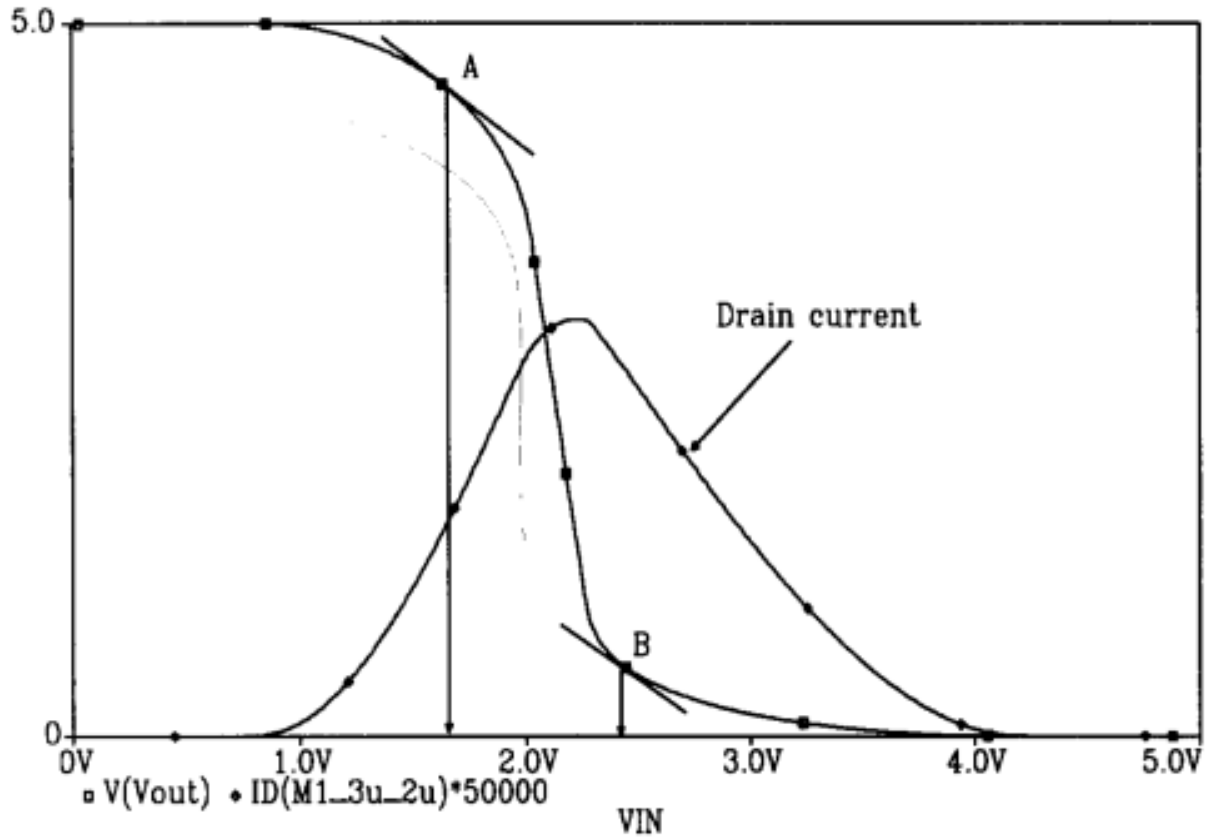



**Figure 11.3** Transfer characteristics of a minimum-size inverter used in Example 11.1.

# I-V Characteristics of a CMOS Inverter

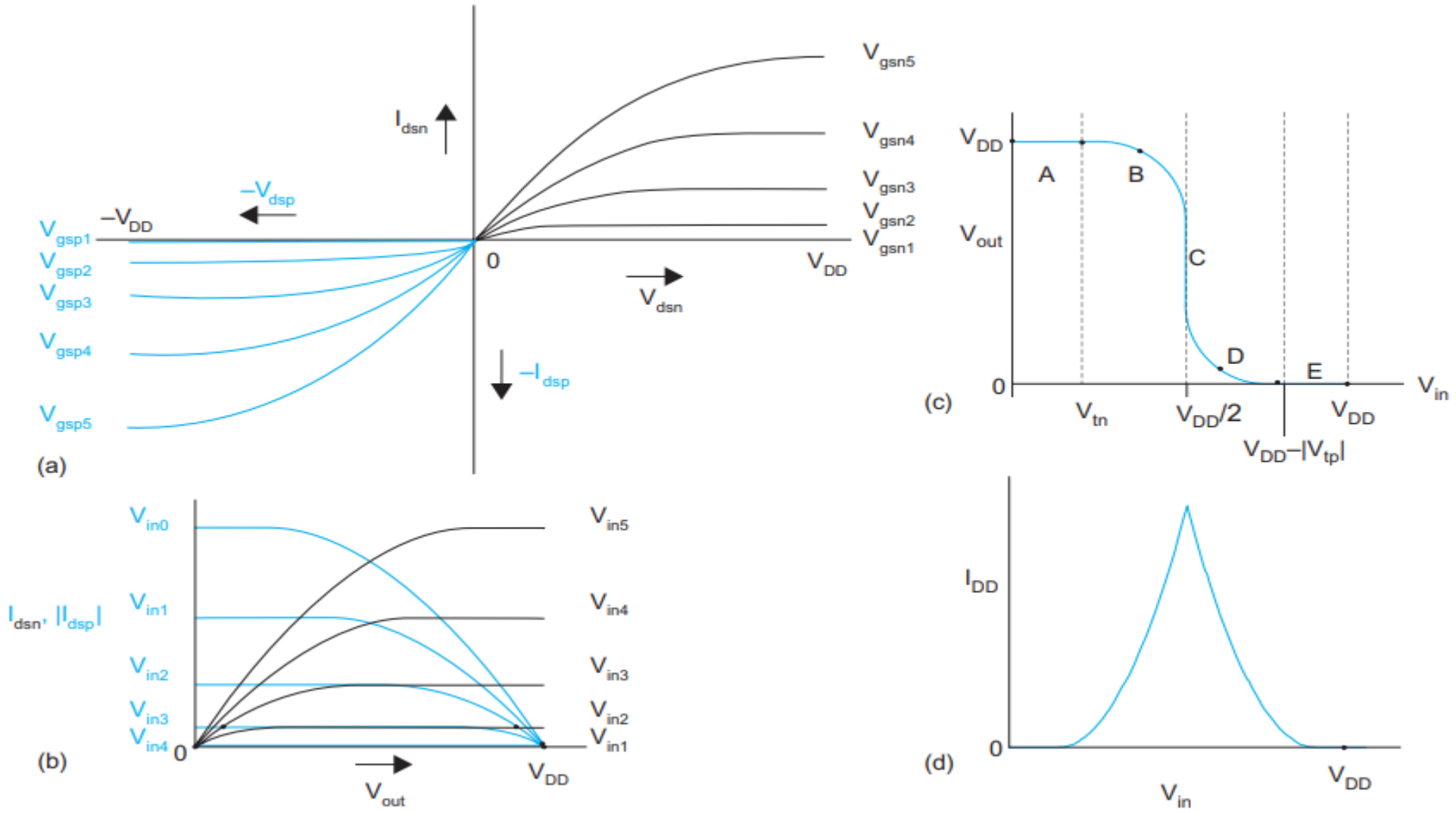



**FIGURE 2.26** Graphical derivation of CMOS inverter DC characteristic

# CMOS Inverter Voltages - Explained

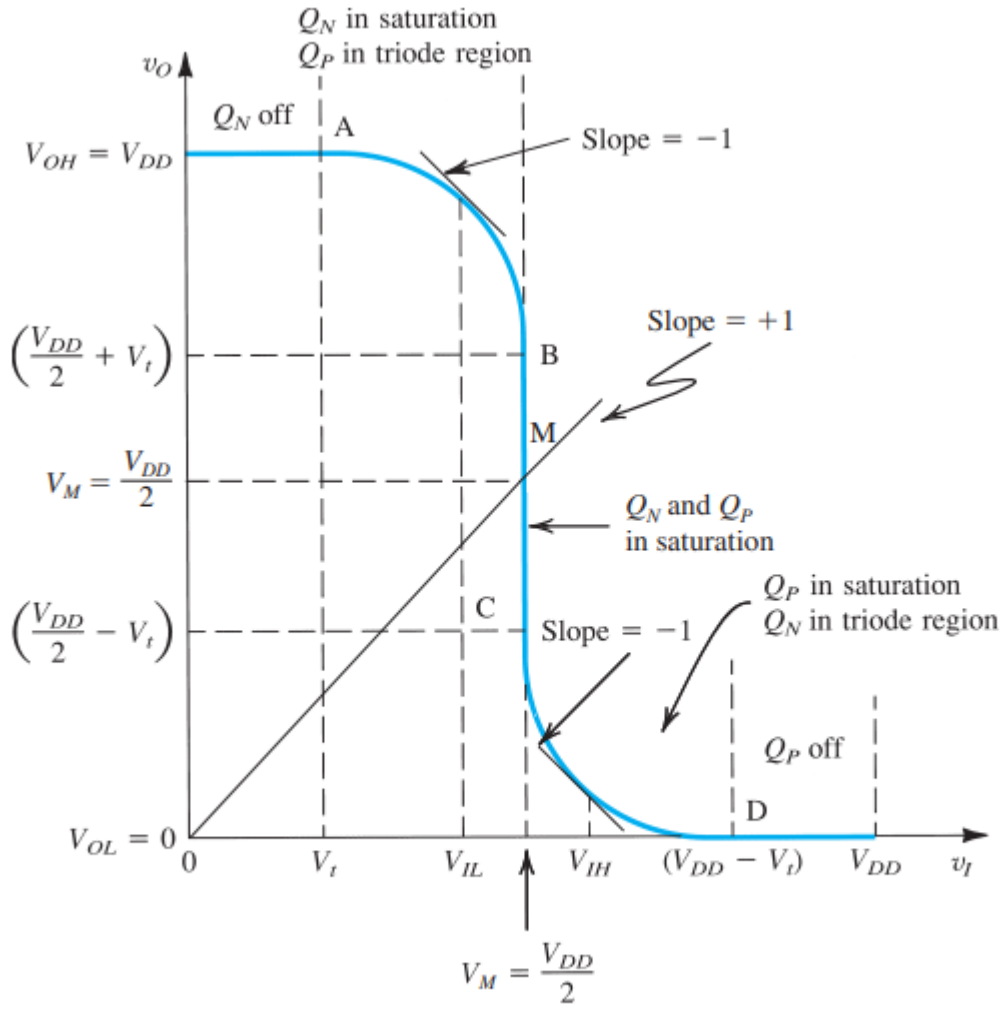



**Figure 14.25** The voltage-transfer characteristic of the CMOS inverter when $Q_N$ and $Q_P$ are matched.

# Operating Regions for MOSFETs in Inverter

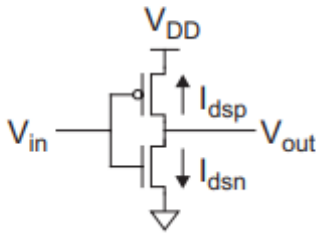



**FIGURE 2.25**
A CMOS inverter

## 2.5.1 Static CMOS Inverter DC Characteristics

Let us derive the DC transfer function ($V_{out}$ vs. $V_{in}$) for the static CMOS inverter shown in Figure 2.25. We begin with Table 2.2, which outlines various regions of operation for the n- and p-transistors. In this table, $V_{tn}$ is the threshold voltage of the n-channel device, and $V_{tp}$ is the threshold voltage of the p-channel device. Note that $V_{tp}$ is negative. The equations are given both in terms of $V_{gs}/V_{ds}$ and $V_{in}/V_{out}$. As the source of the nMOS transistor is grounded, $V_{gsn} = V_{in}$ and $V_{dsn} = V_{out}$. As the source of the pMOS transistor is tied to $V_{DD}$, $V_{gsp} = V_{in} - V_{DD}$ and $V_{dsp} = V_{out} - V_{DD}$.

**TABLE 2.2** Relationships between voltages for the three regions of operation of a CMOS inverter

| | Cutoff | Linear | Saturated |
|---|---|---|---|
| nMOS | $V_{gsn} < V_{tn}$ | $V_{gsn} > V_{tn}$ | $V_{gsn} > V_{tn}$ |
| | $V_{in} < V_{tn}$ | $V_{in} > V_{tn}$ | $V_{in} > V_{tn}$ |
| | | $V_{dsn} < V_{gsn} - V_{tn}$ | $V_{dsn} > V_{gsn} - V_{tn}$ |
| | | $V_{out} < V_{in} - V_{tn}$ | $V_{out} > V_{in} - V_{tn}$ |
| pMOS | $V_{gsp} > V_{tp}$ | $V_{gsp} < V_{tp}$ | $V_{gsp} < V_{tp}$ |
| | $V_{in} > V_{tp} + V_{DD}$ | $V_{in} < V_{tp} + V_{DD}$ | $V_{in} < V_{tp} + V_{DD}$ |
| | | $V_{dsp} > V_{gsp} - V_{tp}$ | $V_{dsp} < V_{gsp} - V_{tp}$ |
| | | $V_{out} > V_{in} - V_{tp}$ | $V_{out} < V_{in} - V_{tp}$ |

# PMOS and NMOS Regions of Operation in Inverter

**TABLE 2.3** Summary of CMOS inverter operation

| Region | Condition | p-device | n-device | Output |
|---|---|---|---|---|
| A | $0 \le V_{in} < V_{tn}$ | linear | cutoff | $V_{out} = V_{DD}$ |
| B | $V_{tn} \le V_{in} < V_{DD}/2$ | linear | saturated | $V_{out} > V_{DD}/2$ |
| C | $V_{in} = V_{DD}/2$ | saturated | saturated | $V_{out}$ drops sharply |
| D | $V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$ | saturated | linear | $V_{out} < V_{DD}/2$ |
| E | $V_{in} > V_{DD} - \lvert V_{tp} \rvert$ | cutoff | linear | $V_{out} = 0$ |

# Inverter Switching Current

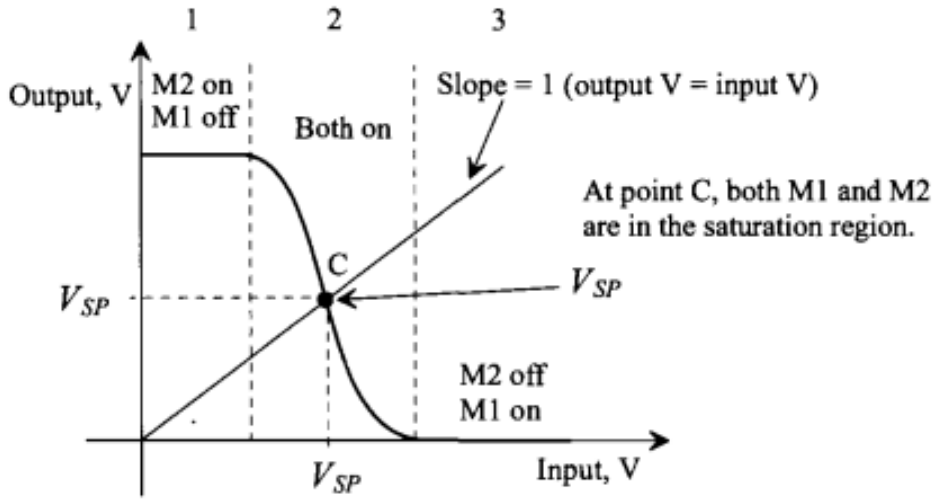



**Figure 11.5** Transfer characteristics of the inverter showing the switching point.

*Inverter Switching Point*

Consider the transfer characteristics of the basic inverter as shown in Fig. 11.5. Point C corresponds to the point on the curve when the input voltage is equal to the output voltage. At this point, the input (or output) voltage is called the *inverter switching point voltage*, $V_{SP}$, and both MOSFETs in the inverter are in the saturation region. Since the drain current in each MOSFET must be equal, the following is true:

$$\frac{\beta_n}{2}(V_{SP} - V_{THN})^2 = \frac{\beta_p}{2}(VDD - V_{SP} - V_{THP})^2 \qquad (11.3)$$

Solving for $V_{SP}$ gives

$$V_{SP} = \frac{\sqrt{\frac{\beta_n}{\beta_p}} \cdot V_{THN} + (VDD - V_{THP})}{1 + \sqrt{\frac{\beta_n}{\beta_p}}} \qquad (11.4)$$

**Example 11.2**

Estimate $\beta_n$ and $\beta_p$ so that the switching point voltage of a CMOS inverter designed in the long-channel CMOS process is 2.5 V (= $VDD/2$).

Solving Eq. (11.4) with $V_{SP}$ = 2.5 V for the ratio $\beta_n/\beta_p$ gives a value of approximately unity. That is,

$$\beta_n = \beta_p = KP_n\frac{W_1}{L_1} = KP_p\frac{W_2}{L_2}$$

Since $KP_n = 3KP_p$, the width of the PMOS device must be three times the width of the NMOS, assuming equal-length MOSFETs. For $V_{SP}$ = 2.5 V, this requires

$$W_2 = 3W_1$$

# Reading and Book

- Textbook can be downloaded online “CMOS VLSI Design by Weste and Harris, 4th Edition”
- Readings from Chapter 2