VLSI Design EE 523
Spring 2025

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Lecture 24

Topics for lecture 24

- Arbiter Circuit
- Sources of Clock Jitter and Clock Skew
  - How Jitter and Skew affects Timing in Sequential Circuits
- Sequencing using Flipflops and Latches
- Timing parameters associated with:
  - Combinational Logic
  - Flip flops
  - Latches (two phase and pulsed latch)
- Max Delay and Min Delay determination for Flip flops and Latches
- Looked at some I/O Pad Designs
- **QUIZ 5 in next lecture**

Arbiter Circuit

10.6.5 Arbiters

The *arbiter* of Figure 10.51(a) is closely related to the synchronizer. It determines which of two inputs arrived first. If the spacing between the inputs exceeds some aperture time, the first input should be acknowledged. If the spacing is smaller, exactly one of the two inputs should be acknowledged, but the choice is arbitrary. For example, in a television game show, two contestants may pound buttons to answer a question. If one presses the button first, she should be acknowledged. If both press the button at times too close to distinguish, the host may choose one of the two contestants arbitrarily (but must not lock up or catch on fire).

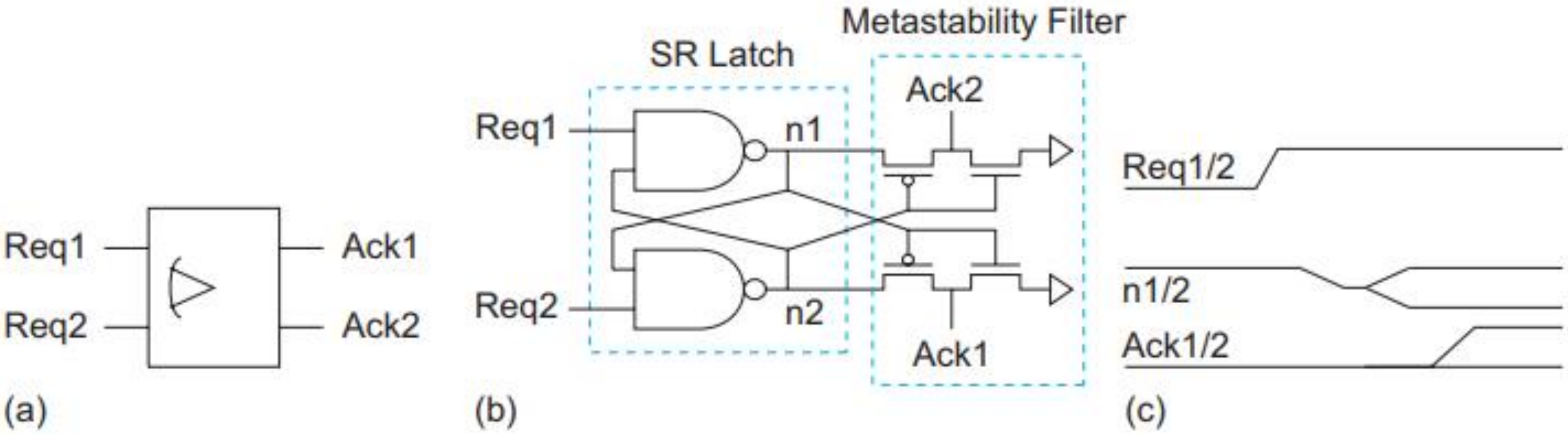


FIGURE 10.51 Arbiter

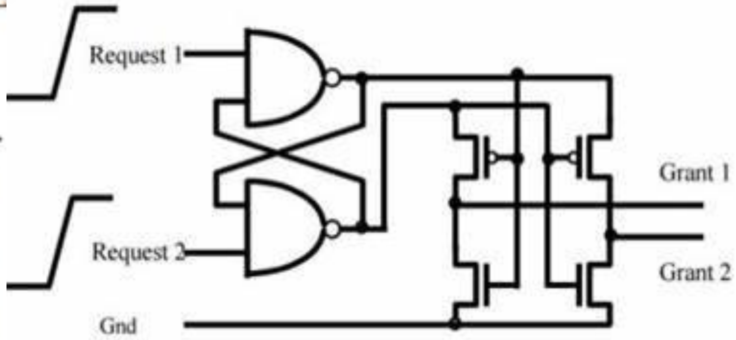


FIG: 2 bit input arbiter circuit

Table 1: Truth table of two Bit input asynchronous arbiter.

INPUT		OUTPUT	
Request (R1)	Request (R2)	Grant (G1)	Grant(G2)
0	0	illegal input	
0	1	0	1
1	0	1	0
1	1	illegal input	

Latches and Flipflops

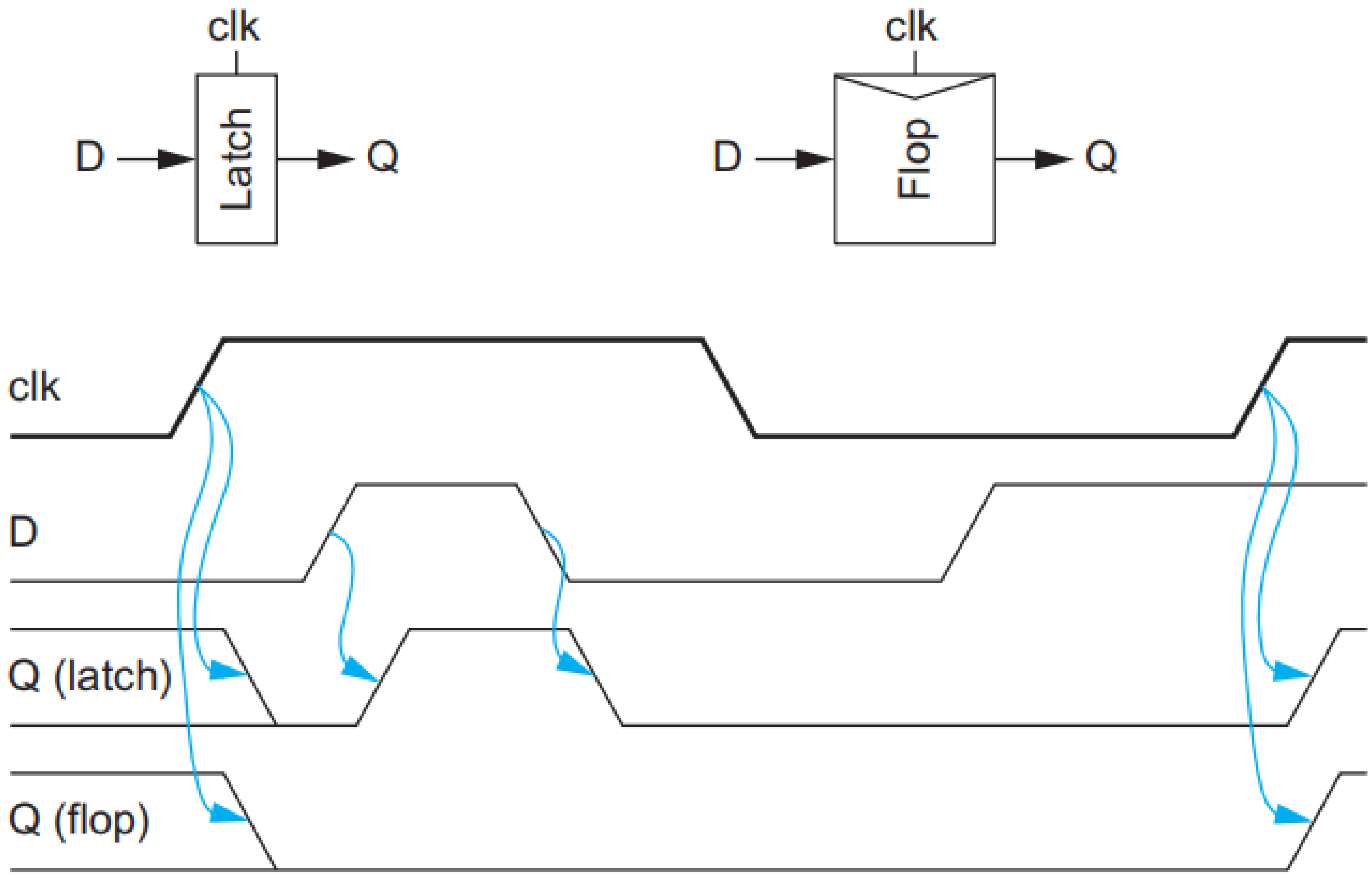
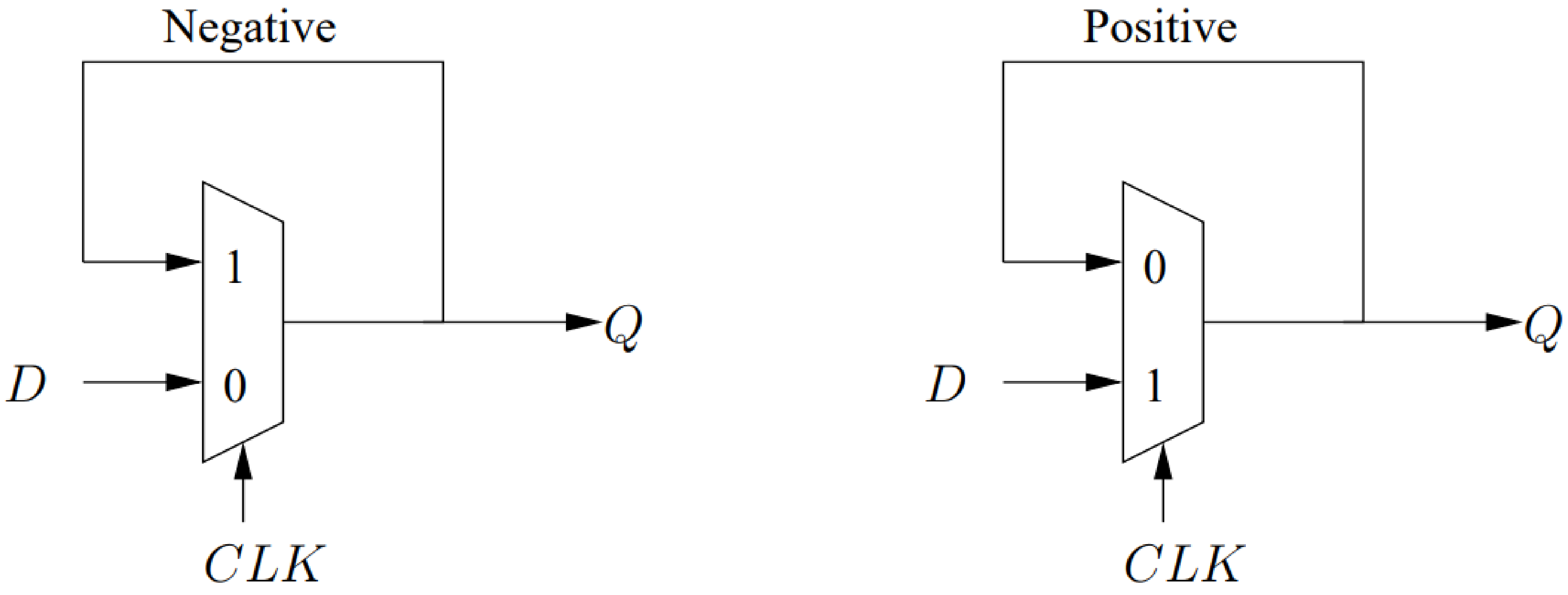


FIGURE 10.1 Latches and flip-flops

Mux Based Latches

Multiplexer Based Latches



Edge Triggered Pass Transistor DFF

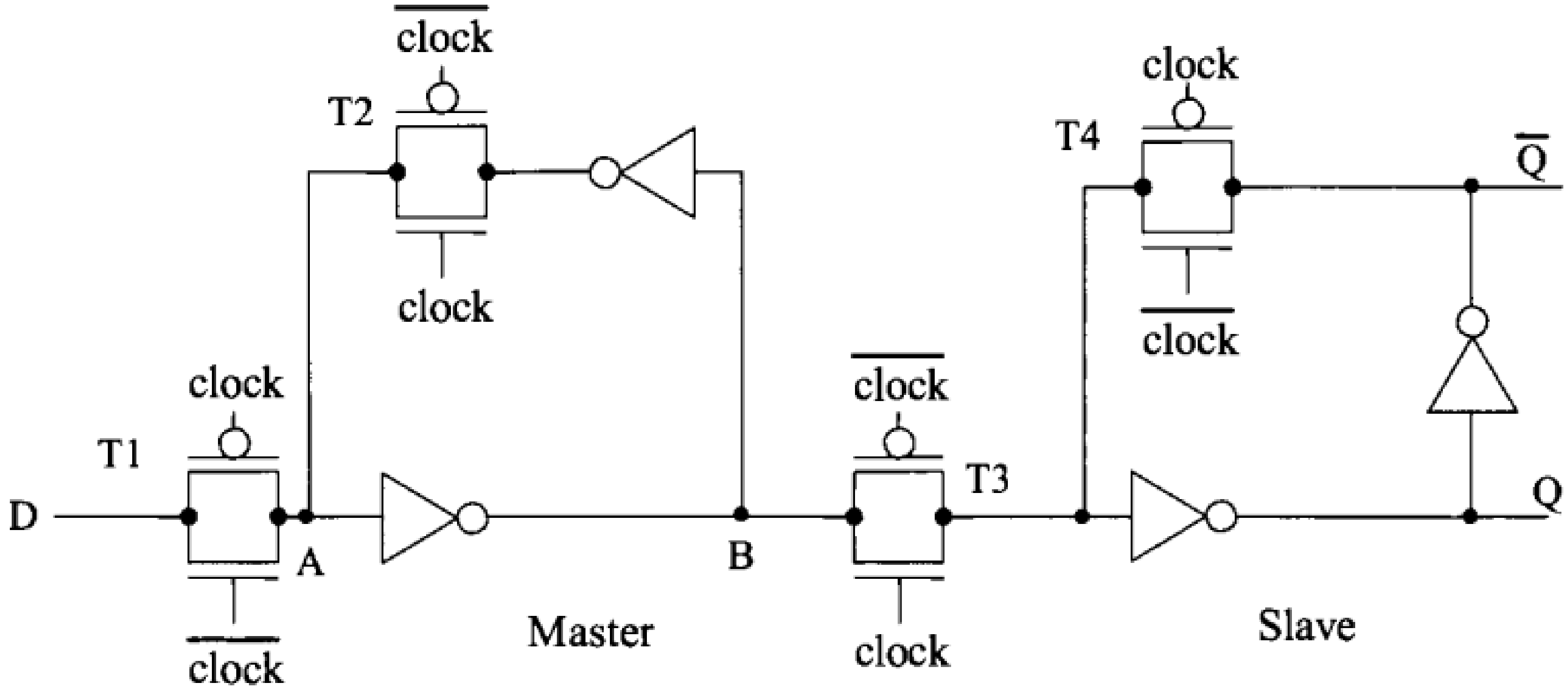
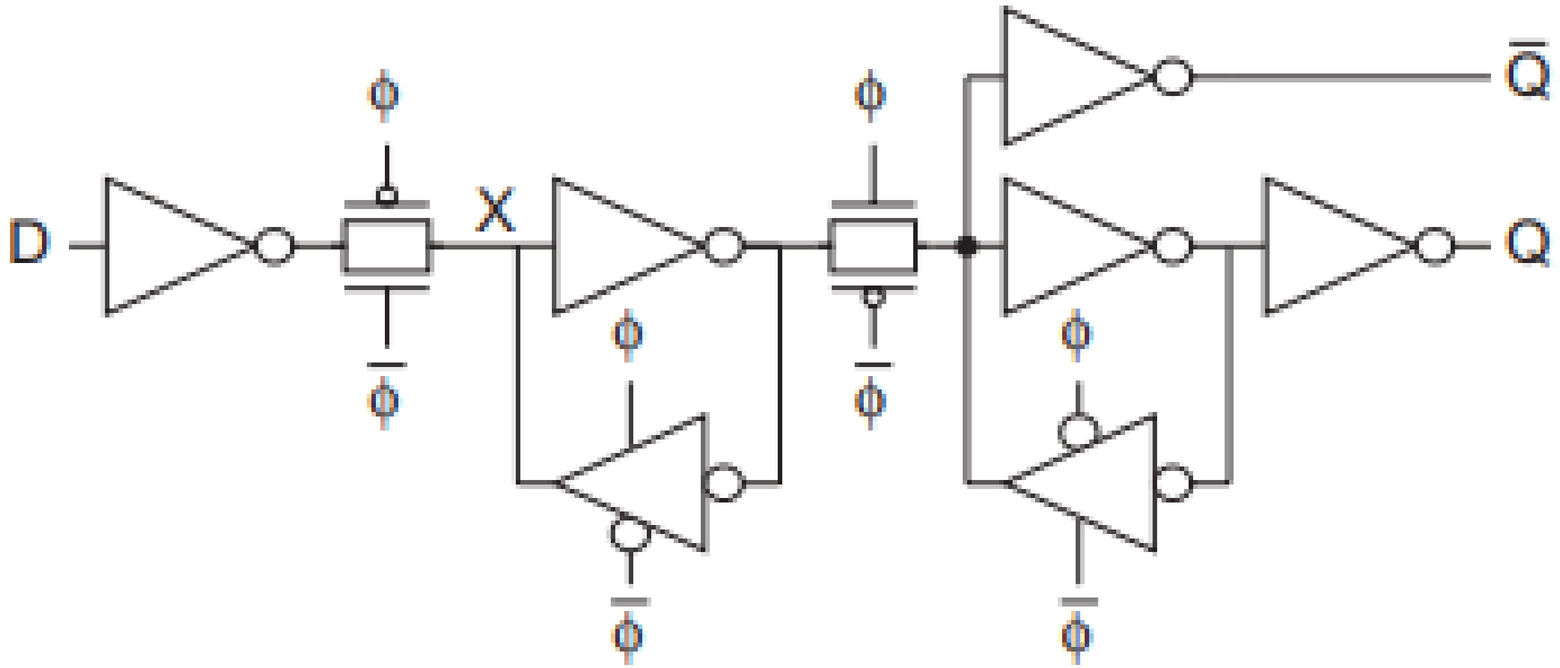


Figure 13.22 An edge-triggered D-FF.

Another DFF using Switches and Inverters



(b)

FIGURE 10.19 Flip-flops

Edge Triggered DFF with Asynch Set and Clear

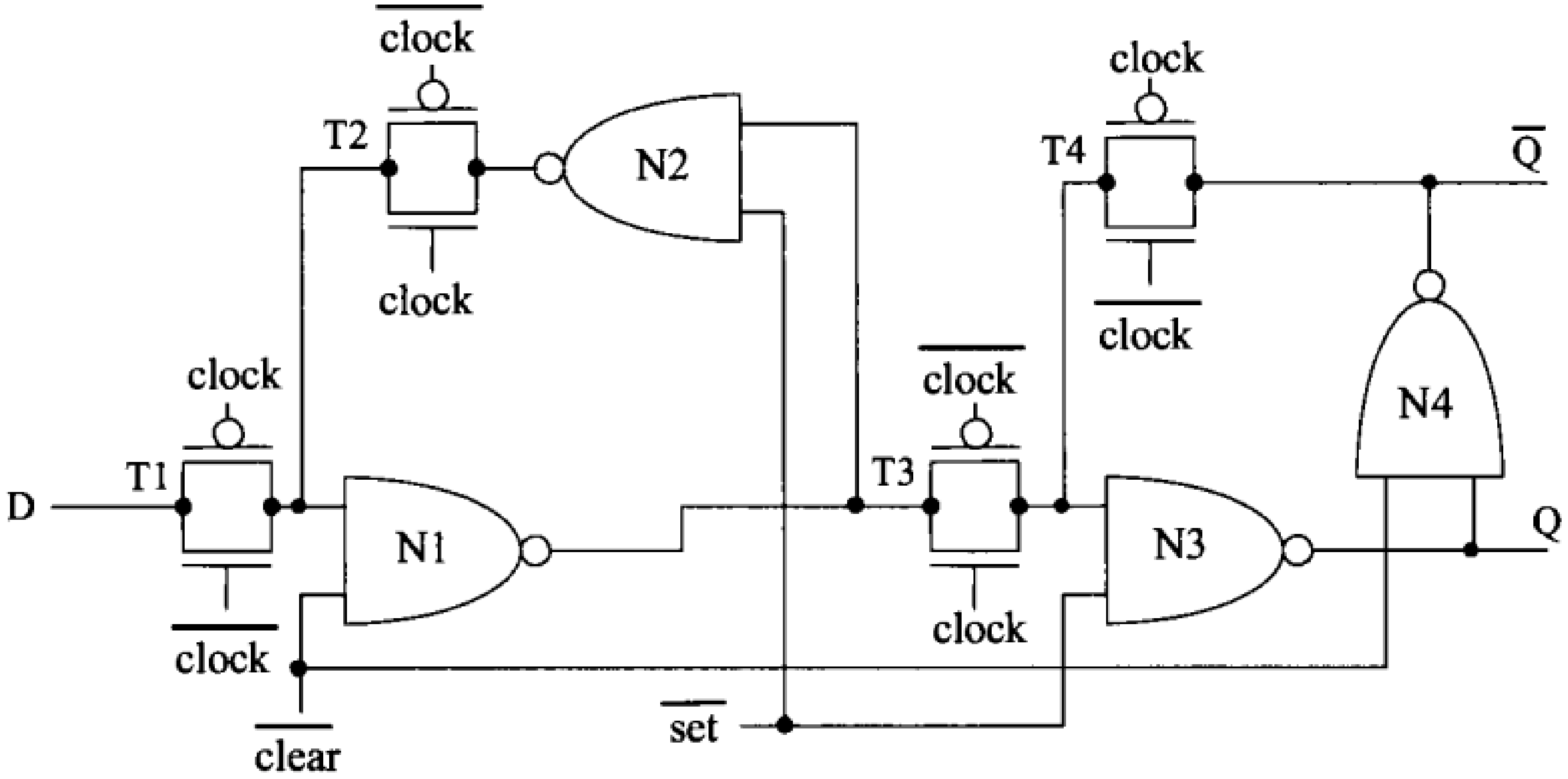


Figure 13.24 An edge-triggered FF with asynchrounous set and clear.

SR Latch to D Flipflop

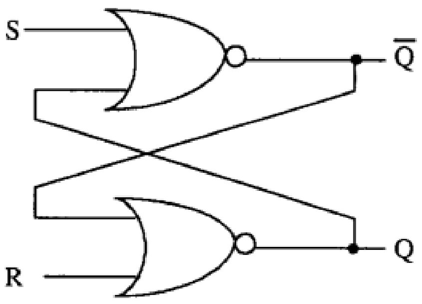


Figure 13.15 Set-reset flip-flop made using NOR gates.

Truth table

S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
1	0	1	0
0	1	0	1
1	1	0	0

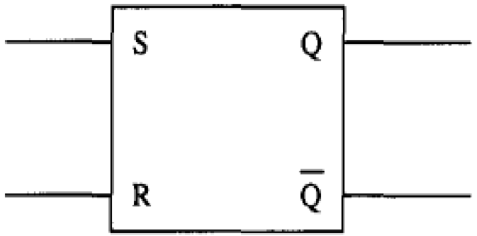


Figure 13.16 Logic symbol of the SR flip-flop.

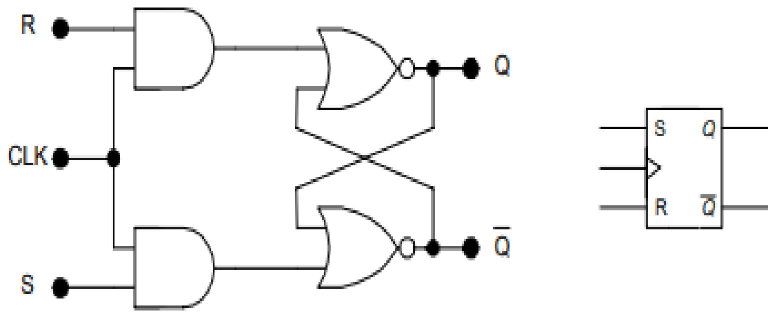
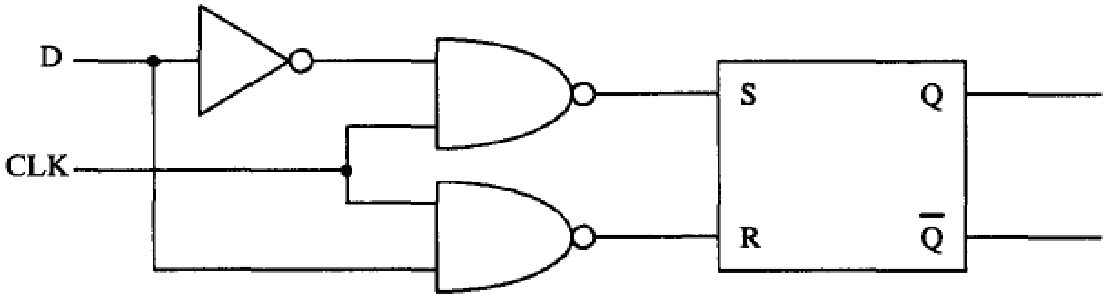


FIGURE 15.9
Clocked RS flip-flop.



Logic symbol

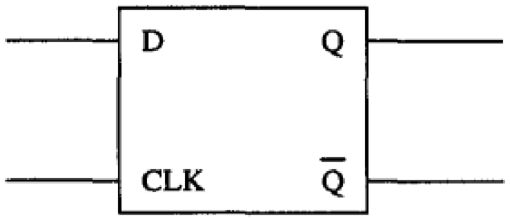
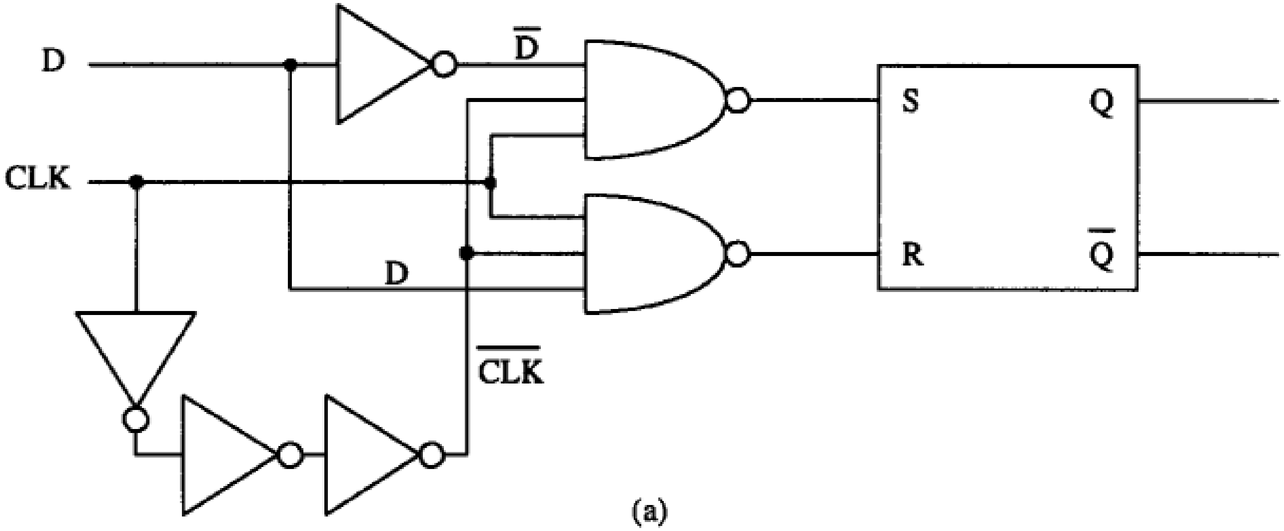


Figure 13.18 Level-sensitive D flip-flop.

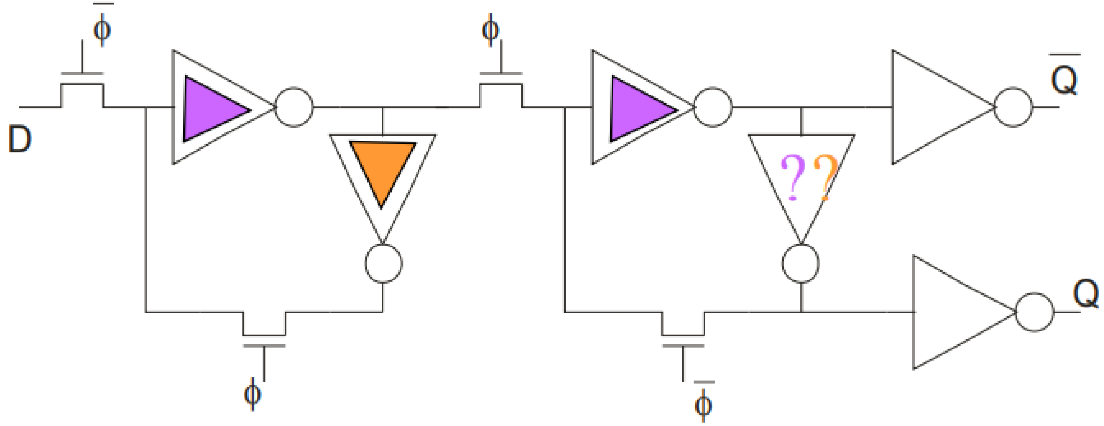


(a)

Transistor Sizing in Flip Flops

Transistor Sizing in Flip Flops

- All Minimum-Size Tx Flip Flops
  - will not be optimized for speed
  - might have some output glitches
  - but much more simple to lay out



- Size Considerations
  - varies widely with chosen FF design
  - feedback INV can be weak
  - tx in direct path to signal output should be larger
  - switches -typically minimum sized to reduce noise

Pulse Generators

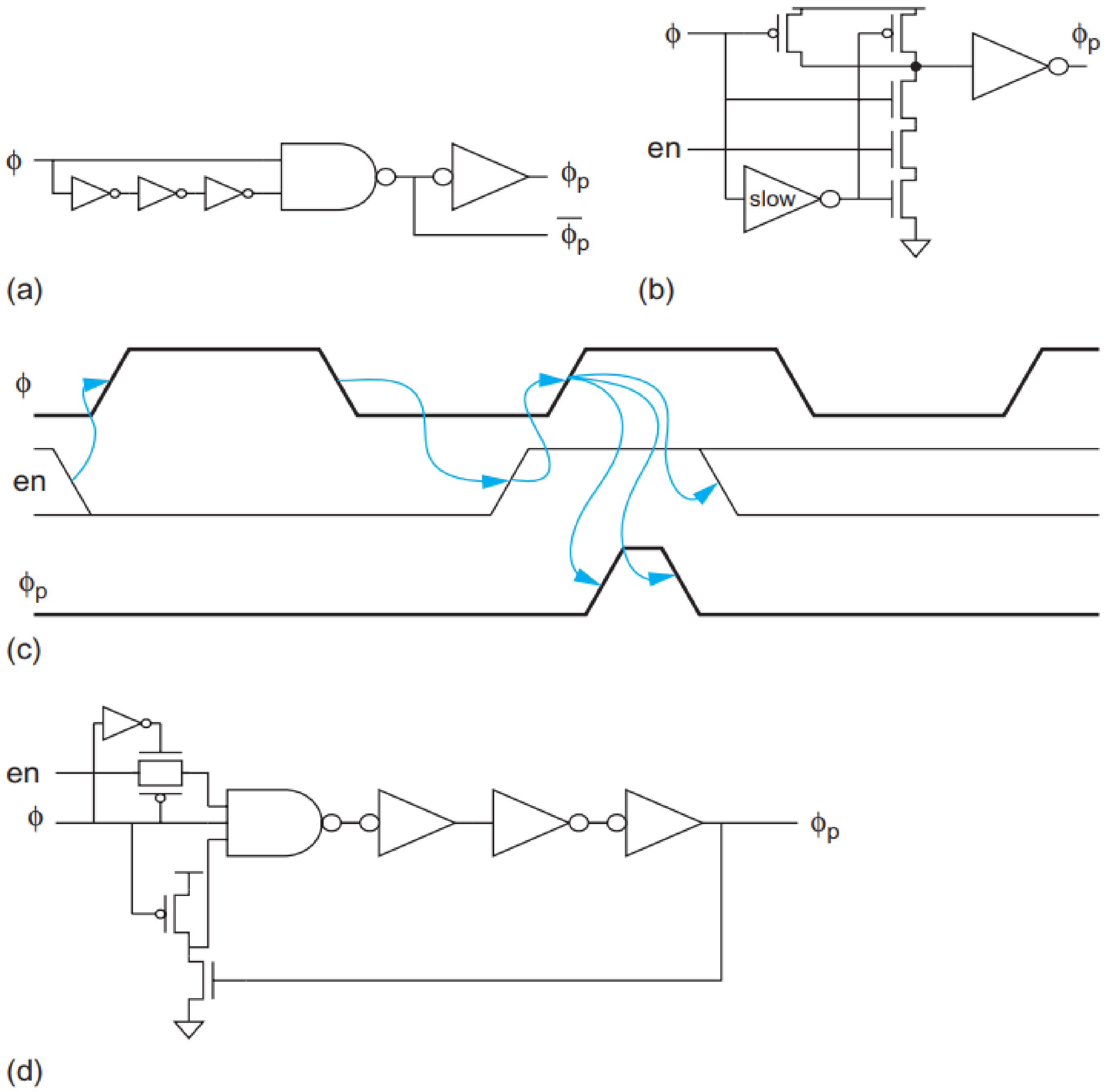
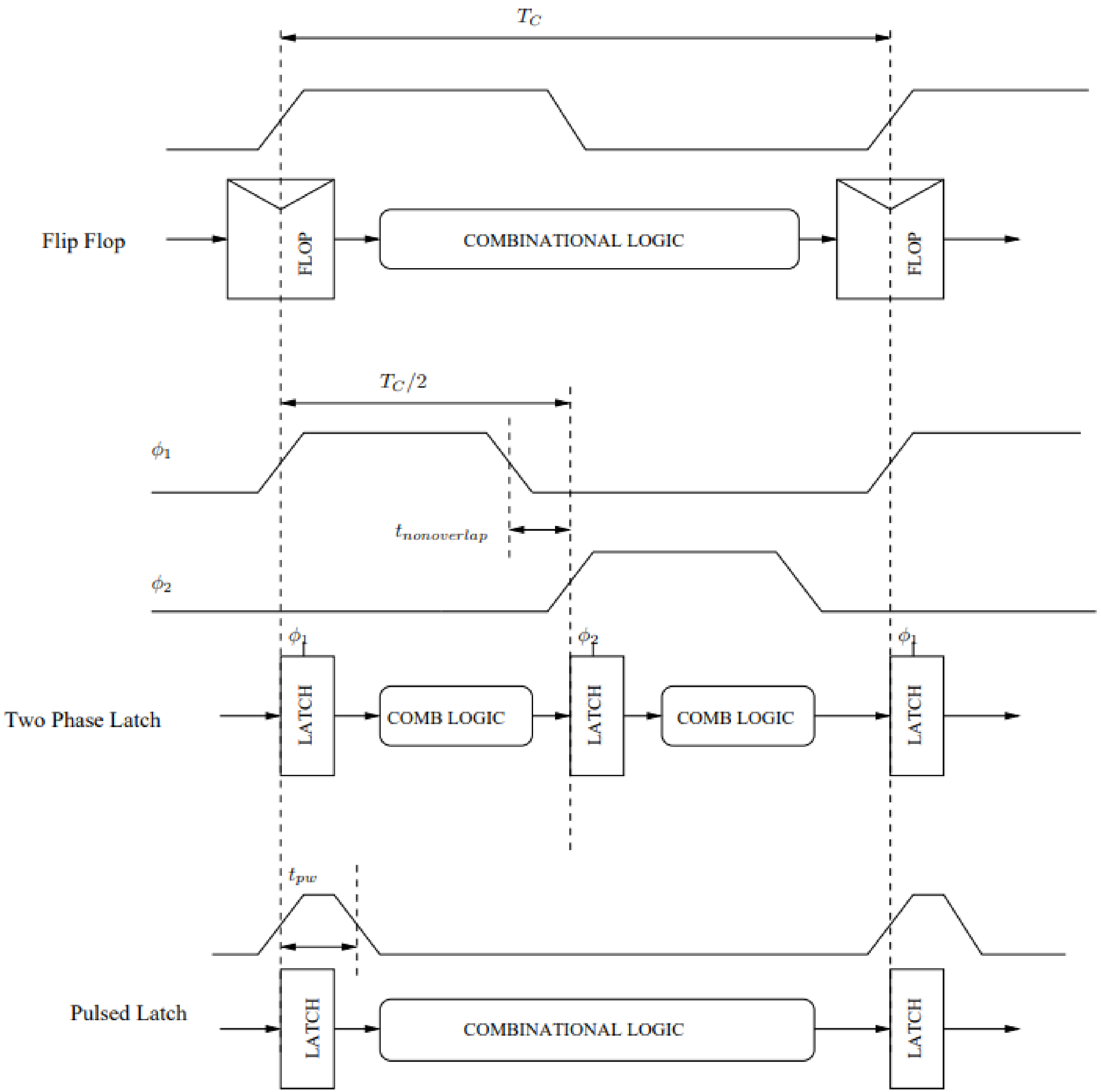


FIGURE 10.22 Pulse generators

Sequencing

Sequencing Methods

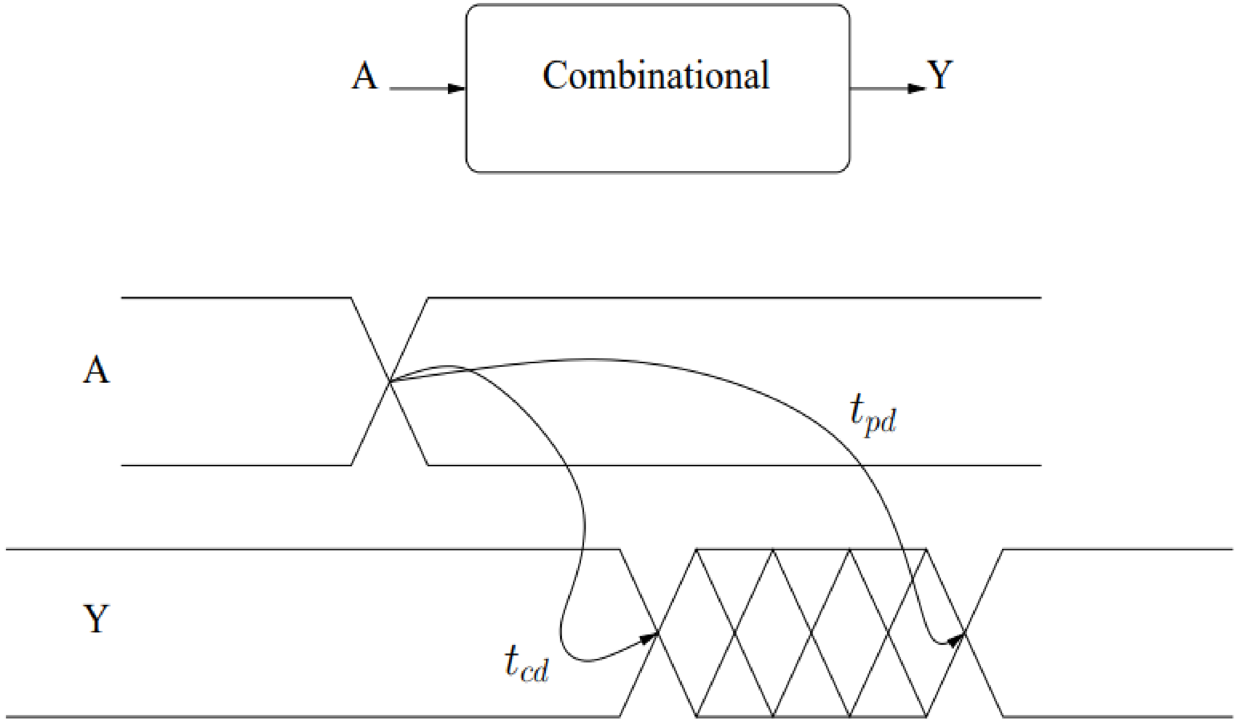


Timing Notation Table

TABLE 10.1 Sequencing element timing notation

Term	Name
t_{pd}	Logic Propagation Delay
t_{cd}	Logic Contamination Delay
t_{pcq}	Latch/Flop Clock-to-Q Propagation Delay
t_{ccq}	Latch/Flop Clock-to-Q Contamination Delay
t_{pdq}	Latch D-to-Q Propagation Delay
t_{cdq}	Latch D-to-Q Contamination Delay
t_{setup}	Latch/Flop Setup Time
t_{hold}	Latch/Flop Hold Time

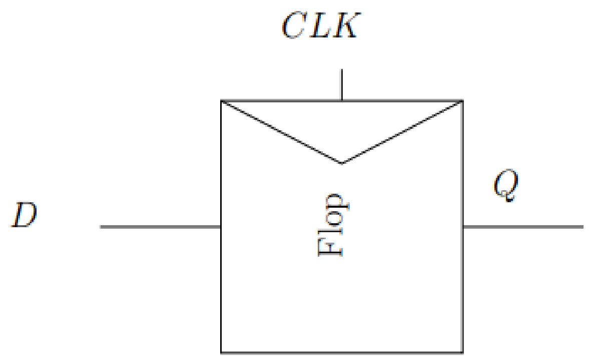
Combinational Logic Delay

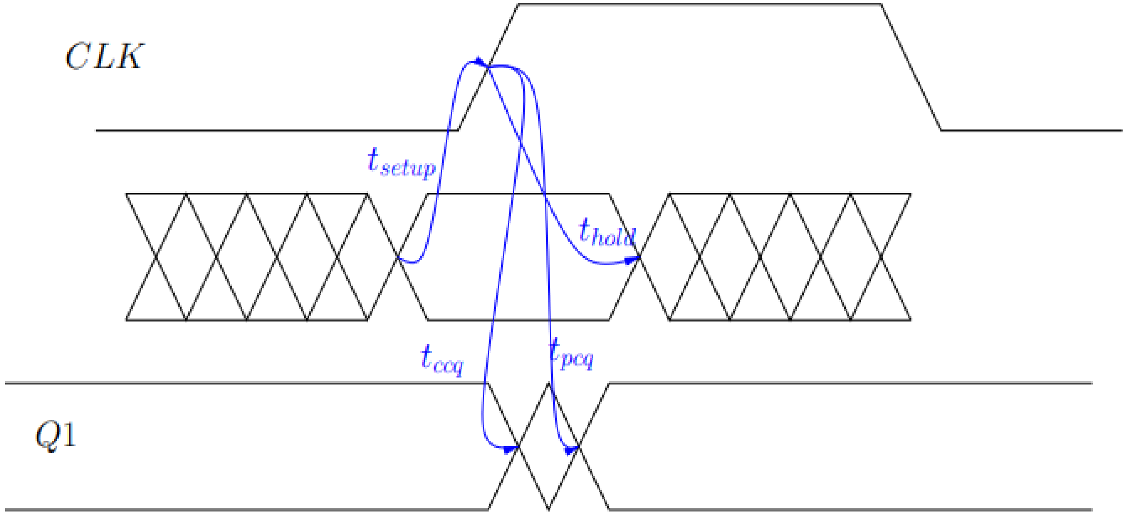


- t_{cd} - Contamination delay - Min delay through the circuit
- t_{pd} - Propagation delay - Max delay through the circuit

Flip Flop Delay

Flip Flop Delay

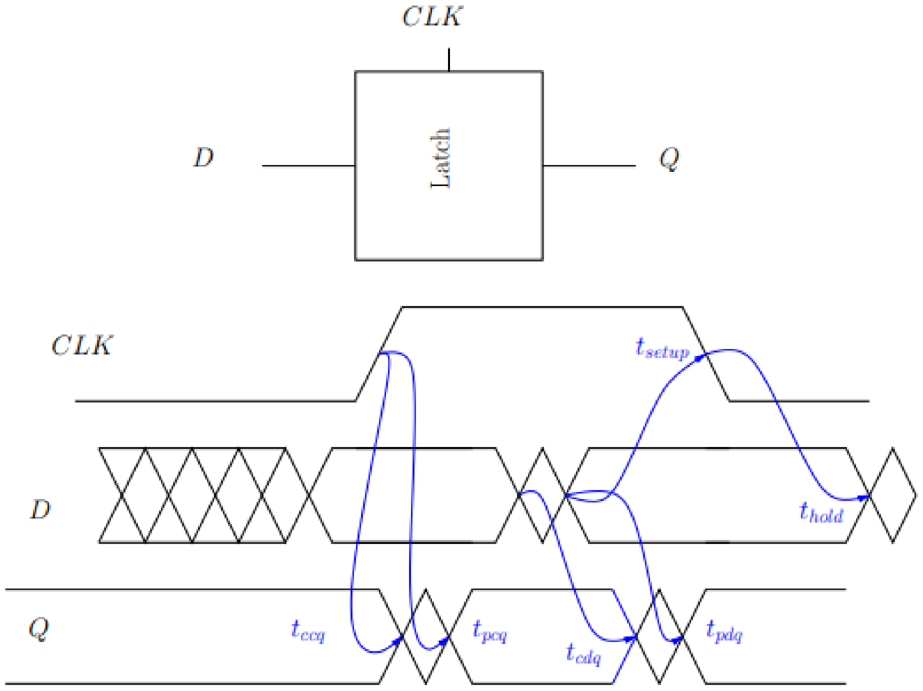




- t_{ccq} - Contamination Clock-Q delay
- t_{pcq} - Propagation Clock-Q delay
- t_{setup} - Set up time
- t_{hold} - Hold time

Latch Delay

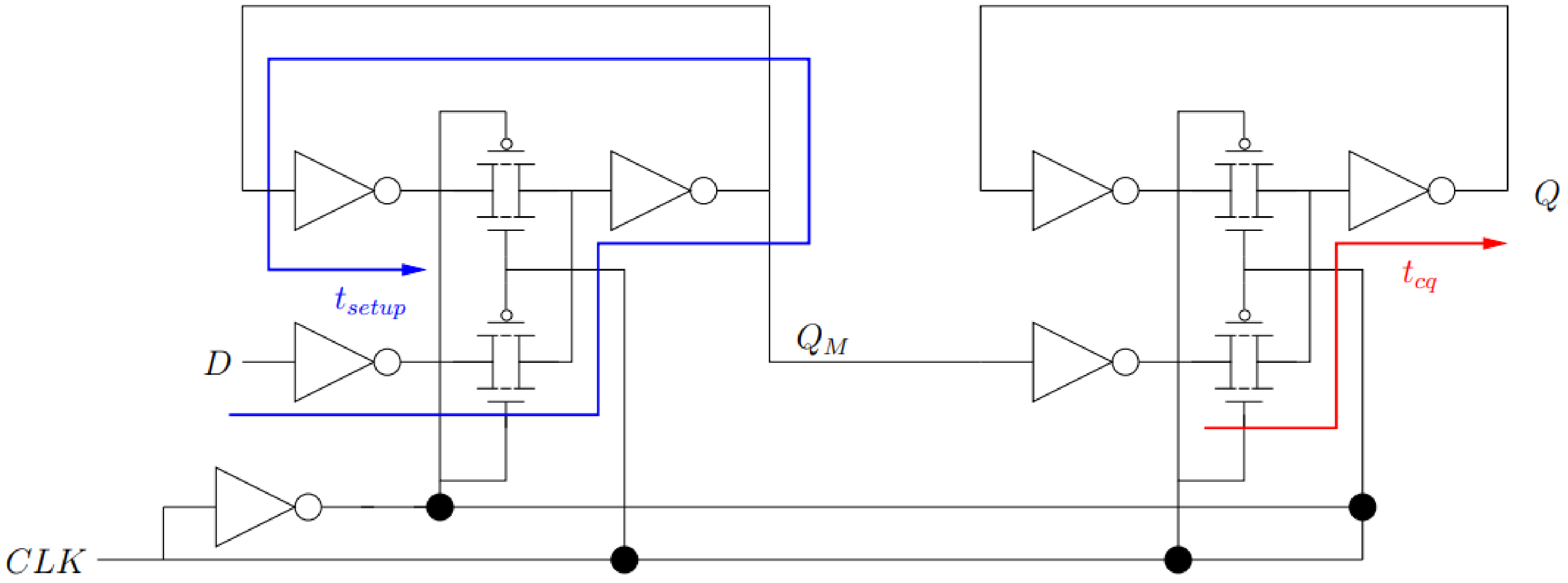
Latch Delay



- t_{ccq} - Contamination Clock-Q delay
- t_{pcq} - Propagation Clock-Q delay
- t_{cdq} - Contamination D-Q delay
- t_{pdq} - Propagation D-Q delay
- t_{setup} - Set up time
- t_{hold} - Hold time

MUX Based DFF – Setup and Hold Timing

Multiplexer Based Flop - Setup and Hold Times



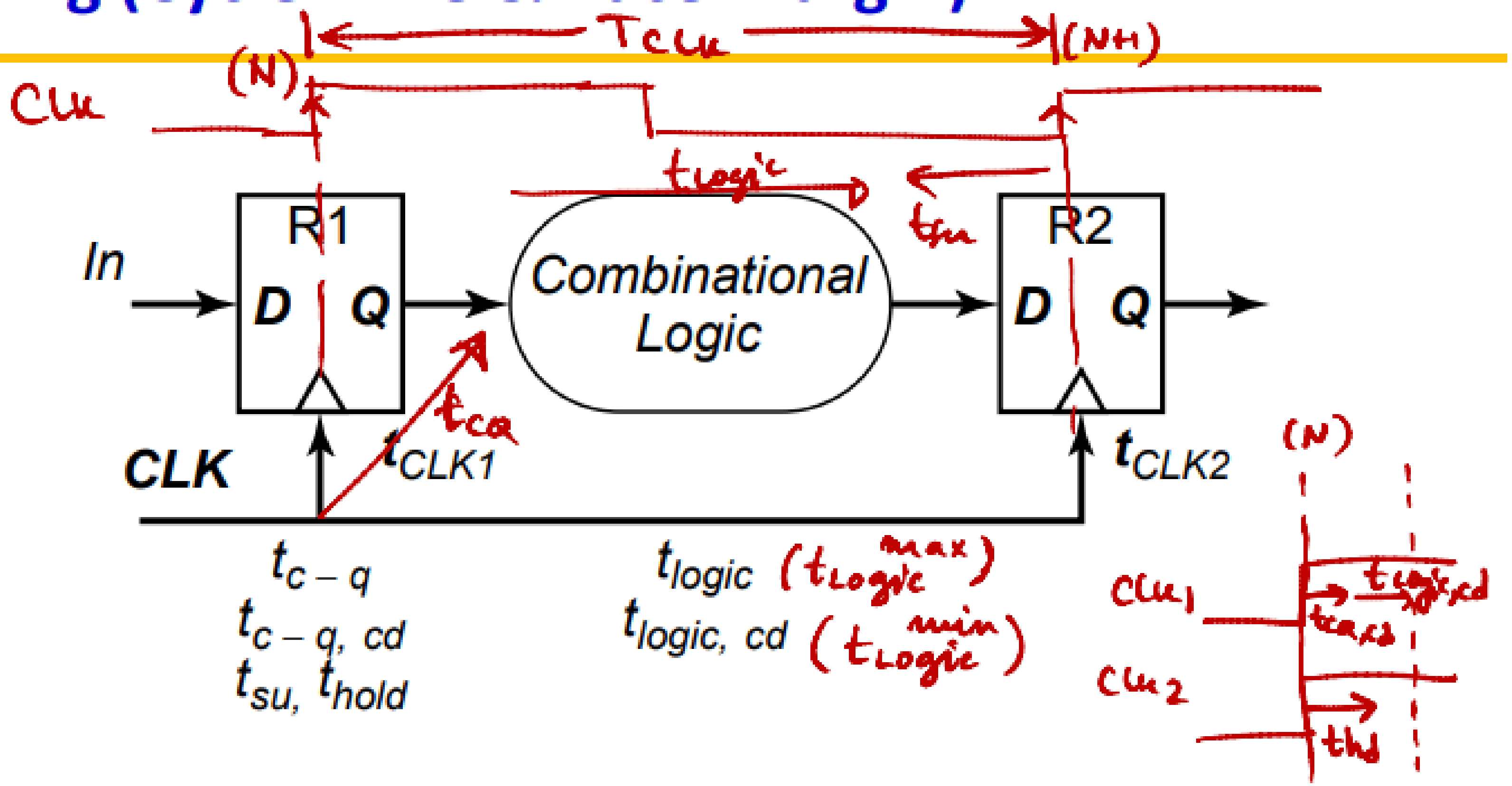
$$t_{setup} = 3t_{inv-pd} + t_{tx-pd}$$

$$t_{cq} = t_{pd-tx} + t_{pd-inv}$$

$$t_{hold} = 0$$

Timing Cycle

Timing (Cycle Time & Race Margin)

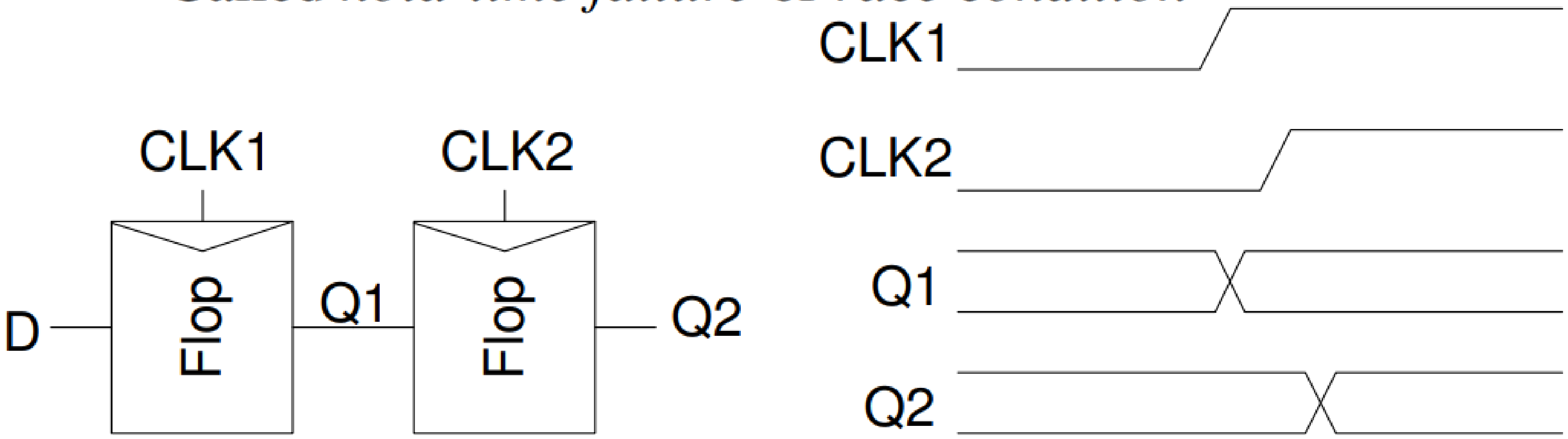


Cycle time: $T_{Clk} > t_{c\text{-}q} + t_{logic} + t_{su}$

Race margin: $t_{hold} < t_{c\text{-}q,cd} + t_{logic,cd}$

Race Condition

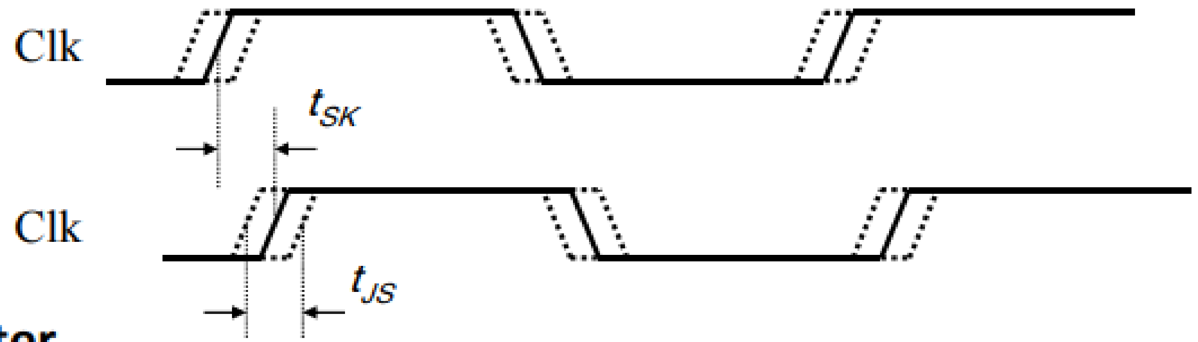
- Back-to-back flops can malfunction from clock skew
  - Second flip-flop fires late
  - Sees first flip-flop change and captures its result
  - Called *hold-time failure* or *race condition*



Non-Ideal Clock

Clock Nonidealities

- **Clock skew**
  - **Spatial** variation in temporally equivalent clock edges; deterministic + random, t_{SK}

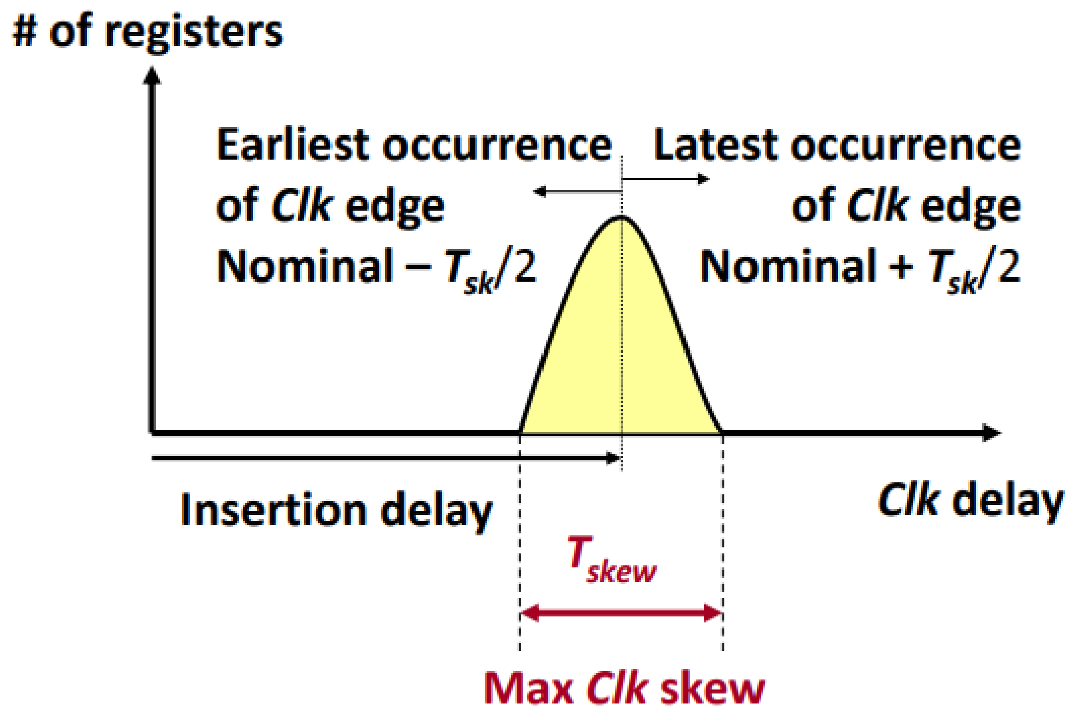


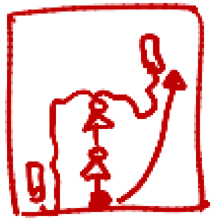
- **Clock jitter**
  - **Temporal** variations in consecutive edges of the clock signal; modulation + random noise
- **Variation of the pulse width**
  - For level-sensitive clocking

Clock Skew

Clock Skew

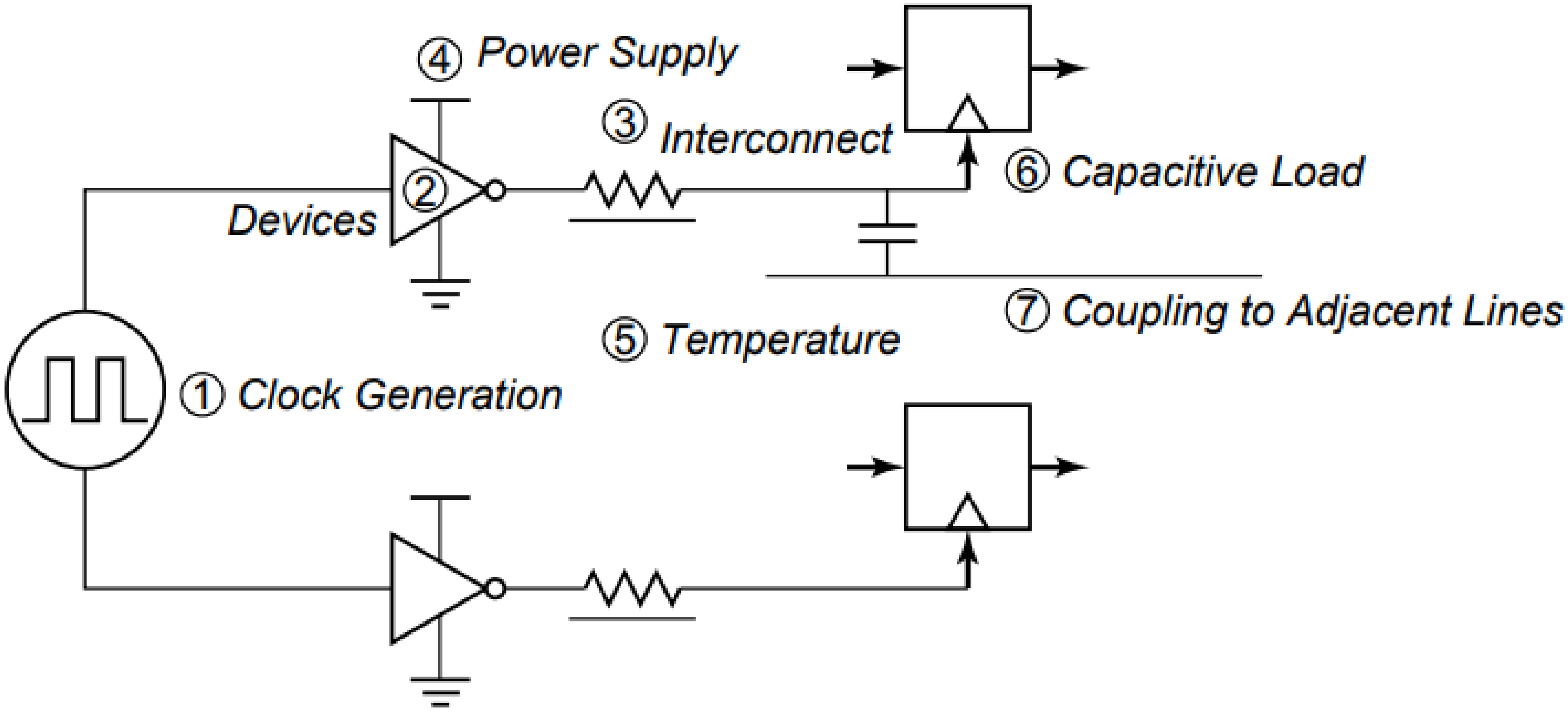
- Distribution of clock tree insertion delay





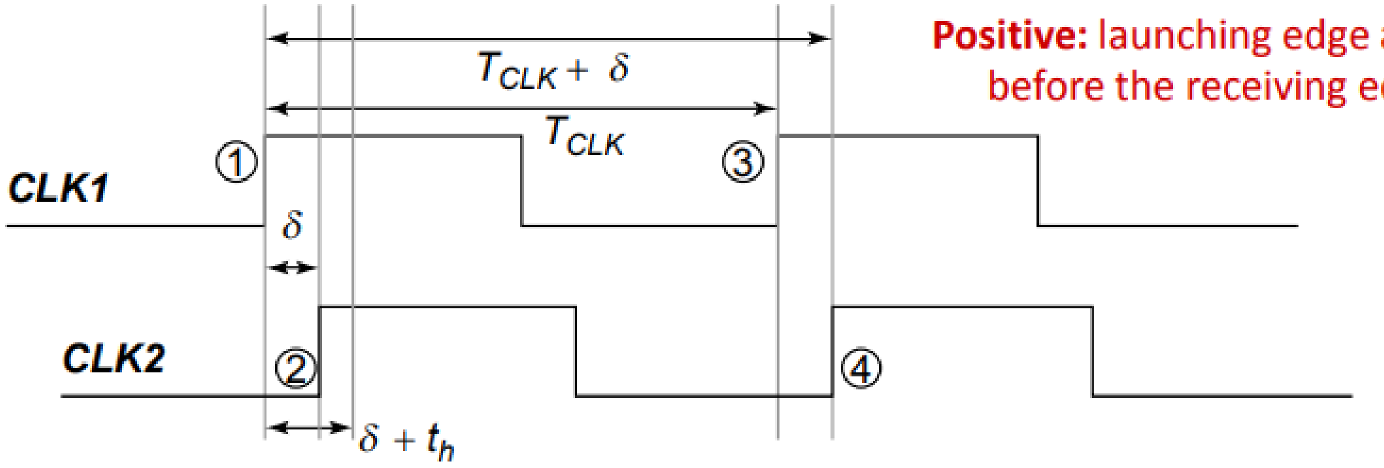
Sources of Skew and Jitter

Sources of Skew and Jitter

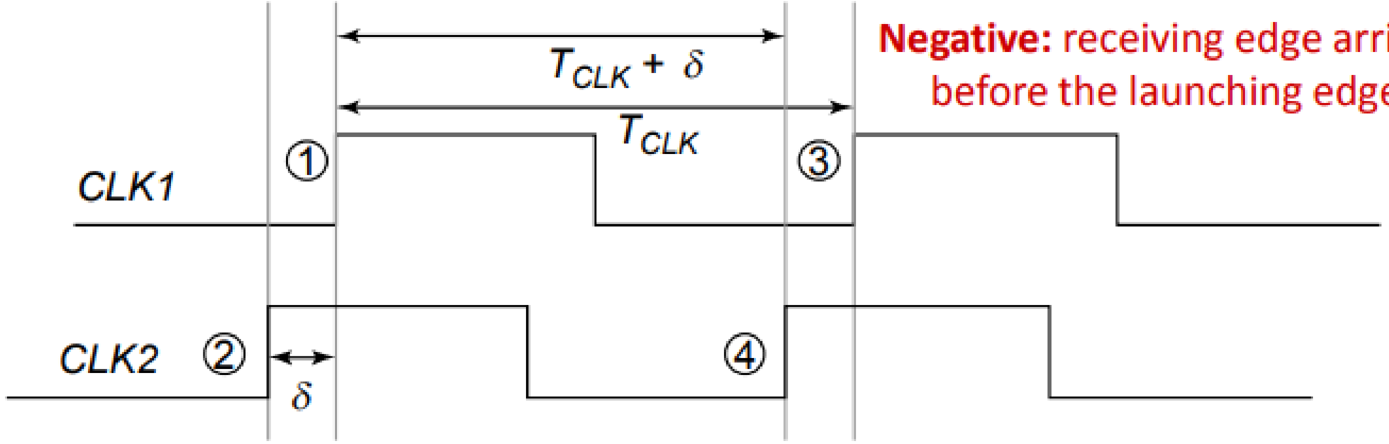


Positive and Negative Skew

Positive and Negative Skew



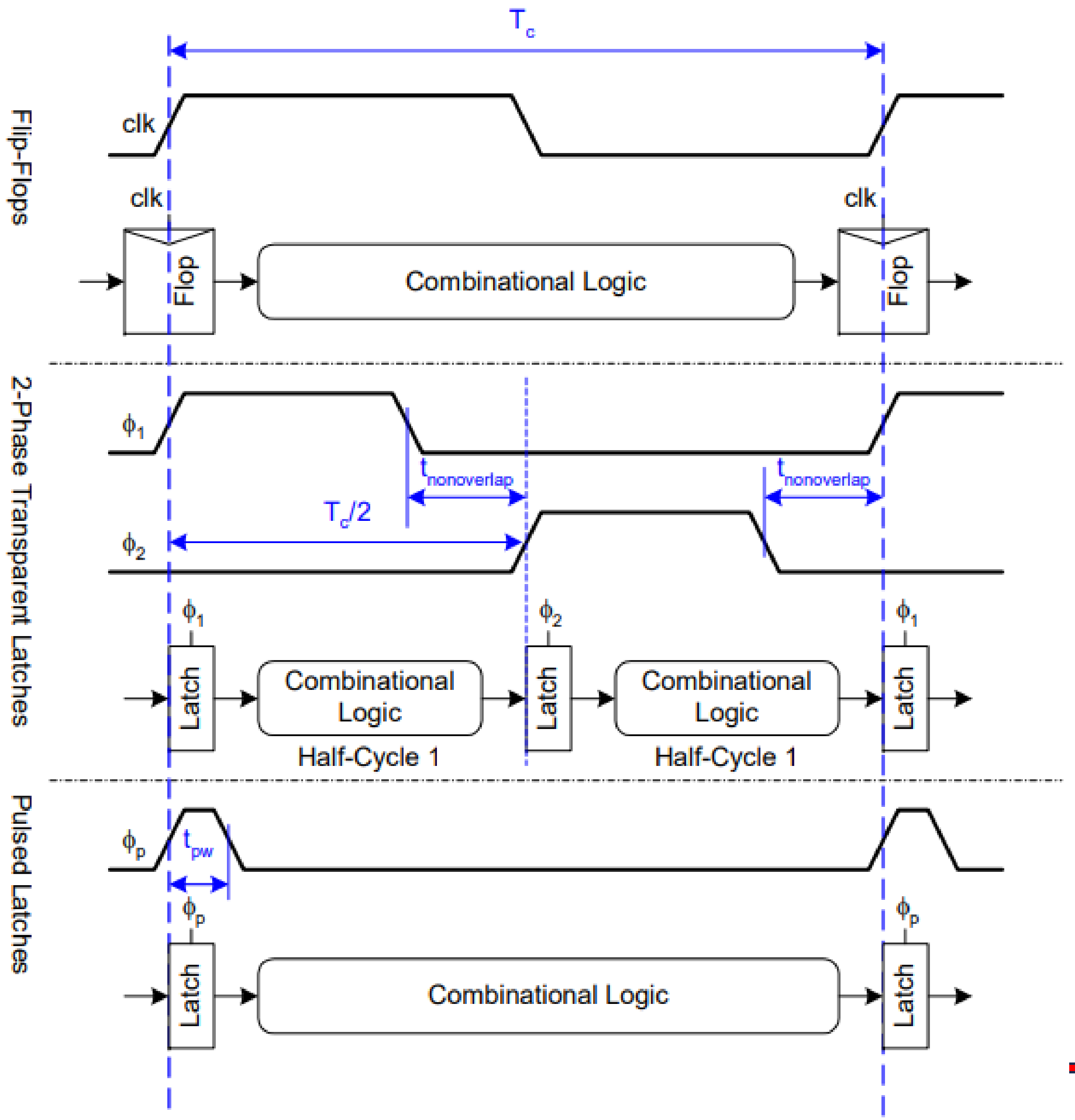
Positive: launching edge arrives before the receiving edge



Negative: receiving edge arrives before the launching edge

Data Sequencing Methods

- Flip-flops
- 2-Phase Latches
- Pulsed Latches



Timing Diagrams with Notations

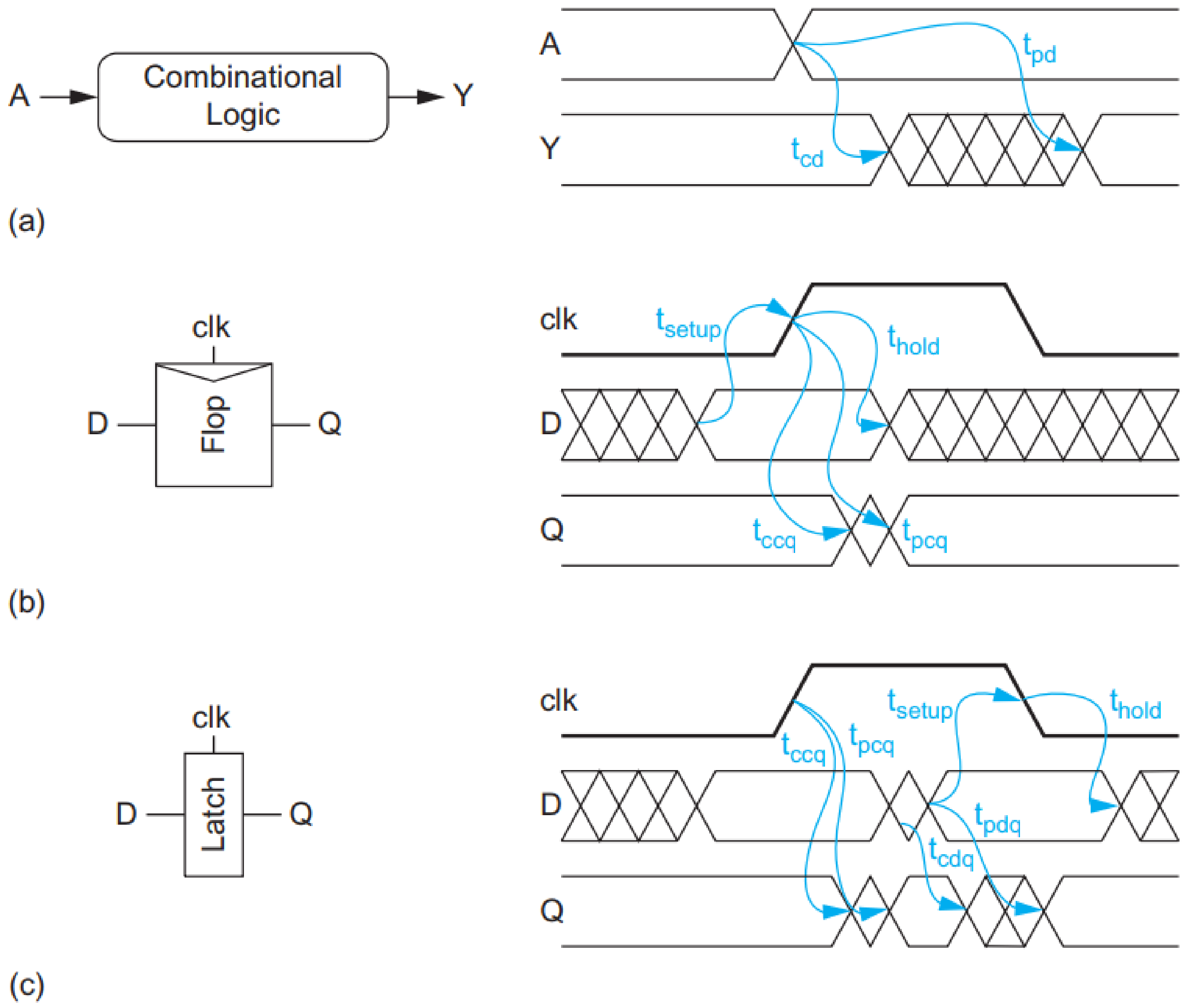
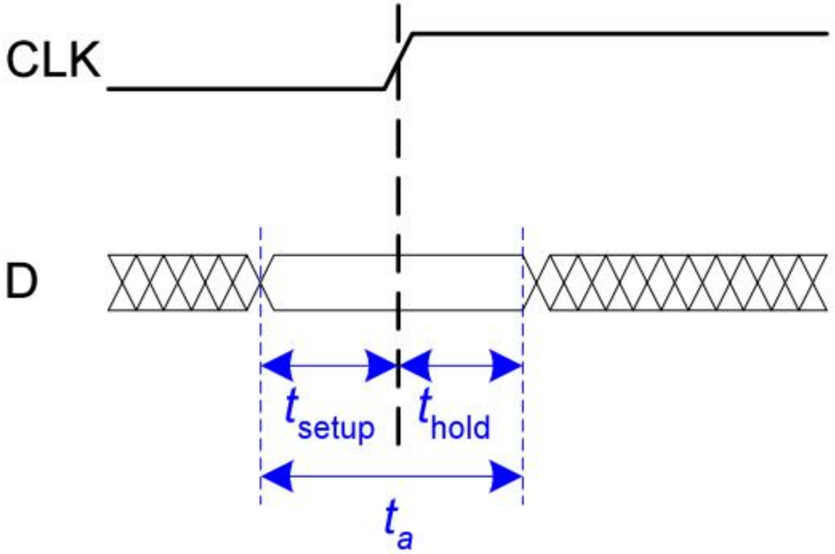


FIGURE 10.4 Timing diagrams

Input Timing Constraints

Input Timing Constraints

- Setup time: t_{setup} = time *before* the clock edge that data must be stable (i.e. not changing)
- Hold time: t_{hold} = time *after* the clock edge that data must be stable
- Aperture time: t_a = time around clock edge that data must be stable ($t_a = t_{setup} + t_{hold}$)



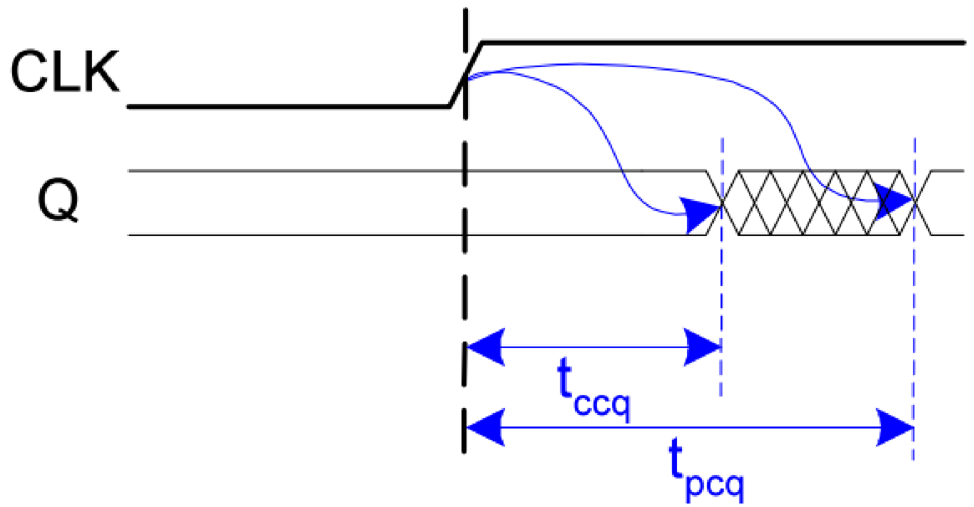
Dynamic Discipline

- The input to a synchronous sequential circuit must be stable during the aperture (setup and hold) time around the clock edge.
- Specifically, the input must be stable
  - at least t_{setup} before the clock edge
  - at least until t_{hold} after the clock edge

Output Timing Constraints

Output Timing Constraints

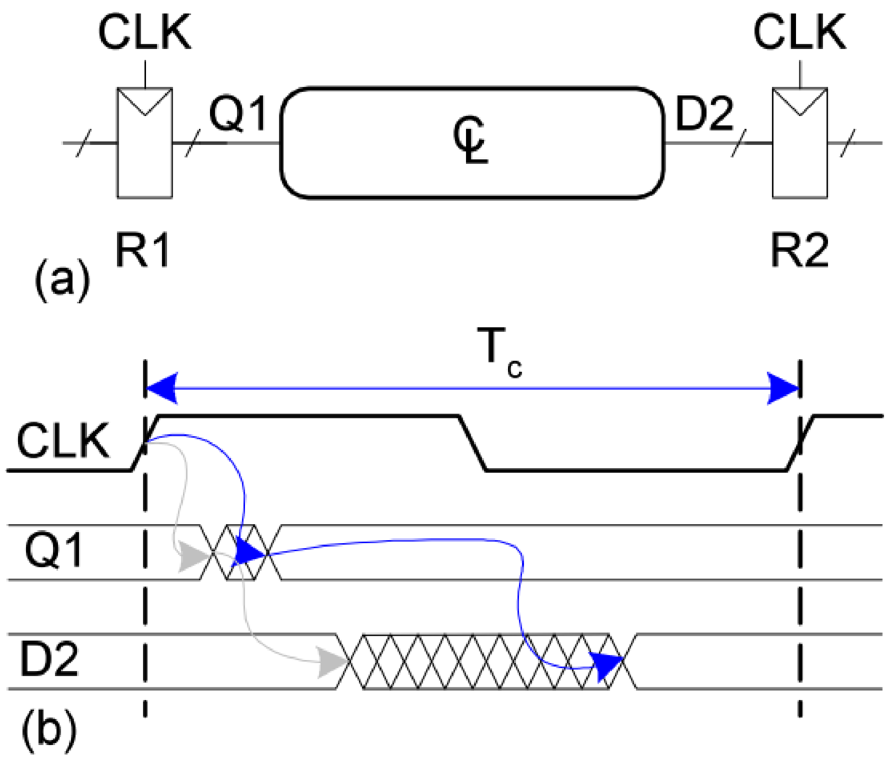
- Propagation delay: t_{pcq} = time after clock edge that the output Q is guaranteed to be stable (i.e., to stop changing)
- Contamination delay: t_{ccq} = time after clock edge that Q might be unstable (i.e., start changing)



Dynamic Delay Discipline

Dynamic Discipline

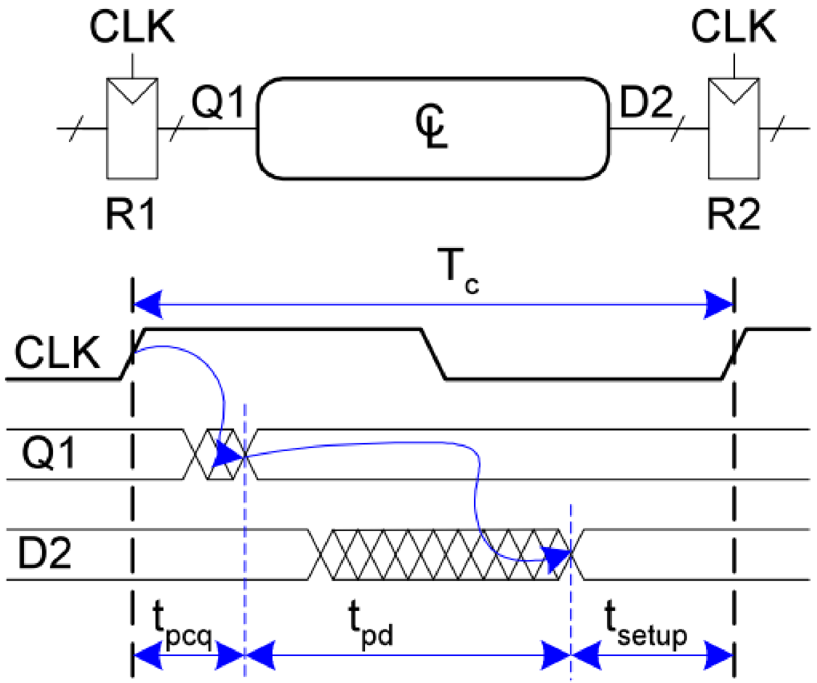
- The delay between registers has a **minimum** and **maximum** delay, dependent on the delays of the circuit elements



Setup Time Constraints

Setup Time Constraint

- The setup time constraint depends on the **maximum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable at least t_{setup} before the clock edge.

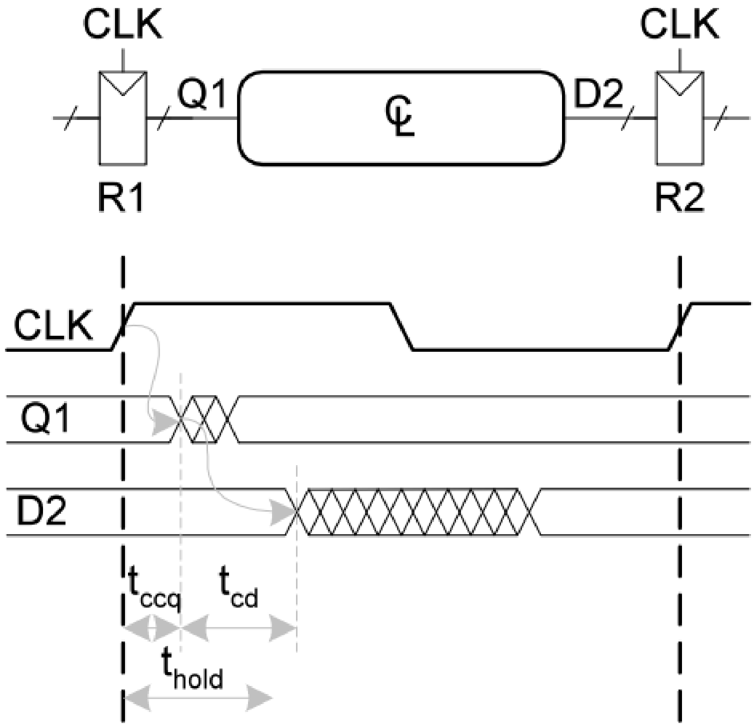


$$T_c \geq t_{pcq} + t_{pd} + t_{setup}$$
$$t_{pd} \leq T_c - (t_{pcq} + t_{setup})$$

Hold Time Constraints

Hold Time Constraint

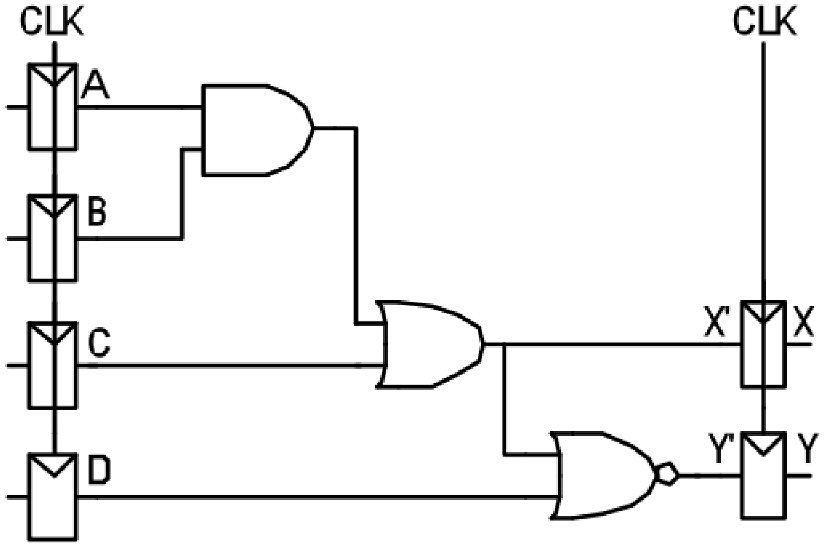
- The hold time constraint depends on the **minimum** delay from register R1 through the combinational logic.
- The input to register R2 must be stable for at least t_{hold} after the clock edge.



$$t_{hold} < t_{ccq} + t_{cd}$$
$$t_{cd} > t_{hold} - t_{ccq}$$

Example of Timing Analysis

Timing Analysis



Timing Characteristics

t_{ccq} = 30 ps

t_{pcq} = 50 ps

t_{setup} = 60 ps

t_{hold} = 70 ps

per gate
t_{pd} = 35 ps
t_{cd} = 25 ps

t_{pd} = 3 x 35 ps = 105 ps

t_{cd} = 25 ps

Setup time constraint:

$T_c \geq (50 + 105 + 60)$ ps = 215 ps

$f_c = 1/T_c$ = 4.65 GHz

Hold time constraint:

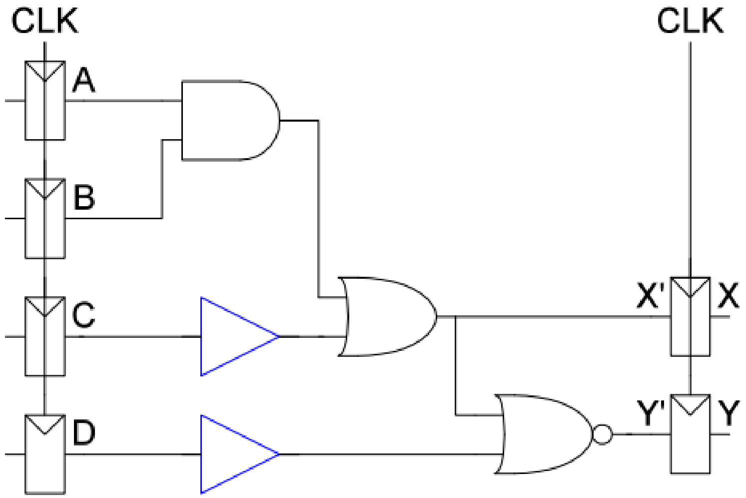
$t_{ccq} + t_{pd} > t_{hold}$?

(30 + 25) ps > 70 ps ? No!

Fixing Hold Time Violation

Fixing Hold Time Violation

Add buffers to the short paths:



t_{pd} = 3 x 35 ps = 105 ps

t_{cd} = 2 x 25 ps = 50 ps

Setup time constraint:

$T_c \geq (50 + 105 + 60)$ ps = 215 ps

$f_c = 1/T_c$ = 4.65 GHz

Timing Characteristics

t_{ccq} = 30 ps

t_{pcq} = 50 ps

t_{setup} = 60 ps

t_{hold} = 70 ps

per gate $\left[\begin{array}{l} t_{pd} = 35 \text{ ps} \\ t_{cd} = 25 \text{ ps} \end{array}\right.$

Hold time constraint:

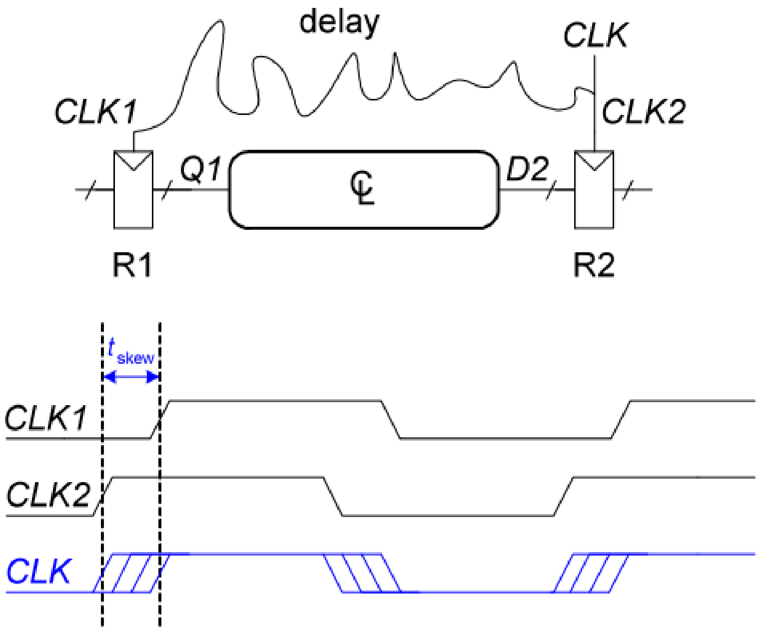
$t_{ccq} + t_{pd} > t_{hold}$?

(30 + 50) ps > 70 ps ? Yes!

Clock Skew

Clock Skew

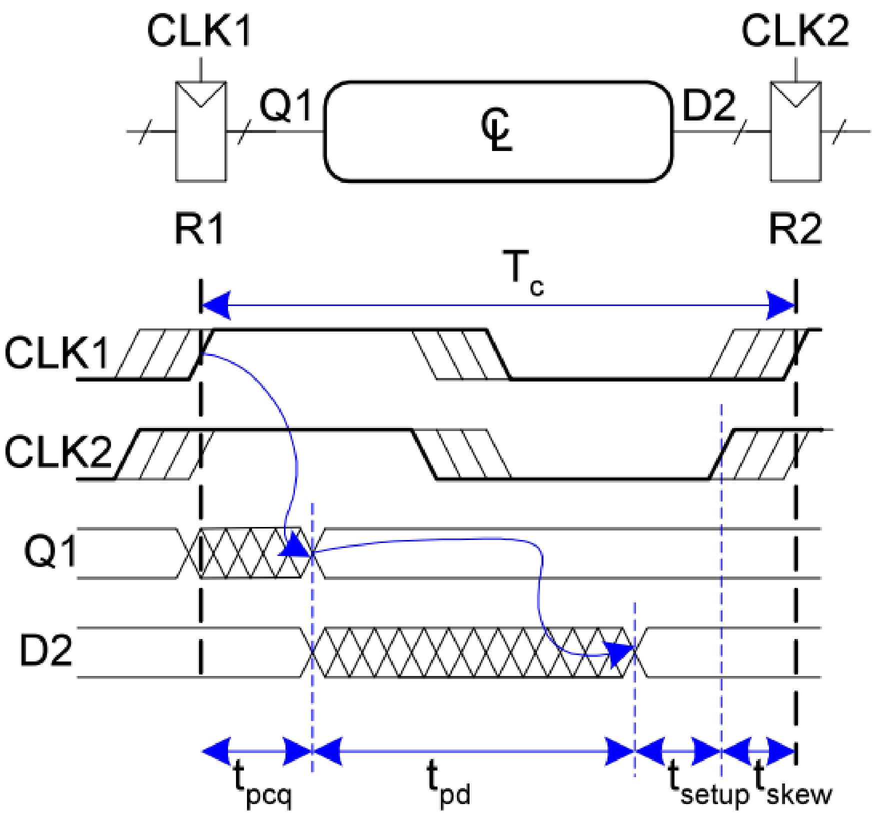
- The clock doesn't arrive at all registers at the same time
- Skew is the difference between two clock edges
- Examine the worst case to guarantee that the dynamic discipline is not violated for any register – many registers in a system!



Setup Time Constraint with Clock Skew

Setup Time Constraint with Clock Skew

- In the worst case, the CLK2 is earlier than CLK1



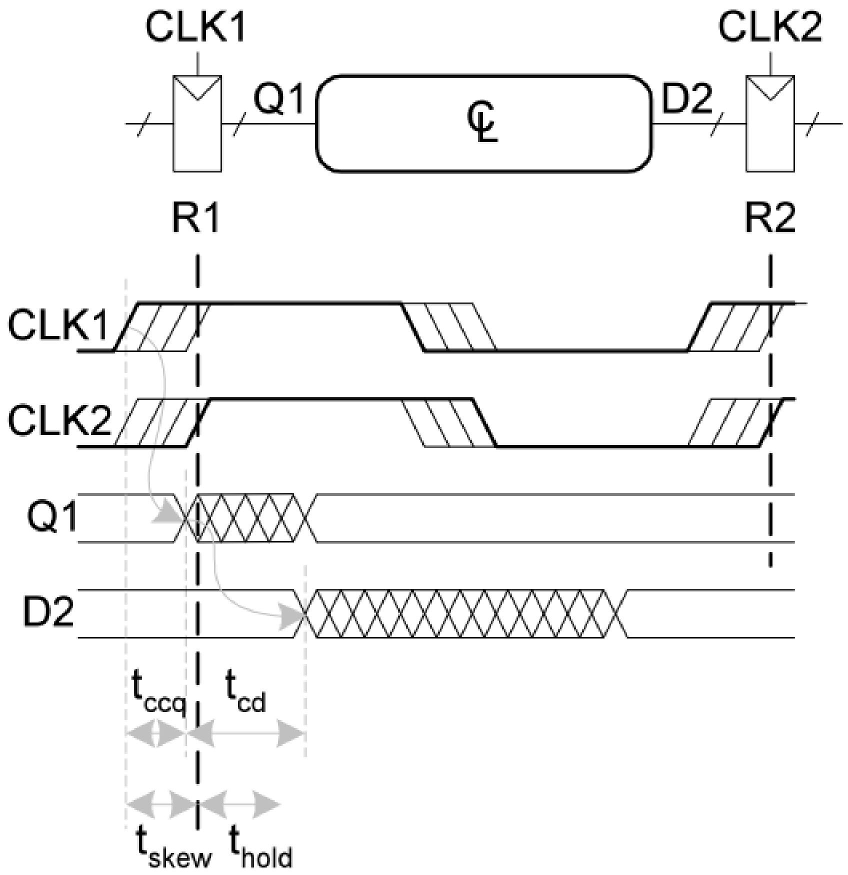
$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} + t_{\text{skew}}$$

$$t_{pd} \leq T_c - (t_{pcq} + t_{\text{setup}} + t_{\text{skew}})$$

Hold Time Constraint with Clock Skew

Hold Time Constraint with Clock Skew

- In the worst case, CLK2 is later than CLK1



$$t_{ccq} + t_{cd} > t_{\text{hold}} + t_{\text{skew}}$$
$$t_{cd} > t_{\text{hold}} + t_{\text{skew}} - t_{ccq}$$

Flip Flop Max Delay Constraint

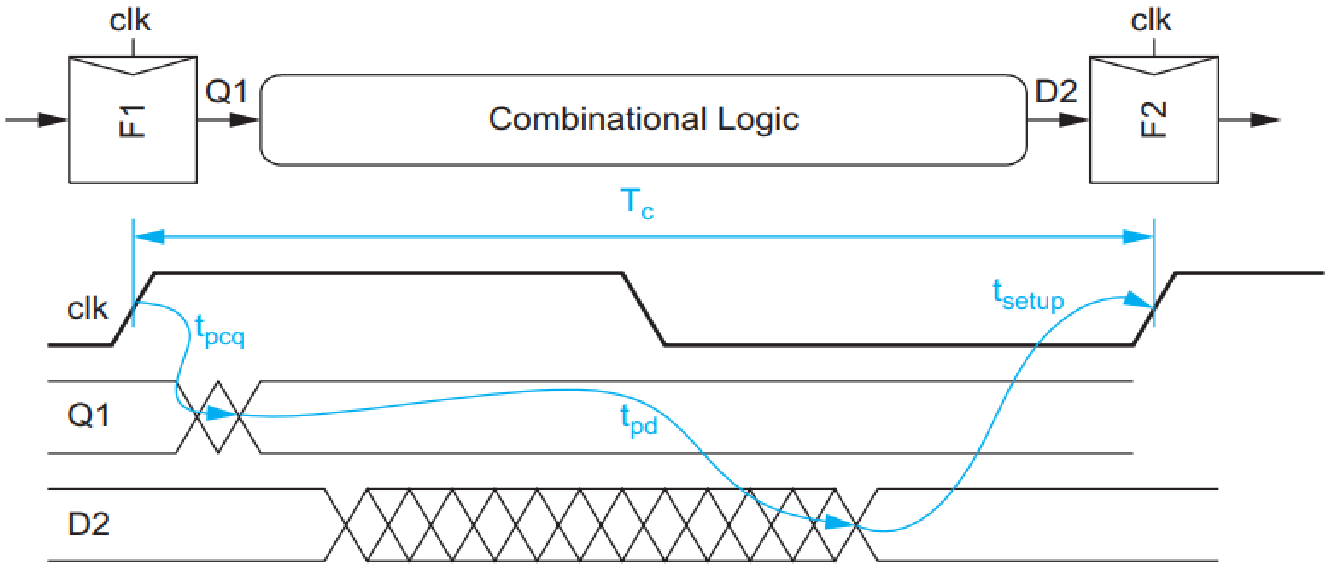


FIGURE 10.5 Flip-flop max-delay constraint

This implies that the clock period must be at least

$$T_c \geq t_{pcq} + t_{pd} + t_{\text{setup}} \tag{10.1}$$

Alternatively, we can solve for the maximum allowable logic delay, which is simply the cycle time less the sequencing overhead introduced by the propagation delay and setup time of the flip-flop.

$$t_{pd} \leq T_c - \underbrace{\left(t_{\text{setup}} + t_{pcq}\right)}_{\text{sequencing overhead}} \tag{10.2}$$

Pulsed Latch Max Delay Constraint

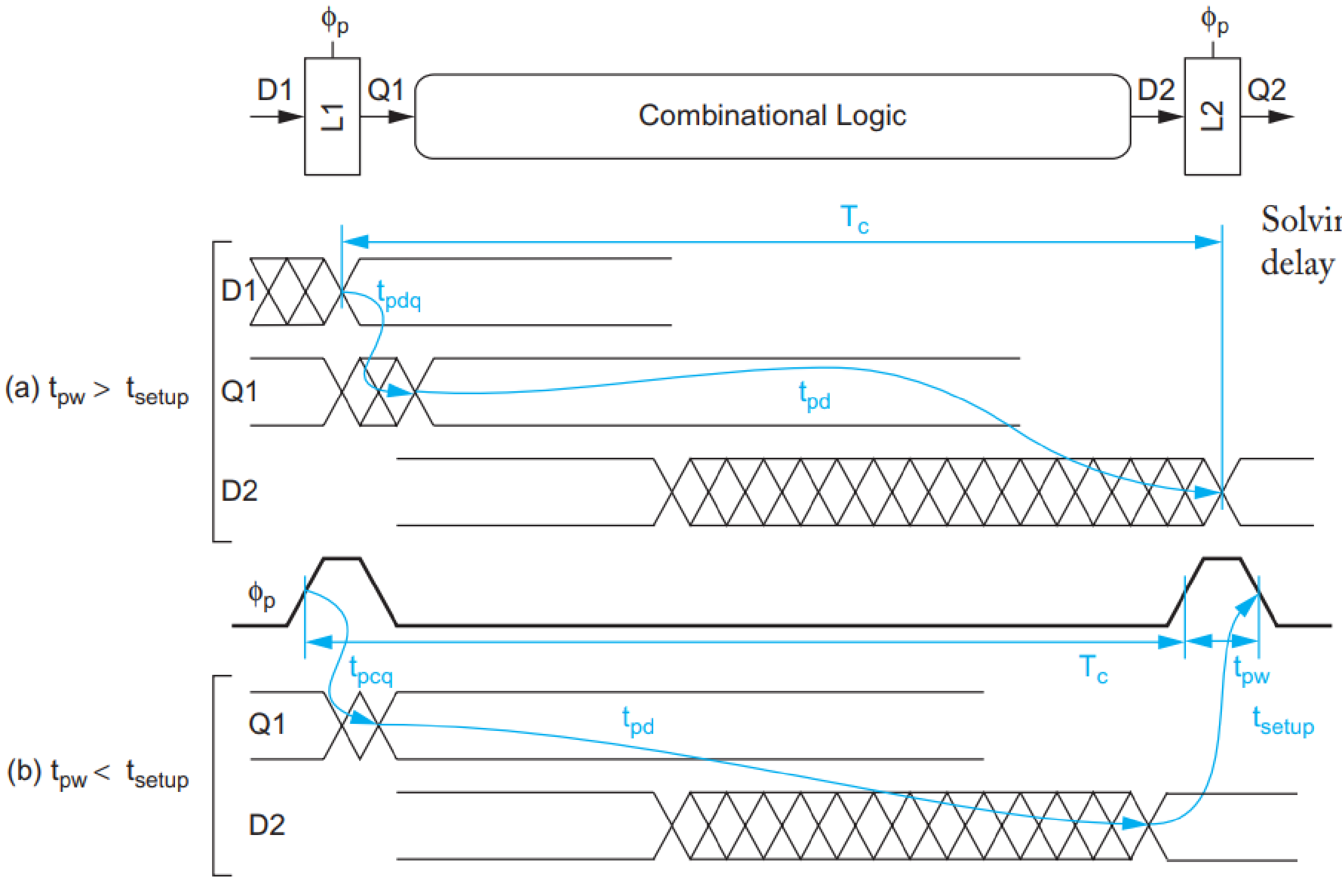


FIGURE 10.8 Pulsed latch max-delay constraint

except that only one latch is in the critical path, as shown in Figure 10.8(a). However, if the pulse is narrower than the setup time, the data must set up before the pulse rises, as shown in Figure 10.8(b). Combining these two cases gives

$$T_c \geq \max\left(t_{pdq} + t_{pd},\ t_{pcq} + t_{pd} + t_{\text{setup}} - t_{pw}\right) \qquad \textbf{(10.5)}$$

Solving for the maximum logic delay shows that the sequencing overhead is just one latch delay if the pulse is wide enough to hide the setup time

$$t_{pd} \leq T_c - \underbrace{\max\left(t_{pdq},\ t_{pcq} + t_{\text{setup}} - t_{pw}\right)}_{\text{sequencing overhead}} \qquad \textbf{(10.6)}$$

Flip Flop / Latch Min Delay Constraint

Figure 10.9 shows the min-delay timing constraints on a path from one flip-flop to the next assuming ideal clocks with no skew. The path begins with the rising edge of the clock triggering $F1$. The data may begin to change at $Q1$ after a *clk*-to-Q contamination delay, and at $D2$ after another logic contamination delay. However, it must not reach $D2$ until at least the hold time t_{hold} after the clock edge, lest it corrupt the contents of $F2$. Hence, we solve for the minimum logic contamination delay:

$$t_{cd} \geq t_{\text{hold}} - t_{ccq} \tag{10.7}$$

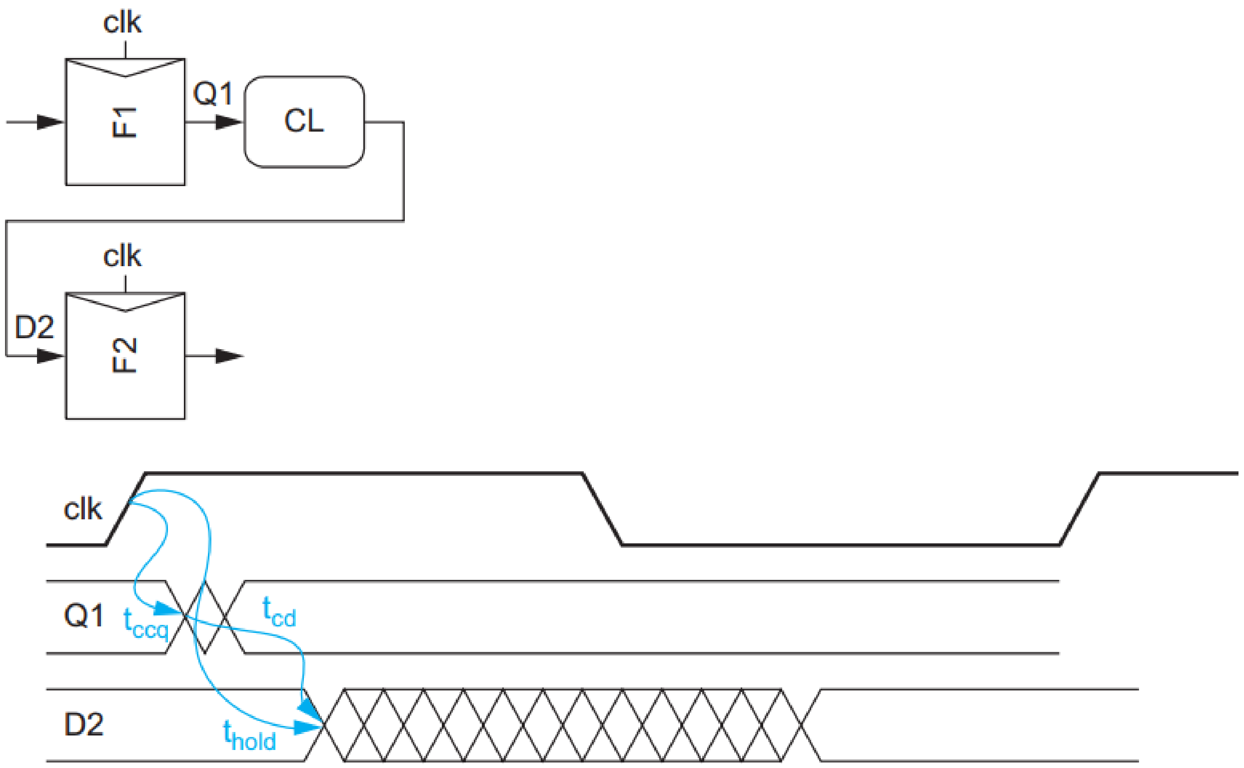
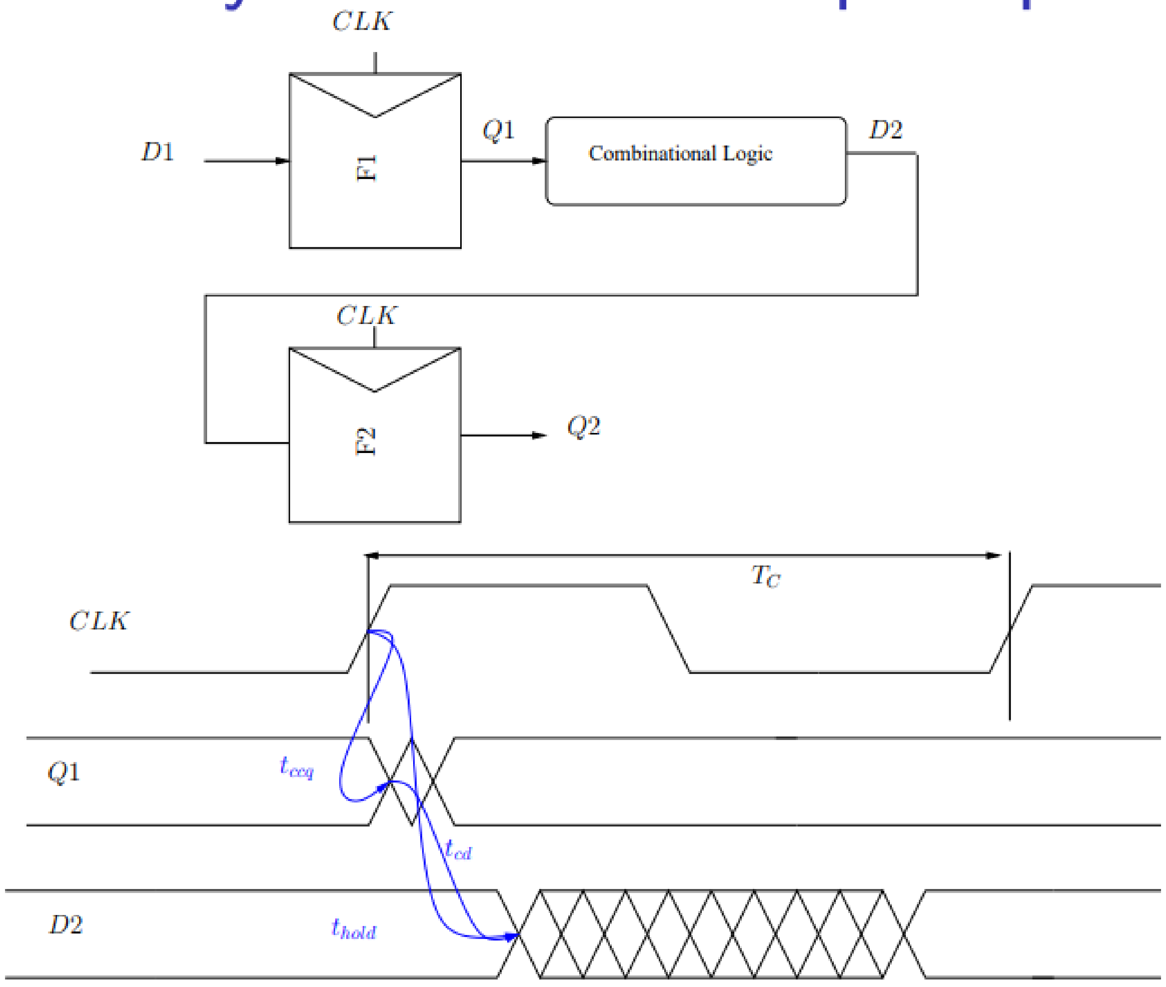


FIGURE 10.9 Flip-flop latch min-delay constraint

Min Delay Constraint DFF

Min Delay Constraint - Flip Flop

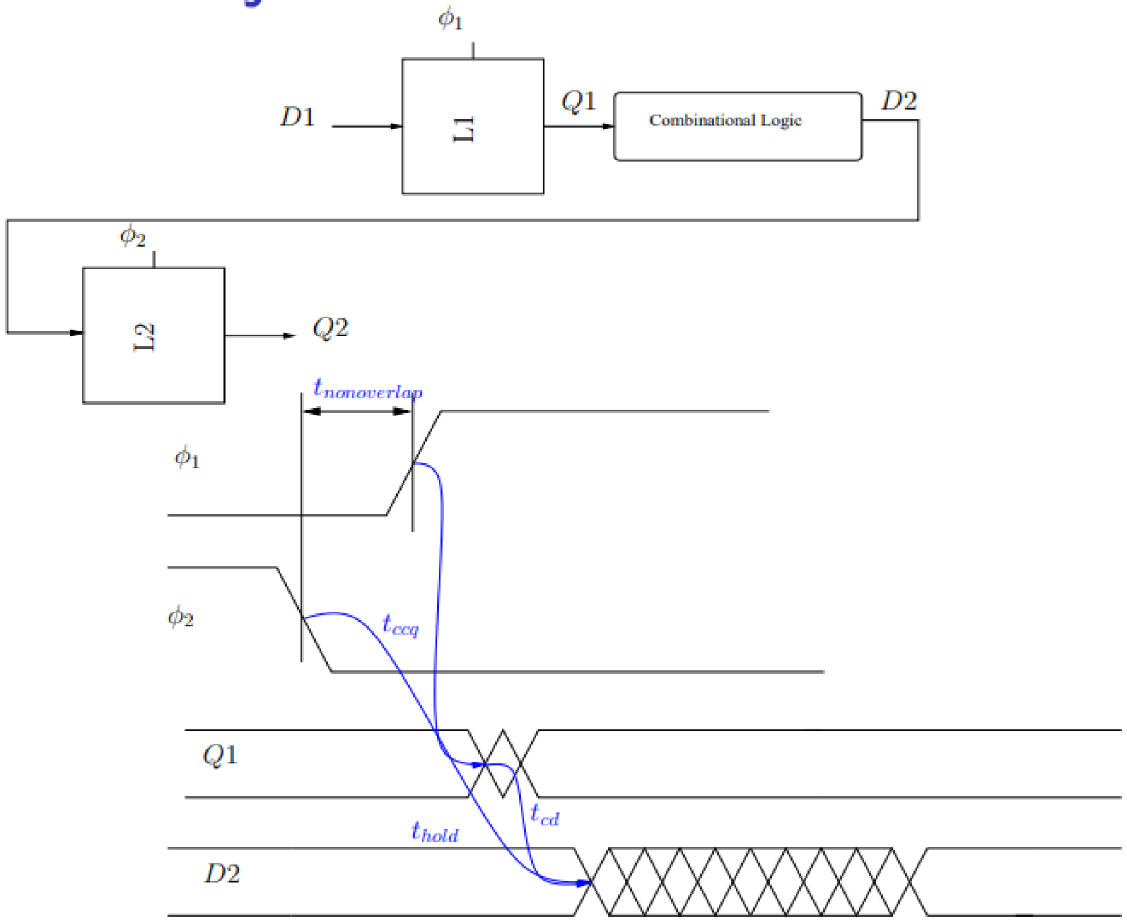


$$t_{hold} \leq t_{cd} + t_{ccq}$$

$$t_{cd} \geq t_{hold} - t_{ccq}$$

Min Delay Constraint Latch

Min Delay Constraint - Latch



$$t_{hold} \leq t_{cd1}, t_{cd2} + t_{ccq} + t_{nonoverlap}$$

$$t_{cd1}, t_{cd2} \geq t_{hold} - t_{ccq} - t_{nonoverlap}$$

Bidirectional I/O Pad Circuit

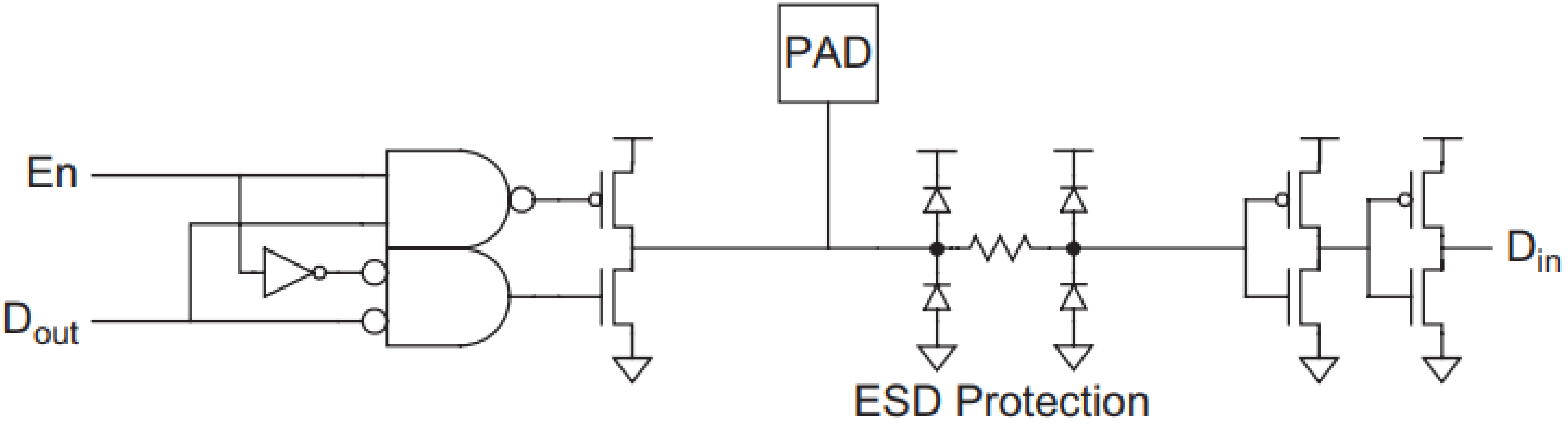


FIGURE 13.47 Bidirectional pad circuitry

Two Phase Max Delay Constraint

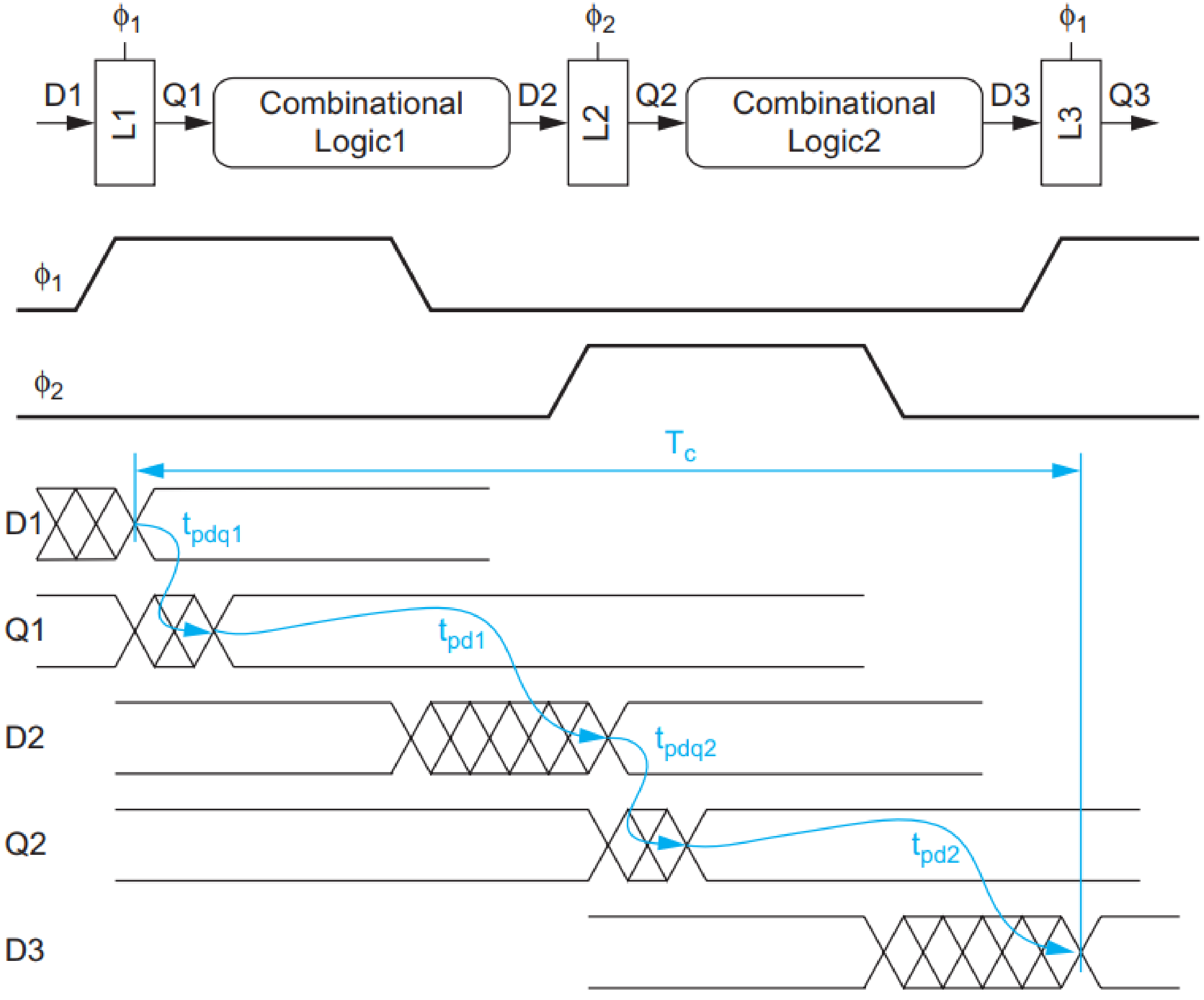


FIGURE 10.7 Two-phase latch max-delay constraint

time borrowing and will be addressed in Section 10.2.4. Assuming the path takes no more than a cycle, we see the cycle time must be

$$T_c \geq t_{pdq1} + t_{pd1} + t_{pdq2} + t_{pd2} \tag{10.3}$$

national logic between latches even while both clocks are low. Realizing that a flip-flop can be made from two latches whose delays determine the flop propagation delay and setup time, we see EQ (10.4) is closely analogous to EQ (10.2).

$$t_{pd} = t_{pd1} + t_{pd2} \leq T_c - \underbrace{\left(2t_{pdq}\right)}_{\text{sequencing overhead}} \tag{10.4}$$

Input Protection Circuit

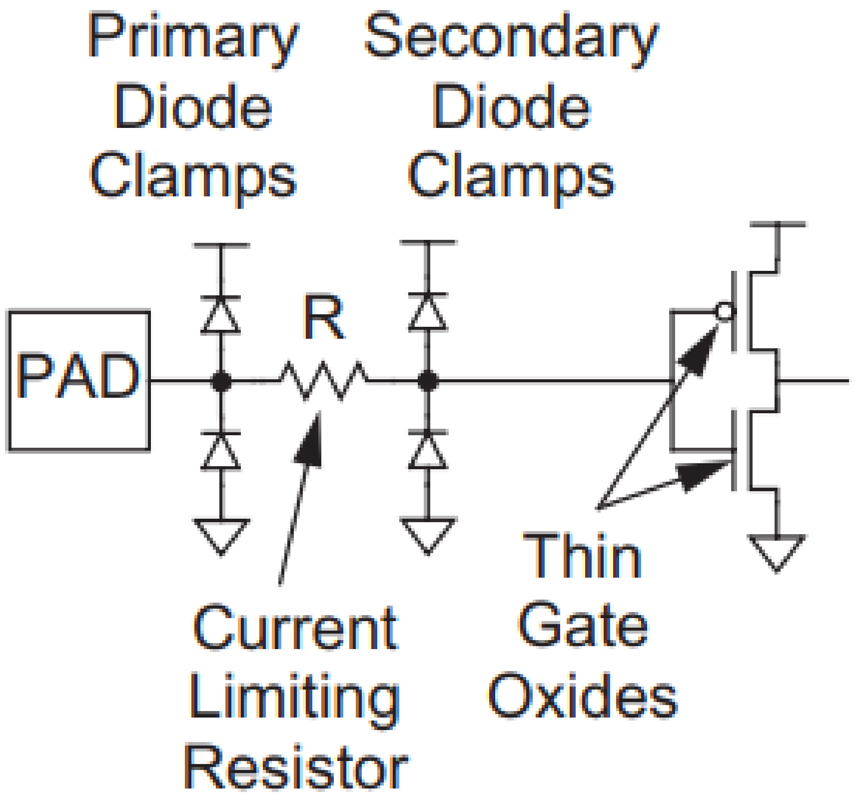


FIGURE 13.49 Input protection circuitry

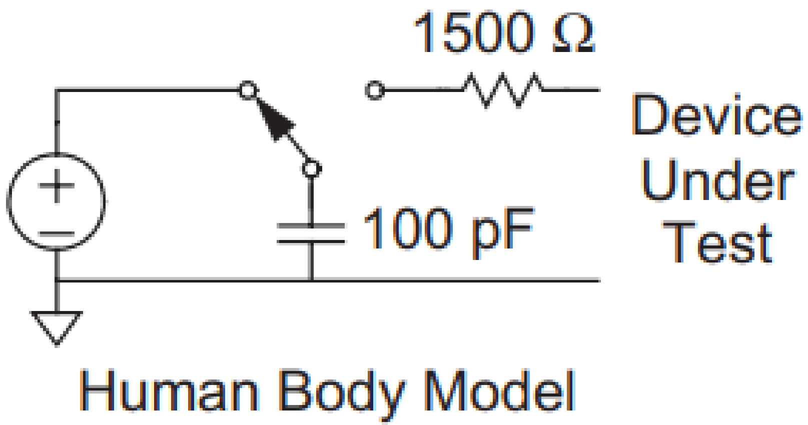
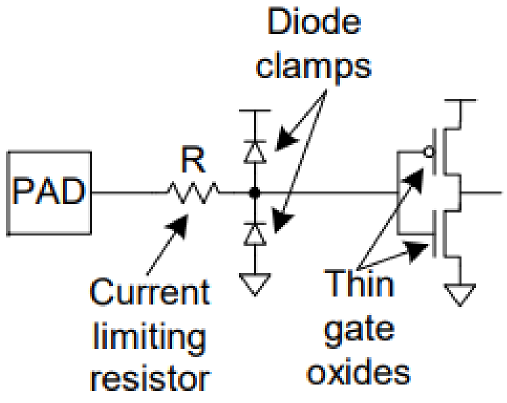


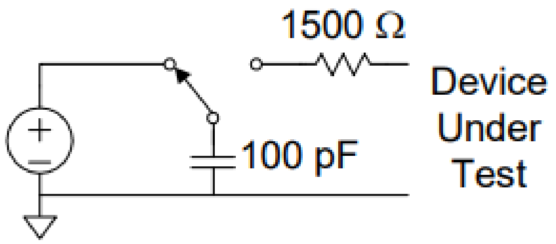
FIGURE 13.50 ESD test circuits

ESD Protection in I/O Pads

- Static electricity builds up on your body
  - Shock delivered to a chip can fry thin gates
  - Must dissipate this energy in protection circuits before it reaches the gates
- ESD protection circuits
  - Current limiting resistor
  - Diode clamps



- ESD testing
  - Human body model
  - Views human as charged capacitor



MOSIS I/O Pad Schematic

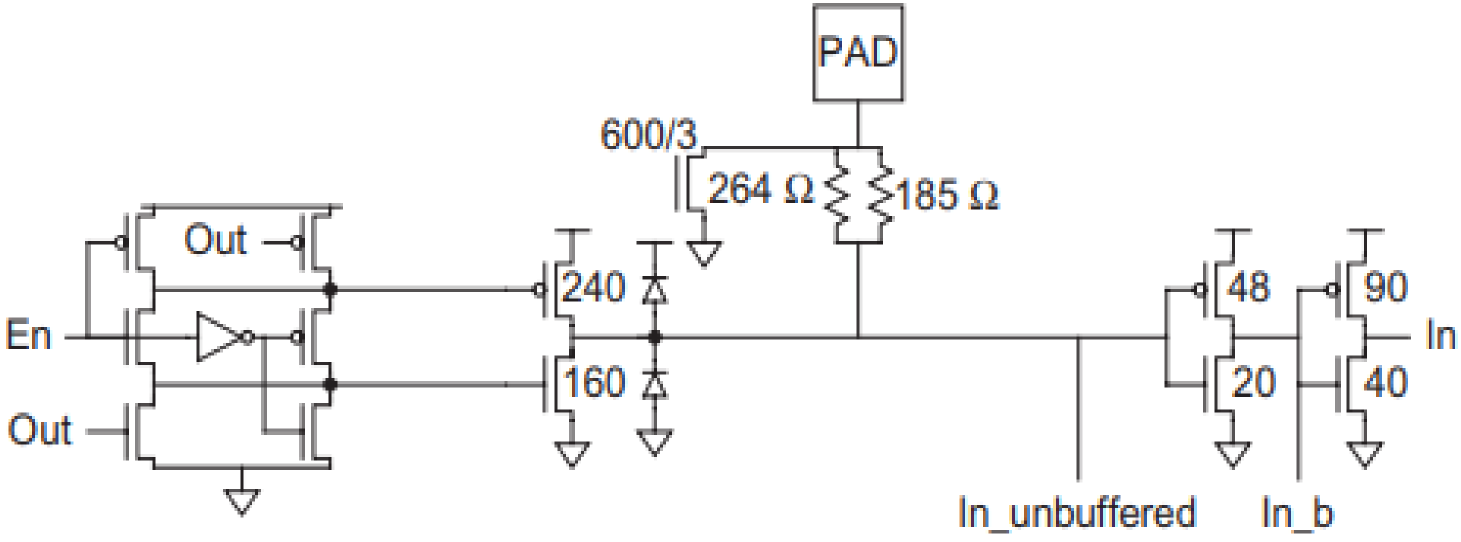


FIGURE 13.52 MOSIS bidirectional pad schematic

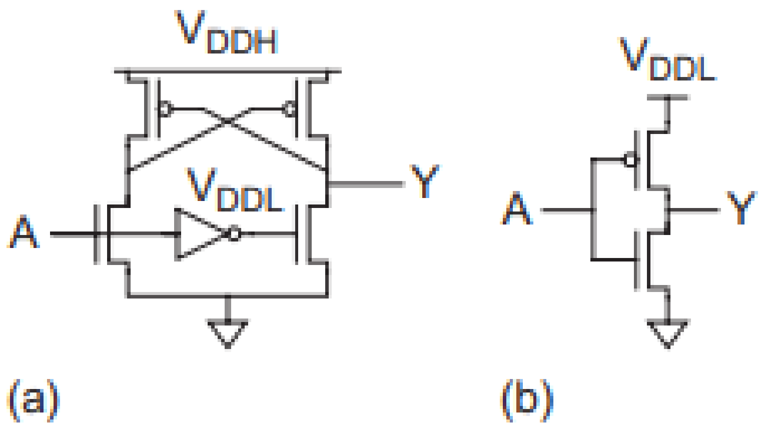
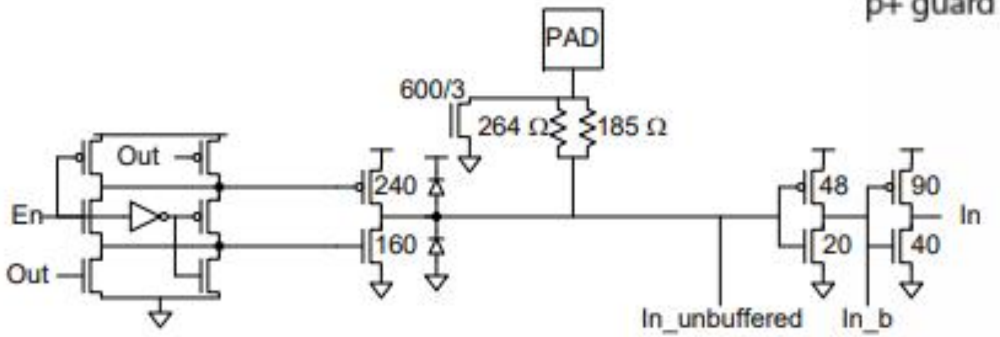
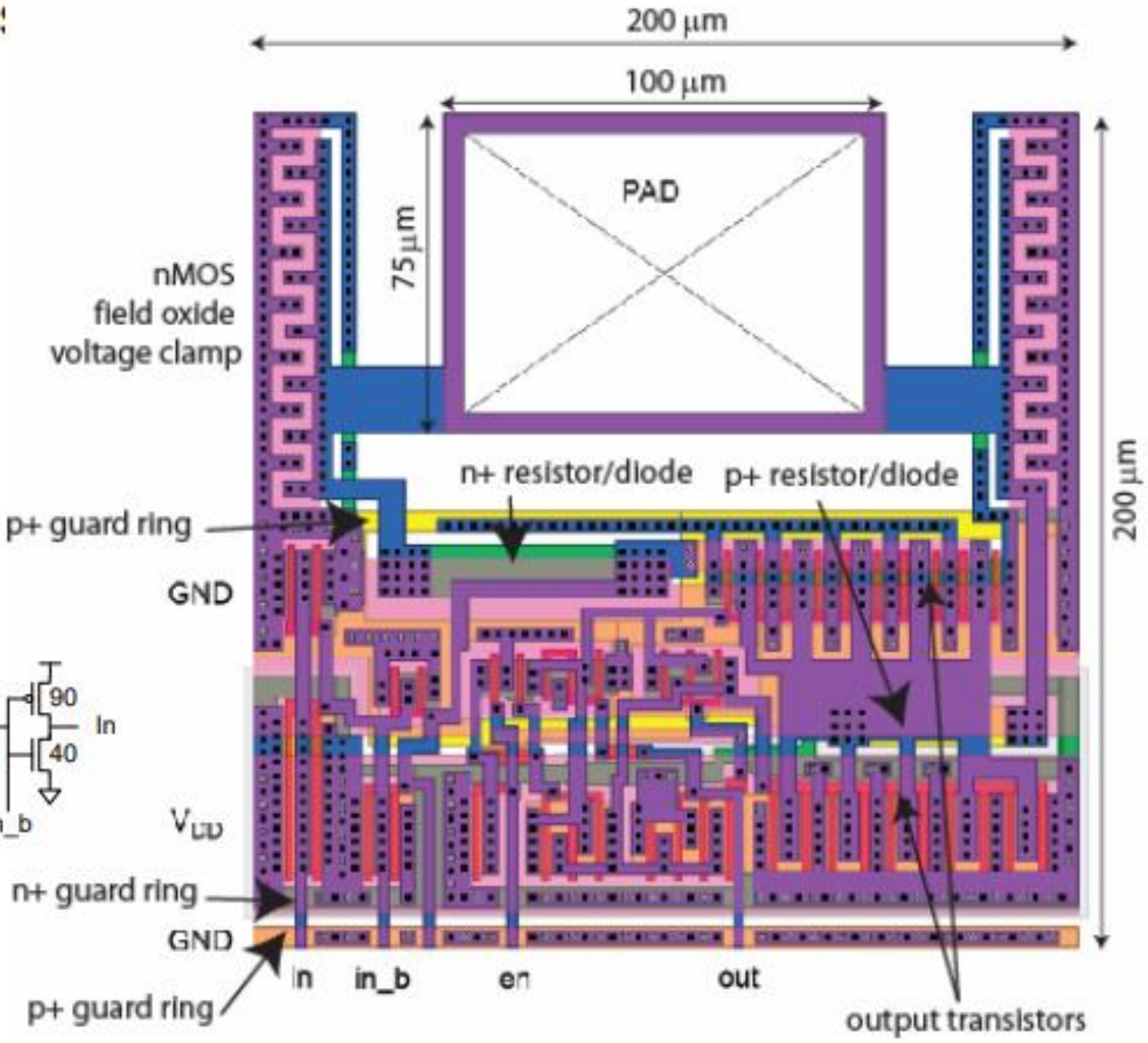


FIGURE 13.53 Level converters

Example of MOSIS I/O Pad Design

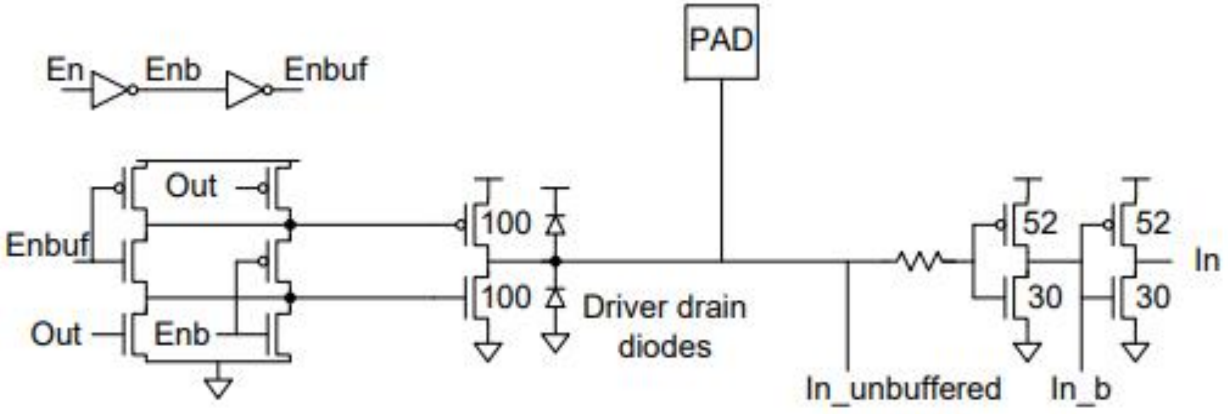
- 1.6 µm two-metal process
  - Protection resistors
  - Protection diodes
  - Guard rings
  - Field oxide clamps

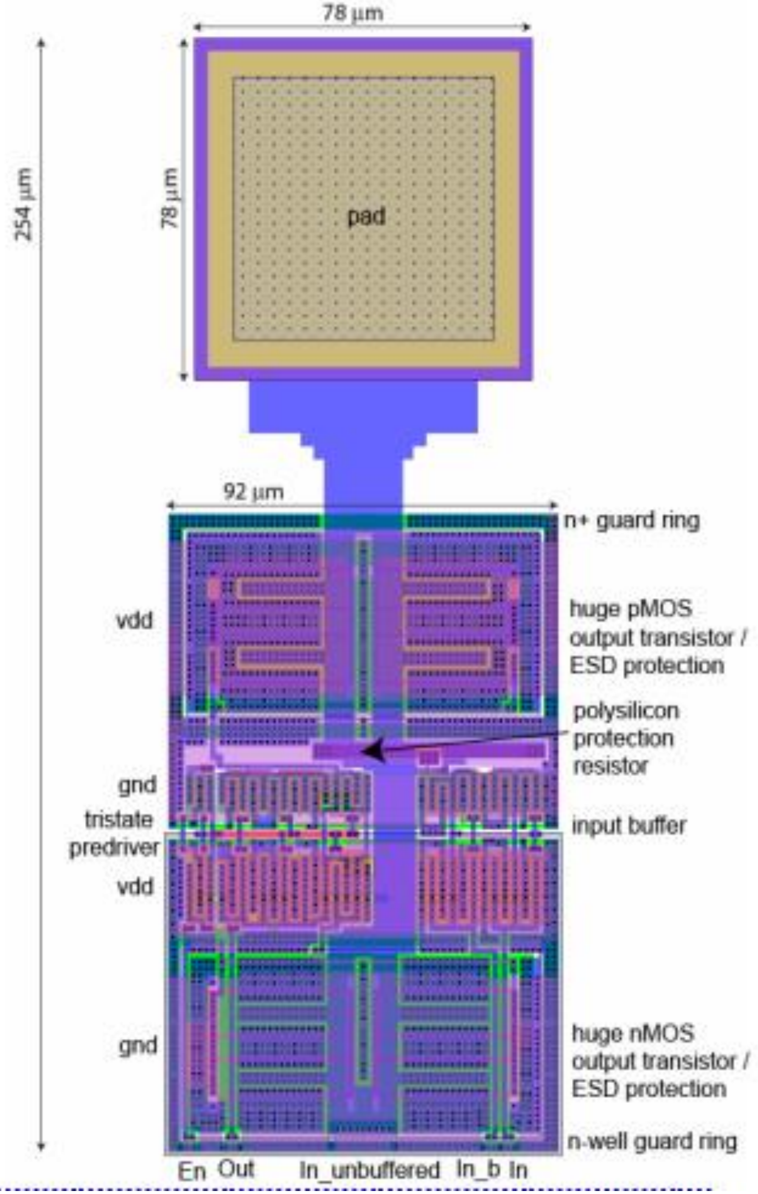




Another I/O Pad Design from Utah University

- 0.6 μm three-metal process
  - Similar I/O drivers
  - Big driver transistors provide ESD protection
  - Guard rings around driver





Readings

- Sequencing and Timing parameters are discussed in Section 10.2 of Course textbook
- I/O PADS in Chapter 13 of textbook
- Memory arrays are discussed in Chapter 12 of Course textbook