VLSI Design EE 523
Spring 2025

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Lecture 19

Topics for lecture 19

- Solve Examples from Last Lecture
- Interconnect Modelling and examples
- How to deal with Coupling effects?
- ----------
- Combinational Circuit Design Styles
  - Pseudo NMOS
  - Cascode / Differential Circuits

Quiz After Eid Break

Lab in Week 12

Reducing Crosstalk

There are several approaches to controlling this crosstalk:

- Increase spacing to adjacent lines
- Shield wires
- Ensure neighbors switch at different times
- Crosstalk cancellation

Concept of Repeaters

6.4.2 Repeaters

Both resistance and capacitance increase with wire length l, so the RC delay of a wire increases with l^2, as shown in Figure 6.26(a). The delay may be reduced by splitting the wire into N segments and inserting an inverter or buffer called a *repeater* to actively drive the wire [Glasser85], as shown in Figure 6.26(b). The new wire involves N segments with RC flight time of $(l/N)^2$, for a total delay of l^2/N. If the number of segments is proportional to the length, the overall delay increases only linearly with l.

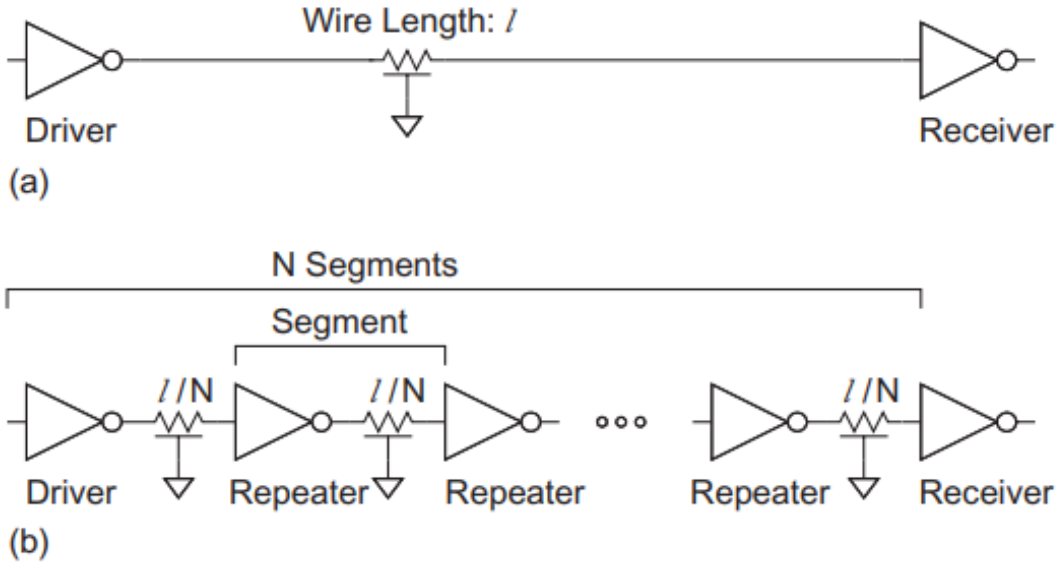


FIGURE 6.26 Wire with and without repeaters

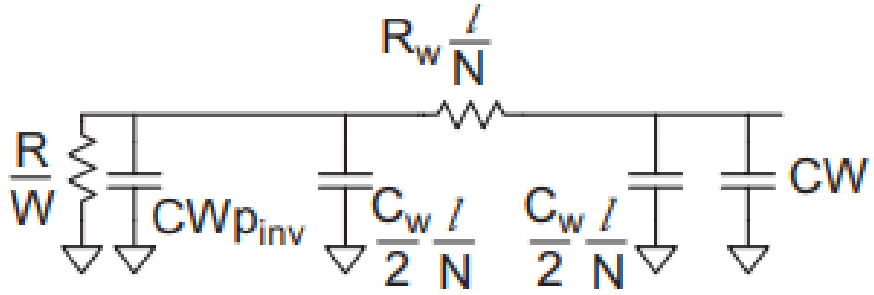


FIGURE 6.27 Equivalent circuit for segment of repeated wire

Crosstalk Control

6.4.3 Crosstalk Control

Recall from EQ (6.20) that the capacitive crosstalk is proportional to the ratio of coupling capacitance to total capacitance. For modern wires with an aspect ratio (t/w) of 2 or greater, the coupling capacitance can account for 2/3 to 3/4 of the total capacitance and crosstalk can create large amounts of noise and huge data-dependent delay variations. There are several approaches to controlling this crosstalk:

- Increase spacing to adjacent lines
- Shield wires
- Ensure neighbors switch at different times
- Crosstalk cancellation

The easiest approach to fix a minor crosstalk problem is to increase the spacing. If the crosstalk is severe, the spacing may have to be increased by more than one full track. In such a case, it is more efficient to shield critical signals with power or ground wires on one or both sides to eliminate coupling. For example, clock wires are usually shielded so that switching neighbors do not affect the delay of the clock wire and introduce clock jitter. Sensitive analog wires passing near digital signals should also be shielded.

Shielding Topologies

An alternative to shielding is to interleave busses that are guaranteed to switch at different times. For example, if bus *A* switches on the rising edge of the clock and bus *B* switches on the falling edge of the clock, by interleaving the bits of the two busses you can guarantee that both neighbors are constant during a switching event. This avoids the delay impact of coupling; however, you must still ensure that coupling noise does not exceed noise budgets. Figure 6.28 shows wires shielded (a) on one side, (b) on both sides, and (c) interleaved. Critical signals such as clocks or analog voltages can be shielded above and below as well.

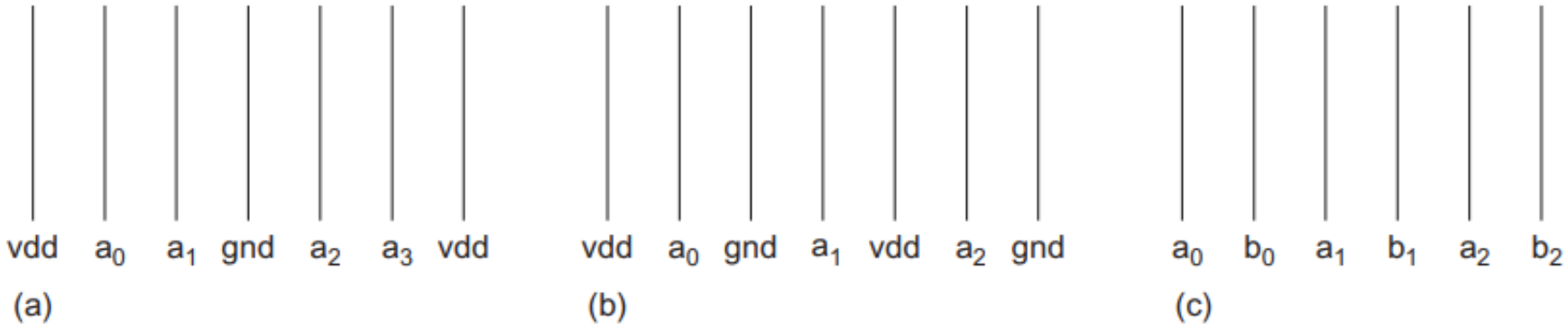


FIGURE 6.28 Wire shielding topologies

Repeaters Example

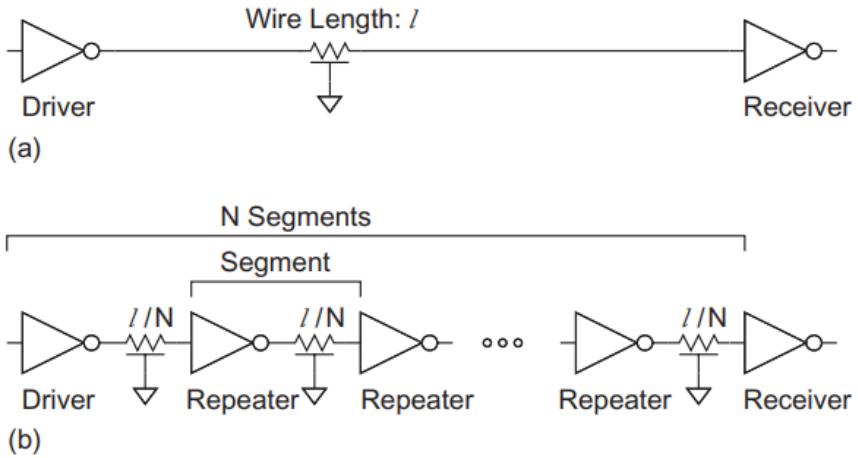


FIGURE 6.26 Wire with and without repeaters

The delay per unit length of a properly repeated wire is

$$\frac{t_{pd}}{l} = \left(2 + \sqrt{2\left(1 + p_{\text{inv}}\right)}\right)\sqrt{RCR_w C_w} \approx 1.67\sqrt{\text{FO4}\, R_w C_w}$$

To achieve this delay, the inverters should use an nMOS transistor width of

$$W = \sqrt{\frac{RC_w}{R_w C}} \qquad (6.30)$$

The energy per unit length to send a bit depends on the wire and repeater capacitances

$$\frac{E}{l} = C_w + NWC\left(1 + p_{\text{inv}}\right) = C_w\left(1 + \sqrt{\frac{1 + p_{\text{inv}}}{2}}\right)V_{DD}^2 \approx 1.87 C_w V_{DD}^2 \qquad (6.31)$$

Example 6.10

Compute the delay per mm of a repeated wire in a 65 nm process. Assume the wire is on a middle routing layer and has 2x width, spacing, and height, so its resistance is 200 Ω/mm and capacitance is 0.2 pF/mm. The FO4 inverter delay is 15 ps. Also find the repeater spacing and driver size to achieve this delay and the energy per bit.

SOLUTION: Using EQ (6.29), the delay is

$$t_{pd} = 1.67\sqrt{(15\text{ ps})(200\ \Omega/\text{mm})(0.2\text{ pF/mm})} = 41\text{ ps/mm} \qquad (6.32)$$

This delay is achieved using a spacing of 0.45 mm between repeaters and an nMOS driver width of 18 μm (180x unit size). The energy per bit is 0.4 pJ/mm.

RMS Current Estimation

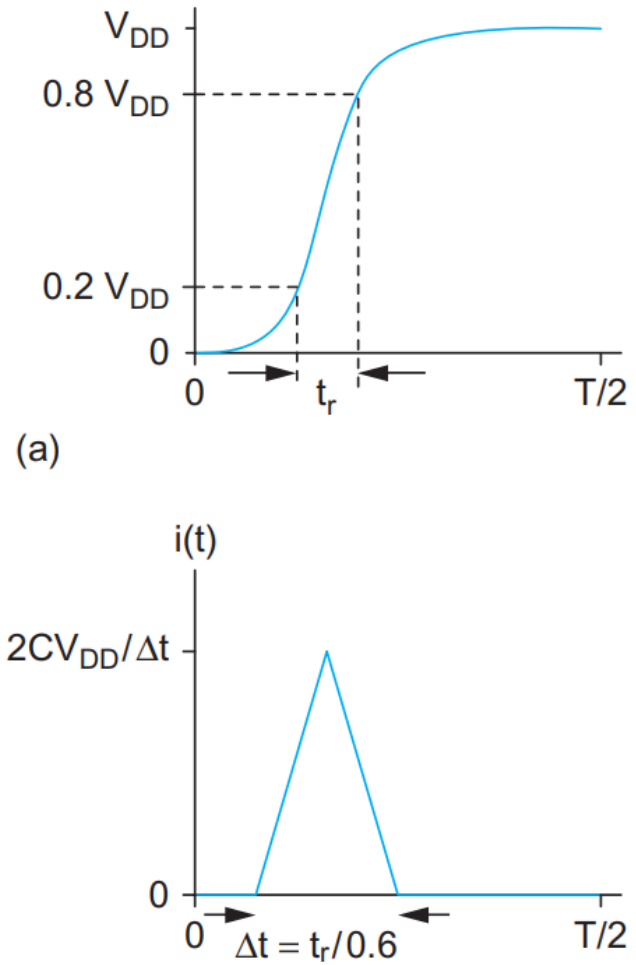


FIGURE 7.9 Switching waveforms for RMS current estimation

the RMS current. If a signal has symmetric rising and falling edges, we only need to consider half of a period. Figure 7.9(a) shows a signal with a 20–80% rise time t_r and an average period $T = 1/\alpha f$. The switching current $i(t)$ can be approximated as a triangular pulse of duration $\Delta t = t_r / (0.8–0.2)$, as shown in Figure 7.9(b). Then, the RMS current is

$$I_{rms} = \sqrt{\frac{1}{0.5T}\int_0^{0.5T} i^2(t)\,dt}$$

$$= \sqrt{\frac{2}{0.5T}\int_0^{\Delta t/2}\left(\frac{2CV_{DD}}{\Delta t}\frac{t}{\Delta t/2}\right)^2 dt} \qquad (7.5)$$

$$\approx 1.26CV_{DD}\sqrt{\frac{\alpha f}{t_r}}$$

void excessive self-heating, the wire and load capacitance should be less than

$$C = \frac{I_{rms-\max}}{1.26V_{DD}\sqrt{\frac{\alpha f}{t_r}}} \qquad (7.6)$$

Example of Self Heating Calculation

$$C = \frac{I_{rms-\max}}{1.26 V_{DD} \sqrt{\frac{\alpha f}{t_r}}}$$

Example 7.1

A clock signal is routed on the top metal layer using a wire that is 1 μm wide and has a self-heating limit of 10 mA. The wire has a capacitance of 0.4 fF/μm and the load capacitance is 85 fF. The clock switches at 3 GHz and has a 20 ps rise time. How far can the wire run between repeaters without overheating?

SOLUTION: A clock has an activity factor of 1. According to EQ (7.6), the maximum capacitance of the line is

$$C = \frac{10^{-2}\ \text{A}}{1.26(1\ \text{V})\sqrt{\frac{1 \cdot 3 \times 10^{9}\ \text{Hz}}{20 \times 10^{-12}\ \text{s}}}} = 685\ \text{fF} \qquad (7.7)$$

Thus, the maximum wire length is (685 − 85 fF) / (0.4 fF/μm) = 1500 μm.

Interconnect Modelling

6.2 Interconnect Modeling

A pipe makes a good mechanical analogy for a wire, as shown in Figure 6.4 [Ho07]. The resistance relates to the wire's cross-sectional area. A narrow pipe impedes the flow of current. The capacitance relates to a trough underneath the leaky pipe that must fill up before current passes out the end of the pipe. And the inductance relates to a paddle wheel along the wire with inertia that opposes changes in the rate of flow. Each of these elements is discussed further in this section.

A wire is a distributed circuit with a resistance and capacitance per unit length. Its behavior can be approximated with a number of lumped elements. Three standard approximations are the L-model, π-model, and T-model, so-named because of their shapes. Figure 6.5 shows how a distributed RC circuit is equivalent to N distributed RC segments of proportionally smaller resistance and capacitance, and how these segments can be modeled with lumped elements. As the number of segments approaches infinity, the lumped approximation will converge with the true distributed circuit. The L-model is a poor choice because a large number of segments are required for accurate results. The π-model is much better; three segments are sufficient to give results accurate to 3% [Sakurai83]. The

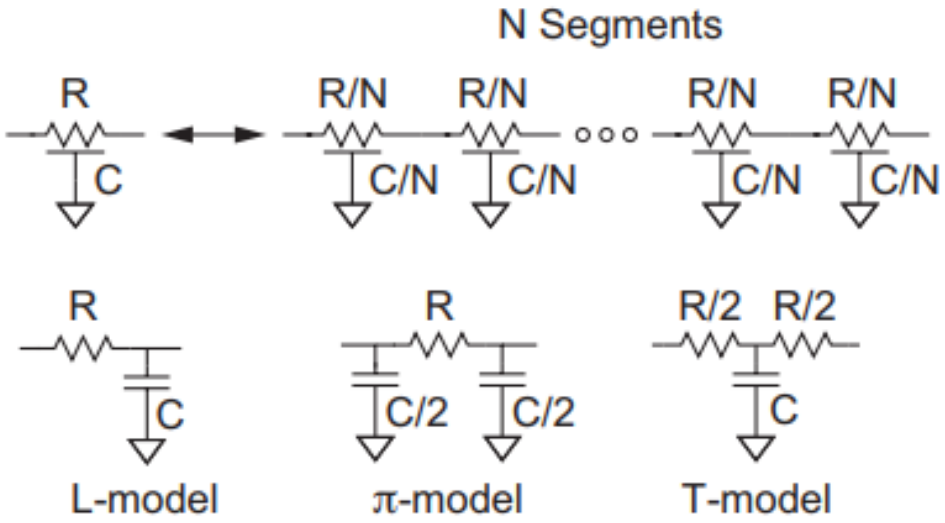


FIGURE 6.5 Lumped approximation to distributed RC circuit

Example of Pi Model

Example 6.3

A 10x unit-sized inverter drives a 2x inverter at the end of the 1 mm wire from Example 6.1. Suppose that wire capacitance is 0.2 fF/μm and that unit-sized nMOS transistor has $R = 10$ kΩ and $C = 0.1$ fF. Estimate the propagation delay using the Elmore delay model; neglect diffusion capacitance.

SOLUTION: The driver has a resistance of 1 kΩ.The receiver has a 2-unit nMOS transistor and a 4-unit pMOS transistor, for a capacitance of 0.6 fF. The wire capacitance is 200 fF.

Figure 6.14 shows an equivalent circuit for the system using a single-segment π-model. The Elmore delay is $t_{pd} = (1000\ \Omega)(100\text{ fF}) + (1000\ \Omega + 800\ \Omega)(100\text{ fF} + 0.6\text{ fF}) = 281$ ps. The capacitance of the long wire dominates the delay; the capacitance of the 2x inverter is negligible in comparison.

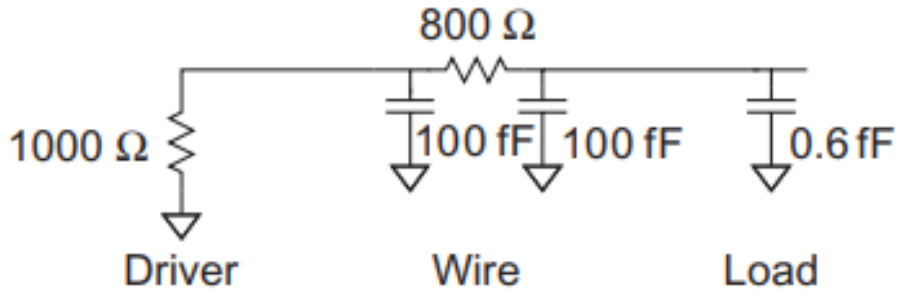


FIGURE 6.14 Equivalent circuit for example

Active Techniques for Crosstalk Control

Figure 6.29(a) shows two wires with staggered repeaters. Each segment of the victim sees half of a rising aggressor segment and half of a falling aggressor segment. Although the cancellation is not perfect because of delays along the segments, staggering is a very effective approach. Figure 6.29(b) shows charge compensation in which an inverter and transistor are added between the aggressor and victim. The transistor is connected to behave as a capacitor. When the aggressor rises and couples the victim upward, the inverter falls and couples the victim downward. By choosing an appropriately sized compensation transistor, most of the noise can be canceled at the expense of the extra circuitry. Figure 6.29(c) shows twisted differential signaling in which each signal is routed differentially. The signals are swapped or *twisted* such that the victim and its complement each see equal coupling from the aggressor and its complement. This approach is expensive in wiring resources, but it effectively eliminates crosstalk. It is widely used in memory designs that are naturally differential, as explored in Section 12.2.3.3.

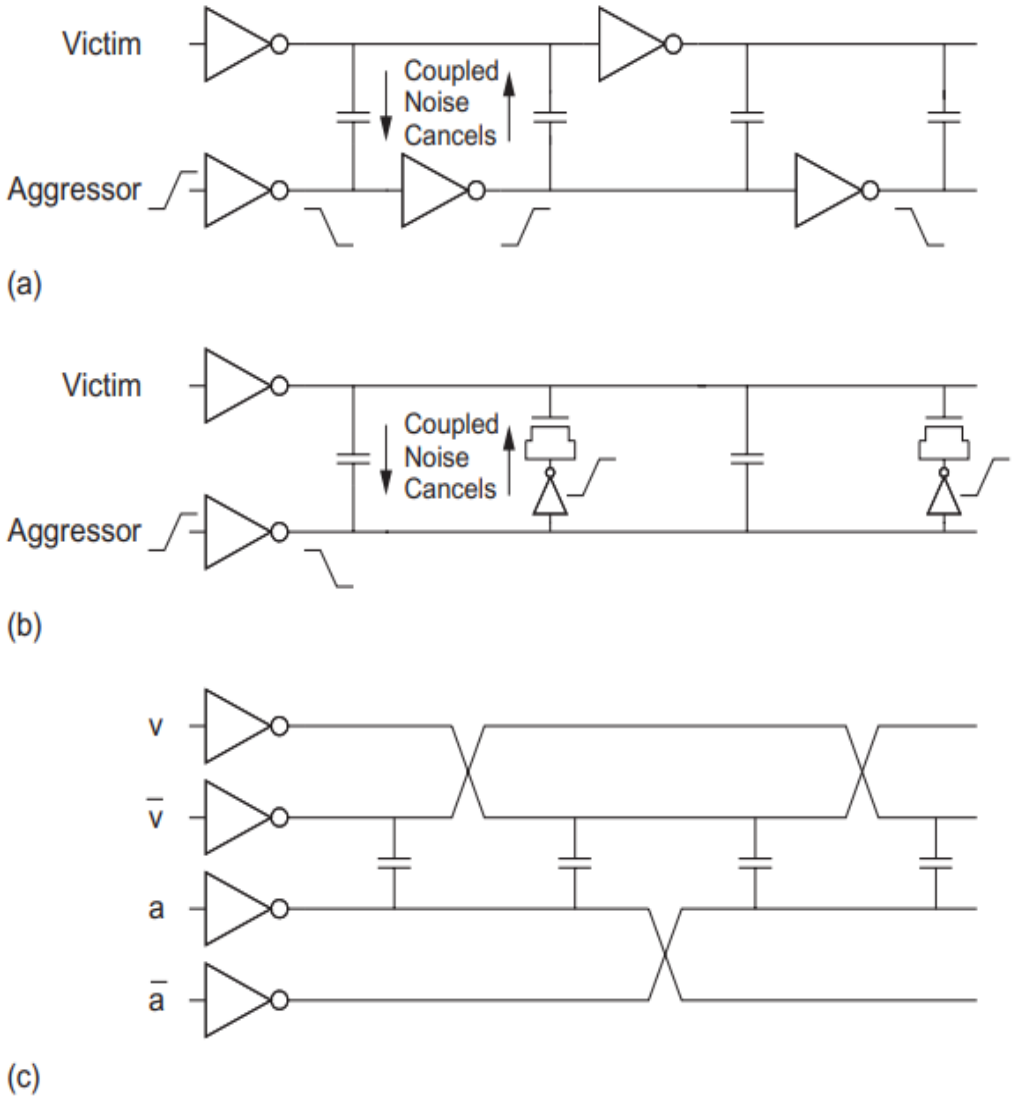


FIGURE 6.29 Crosstalk control schemes

Interconnect E.g.

Example 6.5

Figure 6.15 models a gate driving wires to two destinations. The gate is represented as a voltage source with effective resistance R_1. The two receivers are located at nodes 3 and 4. The wire to node 3 is long enough that it is represented with a pair of π-segments, while the wire to node 4 is represented with a single segment. Find the Elmore delay from input x to each receiver.

SOLUTION: The Elmore delays are

$$T_{D_3} = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3 + R_1C_4$$
$$T_{D_4} = R_1C_1 + R_1(C_2 + C_3) + (R_1 + R_4)C_4 \qquad (6.18)$$

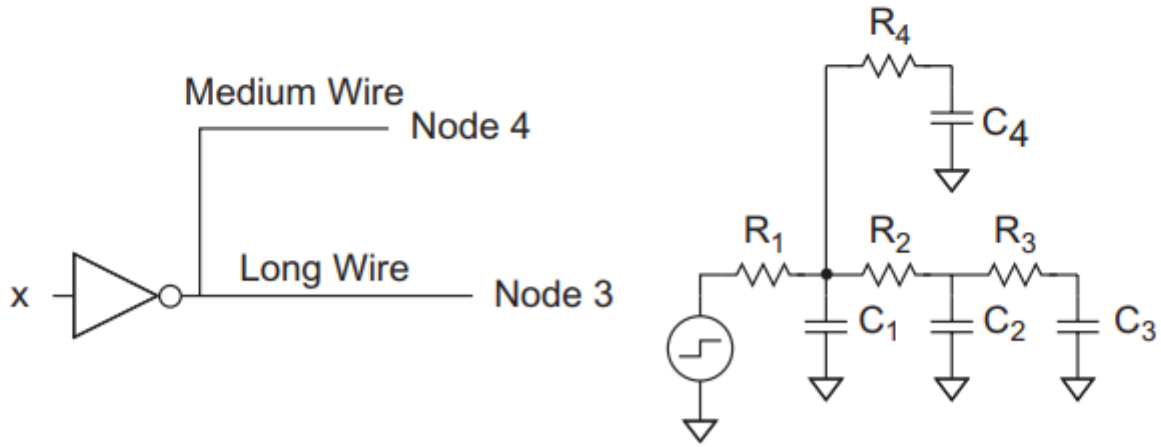


FIGURE 6.15 Interconnect modeling with RC tree

Interconnect Example 2

Example 6.8

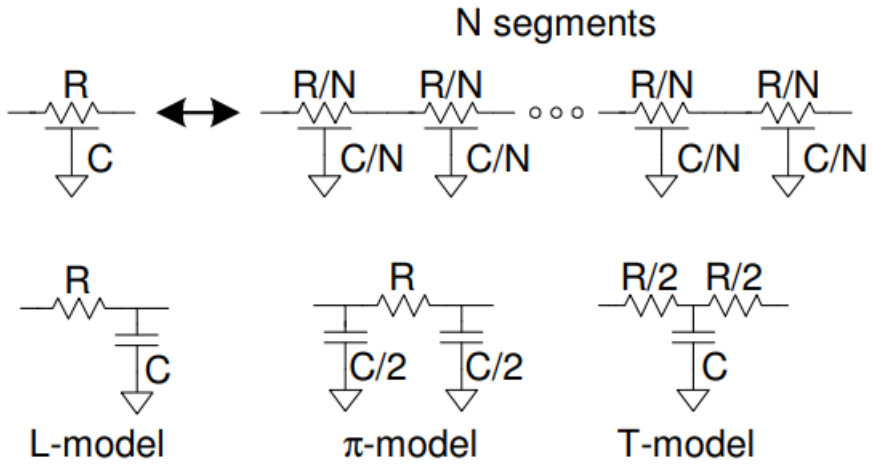
Each wire in a pair of 1 mm lines has capacitance of 0.08 fF/μm to ground and 0.12 fF/μm to its neighbor. Each line is driven by an inverter with a 1 kΩ effective resistance. Estimate the contamination and propagation delays of the path. Neglect parasitic capacitance of the inverter and resistance of the wires.

SOLUTION: We find $C_{gnd} = (0.08\ \text{fF}/\mu\text{m})(1000\ \mu\text{m}) = 80\ \text{fF}$ and $C_{adj} = 120\ \text{fF}$. The delay is RC_{eff}. The contamination delay is the minimum possible delay, which occurs when both wires switch in the same direction. In that case, $C_{eff} = C_{gnd}$ and the delay is $t_{cd} = (1\ \text{k}\Omega)(0.08\ \text{pF}) = 80\ \text{ps}$. The propagation delay is the maximum possible delay, which occurs when both wires switch in opposite directions. In this case, $C_{eff} = C_{gnd} + 2C_{adj}$ and the delay is $t_{pd} = (1\ \text{k}\Omega)(0.32\ \text{pF}) = 320\ \text{ps}$. This is a factor of four difference between best and worst case.

Examples of Pi Model

Lumped Element Models

- Wires are a distributed system
  - Approximate with lumped element models

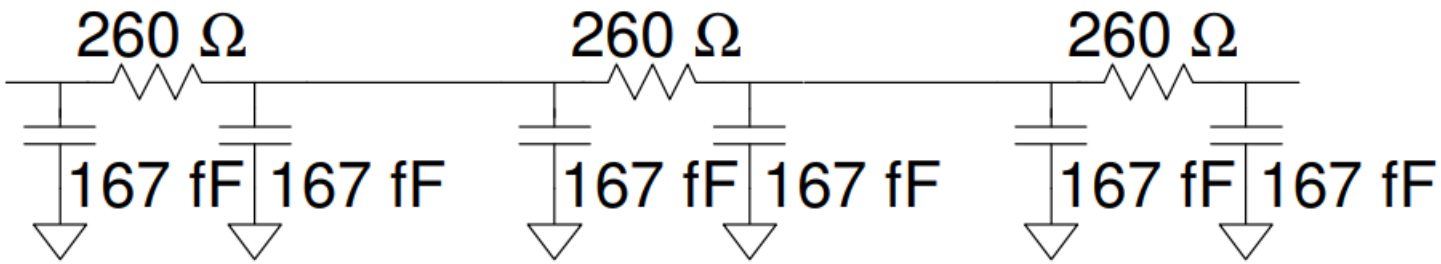


- 3-segment π-model is accurate to 3% in simulation
- L-model needs 100 segments for same accuracy!
- Use single segment π-model for Elmore delay

Example of making a Pi Model

Example

- Metal2 wire in 180 nm process
  - 5 mm long
  - 0.32 µm wide
  - Number of squares = 5000/0.32 = 15625
- Construct a 3-segment π-model
  - $R_{\square} = 0.05\ \Omega/\square$ => R = 15625 * 0.05 = 781 Ω
  - $C_{permicron} = 0.2$ fF/µm => C = 0.2 fF/µm * 5000 µm = 1 pF

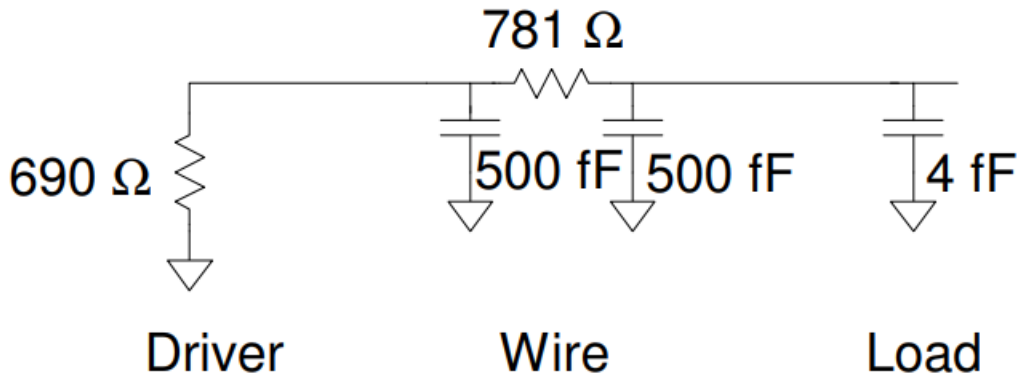


Example of Wire RC Delay

Wire RC Delay

Estimate the delay of a 10x inverter driving a 2x inverter at the end of the 5mm wire from the previous example.

- R = 2.5 kΩ*µm for gates
- Unit inverter: 0.36 µm nMOS, 0.72 µm pMOS
- Unit inverter has 4λ = 0.36µm wide nMOS, 8λ = 0.72µm wide pMOS
- Unit inverter: effective resistance of (2.5 kΩ*µm)/(0.36µm) = 6.9 kΩ
- Capacitance: (0.36µm + 0.72 µm) * (2fF/µm) = 2fF



- t_{pd} = 1.1 ns

Interconnect E.g.

Example 6.5

Figure 6.15 models a gate driving wires to two destinations. The gate is represented as a voltage source with effective resistance R_1. The two receivers are located at nodes 3 and 4. The wire to node 3 is long enough that it is represented with a pair of π-segments, while the wire to node 4 is represented with a single segment. Find the Elmore delay from input x to each receiver.

SOLUTION: The Elmore delays are

$$T_{D_3} = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3 + R_1C_4$$
$$T_{D_4} = R_1C_1 + R_1(C_2 + C_3) + (R_1 + R_4)C_4 \qquad (6.18)$$

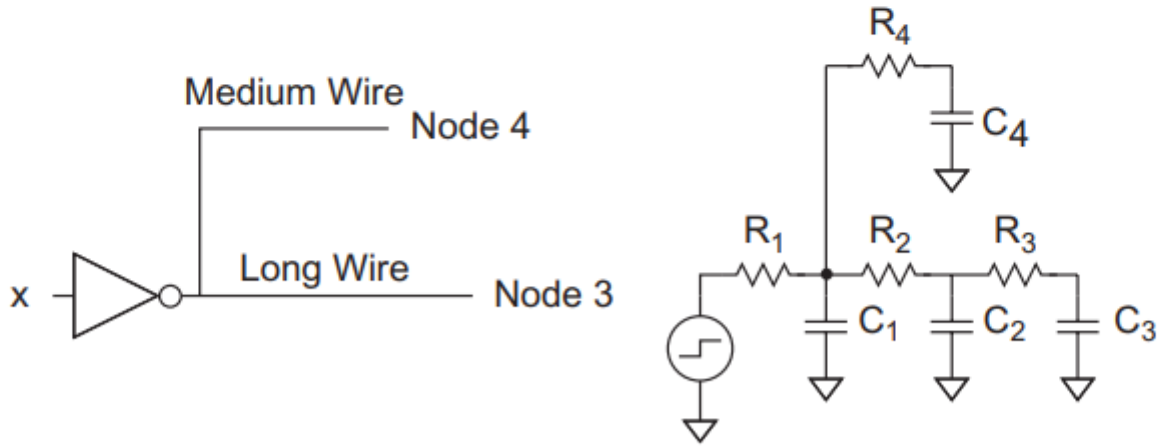


FIGURE 6.15 Interconnect modeling with RC tree

Interconnect Capacitance Coupling Example 2

Example 6.8

Each wire in a pair of 1 mm lines has capacitance of 0.08 fF/μm to ground and 0.12 fF/μm to its neighbor. Each line is driven by an inverter with a 1 kΩ effective resistance. Estimate the contamination and propagation delays of the path. Neglect parasitic capacitance of the inverter and resistance of the wires.

SOLUTION: We find $C_{gnd} = (0.08\ \text{fF}/\mu\text{m})(1000\ \mu\text{m}) = 80\ \text{fF}$ and $C_{adj} = 120\ \text{fF}$. The delay is RC_{eff}. The contamination delay is the minimum possible delay, which occurs when both wires switch in the same direction. In that case, $C_{eff} = C_{gnd}$ and the delay is $t_{cd} = (1\ \text{k}\Omega)(0.08\ \text{pF}) = 80\ \text{ps}$. The propagation delay is the maximum possible delay, which occurs when both wires switch in opposite directions. In this case, $C_{eff} = C_{gnd} + 2C_{adj}$ and the delay is $t_{pd} = (1\ \text{k}\Omega)(0.32\ \text{pF}) = 320\ \text{ps}$. This is a factor of four difference between best and worst case.

Combinational Gates Design

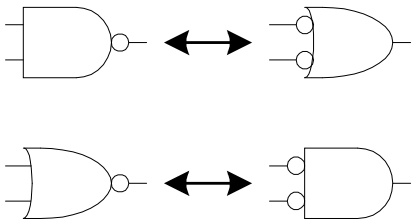
From Chapter 9 of textbook

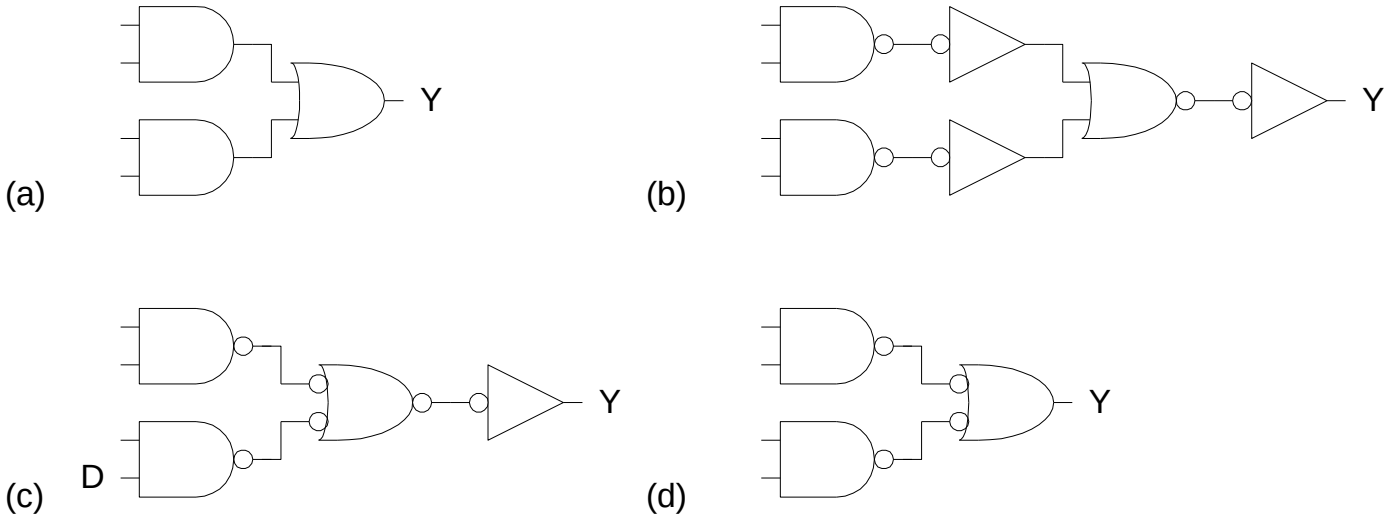
Bubble Pushing

- Start with network of AND / OR gates
- Convert to NAND / NOR + inverters
- Push bubbles around to simplify logic
  - Remember DeMorgan's Law

9.2.1.1 Bubble Pushing CMOS stages are inherently inverting, so AND and OR functions must be built from NAND and NOR gates. DeMorgan's law helps with this conversion:

$$\overline{A \cdot B} = \bar{A} + \bar{B}$$
$$\overline{A + B} = \bar{A} \cdot \bar{B} \qquad (9.2)$$





Example – Bubble Pushing Simplification

Example 9.1

Design a circuit to compute $F = AB + CD$ using NANDs and NORs.

SOLUTION: By inspection, the circuit consists of two ANDs and an OR, shown in Figure 9.2(a). In Figure 9.2(b), the ANDs and ORs are converted to basic CMOS stages. In Figure 9.2(c and d), bubble pushing is used to simplify the logic to three NANDs.

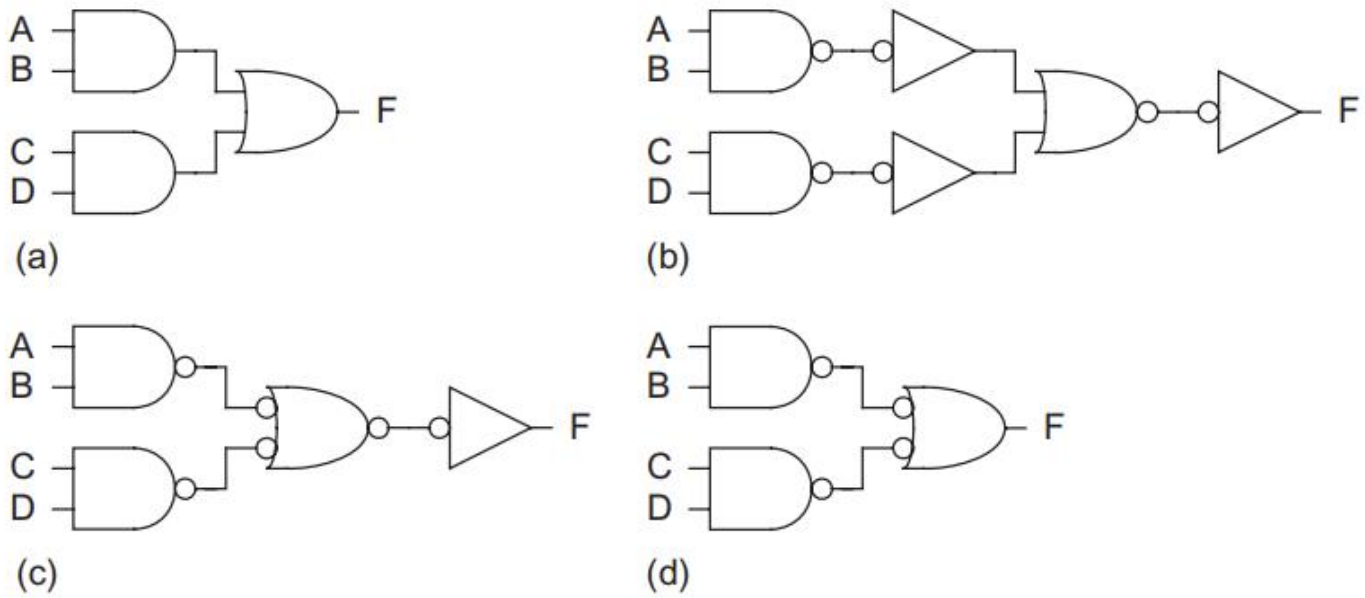


FIGURE 9.2 Bubble pushing to convert ANDs and ORs to NANDs and NORs

AOI Compound Gates

9.2.1.2 Compound Gates As described in Section 1.4.5, static CMOS also efficiently handles compound gates computing various inverting combinations of AND/OR functions in a single stage. The function $F = AB + CD$ can be computed with an AND-OR-INVERT-22 (AOI22) gate and an inverter, as shown in Figure 9.3.

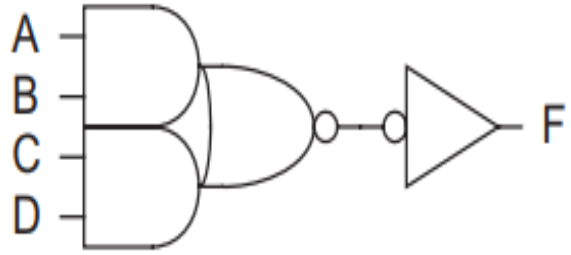


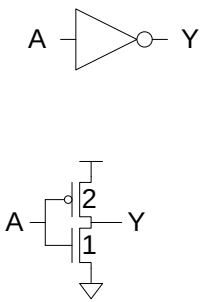
FIGURE 9.3 Logic using AOI22 gate

Compound Gates, LE and Parasitic

- Logical Effort of compound gates

unit inverter

$Y = \overline{A}$

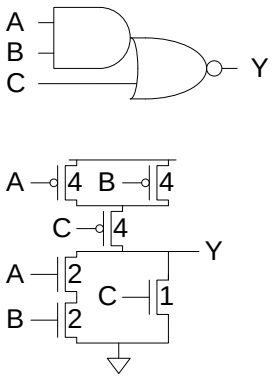


$g_A = 3/3$

$p = 3/3$

AOI21

$Y = \overline{A \cdot B + C}$



$g_A = 6/3$

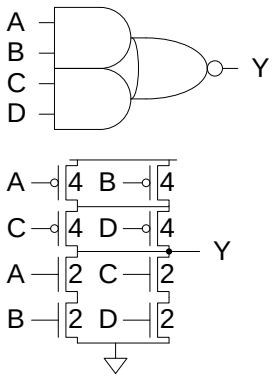
$g_B = 6/3$

$g_C = 5/3$

$p = 7/3$

AOI22

$Y = \overline{A \cdot B + C \cdot D}$



$g_A =$

$g_B =$

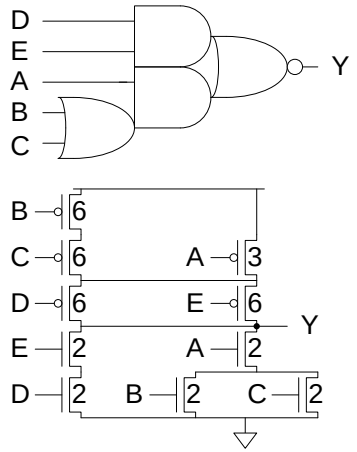
$g_C =$

$g_D =$

$p =$

Complex AOI

$Y = \overline{A \cdot (B + C) + D \cdot E}$



$g_A =$

$g_B =$

$g_C =$

$g_D =$

$g_E =$

$p =$

Logical Effort and Parasitic Delay of AOI

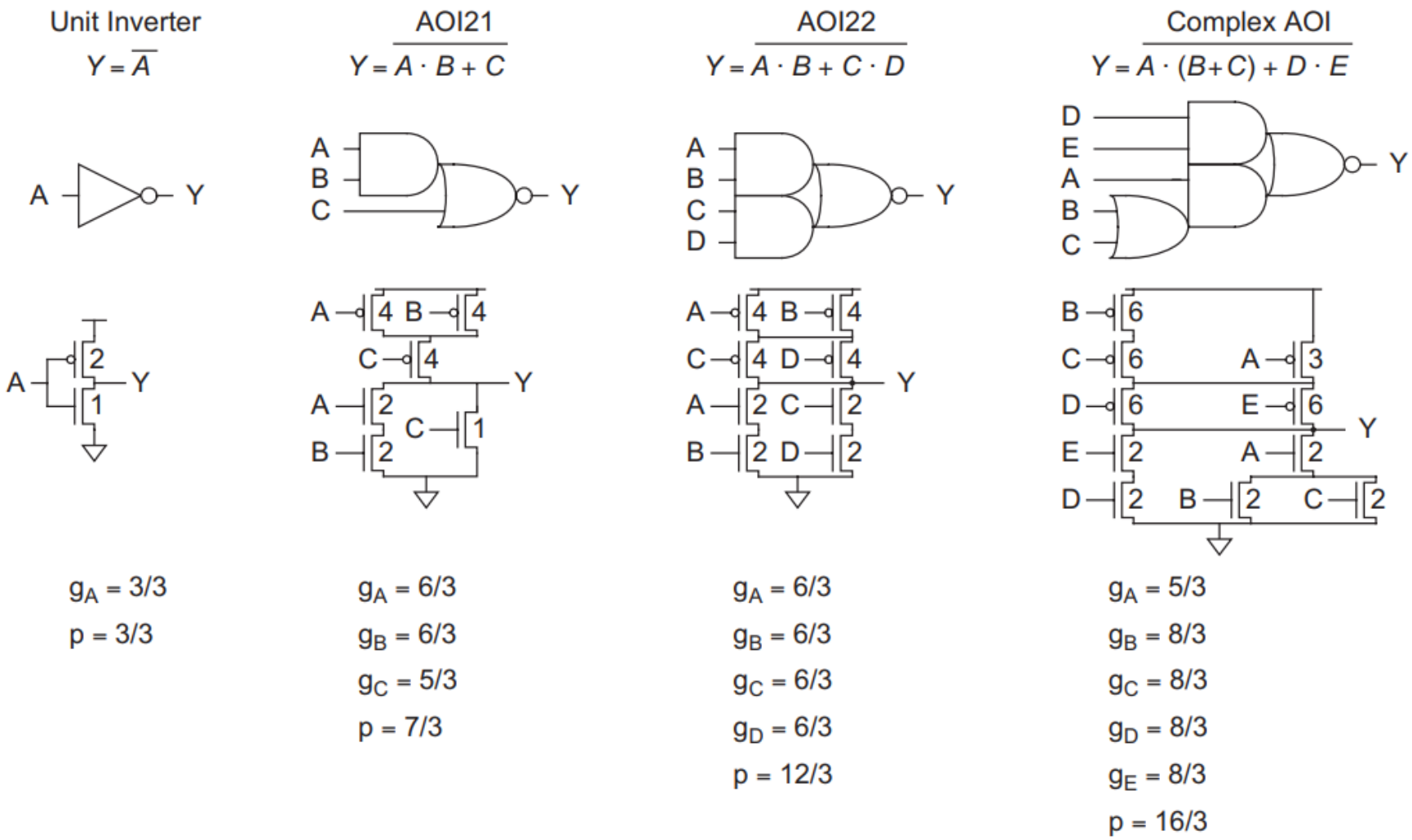
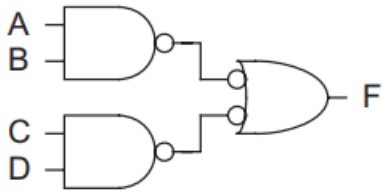


FIGURE 9.4 Logical efforts and parasitic delays of AOI gates

Example AOI Delay



(d)

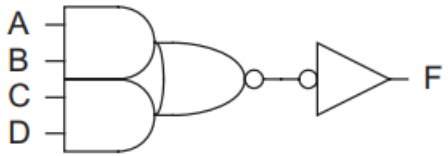
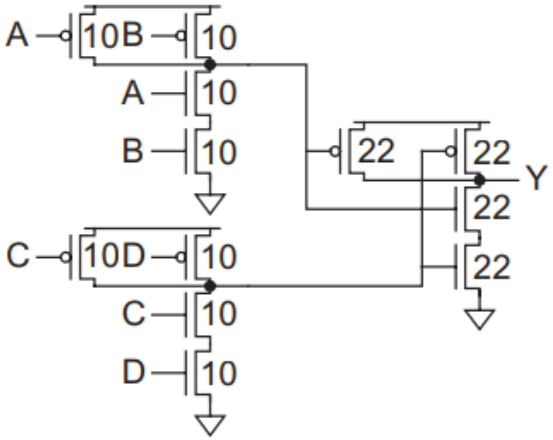


FIGURE 9.3 Logic using AOI22 gate



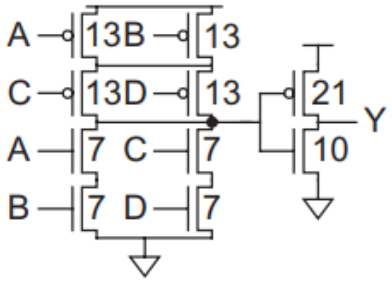


FIGURE 9.5 Paths with transistor widths

Example 9.2

Calculate the minimum delay, in τ, to compute $F = AB + CD$ using the circuits from Figure 9.2(d) and Figure 9.3. Each input can present a maximum of 20 λ of transistor width. The output must drive a load equivalent to 100 λ of transistor width. Choose transistor sizes to achieve this delay.

SOLUTION: The path electrical effort is $H = 100/20 = 5$ and the branching effort is $B = 1$. The design using NAND gates has a path logical effort of $G = (4/3) \times (4/3) = 16/9$ and parasitic delay of $P = 2 + 2 = 4$. The design using the AOI22 and inverter has a path logical effort of $G = (6/3) \times 1 = 2$ and a parasitic delay of $P = 12/3 + 1 = 5$. Both designs have $N = 2$ stages. The path efforts $F = GBH$ are 80/9 and 10, respectively. The path delays are $NF^{1/N} + P$, or 10.0 τ and 11.3 τ, respectively. Using compound gates does not always result in faster circuits; simple 2-input NAND gates can be quite fast.

To compute the sizes, we determine the best stage efforts, $\hat{f} = F^{1/N} = 3.0$ and 3.2, respectively. These are in the range of 2.4–6 so we know the efforts are reasonable and the design would not improve too much by adding or removing stages. The input capacitance of the second gate is determined by the capacitance transformation

$$C_{in_i} = \frac{C_{out_i} \times g_i}{\hat{f}}$$

For the NAND design,

$$C_{in} = \frac{100\,\lambda \times (4/3)}{3.0} = 44\,\lambda$$

For the AOI22 design,

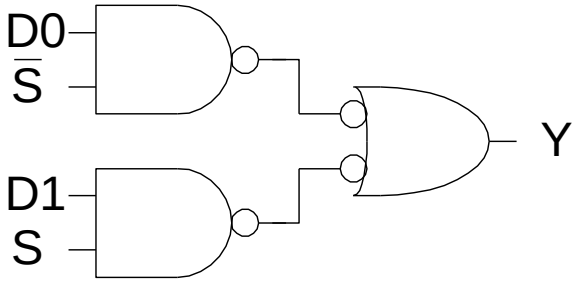
$$C_{in} = \frac{100\,\lambda \times (1)}{3.2} = 31\,\lambda$$

The paths are shown in Figure 9.5 with transistor widths rounded to integer values.

Example of AOI Compound Gate

- The multiplexer has a maximum input capacitance of 16 units on each input. It must drive a load of 160 units. Estimate the delay of the two designs.

H =



$P =$

$G =$

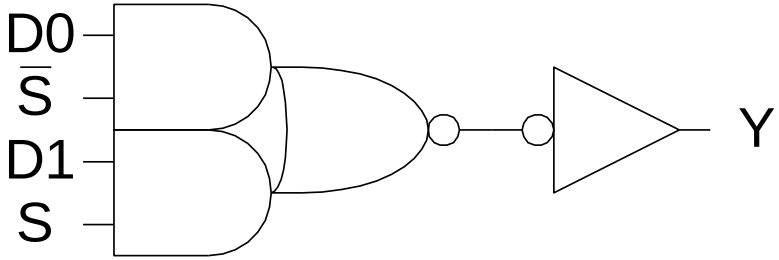
$F =$

$\hat{f} =$

$D =$

B =

N =



$P =$

$G =$

$F =$

$\hat{f} =$

$D =$

Readings

- Reliability is a section in Chapter 7 of textbook ‘CMOS VLSI Design’ by Weste and Harris
- Interconnects are in Chapter 6 of textbook ‘CMOS VLSI Design’ by Weste and Harris
- Combinational Logic Gates Design is in Chapter 9 of Course Text book