VLSI Design EE 523 Spring 2025

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Lecture 15

Topics for lecture 15

- Static Power Dissipation in CMOS Circuits
- Dynamic Power Dissipation in CMOS Circuits
- Power Gating and Clock Gating
- Reducing Leakage Current through bulk voltage Vsb
- **QUIZ 3 Was Held**

Basic Definitions of Power Dissipation

The *instantaneous power* $P(t)$ consumed or supplied by a circuit element is the product of the current through the element and the voltage across the element

$$P(t) = I(t)V(t) \tag{5.1}$$

The *energy* consumed or supplied over some time interval T is the integral of the instantaneous power

$$E = \int_0^T P(t)dt \tag{5.2}$$

The *average power* over this interval is

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T P(t)dt \tag{5.3}$$

Power is expressed in units of Watts (W). Energy in circuits is usually expressed in Joules (J), where 1 W = 1 J/s. Energy in batteries is often given in W-hr, where 1 W-hr = (1 J/s)(3600 s/hr)(1 hr) = 3600 J.

Energy Dissipated in Components

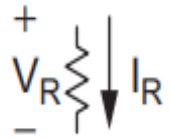

FIGURE 5.1
Resistor

Figure 5.1 shows a resistor. The voltage and current are related by Ohm's Law, $V = IR$, so the instantaneous power dissipated in the resistor is

$$P_R(t) = \frac{V_R^2(t)}{R} = I_R^2(t)R \tag{5.4}$$

This power is converted from electricity to heat.

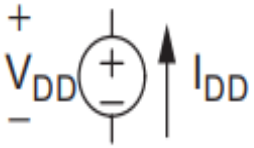

FIGURE 5.2
Voltage source

Figure 5.2 shows a voltage source V_{DD}. It supplies power proportional to its current

$$P_{VDD}(t) = I_{DD}(t)V_{DD} \tag{5.5}$$

Figure 5.3 shows a capacitor. When the capacitor is charged from 0 to V_C, it stores energy E_C

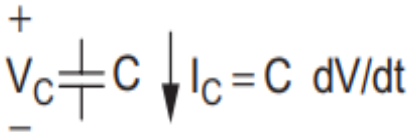

FIGURE 5.3
Capacitor

$$E_C = \int_0^\infty I(t)V(t)dt = \int_0^\infty C\frac{dV}{dt}V(t)dt = C\int_0^{V_C} V(t)dV = \tfrac{1}{2}CV_C^2 \tag{5.6}$$

The capacitor releases this energy when it discharges back to 0.

Energy in Inverter

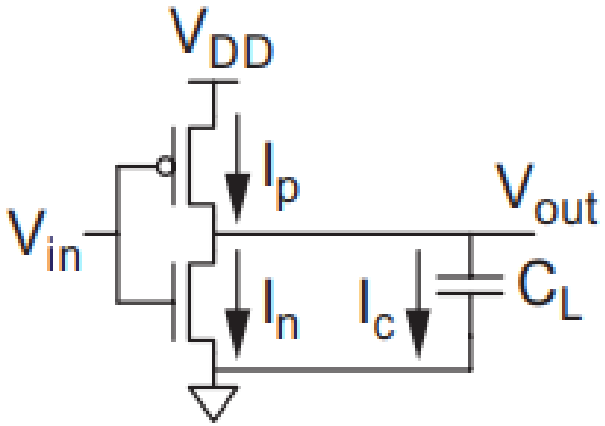

FIGURE 5.4
CMOS inverter

Figure 5.4 shows a CMOS inverter driving a load capacitance. When the input switches from 1 to 0, the pMOS transistor turns ON and charges the load to V_{DD}. According to EQ(5.6), the energy stored in the capacitor is

$$E_C = \frac{1}{2} C_L V_{DD}^2 \tag{5.7}$$

The energy delivered from the power supply is

$$E_C = \int_0^\infty I(t) V_{DD} dt = \int_0^\infty C \frac{dV}{dt} V_{DD} dt = C V_{DD} \int_0^{V_{DD}} dV = C V_{DD}^2 \tag{5.8}$$

Where does the energy go?

Observe that only half of the energy from the power supply is stored in the capacitor. The other half is dissipated (converted to heat) in the pMOS transistor because the transistor has a voltage across it at the same time a current flows through it. The power dissipated depends only on the load capacitance, not on the size of the transistor or the speed at which the gate switches. Figure 5.5 shows the energy and power of the supply and capacitor as the gate switches.

When the input switches from 0 back to 1, the pMOS transistor turns OFF and the nMOS transistor turns ON, discharging the capacitor. The energy stored in the capacitor is dissipated in the nMOS transistor. No energy is drawn from the power supply during this transition. The same analysis applies for any static CMOS gate driving a capacitive load.

Dynamic Power Dissipation

one would expect charging a capacitor through a linear resistor. When V_{in} rises, the pMOS starts to turn OFF. However, there is a small blip of current while the partially ON pMOS fights against the nMOS. This is called *short-circuit current*. The inverter draws power from V_{DD} as V_{out} rises. Half of the power is dissipated in the pMOS transistor and the other half is delivered to the capacitor. V_{DD} supplies a total of 150 fJ of energy, of which half is stored on the capacitor. The inverter is sized for equal rise/fall times so the falling transition is symmetric. The energy on the capacitor is dumped to GND. The short-circuit current consumes an almost imperceptibly small 2.7 fJ of additional energy from V_{DD} during this transition.

Suppose that the gate switches at some average frequency f_{sw}. Over some interval T, the load will be charged and discharged Tf_{sw} times. Then, according to EQ (5.3), the average power dissipation is

$$P_{switching} = \frac{E}{T} = \frac{Tf_{sw}CV_{DD}^2}{T} = CV_{DD}^2 f_{sw} \quad \textbf{(5.9)}$$

This is called the *dynamic power* because it arises from the switching of the load. Because most gates do not switch every clock cycle, it is often more convenient to express switching frequency f_{sw} as an *activity factor* α times the clock frequency f. Now, the dynamic power dissipation may be rewritten as

$$P_{switching} = \alpha CV_{DD}^2 f \quad \textbf{(5.10)}$$

The activity factor is the probability that the circuit node transitions from 0 to 1, because that is the only time the circuit consumes power. A clock has an activity factor of $\alpha = 1$ because it rises and falls every cycle. Most data has a maximum activity factor of 0.5 because it transitions only once each cycle. Truly random data has an activity factor of 0.25 because it transitions every other cycle. Static CMOS logic has been empirically deter-

5.1.3 Sources of Power Dissipation

Power dissipation in CMOS circuits comes from two components:

- Dynamic dissipation due to
  - charging and discharging load capacitances as gates switch
  - "short-circuit" current while both pMOS and nMOS stacks are partially ON
- Static dissipation due to
  - subthreshold leakage through OFF transistors
  - gate leakage through gate dielectric
  - junction leakage from source/drain diffusions
  - contention current in ratioed circuits (see Section 9.2.2)

Putting this together gives the total power of a circuit

$$P_{\text{dynamic}} = P_{\text{switching}} + P_{\text{short circuit}} \tag{5.11}$$

$$P_{\text{static}} = \left(I_{\text{sub}} + I_{\text{gate}} + I_{\text{junct}} + I_{\text{contention}}\right)V_{DD} \tag{5.12}$$

$$P_{\text{total}} = P_{\text{dynamic}} + P_{\text{static}} \tag{5.13}$$

Active, Standby and Sleep Modes of Power

Power can also be considered in active, standby, and sleep modes. *Active power* is the power consumed while the chip is doing useful work. It is usually dominated by $P_{switching}$. *Standby power* is the power consumed while the chip is idle. If clocks are stopped and ratioed circuits are disabled, the standby power is set by leakage. In sleep mode, the supplies to unneeded circuits are turned off to eliminate leakage. This drastically reduces the *sleep power* required, but the chip requires time and energy to wake up so sleeping is only viable if the chip will idle for long enough.

[Gonzalez96] found that roughly one-third of microprocessor power is spent on the clock, another third on memories, and the remaining third on logic and wires. In nanometer technologies, nearly one-third of the power is leakage. High-speed I/O contributes a growing component too. For example, Figure 5.6 shows the active power consumption of Sun's 8-core 84 W Niagra2 processor [Nawathe08]. The cores and other components collectively account for clock, logic, and wires.

The next sections investigate how to estimate and minimize each of these components of power. Many tools are available to assist with power estimation; these are discussed further in Sections 8.5.4 and 14.4.1.6.

Readings

- **Chapter 5** of textbook ‘CMOS VLSI Design’ by Weste and Harris