CS250
VLSI Systems Design

Fall 2020

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with

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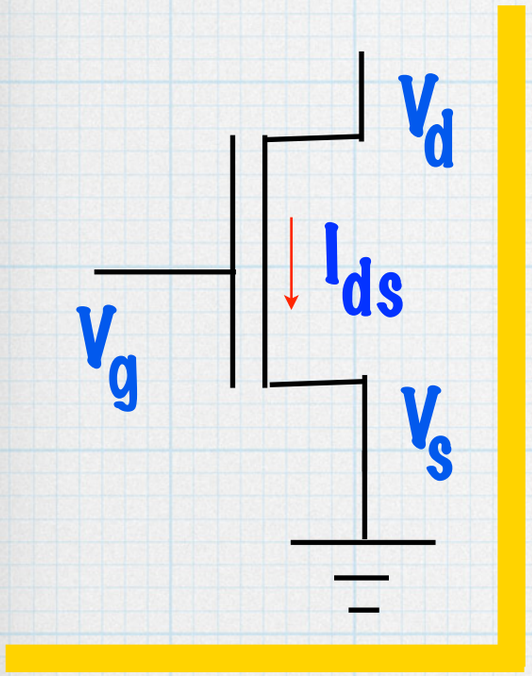
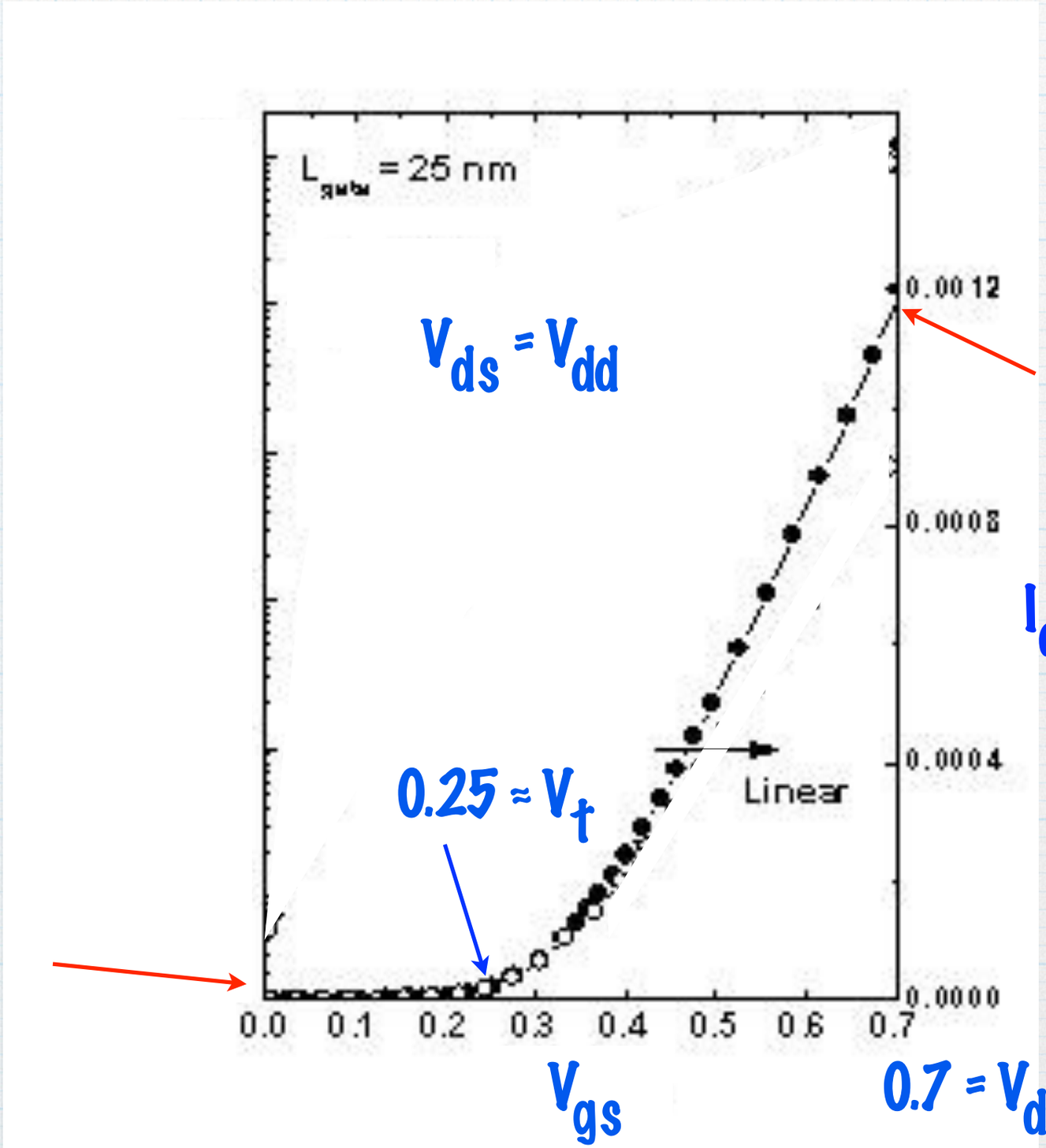
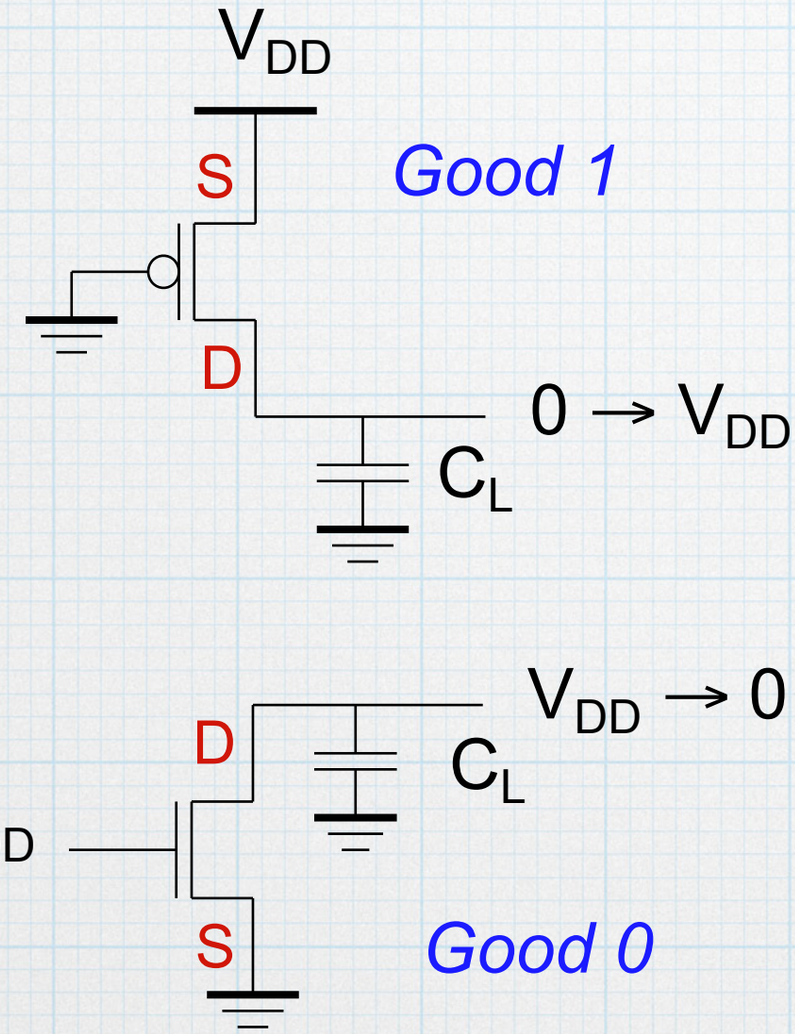
MOSFET Threshold Voltage

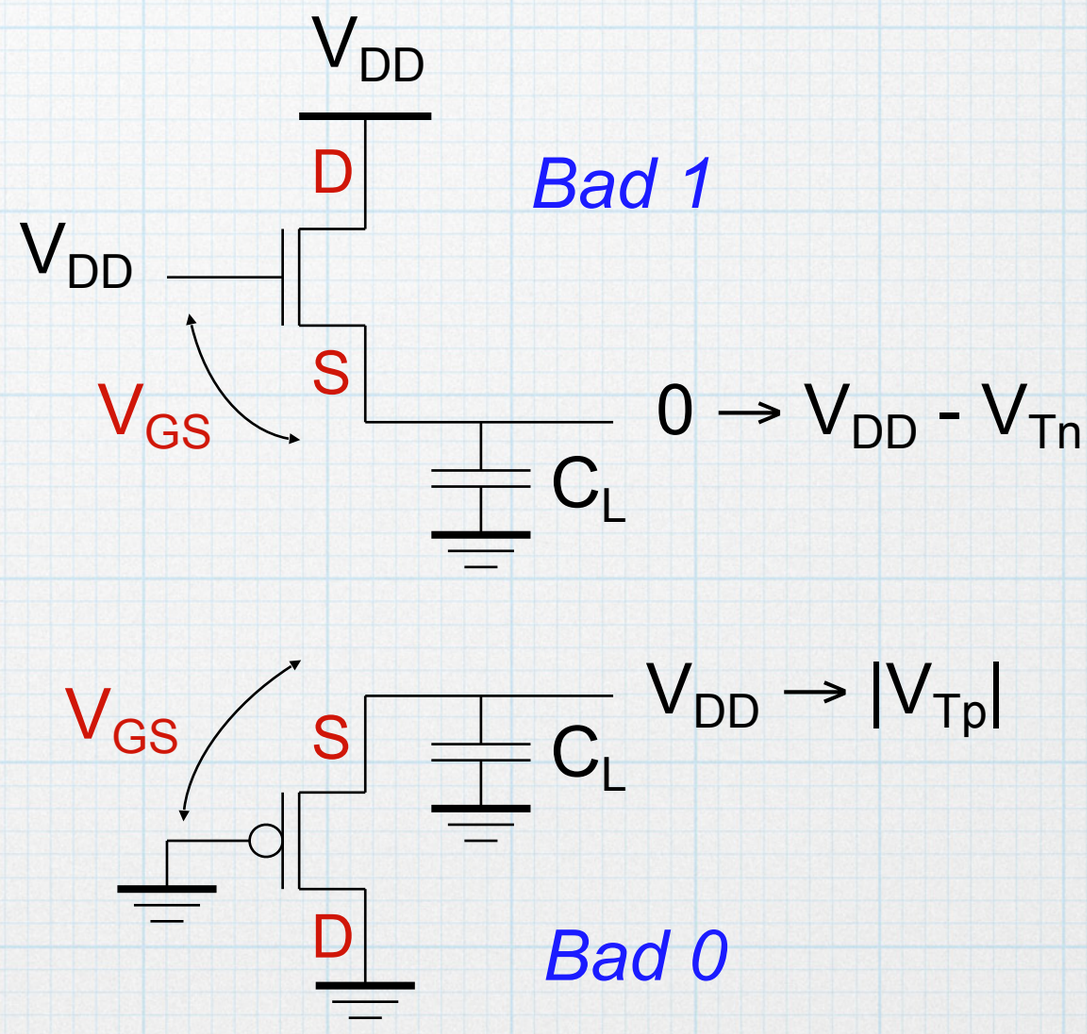


Transistor "turns on" when V_{gs} is > V_t.



CMOS Transistor Limitations

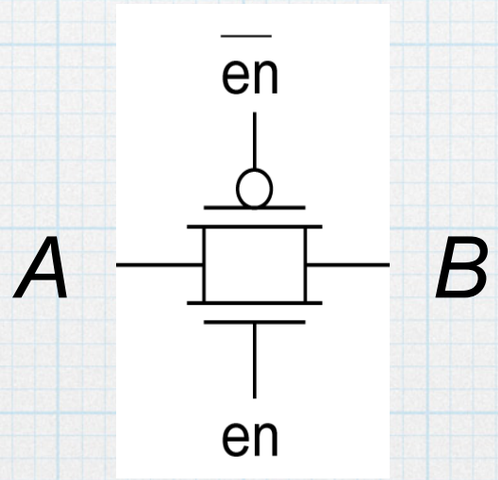




Tough luck …

Transmission Gate

- Transmission gates are the way to build ideal “switches” in CMOS.
- In general, both transistor types are needed:
  - nFET to pass zeros.
  - pFET to pass ones.

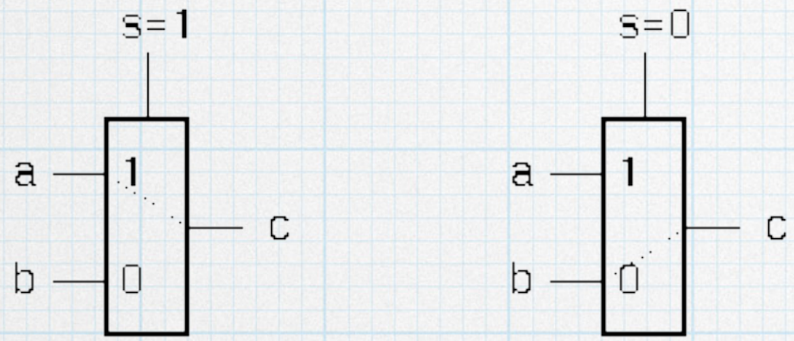


if en==1 then A connects to B

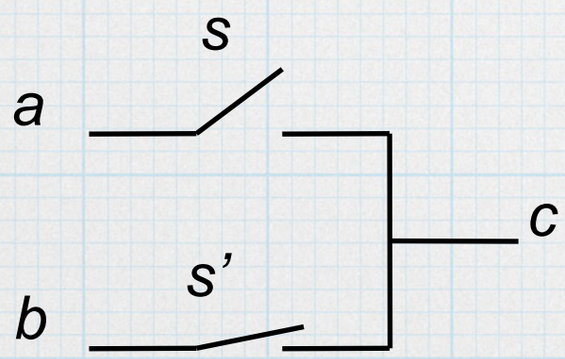
Transmission-gate Multiplexor

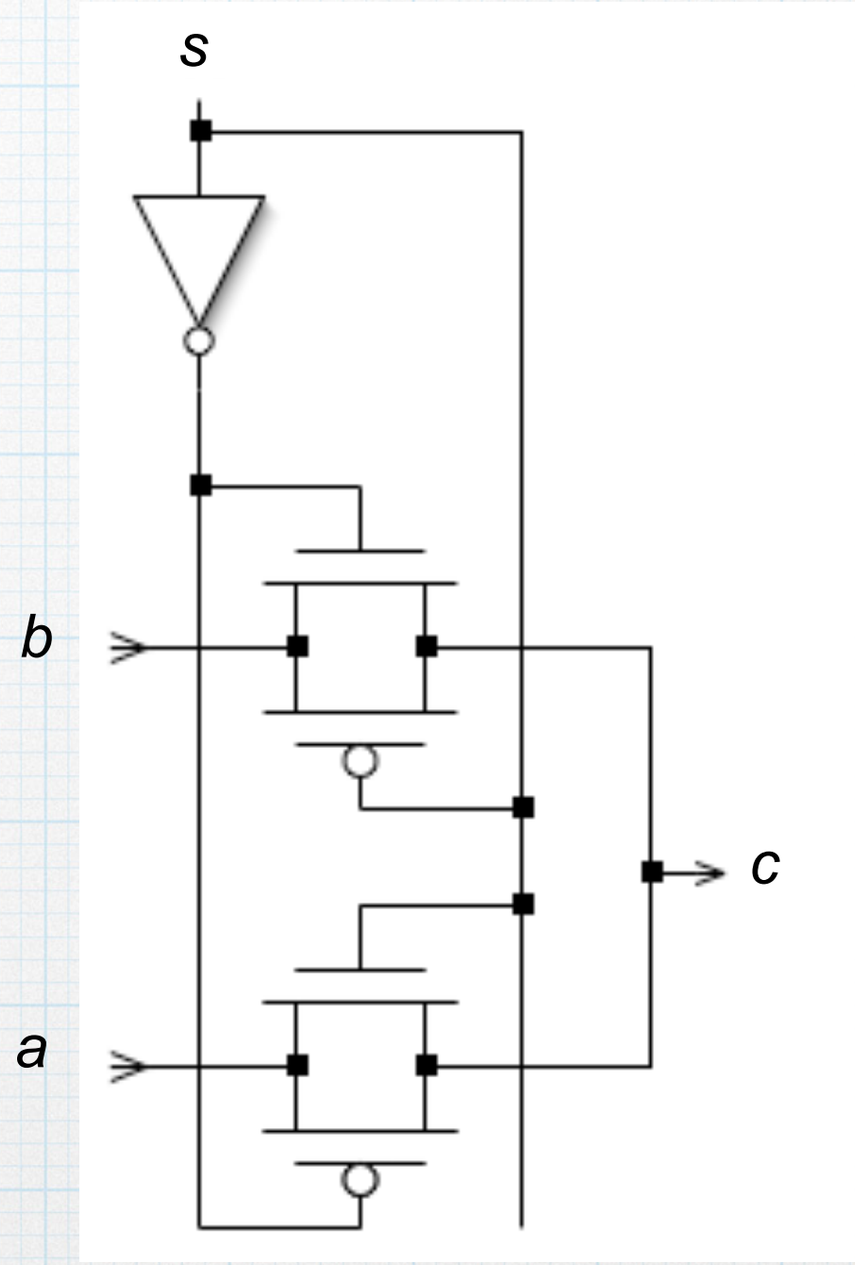
2-to-1 multiplexor:

c = sa + s'b



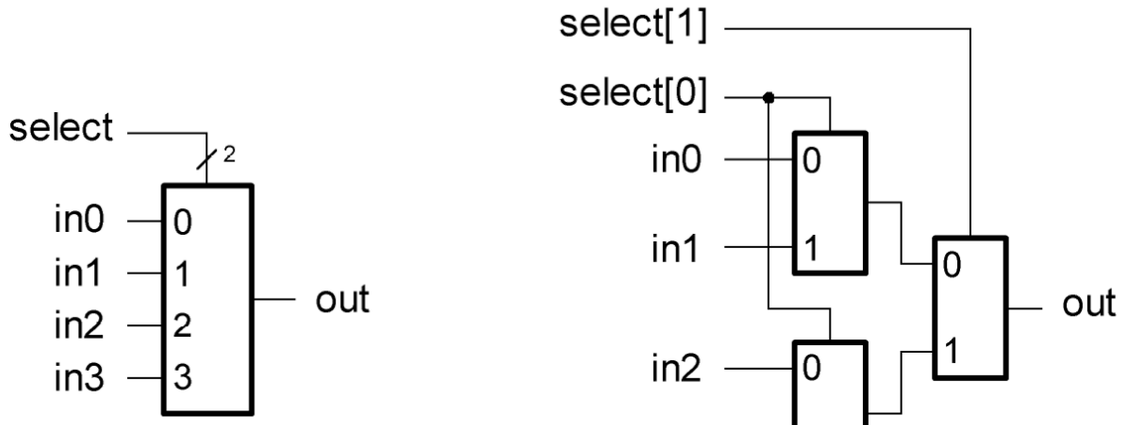
Switches simplify the implementation:





Compare the cost to logic gate implementation.

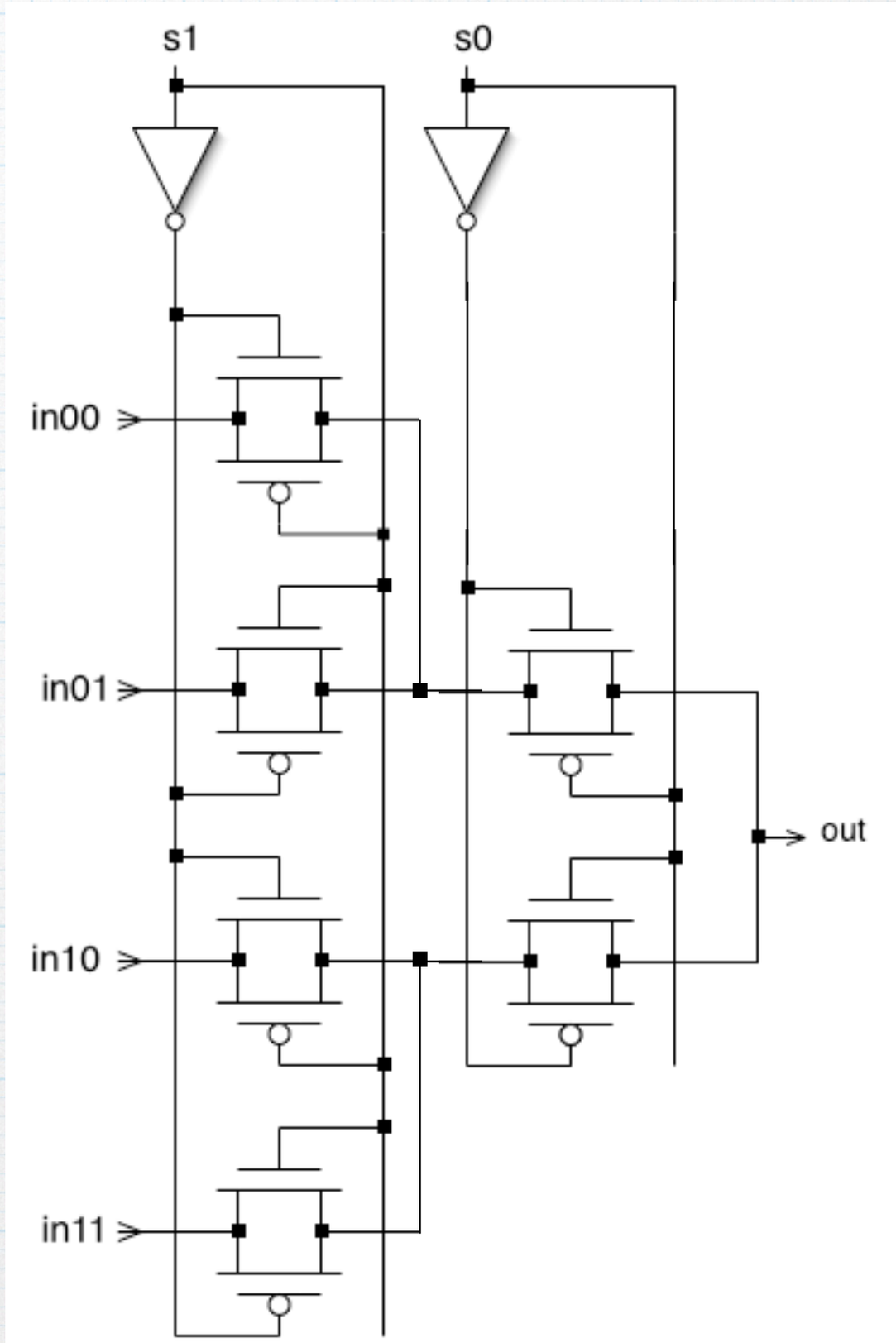
Larger Multiplexors



a) 4-input mux symbol

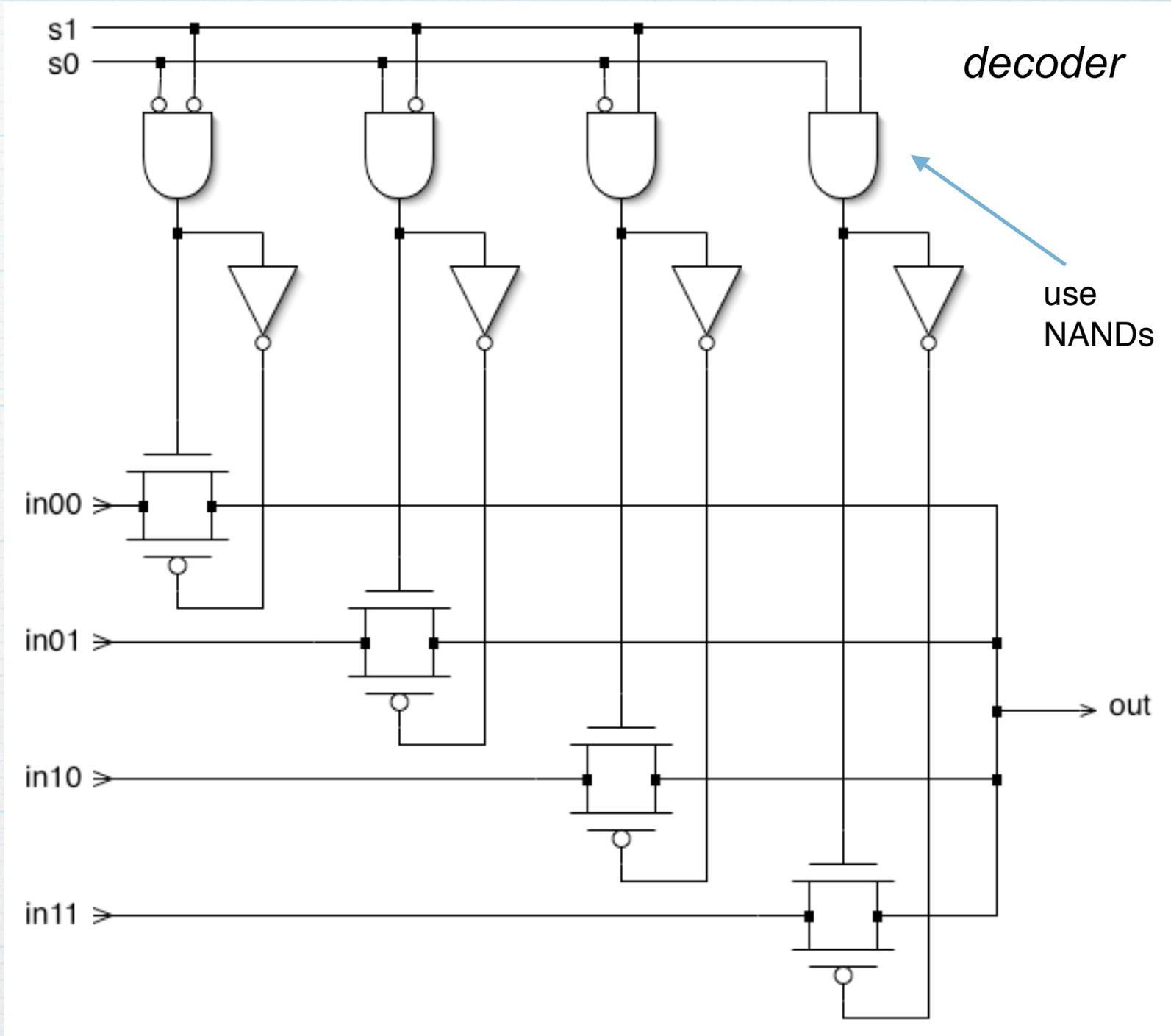
b) 4-input mux implemented with 2-input muxes

Care must be taken to not string together many pass-transistor stages. Occasionally, need to “rebuffer” with static gate (or inverter).



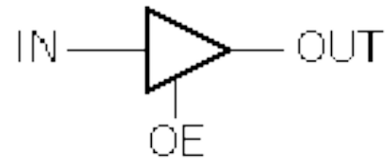
Predecoded 4-to-1 Multiplexor

- This version has less delay from in to out.
- In both versions, care must be taken to avoid turning on multiple paths simultaneously (shorting together the inputs).



Tri-state Buffers

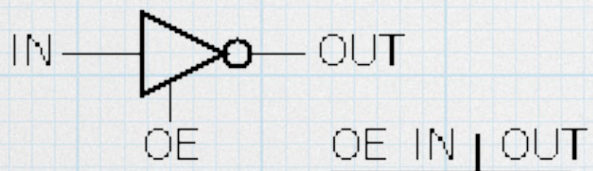
Tri-state Buffer:



OE	IN	OUT
0	0	Z
0	1	Z
1	0	0
1	1	1

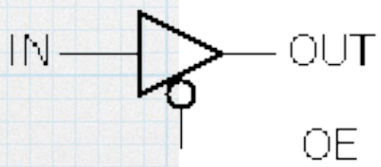
"high impedance" (output disconnected)

Variations:



OE	IN	OUT
0	–	Z
1	0	1
1	1	0

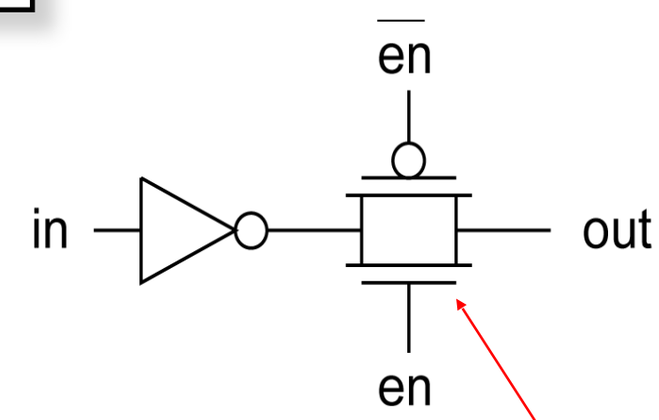
Inverting buffer

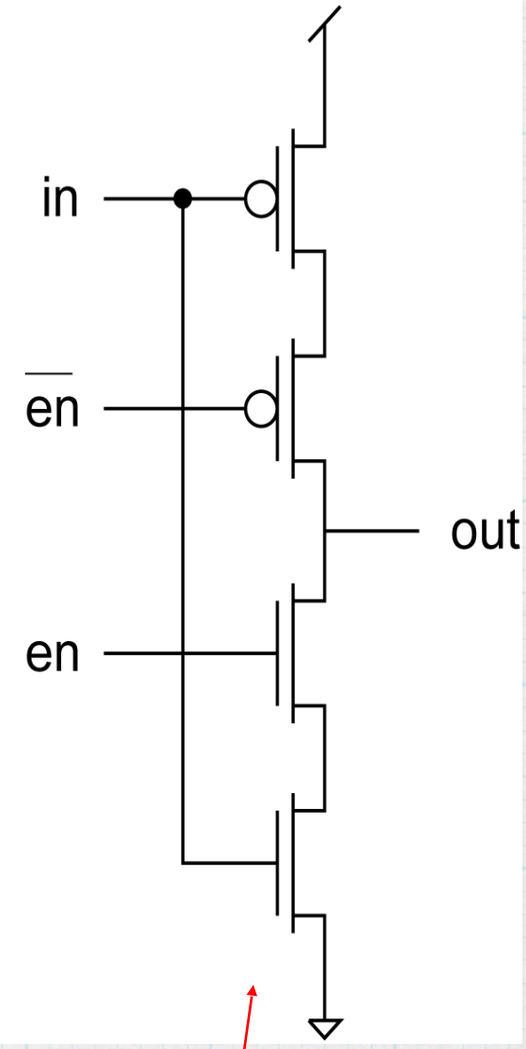


OE	IN	OUT
0	0	0
0	1	1
1	–	Z

Inverted enable

CMOS Implementation

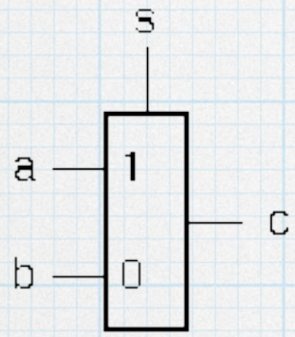




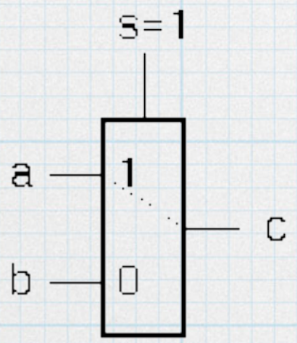
transmission gate provide the isolation:
usually designed this way

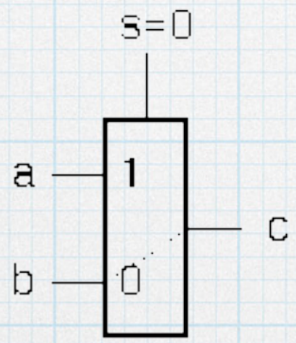
Tri-state Based Multiplexor

Multiplexor:

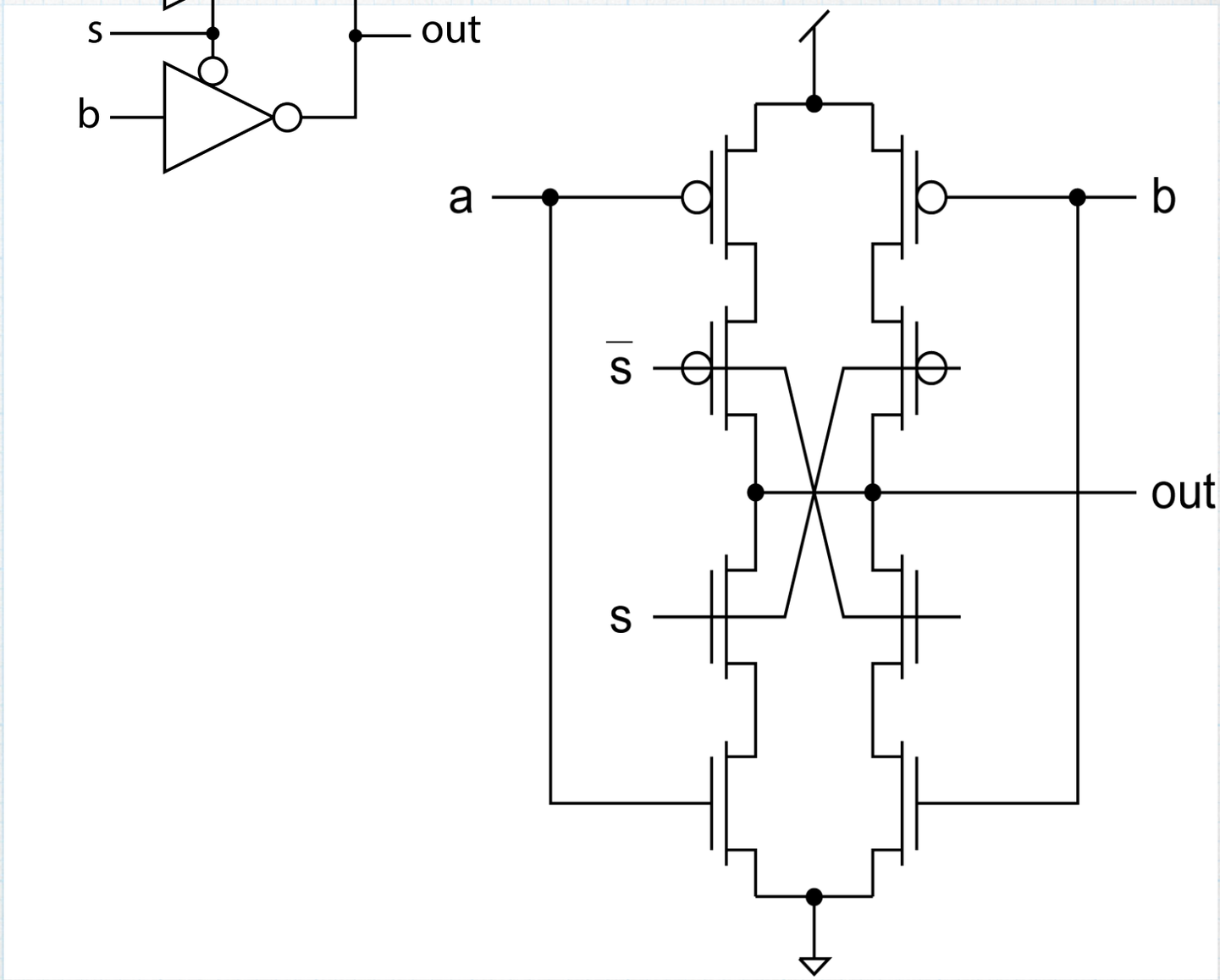


If s=1 then c=a else c=b

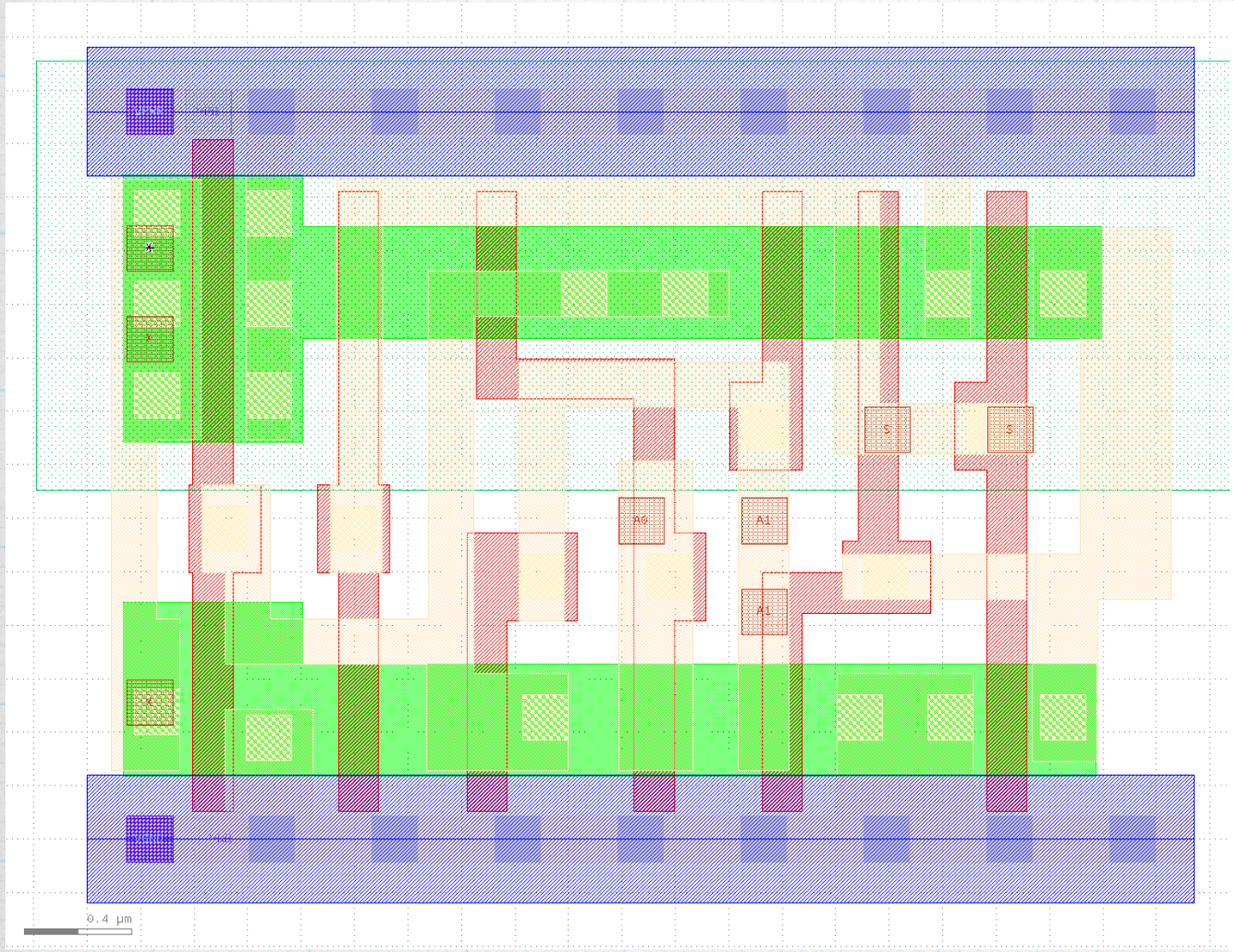


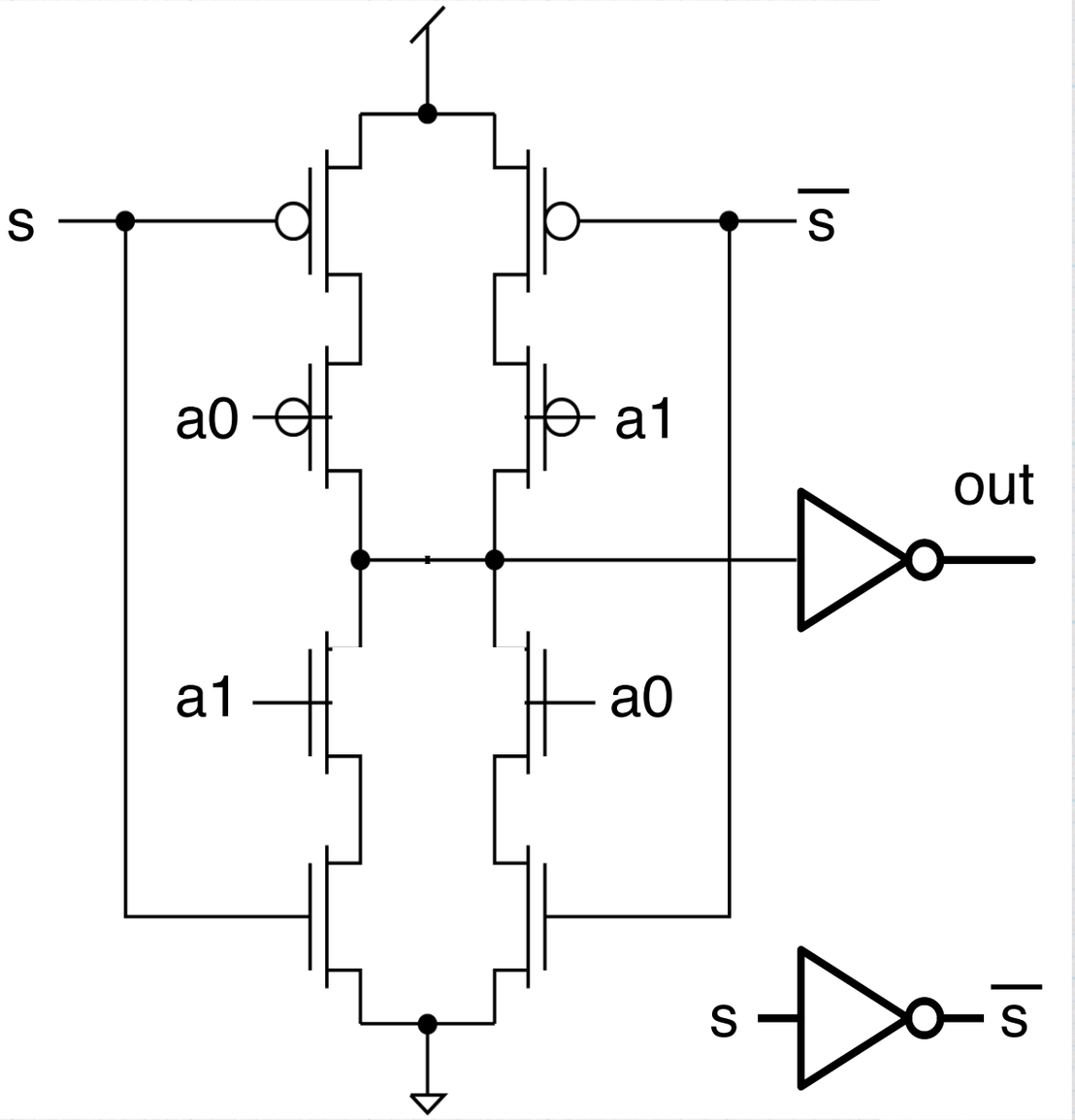


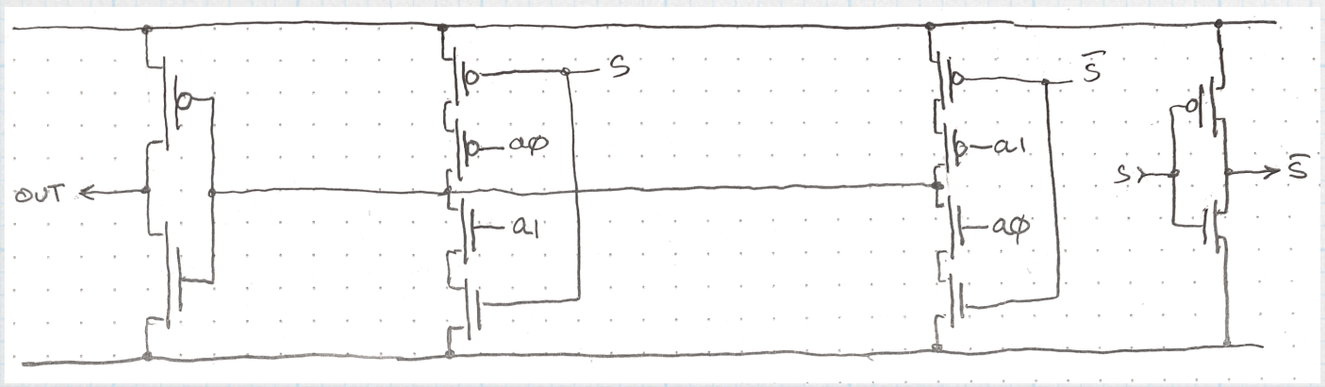
Transistor Circuit for inverting-multiplexor:



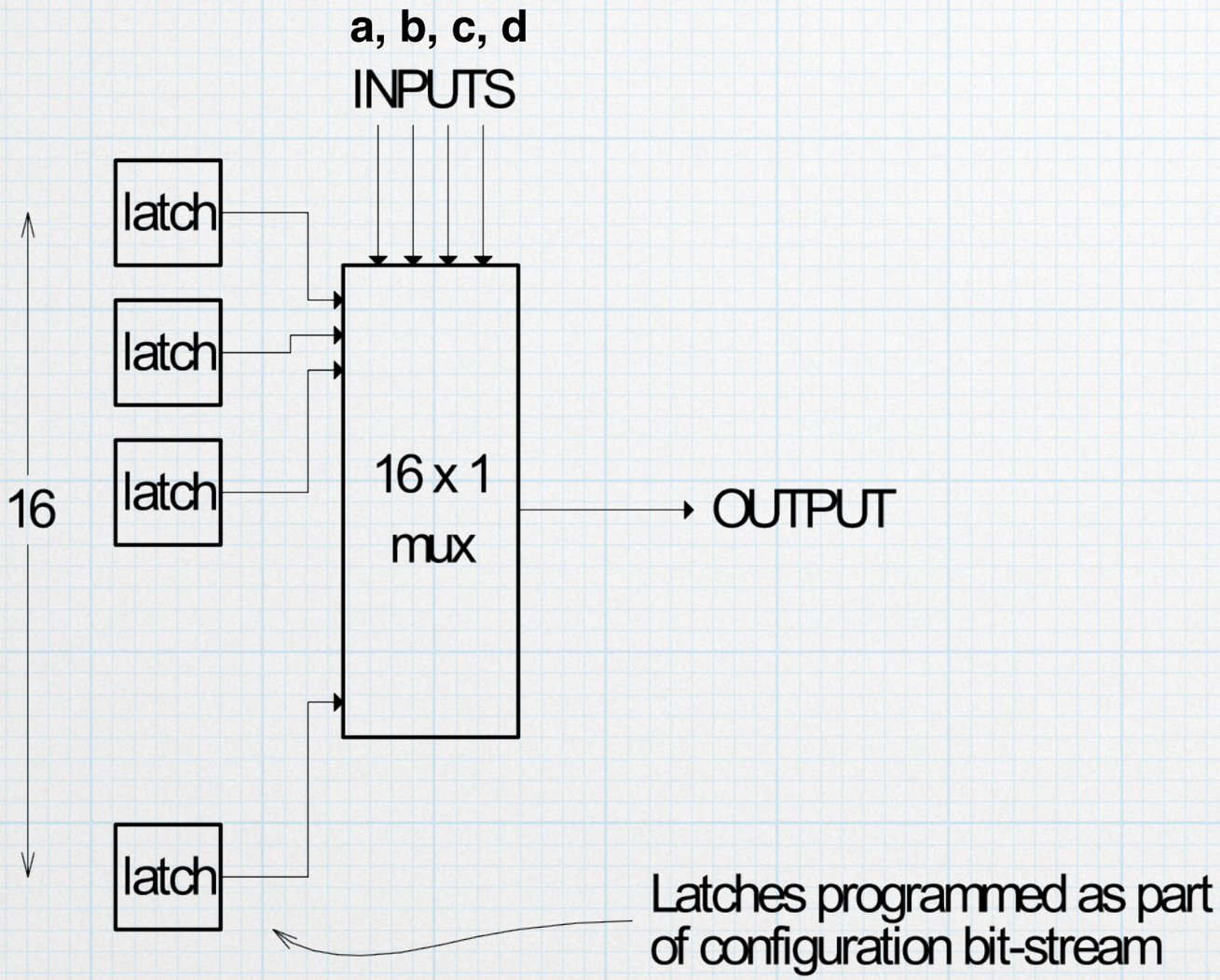
Sky130 Stdcell Multiplexor

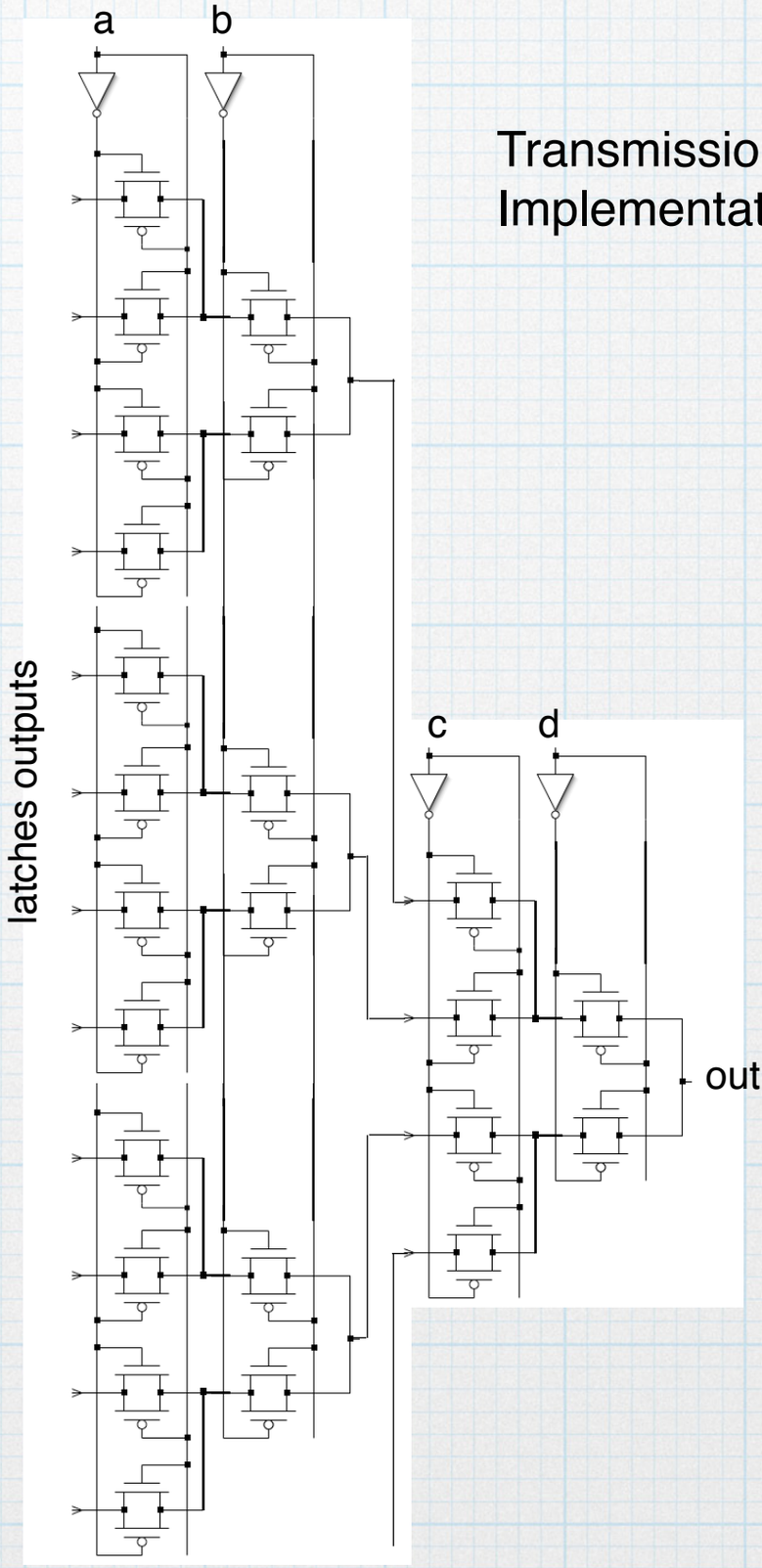






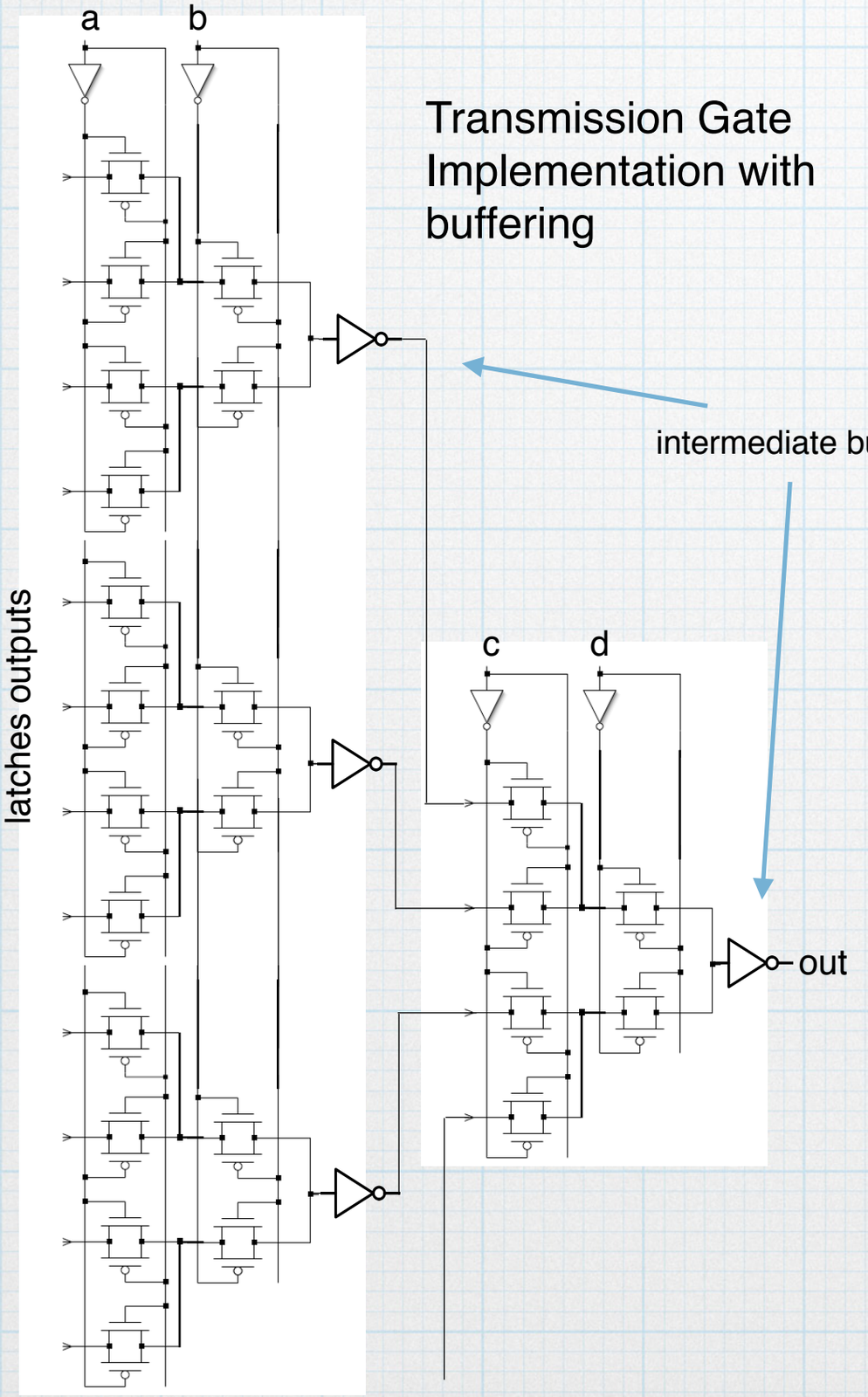
LUT implementation



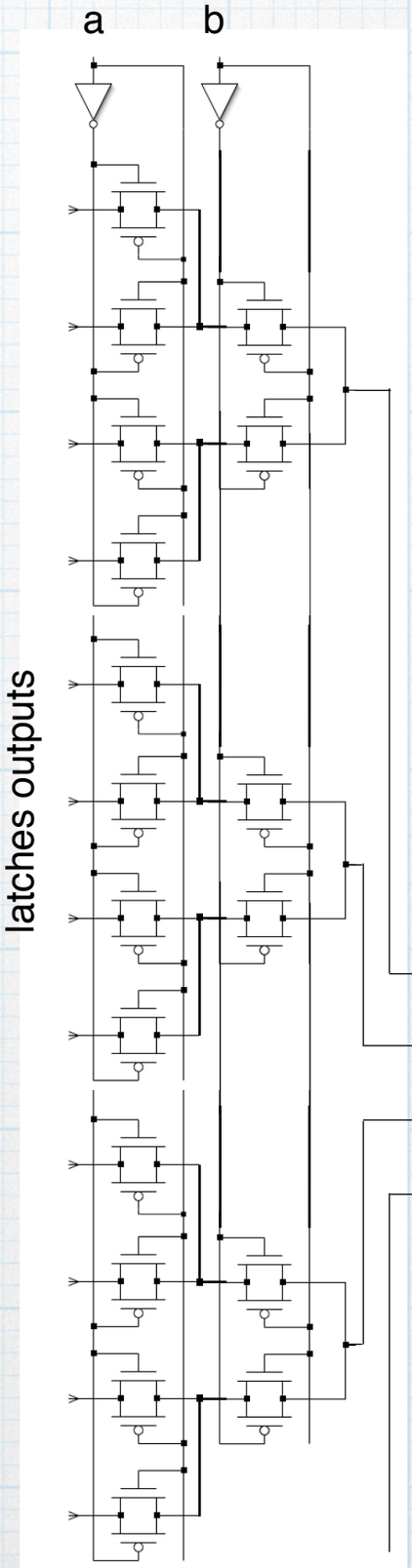


Transmission Gate Implementation

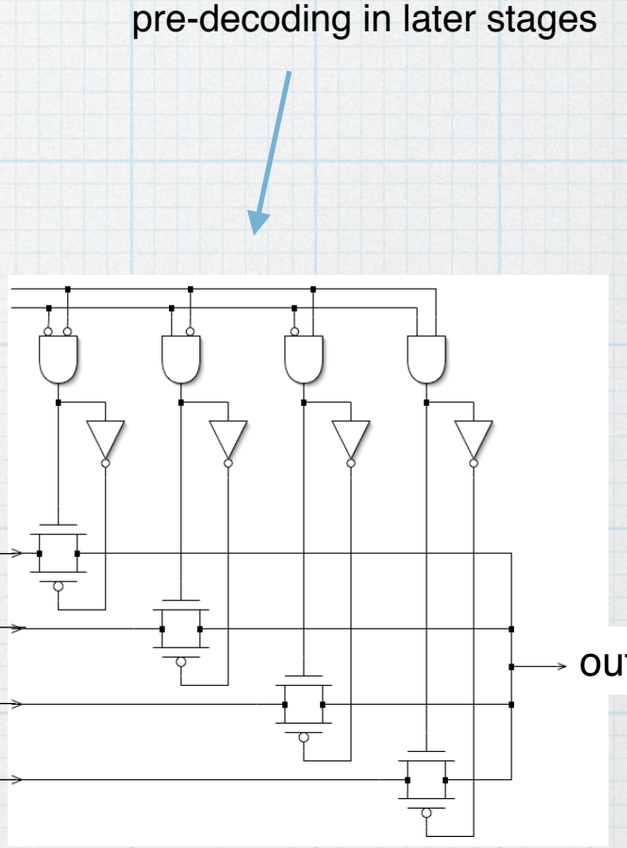
Higher Performance LUTs



Transmission Gate Implementation with buffering

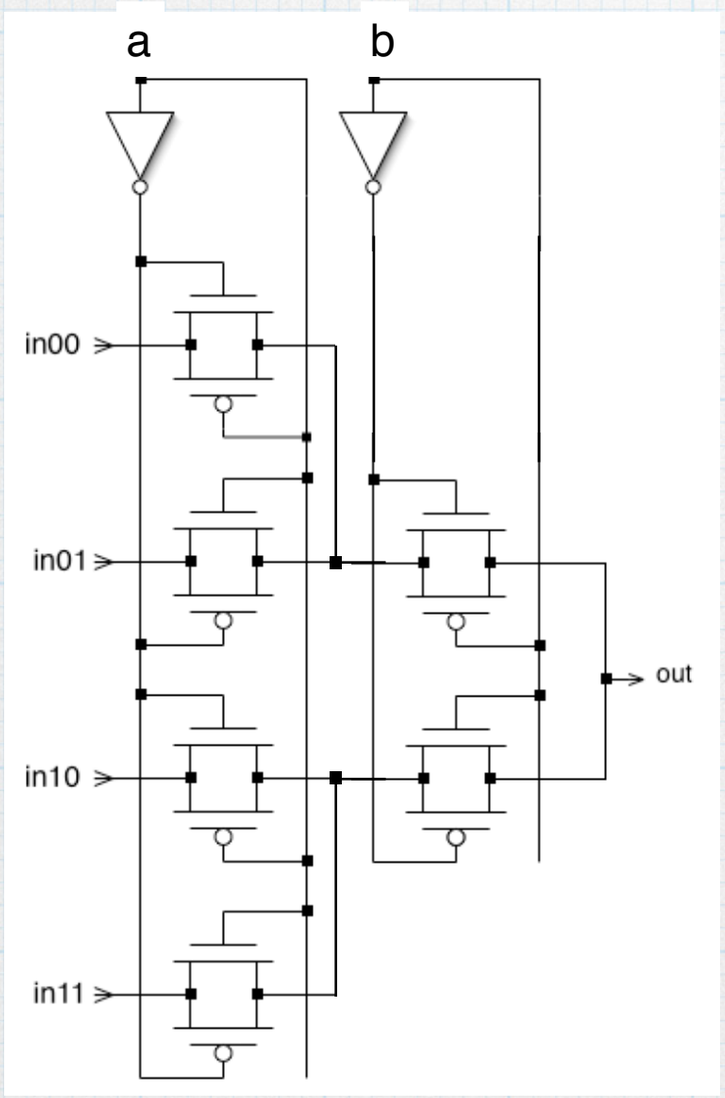


Hybrid Implementation with pre-decoding

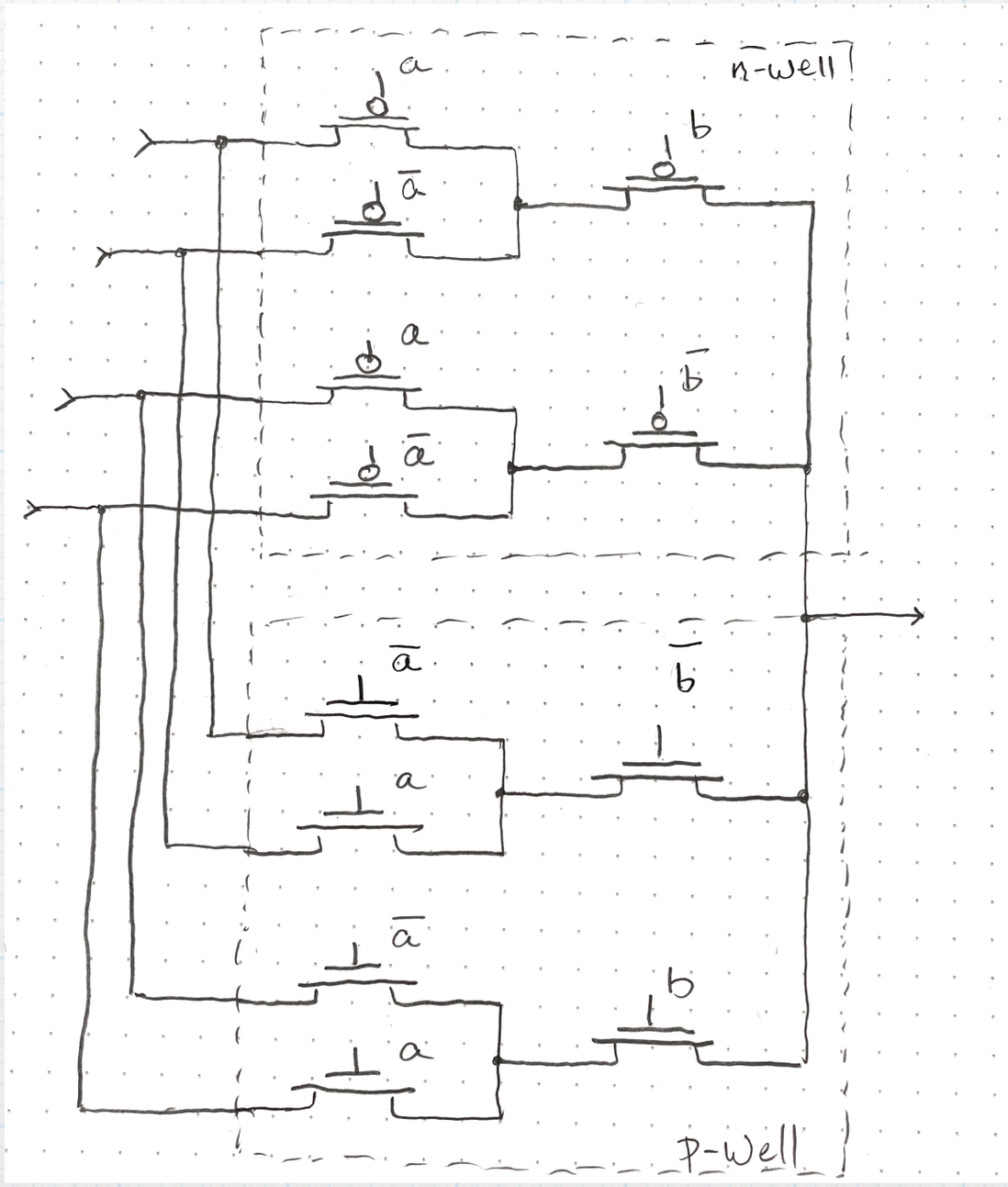


Large Mux layout considerations

- 4-to-1 example
- p-path & n-path for all a,b combinations



separately group p's and n's



End of Lecture 12