VLSI Design EE 523
Spring 2025

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Lecture 10

Topics for lecture 10

- **β ratio** effects in transfer characteristics of inverter
- How **mobility effects β ratios and size of CMOS transistors**
- Resistance of CMOS Transmission Gate (Switch)
- Simple R and C model in a CMOS transistor and Inverter
- Adjust sizing W/L of NMOS and PMOS to achieve R and 2R in Symmetric Unit Inverter
- Capacitance in a Unit Inverter and effect of W/L
- tphl and tplh of Unit Inverter
- Assigning W/L values to NMOS and PMOS in a 3-input Nand gate
- Explore these websites
  - app.siliwiz.com make your own CMOS devices and observe characteristics
  - tinytapeout.com to fabricate your own chips
  - efabless.com to fabricate your own chips
- **QUIZ 2 NEXT LECTURE**

Inver

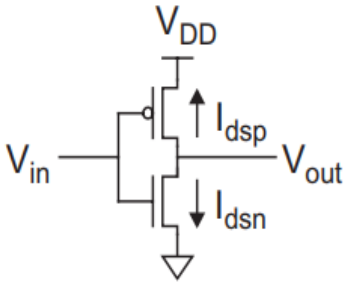


FIGURE 2.25
A CMOS inverter

2.5.1 Static CMOS Inverter DC Characteristics

Let us derive the DC transfer function (V_{out} vs. V_{in}) for the static CMOS inverter shown in Figure 2.25. We begin with Table 2.2, which outlines various regions of operation for the n- and p-transistors. In this table, V_{tn} is the threshold voltage of the n-channel device, and V_{tp} is the threshold voltage of the p-channel device. Note that V_{tp} is negative. The equations are given both in terms of V_{gs}/V_{ds} and V_{in}/V_{out}. As the source of the nMOS transistor is grounded, $V_{gsn} = V_{in}$ and $V_{dsn} = V_{out}$. As the source of the pMOS transistor is tied to V_{DD}, $V_{gsp} = V_{in} - V_{DD}$ and $V_{dsp} = V_{out} - V_{DD}$.

TABLE 2.2 Relationships between voltages for the three regions of operation of a CMOS inverter

	Cutoff	Linear	Saturated
nMOS	$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
		$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
		$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$
		$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
		$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$

Inverter Regions and Characteristics

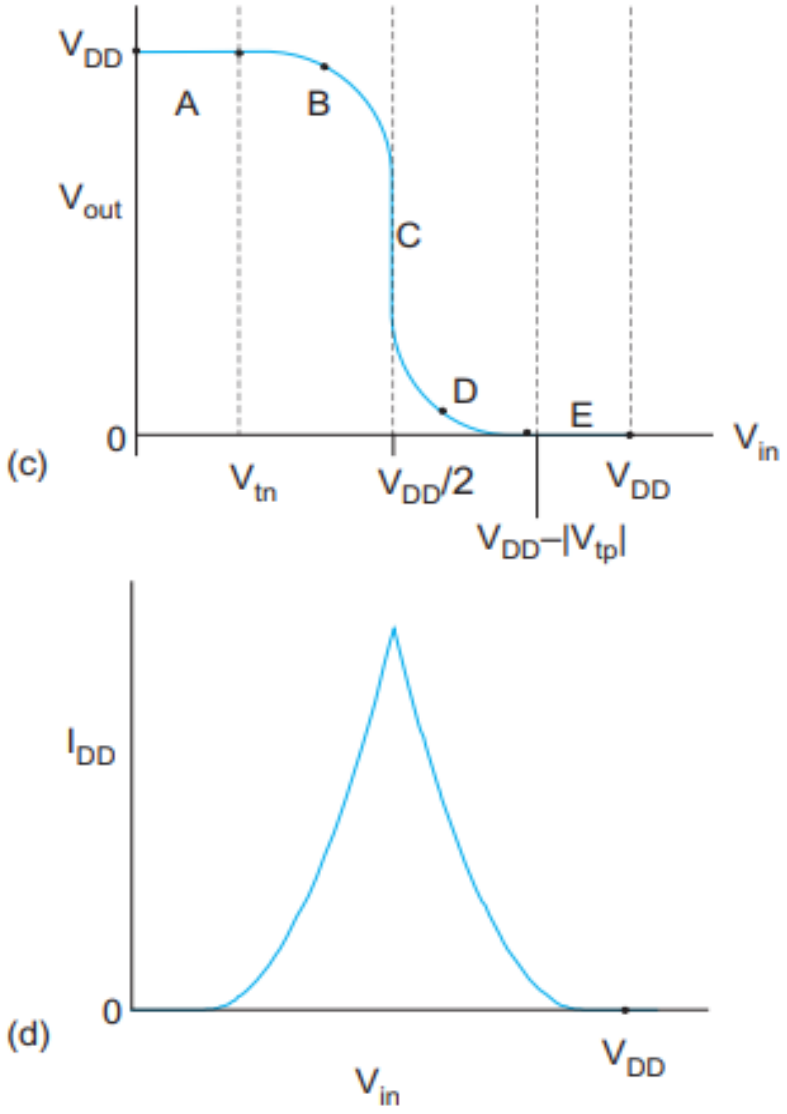


TABLE 2.3 Summary of CMOS inverter operation

Region	Condition	p-device	n-device	Output
A	$0 \le V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \le V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	V_{out} drops sharply
D	$V_{DD}/2 < V_{in} \le V_{DD} - \lvert V_{tp} \rvert$	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} - \lvert V_{tp} \rvert$	cutoff	linear	$V_{out} = 0$

Ids Equations

$$\beta = \mu C_{\text{ox}} \frac{W}{L};\ V_{GT} = V_{gs} - V_t \qquad \textbf{(2.6)}$$

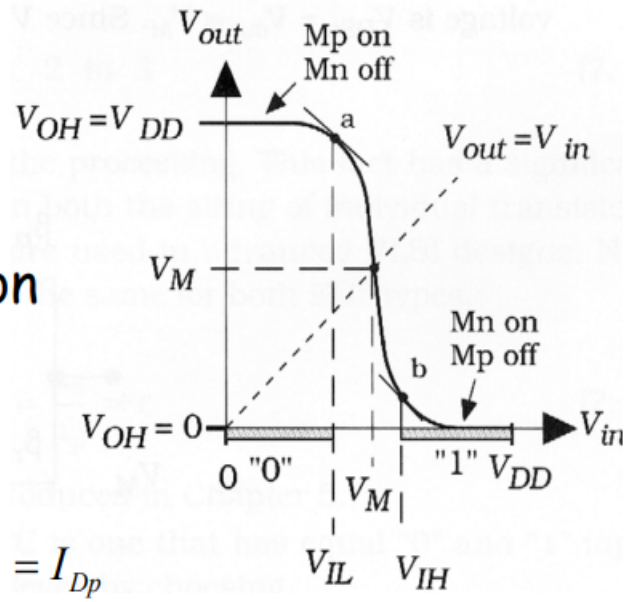
$$k' = \mu C_{\text{ox}} \qquad \textbf{(2.7)}$$

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{Cutoff} \\ \beta\left(V_{GT} - V_{ds}/2\right)V_{ds} & V_{ds} < V_{\text{dsat}} & \text{Linear} \\ \dfrac{\beta}{2}V_{GT}^2 & V_{ds} > V_{\text{dsat}} & \text{Saturation} \end{cases} \qquad \textbf{(2.10)}$$

Midpoint

Switching Threshold

- Switching threshold = point on VTC where Vout = Vin
  - also called midpoint voltage, V_M
  - here, Vin = Vout = V_M
- Calculating V_M
  - at V_M, both nMOS and pMOS in Saturation
  - in an inverter, $I_{Dn} = I_{Dp}$, always!
  - solve equation for V_M



$$I_{Dn} = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{GSn} - V_{tn})^2 = \frac{\beta_n}{2}(V_{GSn} - V_{tn})^2 = \frac{\beta_p}{2}(V_{SGp} - |V_{tp}|)^2 = I_{Dp}$$

  - express in terms of V_M

$$\frac{\beta_n}{2}(V_M - V_{tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_M - |V_{tp}|)^2 \quad \Rightarrow \quad \sqrt{\frac{\beta_n}{\beta_p}}(V_M - V_{tn}) = V_{DD} - V_M - |V_{tp}|$$

  - solve for V_M

$$V_M = \frac{VDD - |V_{tp}| + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Effect of Transistor Size on VTC

- Recall

$$\beta_n = k'_n \frac{W}{L} \qquad \frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$$

$$V_M = \frac{VDD - |V_{tp}| + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

- If nMOS and pMOS are same size
  - (W/L)n = (W/L)p
  - Coxn = Coxp (always)

$$\frac{\beta_n}{\beta_p} = \frac{\mu_n C_{oxn}\left(\frac{W}{L}\right)_n}{\mu_p C_{oxp}\left(\frac{W}{L}\right)_p} = \frac{\mu_n}{\mu_p} \cong 2 or 3$$

- If $\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\mu_n}{\mu_p}, then \frac{\beta_n}{\beta_p} = 1$

since L normally min. size for all tx,
can get betas equal by making Wp larger than Wn

- Effect on switching threshold
  - if $\beta_n \approx \beta_p$ and Vtn = |Vtp|, V_M = VDD/2, exactly in the middle

- Effect on noise margin
  - if $\beta_n \approx \beta_p$, V_{IH} and V_{IL} both close to V_M and noise margin is good

Beta ratio

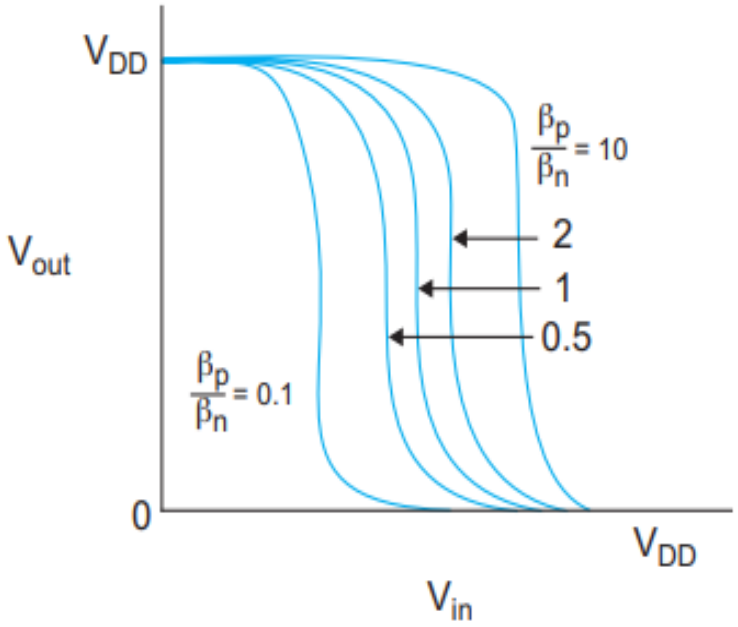


FIGURE 2.28 Transfer characteristics of skewed inverters

2.5.2 Beta Ratio Effects

We have seen that for $\beta_p = \beta_n$, the inverter threshold voltage V_{inv} is $V_{DD}/2$. This may be desirable because it maximizes noise margins (see Section 2.5.3) and allows a capacitive load to charge and discharge in equal times by providing equal current source and sink capabilities (see Section 4.2). Inverters with different beta ratios $r = \beta_p/\beta_n$ are called *skewed* inverters [Sutherland99]. If $r > 1$, the inverter is *HI-skewed*. If $r < 1$, the inverter is *LO-skewed*. If $r = 1$, the inverter has normal skew or is *unskewed*.

A HI-skew inverter has a stronger pMOS transistor. Therefore, if the input is $V_{DD}/2$, we would expect the output will be greater than $V_{DD}/2$. In other words, the input threshold must be higher than for an unskewed inverter. Similarly, a LO-skew inverter has a weaker pMOS transistor and thus a lower switching threshold.

Vinverter

The inverter threshold can also be computed analytically. If the long-channel models of EQ (2.10) for saturated transistors are valid:

$$I_{dn} = \frac{\beta_n}{2}\left(V_{\text{inv}} - V_{tn}\right)^2$$
$$I_{dp} = \frac{\beta_p}{2}\left(V_{\text{inv}} - V_{DD} - V_{tp}\right)^2 \quad \textbf{(2.54)}$$

By setting the currents to be equal and opposite, we can solve for V_{inv} as a function of r:

$$V_{\text{inv}} = \frac{V_{DD} + V_{tp} + V_{tn}\sqrt{\frac{1}{r}}}{1 + \sqrt{\frac{1}{r}}} \quad \textbf{(2.55)}$$

In the limit that the transistors are fully velocity saturated, EQ (2.29) shows

$$I_{dn} = W_n C_{\text{ox}} v_{\text{sat}-n}(V_{\text{inv}} - V_{tn})$$
$$I_{dp} = W_p C_{\text{ox}} v_{\text{sat}-p}(V_{\text{inv}} - V_{DD} - V_{tp}) \quad \textbf{(2.56)}$$

Redefining $r = W_p v_{\text{sat-}p} / W_n v_{\text{sat-}n}$, we can again find the inverter threshold

$$V_{\text{inv}} = \frac{V_{DD} + V_{tp} + V_{tn}\frac{1}{r}}{1 + \frac{1}{r}} \quad \textbf{(2.57)}$$

In either case, if $V_{tn} = -V_{tp}$ and $r = 1$, $V_{\text{inv}} = V_{DD}/2$ as expected. However, velocity saturated inverters are more sensitive to skewing because their DC transfer characteristics are not as sharp.

Inverter Switching Point

11.1.2 Inverter Switching Point

Consider the transfer characteristics of the basic inverter as shown in Fig. 11.4. Point C corresponds to the point on the curve when the input voltage is equal to the output voltage. At this point, the input (or output) voltage is called the inverter switching point voltage, V_{SP}, and both MOSFETs in the inverter are in the saturation region. Since the drain current in each MOSFET must be equal, the following is true:

$$\frac{\beta_n}{2}(V_{SP}-V_{THN})^2=\frac{\beta_p}{2}(VDD-V_{SP}-V_{THP})^2 \qquad (11.3)$$

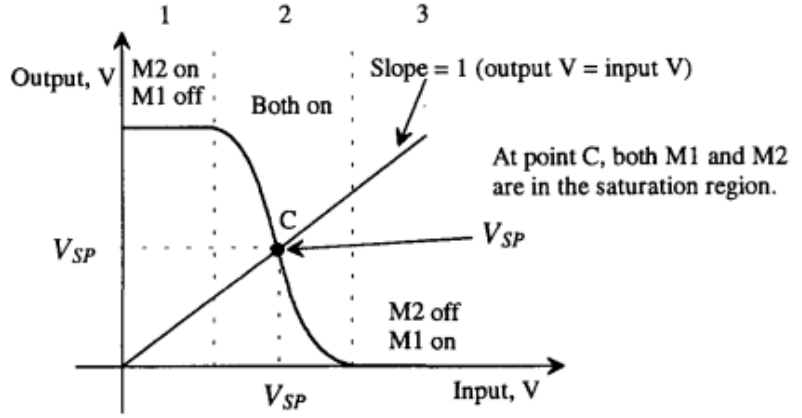


Figure 11.4 Transfer characteristics of the inverter showing the switching point.

$$V_{SP}=\frac{\sqrt{\frac{\beta_n}{\beta_p}}\cdot V_{THN}+(VDD-V_{THP})}{1+\sqrt{\frac{\beta_n}{\beta_p}}} \qquad (11.4)$$

Inverter Capacitances

The switching behavior of the inverter can be generalized by examining the parasitic capacitances and resistances associated with the inverter. Consider the inverter shown in Fig. 11.6 with its equivalent digital model. Although the model is shown with both switches open, in practice one of the switches is closed, keeping the output connected to *VDD* or ground. Notice that the effective input capacitance of the inverter is

$$C_{in} = \frac{3}{2}(C_{ox1} + C_{ox2}) = C_{inn} + C_{inp} \qquad (11.5)$$

The effective output capacitance of the inverter is simply

$$C_{out} = C_{ox1} + C_{ox2} = C_{outn} + C_{outp} \qquad (11.6)$$

RC Model of Inverter

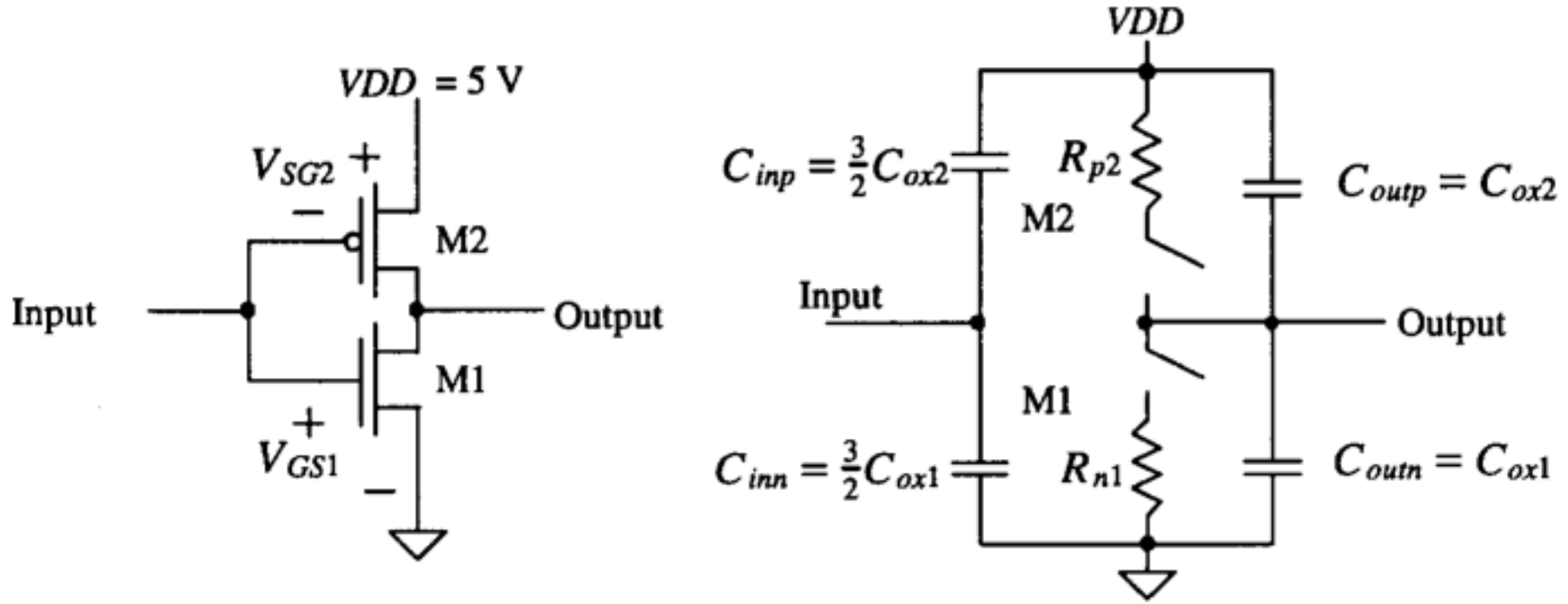


Figure 11.6 The CMOS inverter switching characteristics using the digital model.

Beta Ratio

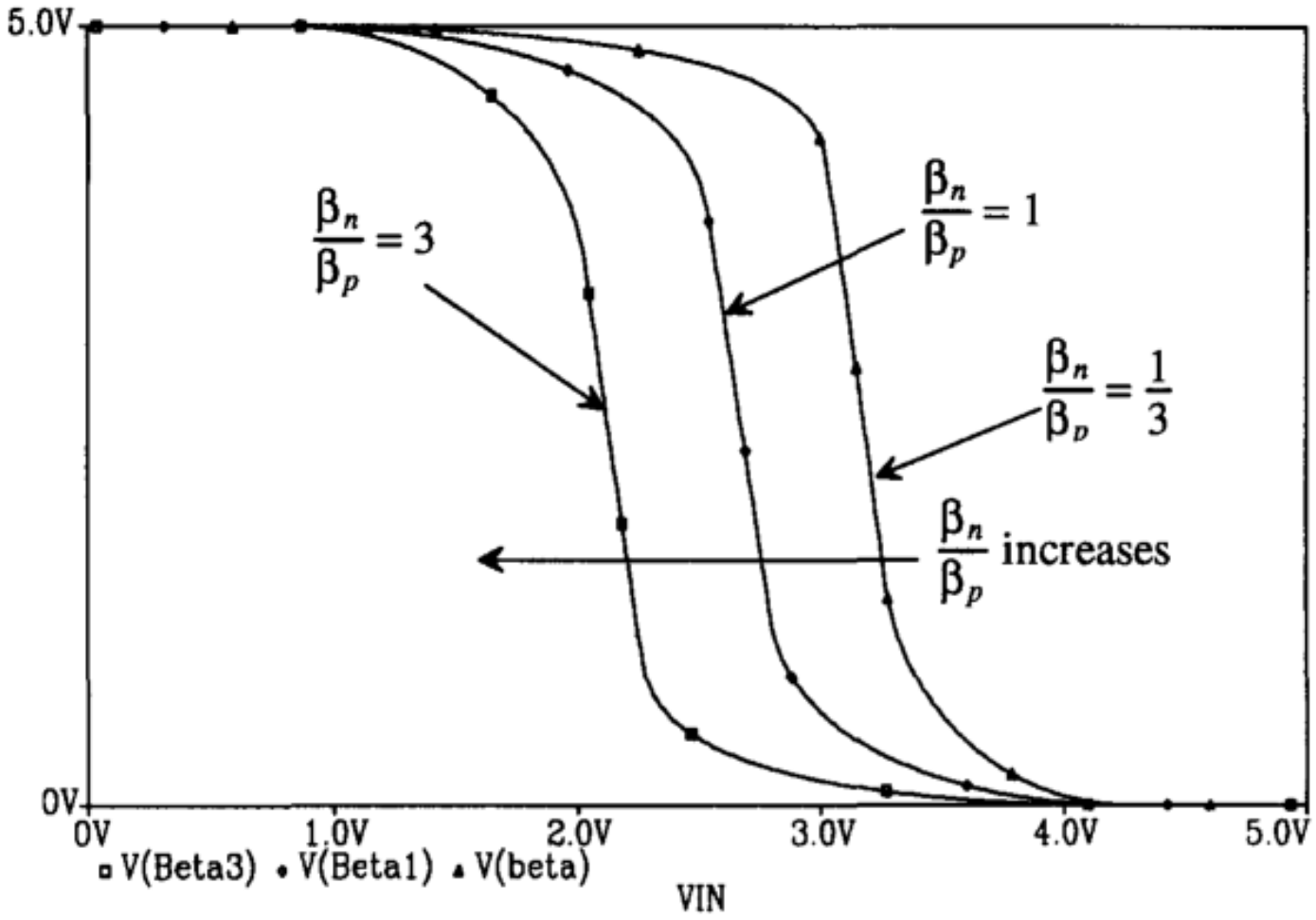


Figure 11.5 Sizing of the CMOS inverter.

Intrinsic Prop Del

Example 11.5

Estimate and simulate the intrinsic propagation delays of the minimum-size inverter.

For the minimum-size inverter $C_{ox1} = C_{ox2} = 3\ \mu m \cdot 2\ \mu m \cdot 800\ aF/\mu m^2 = 4.8\ fF$. $R_{n1} = 12k \cdot 2\ \mu m/3\ \mu m = 8\ k\Omega$, while $R_{p2} = 24\ k\Omega$. The propagation delay times $t_{PHL} = 77$ ps and $t_{PLH} = 230$ ps. The simulation results are shown in Fig. 11.7. ■

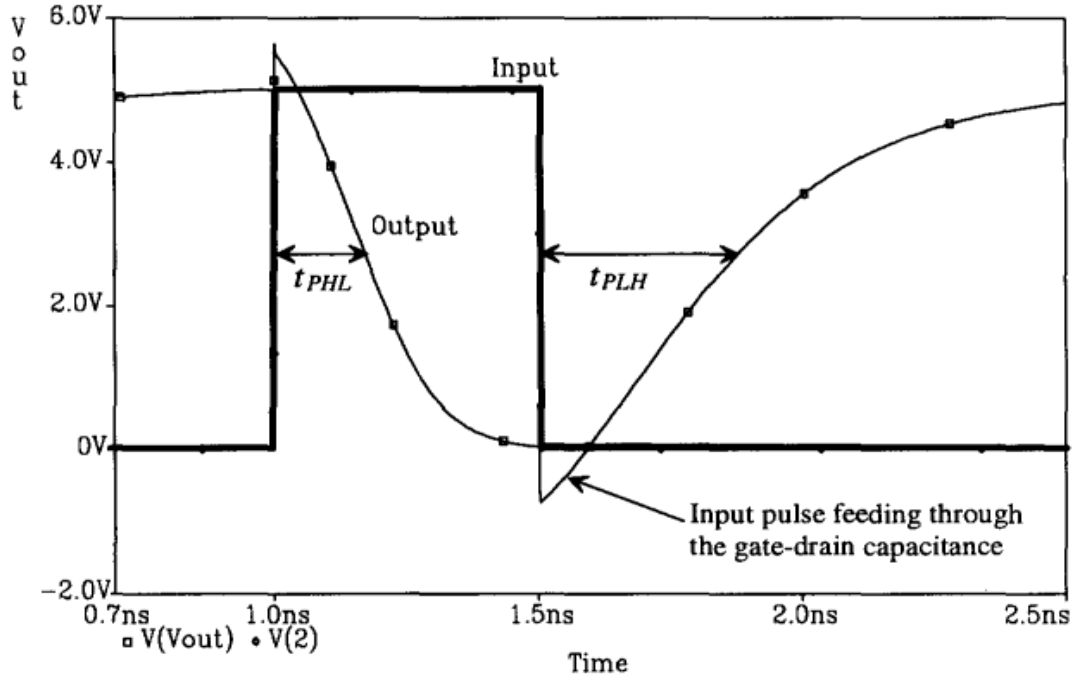


Figure 11.7 Intrinsic inverter delay.

The intrinsic propagation delays of the inverter are

$$t_{PLH} = R_{p2} \cdot C_{out} \tag{11.7}$$

$$t_{PHL} = R_{n1} \cdot C_{out} \tag{11.8}$$

Inverter Driving Capacitance

The propagation delays for an inverter driving a capacitive load are

$$t_{PLH} = R_{p2} \cdot C_{tot} = R_{p2} \cdot (C_{out} + C_{load}) \qquad (11.9)$$

and

$$t_{PHL} = R_{n1} \cdot C_{tot} = R_{n1} \cdot (C_{out} + C_{load}) \qquad (11.10)$$

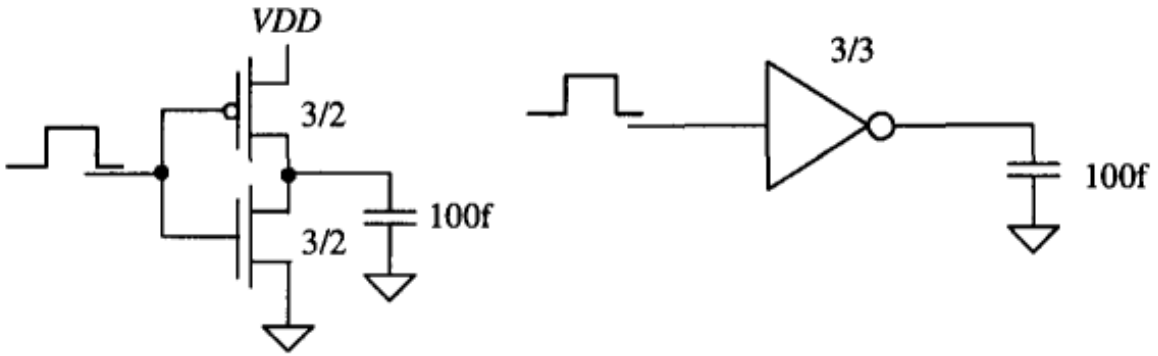


Figure 11.8 Inverter driving a 100 fF load capacitance in Ex. 11.6.

Ring Oscillator

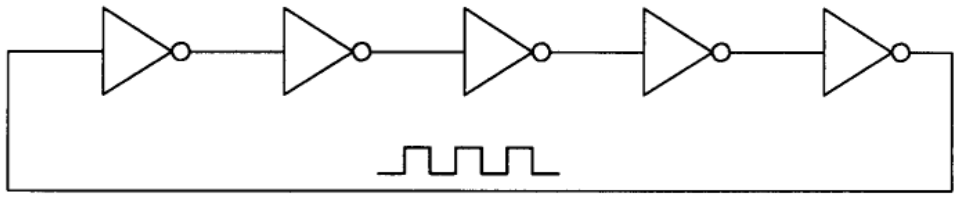


Figure 11.10 A five-stage ring oscillator.

11.2.1 The Ring Oscillator

The odd number of inverters of the circuit shown in Fig. 11.10 forms a closed loop with positive feedback and is called a ring oscillator. The oscillation frequency is given by

$$f_{osc} = \frac{1}{n \cdot (t_{PHL} + t_{PLH})} \tag{11.11}$$

assuming the inverters are identical and n is the number (odd) of inverters in the ring oscillator. Since the ring oscillator is self-starting, it is often added to a test portion of a wafer to give an indication of the speed of a particular run.

Consider the case when a minimum-size inverter is used. Under these conditions, C_{tot} is given by

$$C_{tot} = \overbrace{2C_{ox}}^{C_{out}} + \overbrace{3C_{ox}}^{C_{in}} = 5C_{ox} \tag{11.12}$$

where $C_{ox} = 2\ \mu m \cdot 3\ \mu m \cdot C'_{ox}$, so that

$$t_{PHL} + t_{PLH} = (R_{n1} + R_{p2})C_{tot} = (12k + 36k)\frac{2}{2} \cdot 5C_{ox} = 160k \cdot C_{ox} \tag{11.13}$$

Also consider the case when the inverters are sized to give equal propagation times. For the delays to be identical, W_2 must equal $3W_1$, which leads to a larger oxide capacitance for M_2, or

$$C_{ox2} = 3C_{ox1} \tag{11.14}$$

Therefore, C_{tot} is given by

$$C_{tot} = \overbrace{4C_{ox}}^{C_{out}} + \overbrace{6C_{ox}}^{C_{in}} = 10C_{ox} \tag{11.15}$$

and the propagation delays are given by

$$t_{PHL} + t_{PLH} = \left(12k\frac{2}{3} + 36k\frac{2}{9}\right)10C_{ox} = 160k \cdot C_{ox} \tag{11.16}$$

Power Dissipation in Inverter

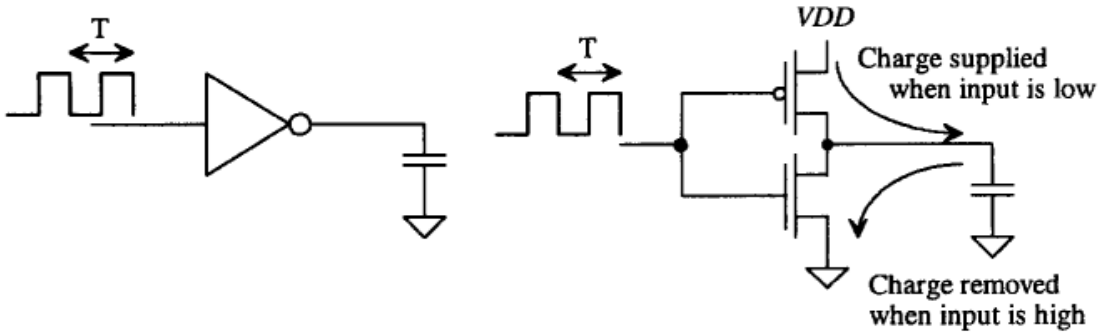


Figure 11.11 Dynamic power dissipation of the CMOS inverter.

11.2.2 Dynamic Power Dissipation

Consider the CMOS inverter driving a capacitive load shown in Fig. 11.11. Each time the inverter changes states, it must either supply a charge to C_{tot} or sink the charge stored on C_{tot} to ground. If a square pulse is applied to the input of the inverter with a period T and frequency, f_{clk}, the average amount of current that the inverter must pull from *VDD*, recalling that current is being supplied from *VDD* only when the p-channel is on, is

$$I_{avg} = \frac{Q_{Ctot}}{T} = \frac{VDD \cdot C_{tot}}{T} \tag{11.17}$$

The average dynamic power dissipated by the inverter is

$$P_{avg} = VDD \cdot I_{avg} = \frac{C_{tot} \cdot VDD^2}{T} = C_{tot} \cdot VDD^2 \cdot f_{clk} \tag{11.18}$$

Notice that the power dissipation is a function of the clock frequency. A great deal of effort is put into reducing the power dissipation in CMOS circuits. One of the major advantages of dynamic logic (Ch. 14) is its lower power dissipation.

To characterize the speed of a digital process, a term called the power delay product (*PDP*) is often used. The *PDP*, measured in joules, is defined by

$$PDP = P_{avg} \cdot (t_{PHL} + t_{PLH}) \tag{11.19}$$

Reading and Book

- Textbook can be downloaded online “CMOS VLSI Design by Weste and Harris, 4th Edition”
- Readings from Chapter 2