

# VLSI Design EE 523

## Spring 2025

Shahid Masud

Lecture 7

# Topics for lecture 8

---



- MOS Capacitance model
- Difference between Area capacitance and Perimeter capacitance
- Concept of Lambda  $\lambda$  based design rules
- Area calculation using  $\lambda$  rules and its relation to technology
- Example of MOS Drain Capacitance Calculation
- Variation of typical MOS transistor characteristics due to:
  - Velocity Saturation, Mobility Degradation, Temperature Effects, Tunneling Effect, Geometry Effect, Channel Length Modulation, Body Effect Voltage
- Simple CMOS Inverter – transfer characteristics  $V_{in}$  and  $V_{out}$
- Noise Margin from these transfer characteristics

# Shockley Model for CMOS Transistor

where

$$\beta = \mu C_{\text{ox}} \frac{W}{L}; \quad V_{GT} = V_{gs} - V_t \quad (2.6)$$

EQ(2.10) summarizes the current in the three regions:

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{Cutoff} \\ \beta(V_{GT} - V_{ds}/2)V_{ds} & V_{ds} < V_{\text{dsat}} & \text{Linear} \\ \frac{\beta}{2}V_{GT}^2 & V_{ds} > V_{\text{dsat}} & \text{Saturation} \end{cases} \quad (2.10)$$

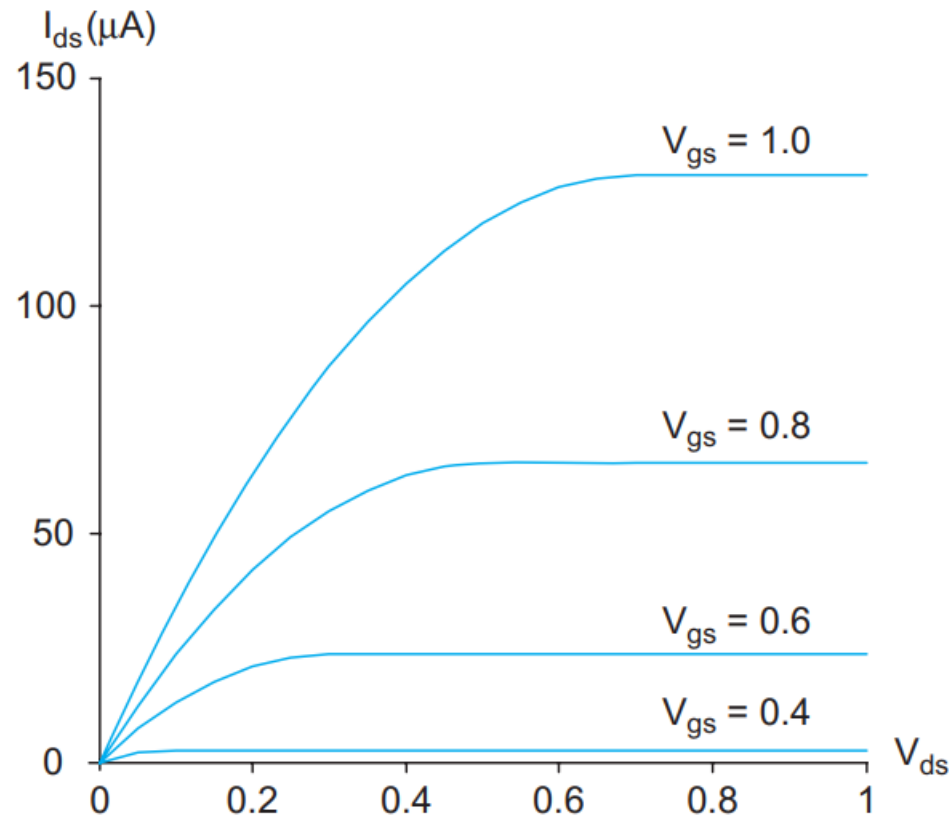
## Example 2.1

Consider an nMOS transistor in a 65 nm process with a minimum drawn channel length of 50 nm ( $\lambda = 25$  nm). Let  $W/L = 4/2 \lambda$  (i.e.,  $0.1/0.05 \mu\text{m}$ ). In this process, the gate oxide thickness is 10.5 Å. Estimate the high-field mobility of electrons to be  $80 \text{ cm}^2/\text{V}\cdot\text{s}$  at  $70^\circ\text{C}$ . The threshold voltage is 0.3 V. Plot  $I_{ds}$  vs.  $V_{ds}$  for  $V_{gs} = 0, 0.2, 0.4, 0.6, 0.8$ , and 1.0 V using the long-channel model.

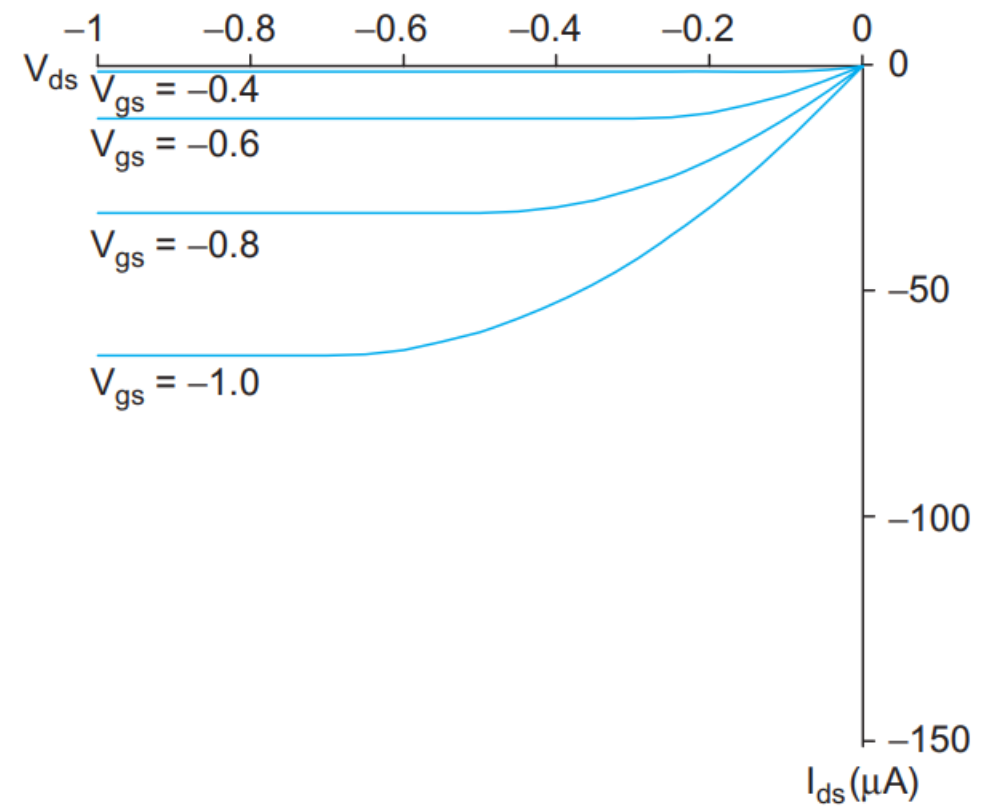
**SOLUTION:** We first calculate  $\beta$ .

$$\beta = \mu C_{\text{ox}} \frac{W}{L} = \left( 80 \frac{\text{cm}^2}{\text{V}\cdot\text{s}} \right) \left( \frac{3.9 \times 8.85 \times 10^{-14} \frac{\text{F}}{\text{cm}}}{10.5 \times 10^{-8} \text{cm}} \right) \left( \frac{W}{L} \right) = 262 \frac{W}{L} \frac{\text{A}}{\text{V}^2} \quad (2.11)$$

# CMOS Output Characteristics



(a)



(b)

**FIGURE 2.7** I-V characteristics of ideal  $4/2 \lambda$  (a) nMOS and (b) pMOS transistors

# Reading and Book

---

- Textbook can be downloaded online “CMOS VLSI Design by Weste and Harris, 4<sup>th</sup> Edition”
- Readings from starting portion of Chapter 2