VLSI Design EE 523
Spring 2026

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Lecture 4

Topics for lecture 4

- Simple working models for NMOS and PMOS as switch
- Pass Transistor Logic using simple CMOS models
  - Difference between restoring and non restoring logic
  - Pass transistor characteristics, Vtn and |Vtp|
- Making 2:1 MUX using pass transistor logic
- Design of a CMOS Tri-state inverter
- Make a D-Latch using pass transistor logic
- Introducing MOS transistor theory – applying voltages at gate, drain, source and bulk terminals and observe different effects and regions
- Study different logic designs made from Pass transistors and Transmission gates

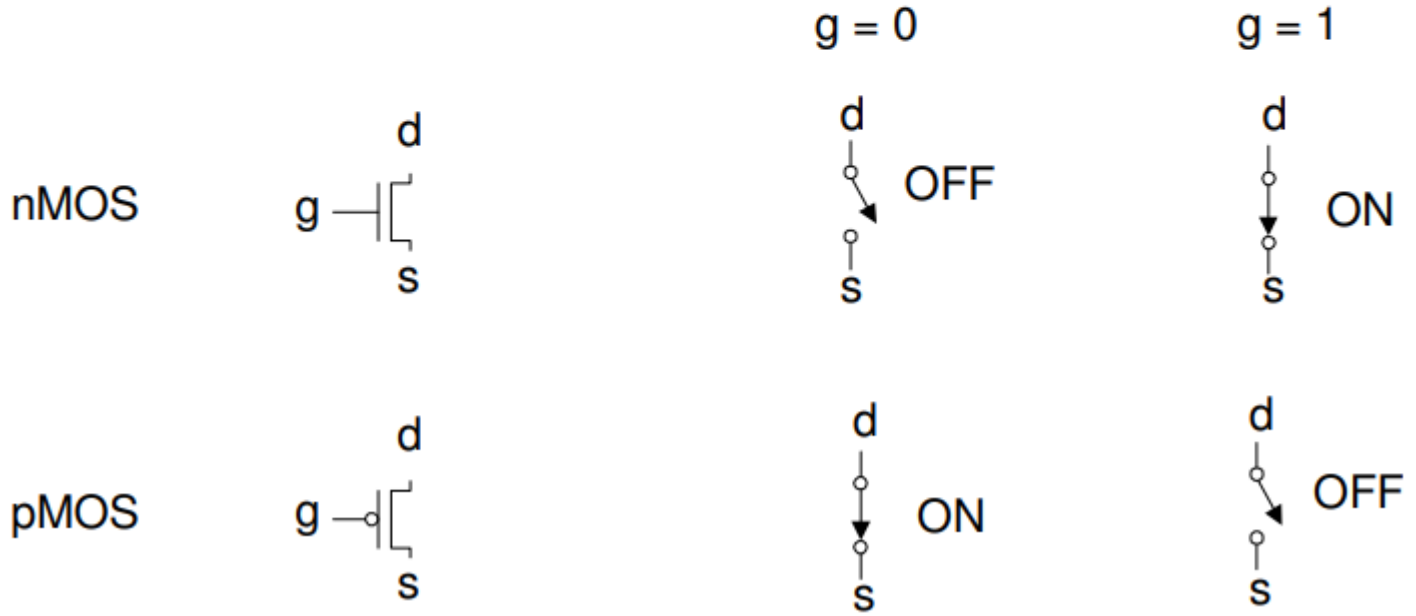
Quiz Next week

Basic Switching Operation of MOSFET

Transistors as Switches

- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain

What is CMOS?
vs
NMOS or PMOS



Weak and Strong Switches

- **nMOS** transistors are great at passing a strong 0 but not so good at passing a 1, which becomes weak.
- On the other hand, **pMOS** transistors are good at passing a strong 1 but pass a weak 0.
- When you combine nMOS and pMOS transistors in parallel, you get a **transmission gate**. This gate can pass both 0s and 1s effectively, making it a better switch for signals.

Strong 1 and Weak 1

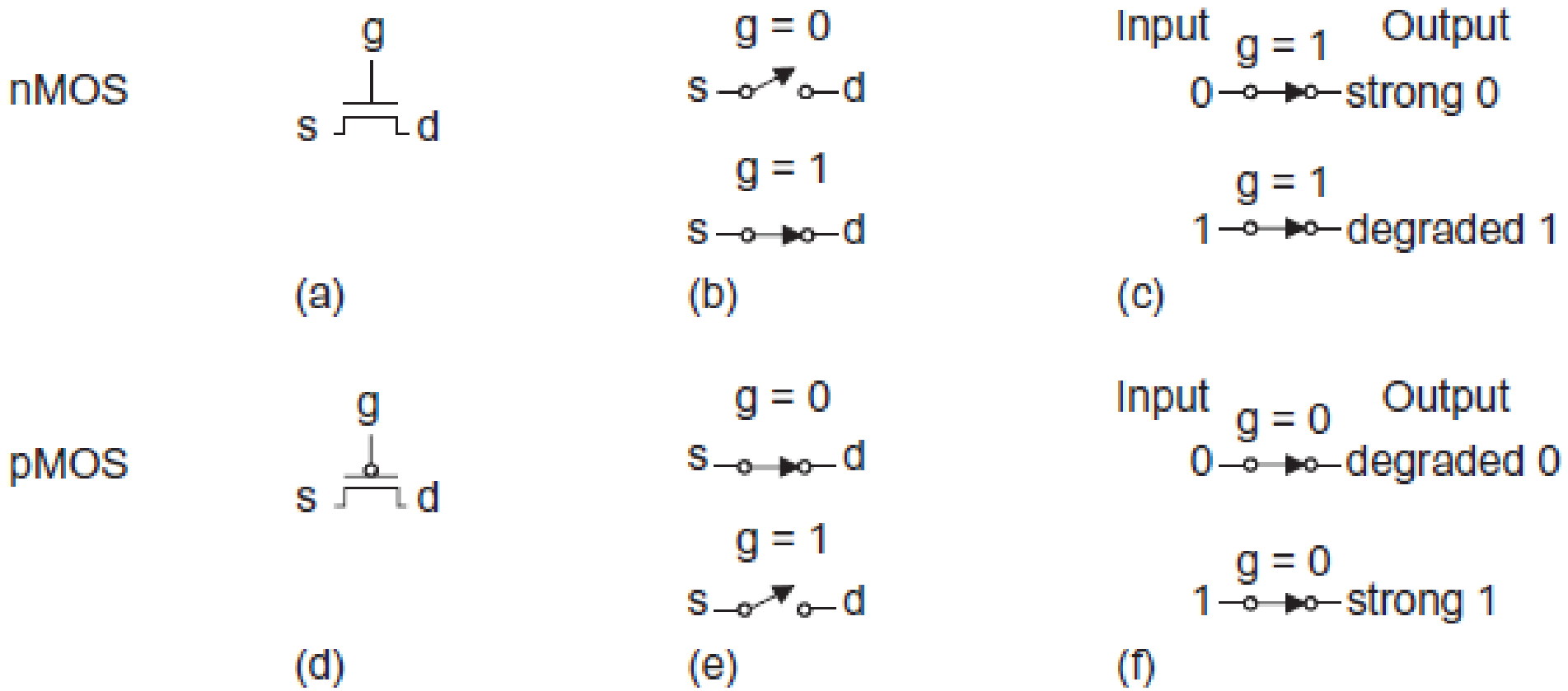


FIGURE 1.20 Pass transistor strong and degraded outputs

Signal Strength in CMOS technology

- **NMOS Transistors**
- nMOS devices are great for **pulling a signal low**. When you apply a high voltage to the gate of an nMOS transistor, it allows current to flow from the drain to the source, effectively grounding the output and driving the signal towards 0V (logic LOW). This makes nMOS transistors strong pull-down devices. However, when you try to use nMOS to pass a HIGH signal, it tends to degrade slightly due to the **threshold voltage drop**, which is why the output might not reach the full supply voltage.
- **PMOS Transistors**
- pMOS transistors, on the other hand, are excellent at **pulling a signal high**. When you apply a low voltage to the gate, it creates a conductive path for current to flow from the source to the drain, driving the output to the supply voltage (logic HIGH). This makes pMOS transistors strong pull-up devices. However, similar to nMOS, pMOS transistors are weaker at passing a LOW signal, as there can be a slight voltage drop.
- **Signal Strength in CMOS Logic**
- When we combine nMOS and pMOS in complementary pairs, as we do in CMOS technology, you get the best of both worlds. The nMOS transistor handles the pull-down operation efficiently, and the pMOS transistor handles the pull-up operation. This ensures strong signal levels for both HIGH and LOW states without significant degradation, which is why CMOS circuits are so reliable and widely used.

Pass Transistor Switches using NMOS and PMOS

1.4.6 Pass Transistors and Transmission Gates

From textbook

The *strength* of a signal is measured by how closely it approximates an ideal voltage source. In general, the stronger a signal, the more current it can source or sink. The power supplies, or *rails*, (V_{DD} and GND) are the source of the strongest 1s and 0s.

An nMOS transistor is an almost perfect switch when passing a 0 and thus we say it passes a *strong* 0. However, the nMOS transistor is imperfect at passing a 1. The high voltage level is somewhat less than V_{DD}, as will be explained in Section 2.5.4. We say it passes a *degraded* or *weak* 1. A pMOS transistor again has the opposite behavior, passing strong 1s but degraded 0s. The transistor symbols and behaviors are summarized in Figure 1.20 with *g*, *s*, and *d* indicating gate, source, and drain.

When an nMOS or pMOS is used alone as an imperfect switch, we sometimes call it a *pass transistor*. By combining an nMOS and a pMOS transistor in parallel (Figure 1.21(a)), we obtain a switch that turns on when a 1 is applied to *g* (Figure 1.21(b)) in which 0s and 1s are both passed in an acceptable fashion (Figure 1.21(c)). We term this a *transmission gate* or *pass gate*. In a circuit where only a 0 or a 1 has to be passed, the appropriate transistor (n or p) can be deleted, reverting to a single nMOS or pMOS device.

Series Connected MOSFET Switches

10.2 Series Connection of MOSFETs

Consider the series connection of MOSFETs shown in Fig. 10.11. The input to this circuit, *I*, is passed to the output *Z* when *A* = *B* = *C* = *VDD* = logic "1." If *A*, *B*, or *C* is at ground (= logic "0"), the output is in the high-impedance state, that is, not a logic 0 or 1. Series connection of MOSFETs occurs frequently in CMOS digital circuit design. In this section, we will analyze the DC and transient behavior of a string of MOSFETs.

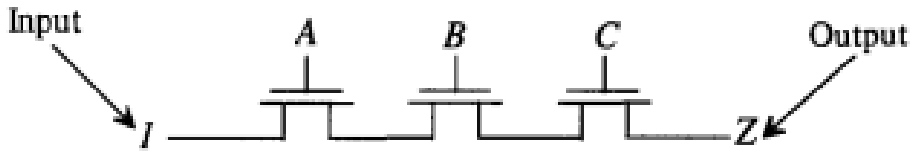


Figure 10.11 Series connection of MOSFETs.

10.2.1 DC Behavior of Series-Connected MOSFETs

To illustrate the DC operation of series-connected MOSFETs, let's use Fig. 10.11 and assume that *I* = *A* = *B* = *C* = *VDD* (see Fig. 10.12a). The maximum voltage we can pass from M1 to M2 is $VDD - V_{thn}$ (with body effect). In fact, this is the largest voltage we can pass to the output *Z* without turning any of the MOSFETs off. Now consider Fig. 10.12b where the input is now a logic low (= 0 V). The output Z can swing all the way down to zero. In other words, the n-channel string passes 0V well and *VDD* with a threshold drop.

Some Examples of Pass-Transistor Logic

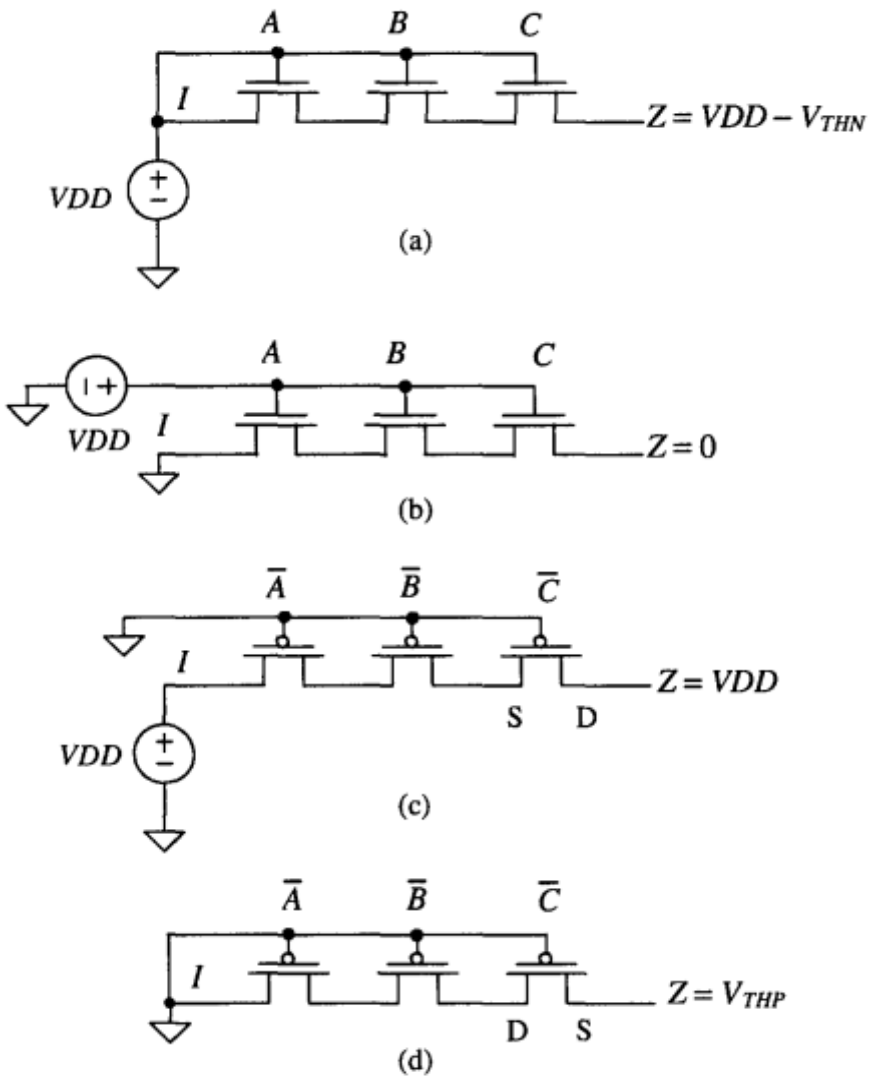


Figure 10.12 DC operation of series-connected MOSFETs.

assume that $I = A = B = C = VDD$ (see Fig. 10.12a). The maximum voltage we can pass from M1 to M2 is $VDD - V_{THN}$ (with body effect). In fact, this is the largest voltage we can pass to the output Z without turning any of the MOSFETs off. Now consider Fig.

A p-channel series connection of MOSFETs is shown in Figs. 10.12c and d. Notice that A, B, and C are now active low; that is, the p-channel MOSFETs turn on when $\overline{A} = \overline{B} = \overline{C} = 0$. The p-channel string can pass a logic high without a voltage drop. However, the minimum voltage through a p-channel string is V_{THP} (with body effect).

Switch Behaviour of MOSFET

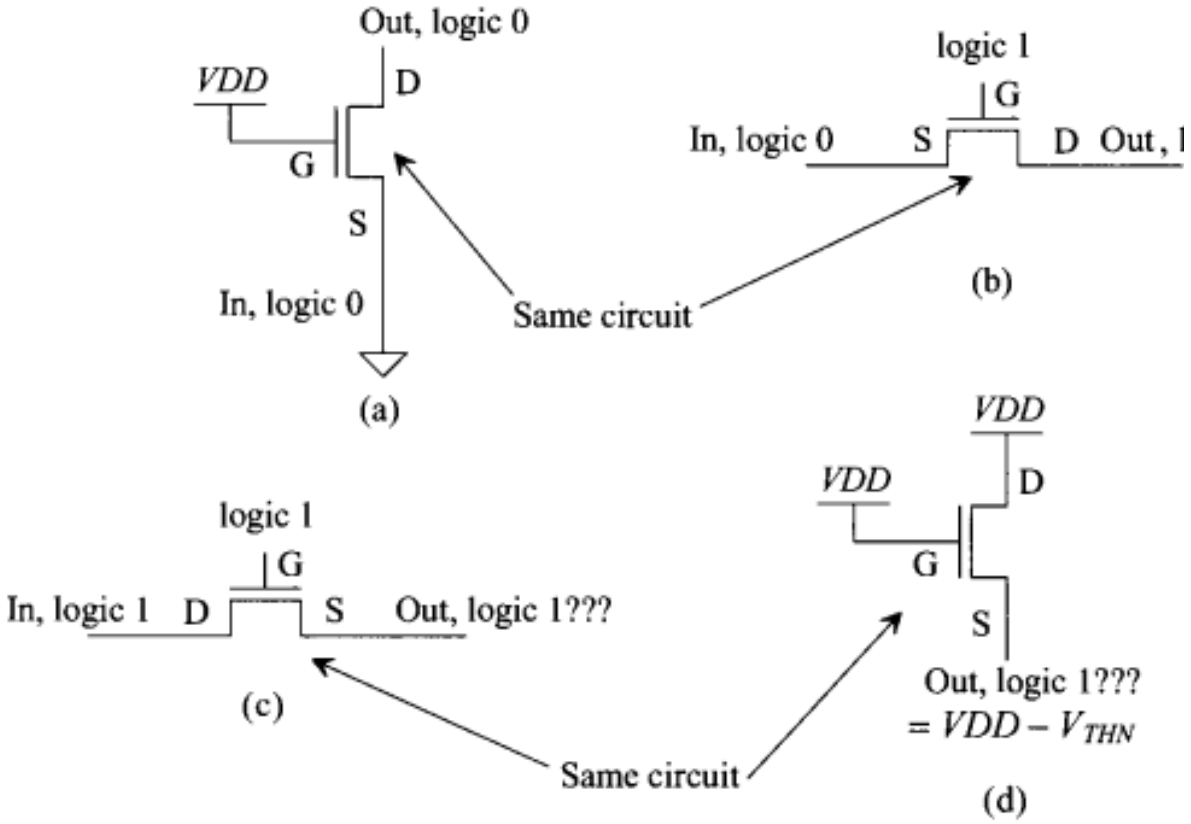


Figure 10.13 Using the NMOS switch as a pass gate.

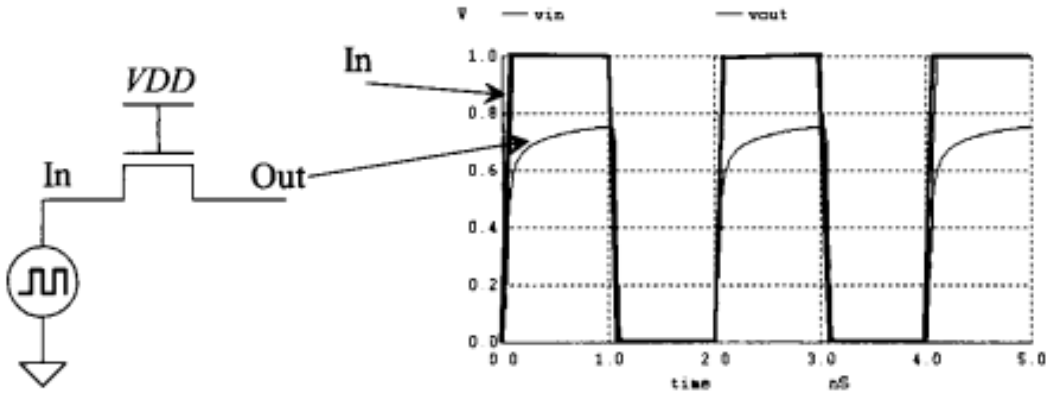


Figure 10.14 The input and output of an NMOS pass gate.

The Pass Transistor Gate

The PMOS Pass Gate

Figure 10.15 shows the operation of the PMOS PG. As expected the operation of the PMOS device is complementary to the NMOS's operation. The PMOS device turns on when its gate is driven to ground. If its gate is pulled to *VDD*, the device is off (and the output is in the Hi-Z state). In Fig. 10.15a the PG is passing a "1" to the output (the V_{SG} is *VDD*). In (b) a "0" is passed to the output. However, noting that the terminals we label drain and source are swapped from (a), the output only gets pulled down to V_{THP}. In (b) the V_{SG} of the MOSFET is V_{THP}. It can be said that a *PMOS PG is good at passing a 1 and bad at passing a 0.*

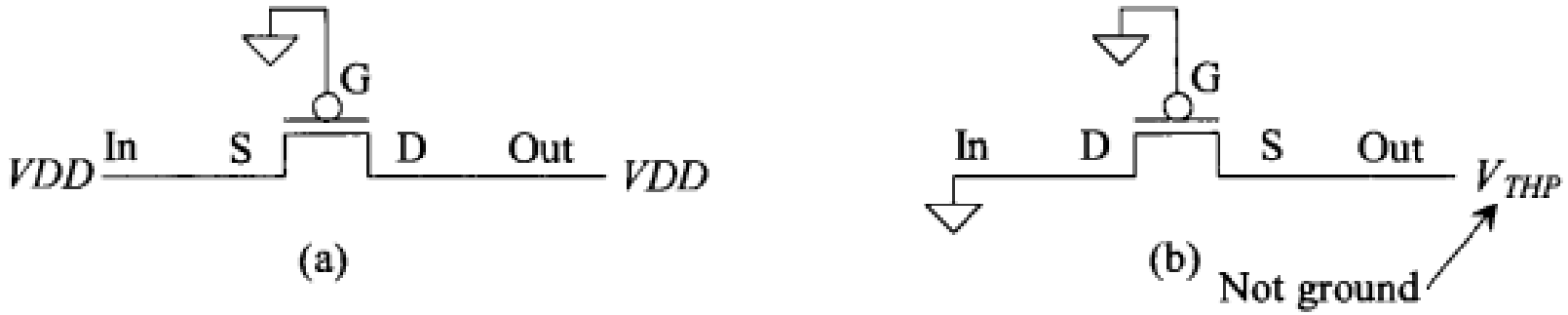


Figure 10.15 How the PMOS device does not pass a logic 0 well.

NMOS Threshold drop in Pass Transistor

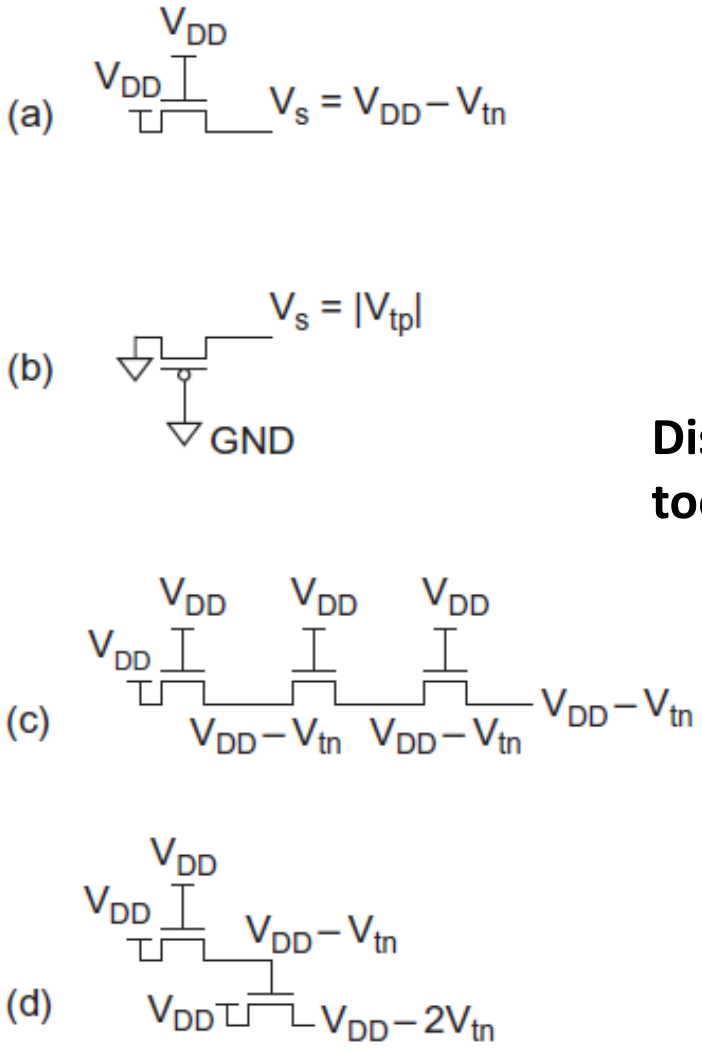


FIGURE 2.31 Pass transistor threshold drops

Discuss later too

2.5.4 Pass Transistor DC Characteristics

Recall from Section 1.4.6 that nMOS transistors pass '0's well but 1s poorly. We are now ready to better define "poorly." Figure 2.31(a) shows an nMOS transistor with the gate and drain tied to V_{DD}. Imagine that the source is initially at $V_s = 0$. $V_{gs} > V_{tn}$, so the transistor is ON and current flows. If the voltage on the source rises to $V_s = V_{DD} - V_{tn}$, V_{gs} falls to V_{tn} and the transistor cuts itself OFF. Therefore, nMOS transistors attempting to pass a 1 never pull the source above $V_{DD} - V_{tn}$.[10] This loss is sometimes called a *threshold drop*.

Moreover, when the source of the nMOS transistor rises, V_{sb} becomes nonzero. As described in Section 2.4.3.1, this nonzero source to body potential introduces the body effect that increases the threshold voltage. Using the data from the example in that section, a pass transistor driven with $V_{DD} = 1$ V would produce an output of only 0.65 V, potentially violating the noise margins of the next stage.

Similarly, pMOS transistors pass 1s well but 0s poorly. If the pMOS source drops below $|V_{tp}|$, the transistor cuts off. Hence, pMOS transistors only pull down to within a threshold above GND, as shown in Figure 2.31(b).

NMOS vs PMOS as Switch

Example 10.3
Estimate the output voltages in the circuits seen in Fig. 10.16.

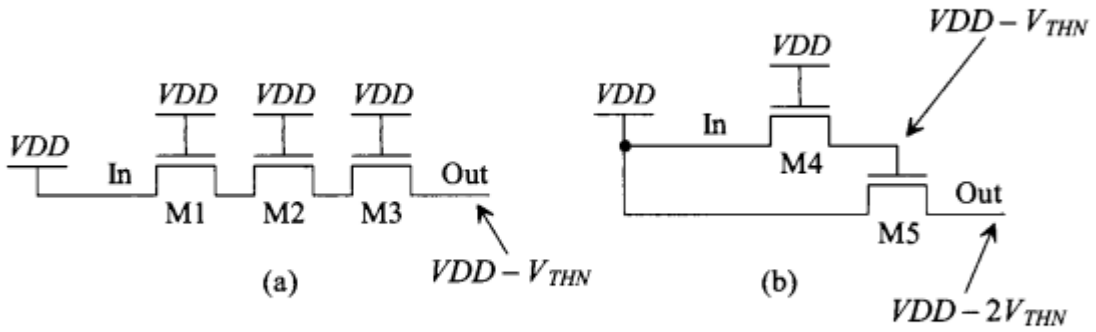


Figure 10.16 Circuits used in Ex. 10.3.

In (a) the output of M1 is $VDD - V_{THN}$. To keep M2 and M3 on, each MOSFET must have a V_{GS} of at least V_{THN}. Because the gates of M2 and M3 are already at VDD, the output of M1 gets passed through M2 and M3 to the final output of the circuit. As seen in the figure this means the overall output is also $VDD - V_{THN}$. We only take one threshold voltage hit.

In (b) the output of the M4 is $VDD - V_{THN}$. This is the gate voltage of M5. For M5 to be on its gate-source voltage must be greater than V_{THN}. The final output is then $VDD - 2V_{THN}$ (again as seen in the figure). ■

Strong 1 and Weak 1

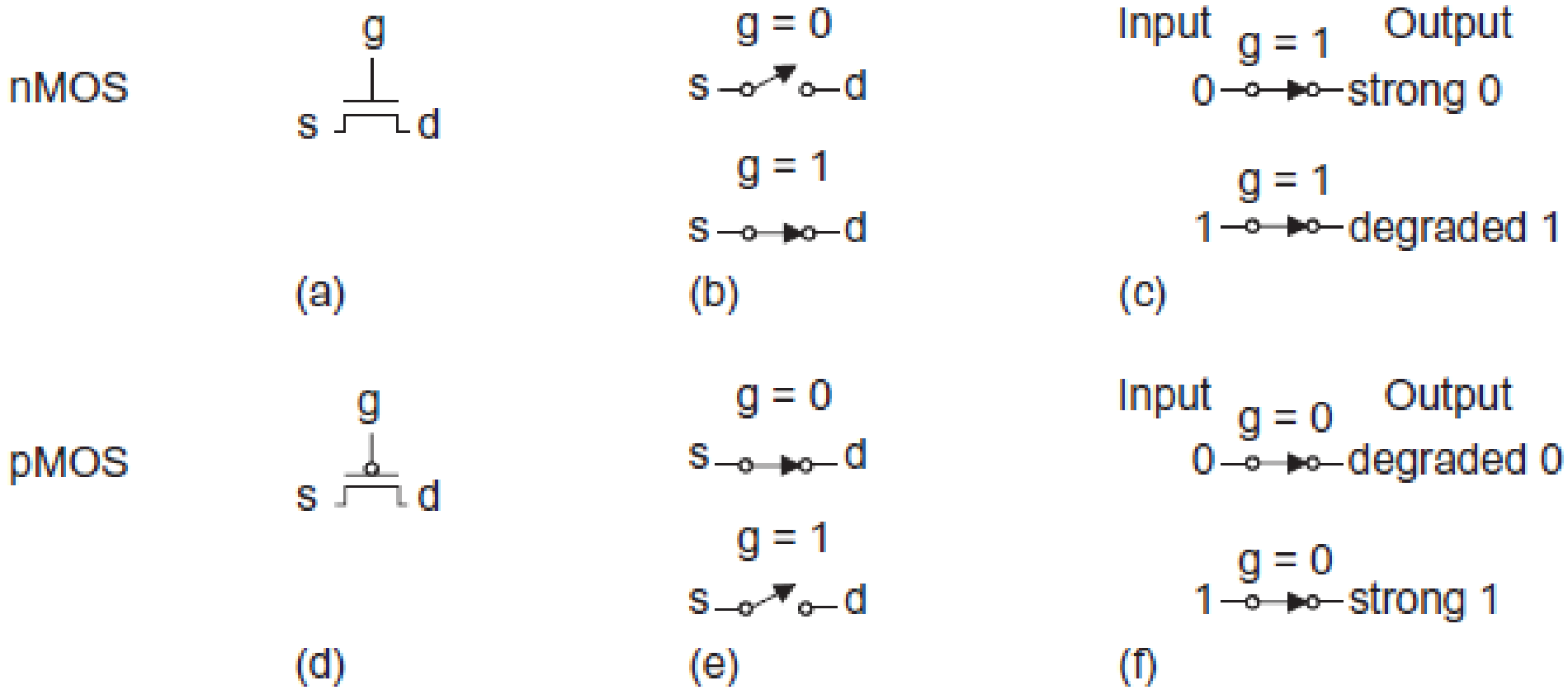


FIGURE 1.20 Pass transistor strong and degraded outputs

Logic Circuits made from CMOS Switches

Examples of Simple CMOS Gates

Reading and Book

- Textbook can be downloaded online “CMOS VLSI Design by Weste and Harris, 4th Edition”
- Readings from Chapter 1, starting portion of Chapter 2
- For quiz, prepare from chapter 1 and lecture notes