VLSI Design EE 523
Spring 2026

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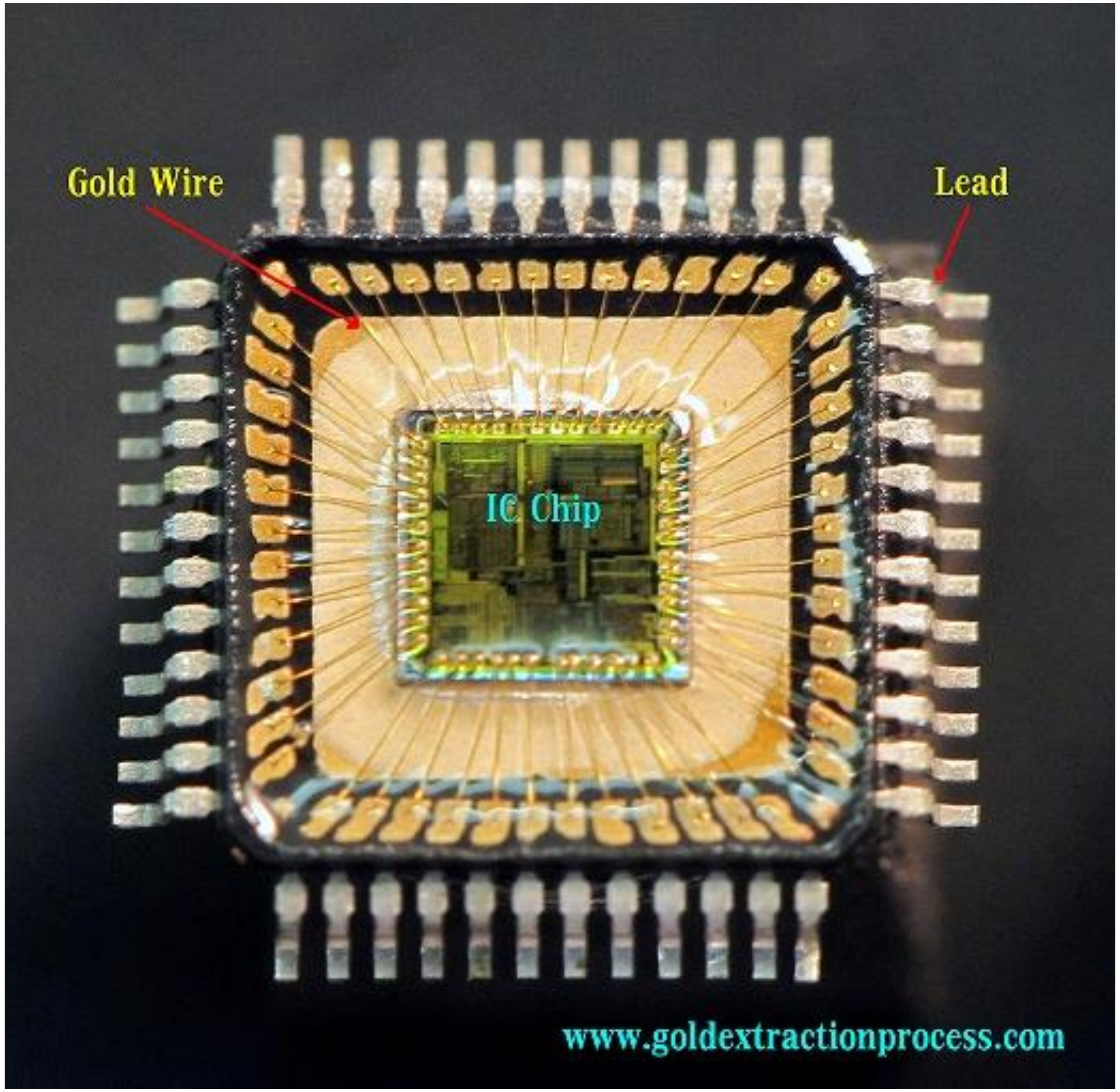
Lecture 1

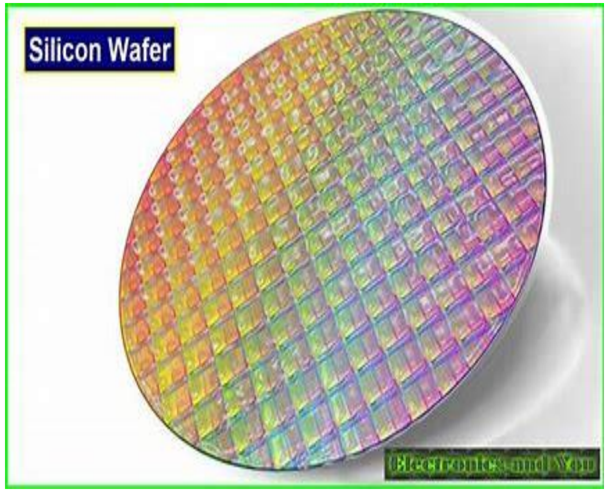
Topics of Introductory Lecture

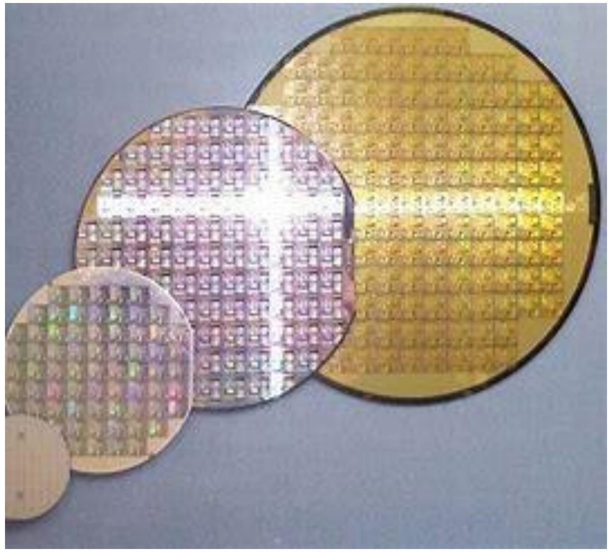
- What are VLSI Chips?
- Invention of Transistors and Integrated Circuits
- How are VLSI Chips are Fabricated?
- Scaling and Integration – Shrinking Feature Size
- Future Trends in VLSI Design and Fabrication

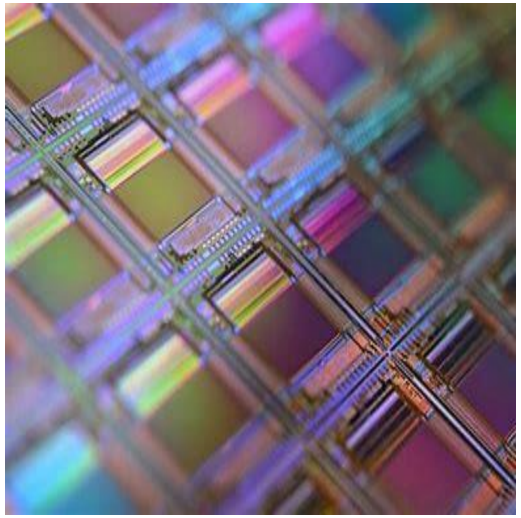
How do VLSI Chips look like – commercial package

How do VLSI Chips look like – research chip



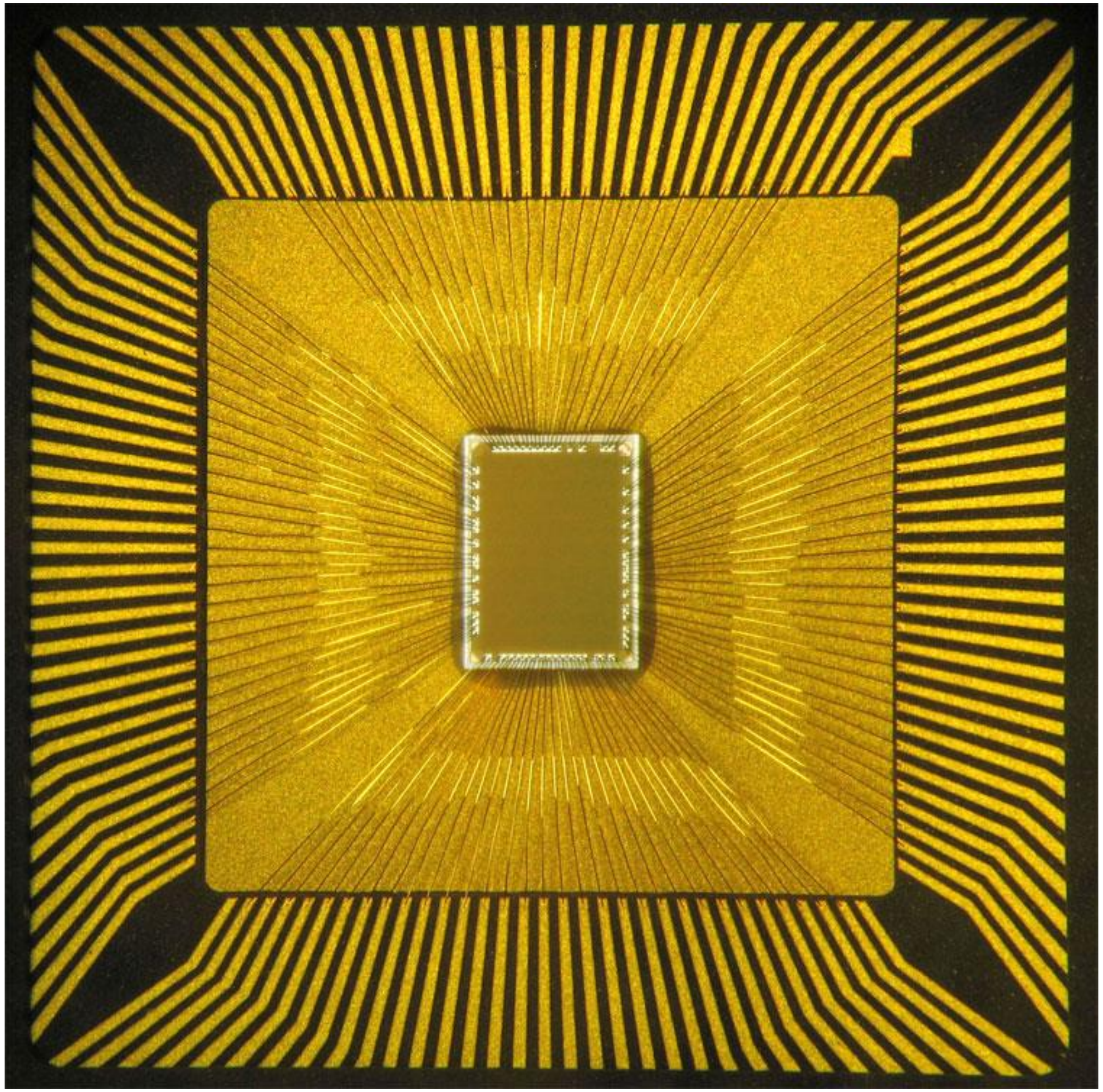




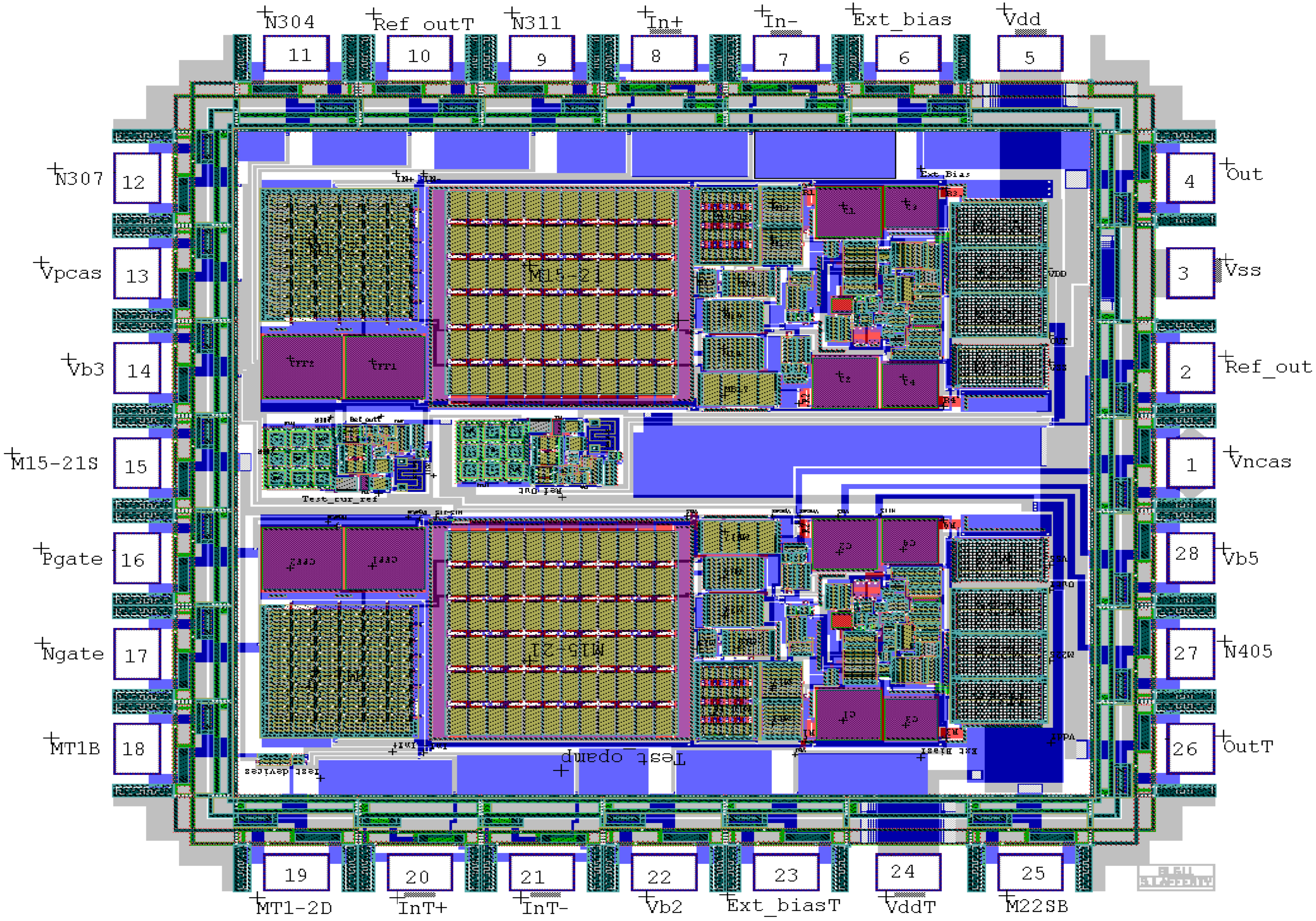


Wafer

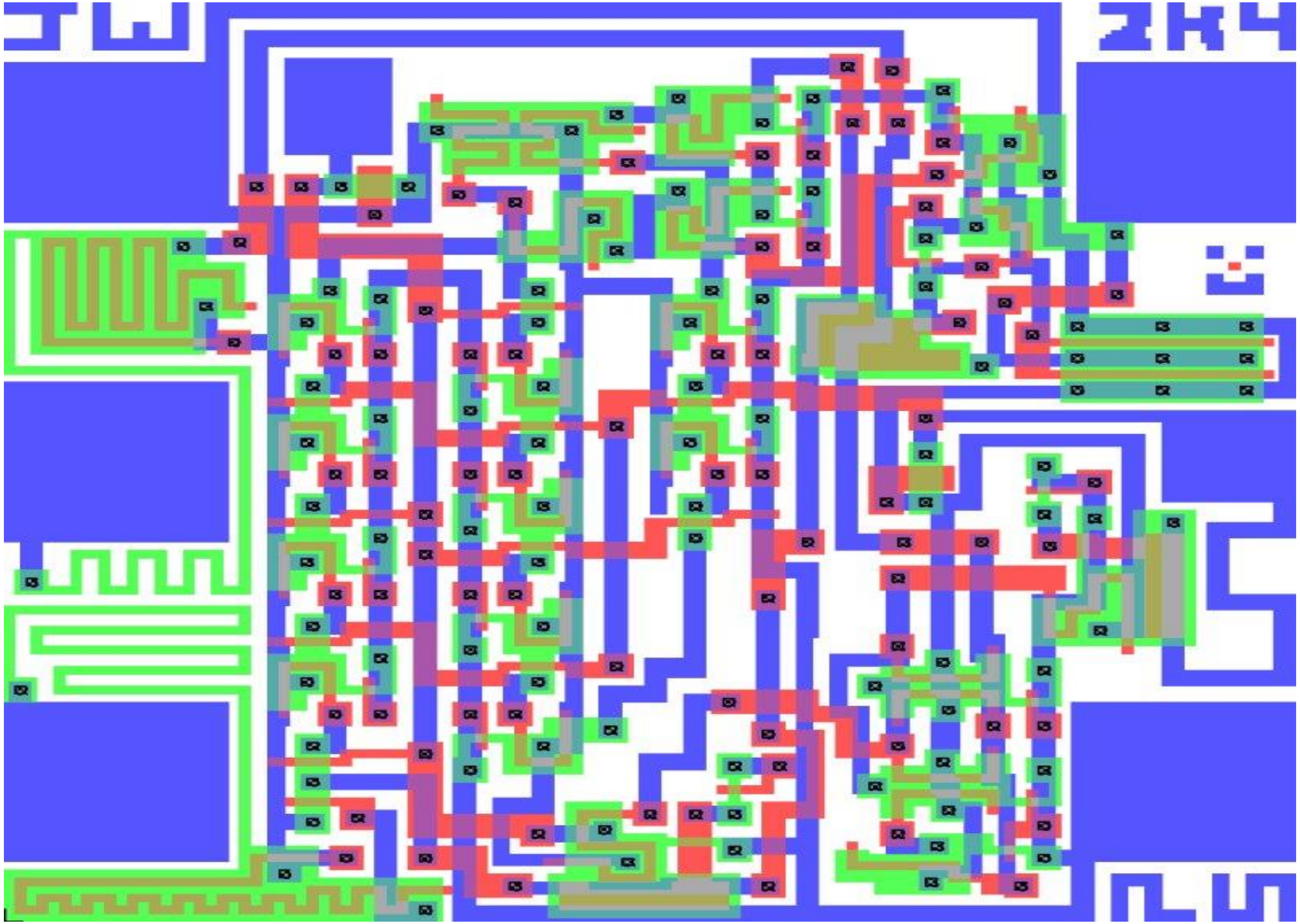
How do VLSI Chips look like – experimental chip



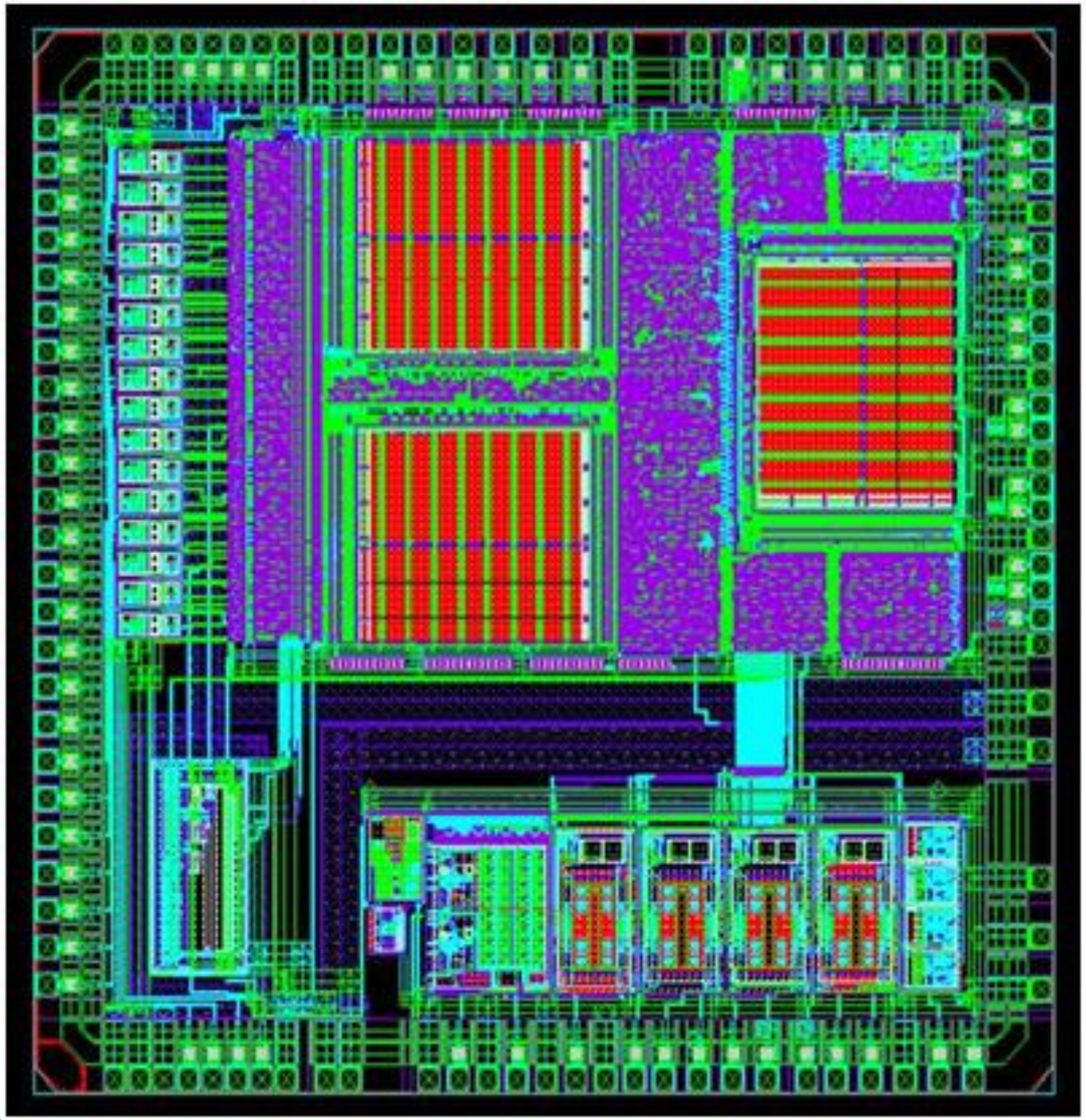
How do VLSI Chips look like – placement and routing



How do VLSI Chips look like – constituent modules and cores



Chips from inside – complex system on chip



Semiconductors in USA

Largest Semiconductor Companies in US: 2025 List

Rank	Company Name	Revenue (USD Billion)	Headquarters	Specialization
1	NVIDIA	130.5	Santa Clara, California	Graphics Processing Units (GPUs), AI Computing
2	Intel Corporation	53.10	Santa Clara, California	Microprocessors, Chipsets, Cloud Computing Solutions
3	Broadcom	51.57	Palo Alto, California	Semiconductors for Networking, Broadband, Wireless
4	QUALCOMM	40.70	San Diego, California	Mobile Chipsets, Wireless Technology
5	Micron Technology	25.1	Boise, Idaho	Memory and Storage Solutions
6	Applied Materials	27.18	Santa Clara, CA	Semiconductor Manufacturing Equipment
7	AMD	25.79	Santa Clara, CA	Microprocessors, GPUs, Server Processors
8	Lam Research	16.21	Fremont, CA	Semiconductor Processing Equipment
9	Texas Instruments	15.64	Dallas, TX	Analog and Embedded Processing Chips
10	KLA	10.85	Milpitas, CA	Process Control and Yield Management Systems

Niche areas of Semiconductor Companies in USA

Top USA Semiconductor Manufacturing Companies

The following are the top 10 U.S. semiconductor manufacturing companies in 2025, along with their core advantages and technological highlights:

Company	Main Focus	Key Strengths
Intel Corporation	CPUs, Foundry Services, AI Chips	Complete production process; 18A node; U.S. foundry services
Nvidia Corporation	GPUs, AI Chips, Data Centers	Leading AI computing platform; H100 chip; CUDA ecosystem
Broadcom Inc.	Communication Chips (Wi-Fi, Bluetooth, Ethernet)	Strong fabless model; partners with top foundries
QUALCOMM Incorporated	Smartphone Chips, 5G, IoT, Automotive	Snapdragon platform; wireless connectivity leader
Texas Instruments Incorporated	Analog Chips, Embedded Processors	Own fabs; cost-efficient; reliable global supplier
Micron Technology Inc.	Memory and Storage Chips (DRAM, NAND)	Independent DRAM & NAND development; low-power innovation
Advanced Micro Devices (AMD)	CPUs, GPUs, High-performance Computing	Modular design; advanced foundry use; rapid market growth
Analog Devices Inc. (ADI)	Analog and Mixed-signal Chips	High precision; acquired Maxim; strong in analog ICs
GlobalFoundries, Inc.	Semiconductor Foundry Services	Customization, mature nodes, U.S.-based foundry
Lam Research	Semiconductor Manufacturing Equipment	Key process tools (etch, clean, deposit); innovation-driven

Fact Sheet: Restoring American Semiconductor Manufacturing Leadership Through an Agreement on Trade & Investment with Taiwan

Semiconductor Industry

ADVANCING AMERICA FIRST TRADE AND INVESTMENT: Today, the American Institute in Taiwan and the Taipei Economic and Cultural Representative Office in the United States signed a historic trade deal that will drive a massive reshoring of America's semiconductor sector. This unprecedented commitment will strengthen U.S. economic resilience, create high-paying jobs, and bolster national security.

FOR IMMEDIATE RELEASE

Thursday, January 15, 2026

Office of Public

https://www.commerce.gov/news/fact-sheets/2026/01/fact-sheet-restoring-american-semiconductor-manufacturing-leadership

232 duties.

SECURING AMERICA'S SEMICONDUCTOR SUPPLY CHAIN: Semiconductors are vital for America's industrial, technological, and military strength. Yet, for far too long, the Washington establishment allowed this strategic sector to move offshore, leaving the United States dependent on foreign manufacturers and brittle global supply chains. The Trump Administration is committed to reversing that trend.

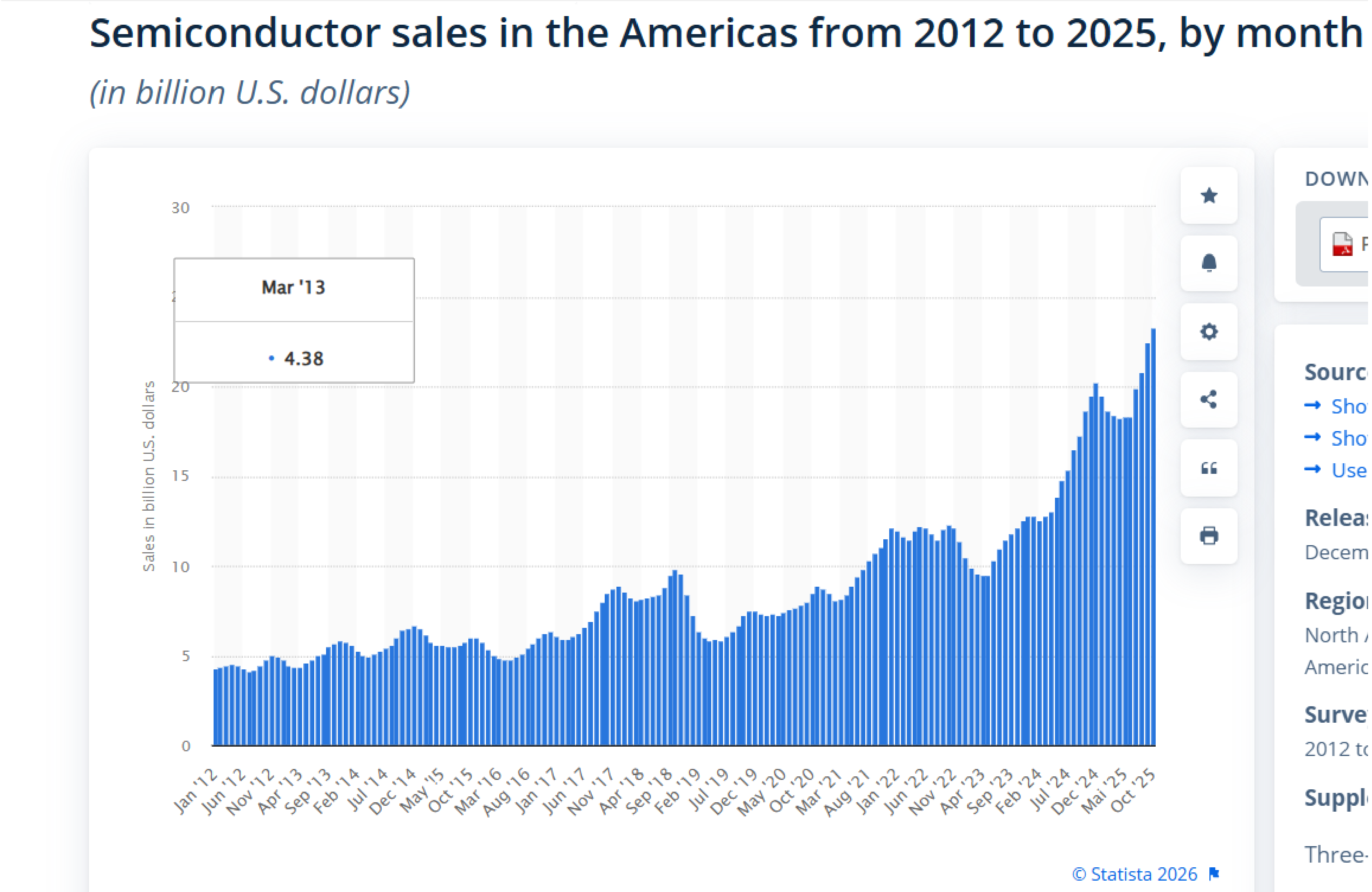
- Semiconductors are the foundational components of modern technology. They power computing systems in products ranging from smartphones and automobiles to telecommunications equipment and military weapons.
- The U.S. share of global wafer fabrication declined sharply from 37 percent in 1990 to less than 10 percent in 2024. Today, most semiconductors are fabricated in East Asia due to foreign industrial policies that distort global trade flows.
- President Trump's Commerce Department is leading a whole-of-government effort to revitalize American semiconductor manufacturing.

BUREAUS AND OFFICES

International Trade Administration

Semiconductor Sales Data in USA

https://www.statista.com/statistics/217462/semiconductor-sales-in-the-americas-since-2011-by-month/



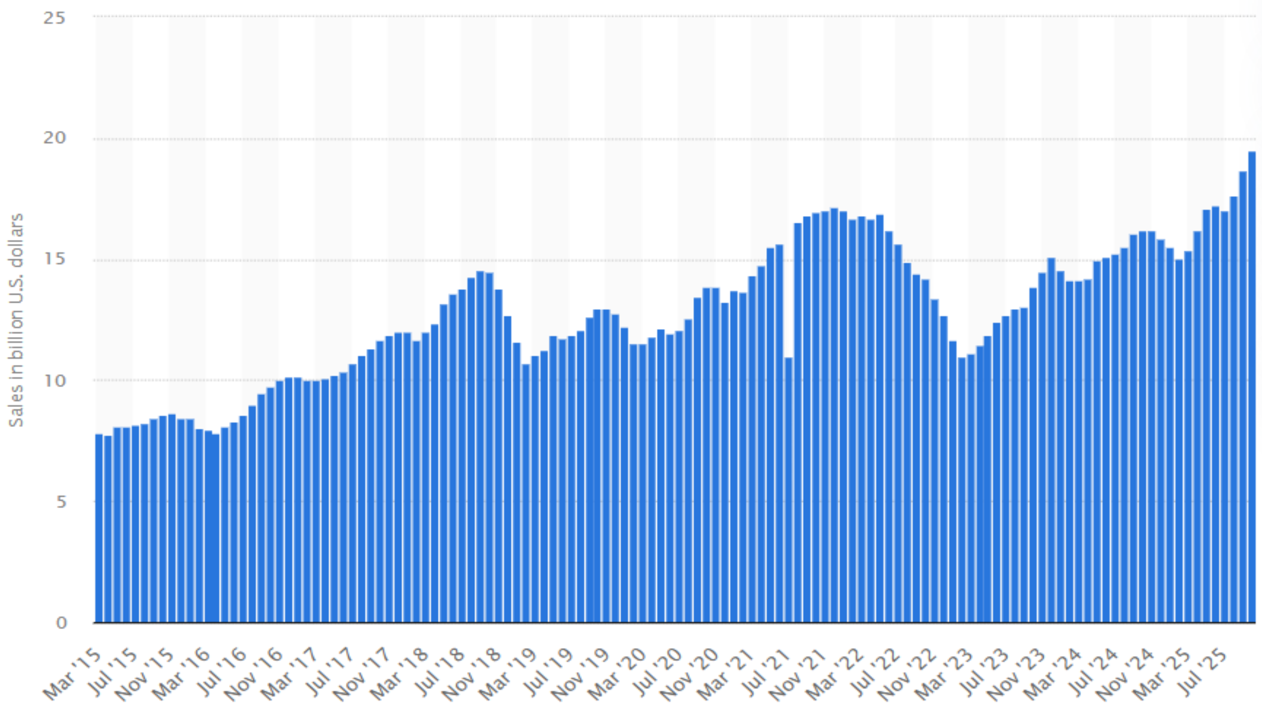
Semiconductor Sales Data in China

https://www.statista.com/statistics/1086441/semiconductor-sales-china/

Technology & Telecommunications › Hardware

Semiconductor sales in China from 2015 to 2025, by month

(in billion U.S. dollars)



Status of CHIPS Act (2022 – 2032)

https://www.semiconductors.org/2024-state-of-the-u-s-semiconductor-industry/

In the decade following CHIPS enactment (2022 to 2032), the United States is projected to more than triple its semiconductor manufacturing capacity — the highest rate of growth in the world during that period — according to a May 2024 SIA-Boston Consulting Group report. The report also forecasts the U.S. will grow its share of advanced (less than 10nm) chip manufacturing to 28% of global capacity by 2032 and capture 28% of total global capital expenditures (capex) from 2024 to 2032. By comparison, in the absence of the CHIPS Act, the report estimates the U.S. would have captured only 9% of global capex by 2032.

US Chips Act 2022 – What's for industry?

WHAT'S IN IT FOR THE INDUSTRY?

The CHIPS and Science Act of 2022 injects $280 billion into US research, innovation, and manufacturing over the next five years. The "CHIPS" name reflects the priority given to the semiconductor industry with $52.7 billion of dedicated semiconductor spending, including $39 billion in grants and a 25% tax credit for on-shore US manufacturing.

The policy goal is to increase the US manufacturing share of this crucial technology after years of decline – from 37% in 1990 to 12% (relative to the US semiconductor consumption of 34%) – mostly due to more aggressive industry investments by other governments. The Act also reflects the urgency of addressing semiconductor shortages and cyclic dynamics which trouble multiple industries (for example, automotive manufacturing) and impede US economic growth.

The global semiconductor market is forecast to be worth $633 billion in 2022, up 13.9% from 2021 of which the US market share is about half. After a period of low profitability in the early 2000s, semiconductor companies have seen their economic profits grow strongly into the double digits since the late 2010s. The industry outlook is strong with no sign of demand abating, which raises the question of why large industry subsidies are needed.

China Semiconductor Status

https://focus.cbbc.org/chinas-semiconductor-sector/

CHINA'S SEMICONDUCTOR INDUSTRY IS RAPIDLY ADVANCING, DRIVEN BY STATE-BACKED INITIATIVES AND DOMESTIC INNOVATION

China's semiconductor sector has emerged as a cornerstone of its technological ambition, propelled by significant government investment and a strategic push for self-sufficiency. In 2024, the industry was valued at £134.2 billion, with projections indicating a compound annual growth rate (CAGR) of 7.8% from 2025 to 2034, potentially reaching £283.7 billion by 2034. This growth reflects China's determination to reduce reliance on foreign chips, which accounted for 83% of its £185.5 billion chip consumption in 2020, and to establish itself as a global leader in semiconductor innovation. The sector's rapid development, driven by advancements in artificial intelligence (AI), 5G, and electric vehicles (EVs), positions China at the forefront of the global tech race, though geopolitical tensions and technological gaps present significant challenges.

US Technology Direction

https://techhq.com/2024/02/us-aims-for-chip-supremacy-from-zero-to-20-by-2030/

T_HQ technology and business

Insights Latest Topics TechForge Sites Even

SUPPLY CHAIN

US aims for chip supremacy: From zero to 20% by 2030

Raimondo acknowledges that the lack of chip manufacturing has undermined US tech leadership in AI and innovation.

28 February 2024

USA chip design vision

The majority of semiconductors worldwide, including the most advanced chips with the highest component densities, are made in Taiwan by various foundries including the world's largest, TSMC, which counts Apple, Qualcomm, Nvidia, and other technology companies among its clients. The next largest manufacturer is Samsung in South Korea.

Both TSMC and Samsung plan to build foundries in the United States: a $12 billion Arizona fab for TSMC and a $17 billion fab in Texas for Samsung. Intel has started construction of its new $20 billion Arizona fabs and will also build new fabs in Ohio for an initial $20 billion investment which could grow to $100 billion making it the world's largest chip plant. Several of these investments were contingent on the CHIPs Act passing. And just after the Act was signed by President Biden, Micron announced a $40 billion investment in US memory chip manufacturing.

China's 1 Trillion Yuan for chip industry

China is struggling in the battle for advanced semiconductor technology. With President Joe Biden's most recent round of export controls on semiconductors, China is now facing an increasingly urgent challenge as it seeks to ramp up its domestic innovative capacity for high-end chips. Yet at the turn of the new year, Bloomberg reported that China is pausing its investment in its domestic semiconductor industry, most likely due to financial strain from COVID-19, ineffective subsidies, and corruption. This came only two weeks after the news that Beijing is preparing a one-trillion yuan ($145.61 billion) incentive package to beef up the competitiveness of its indigenous chip industry.

While the gigantic cost of the COVID-19 lockdown necessitates some belt-tightening, Beijing's rollback of its massive chip investment should not be surprising. It is no secret that China's previous efforts to improve its chip innovation did not bear much fruit. The reason for the lack of success, however, is more than the technical challenge of independently developing one of the most sophisticated products in the world. Rather, the political and institutional factors in China's science and technology innovation base are also impediments to its desired success in reaching a chip breakthrough. Not only does China's top-down model of innovation overshadow its domestic ecosystem of chip development, but the absence of effective oversight and the perverse incentives from the indiscrete dispersion of local government funding together render prospects for chip innovation grim.

China Chip Fund

CHINA

China is planning its biggest state-backed chip fund yet

The Big Fund plans a new state-backed investment fund to raise US$40 billion for China's semiconductor sector.

6 September 2023

Global race for computer chips

The Global Race for Computer Chips

- **CHIPS Act Grants:** The Biden administration awarded its first federal grants from a government program aimed at shoring up U.S. manufacturing of critical semiconductors to BAE Systems and Microchip Technology.
- **A Renewed Crackdown:** The United States is trying to slow China's progress toward technological advances that could help its military by clamping down on sales of chip-making machinery to China.
- **A Geopolitical Test:** South Korea, a critical U.S. ally with a semiconductor sector that depends on China, is wedged between Beijing and Washington in their trade war over technology.
- **A Chip-Making Superpower?:** India, seizing on the world's desire to reduce reliance on China, wants to build a semiconductor manufacturing industry from the ground up, an ambition as unlikely as it is bold.

Rising global interest

Global Semiconductor Funding Round-up - April 2023

Date Published: 14th April 2023

The last few months have seen a surge of public funding in the semiconductor industry, as governments attempt to expedite recovery from the supply chain crisis and increase self-sufficiency. A growing number of countries see their semiconductor ecosystems as central to economic evolution, sustainability and in some cases security.

In the first of our Global Semiconductor Funding Round-ups, we highlight key government investments and initiatives in the chip sector over the 12 months from March 2022 to March 2023:

United Kingdom

The new Department for Science, Innovation and Technology (DSIT) has set out the UK Science and Technology Framework. The plan commits £370 million to five technologies, including semiconductors, by the year 2030. However, this hasn't stopped UK-based chipmakers from calling for additional funding to prevent the country from falling behind in the global market.

United States

In April 2022, the US signed the CHIPS and Science Act into law. The act will invest $250 billion (£227 billion), boosting fab capacity, catalysing R&D and supporting the creation of regional hi-tech hubs. The funding will also go towards expanding the country's science, technology, engineering, and math (STEM) workforce.

Over $52.7 billion (£42 billion) of this funding has been allocated to "American semiconductor research, development, manufacturing, and workforce development". This includes $2 billion (£1.6 billion) for legacy chips used in automobiles and defence systems. The US car manufacturing sector was one of the worst affected by the chip shortage that followed the Covid-19 pandemic.

European Union

The EU has moved to address its own regional chip deficit. Adopted in December 2022, the EU Chips Act aims to strengthen the EU's competitiveness in semiconductor technologies. The EU's share of the microchip market currently stands at 10%, and the Act aims to increase its portion of the global market to at least 20% by the year 2030.

Europe's semiconductor ecosystem will be strengthened by the mobilisation of €43 billion (£37 billion) in public and private investments. Its three main pillars of action are 1) the public-private partnership Chips for Europe; 2) a new framework for attracting investment; and 3) a mechanism to monitor and coordinate supply in crisis situations.

China

According to reports, China's government was working on a support package of more than 1 trillion yen (£114 billion) for its semiconductor industry. However, this plan is said to have stalled in recent weeks, with funds being paused or redirected.

Taiwan

Taiwan accounts for 92% of the world's most advanced (nodes below 10 nanometres) semiconductor capacity. Despite this strong market position, the country's chip sector still faces the stern challenges of a talent shortage and global competition. A recent report revealed Taiwan's National Science and Technology Council has plans for a raft of new funding to progress "talent training and research funding", including an upgrade of facilities by the year 2035.

Spain

In addition to the EU's commitment, individual member states have been investing in their own chip sectors. Spain announces plans to inject €11 billion (£9.6 billion), emphasising the "global geostrategic importance" of semiconductors and a determination that Spain "will not lose the race to the most advanced technology". The funding, which was announced in April 2022, will be partly financed by the EU's pandemic recovery fund.

India

A $10 billion (£8 billion) incentive plan for chip and display production that was originally outlined in December 2021 is still taking shape. India recently signed a memorandum of understanding with the US as it aims to become a key player in the global supply chain.

Europe Chip Vision

https://www.consilium.europa.eu/en/policies/eu-chips-industry/

What is the European Chips Act?

The European Chips Act establishes a framework of measures to **strengthen Europe's semiconductor ecosystem**.

The Chips Act is based on three pillars:

- the **'Chips for Europe Initiative'** that supports large-scale technological capacity building and innovation
- a framework that ensures security of supply and resilience by **attracting increased investment**
- a monitoring and **crisis response system** that will anticipate shortages and coordinate actions in crisis situations

The Chips for Europe Initiative is expected to mobilise **€43 billion** in public and private investments, **with €3.3 billion** coming **from the European budget**.

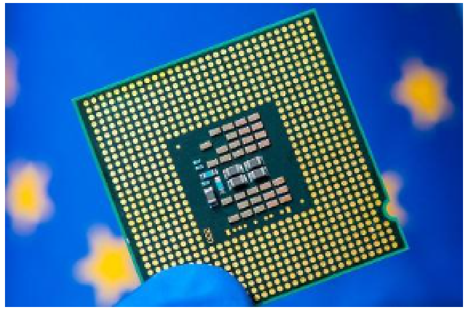
On 25 July 2023, the Council gave its final approval to the 'Chips Act'.

→ Chips Act: Council gives its final approval (press release, 25 July 2023)

EU

https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en

European Chips Act



The European Chips Act will bolster Europe's competitiveness and resilience in semiconductor technologies and applications, and help achieve both the digital and green transition. It will do this by strengthening Europe's technological leadership in the field. Following the approval by the Parliament and the Council, the regulation entered into force on 21 September 2023.

PAGE CONTENTS

The need for EU action

Chips are strategic assets for key industrial value chains. With the digital transformation, new markets for the chip industry are emerging such as highly automated cars, cloud, Internet of Things, connectivity, space, defence and supercomputers.

1 trillion

microchips were manufactured around the world in 2020

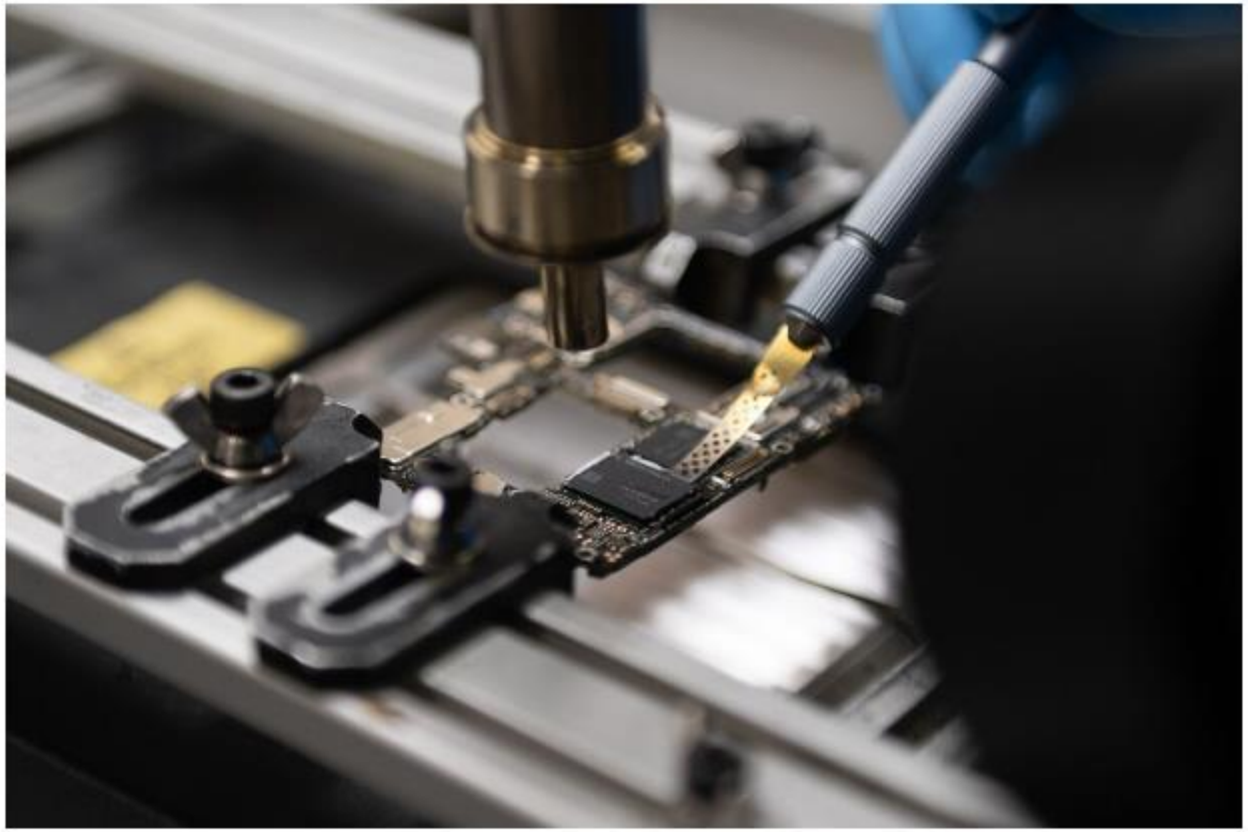
10%

EU's share of the global microchips market

China's vision

China's Investing Billions to Win the Semiconductor Battle

More on a chip breakthrough that shocked the world.



A specialist removes a Kirin 9000s chip fabricated in China by Semiconductor Manufacturing International Corp. (SMIC) from a Huawei Technologies Co. Mate 60 Pro smartphone. *Photographer: James Park/Bloomberg*

Birth of Transistor Device

First transistor in 1947

2.2. History of The Development of IC

With all the theories of semiconductors, at Bell Labs, John Bardeen, Walter Brattain and William Shockley invented the first transistor successfully on December 23, 1947 [5]. This transistor is point-contact transistor, which based on the theories of electric field effects in solid state materials [6]. The design goal of this transistor was to be a substitute of vacuum tubes, and it did achieve the goal. Although the first transistor was ugly, it could work properly in a circuit, with smaller size and less power than vacuum tubes. It became the inflection point of computer, because transistors are smaller than vacuum tube or relay, which were the main components of computer before. The First Transistor Invented at Bell Labs was shown in Figure 1.

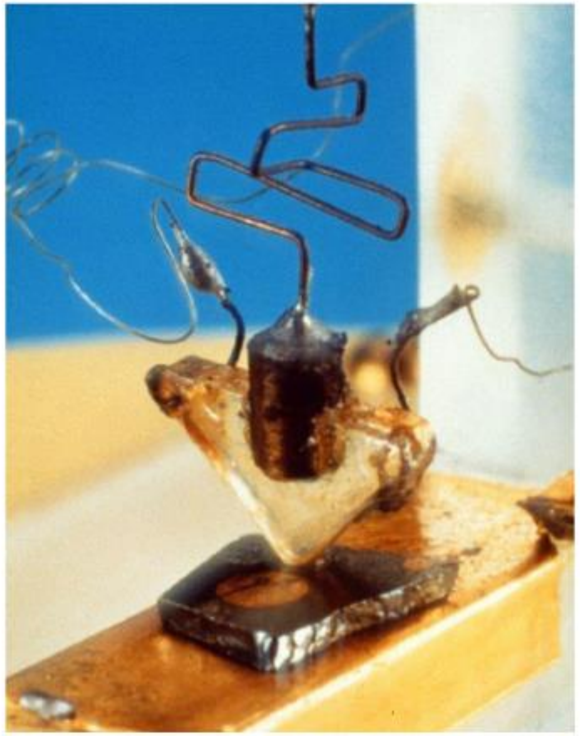


Figure 1. The First Transistor Invented at Bell Labs

First integrated circuit in 1958

FIGURE 1.1
The first transistor, invented at Bell Laboratories in 1947. (Courtesy of Lucent Technologies Inc.)

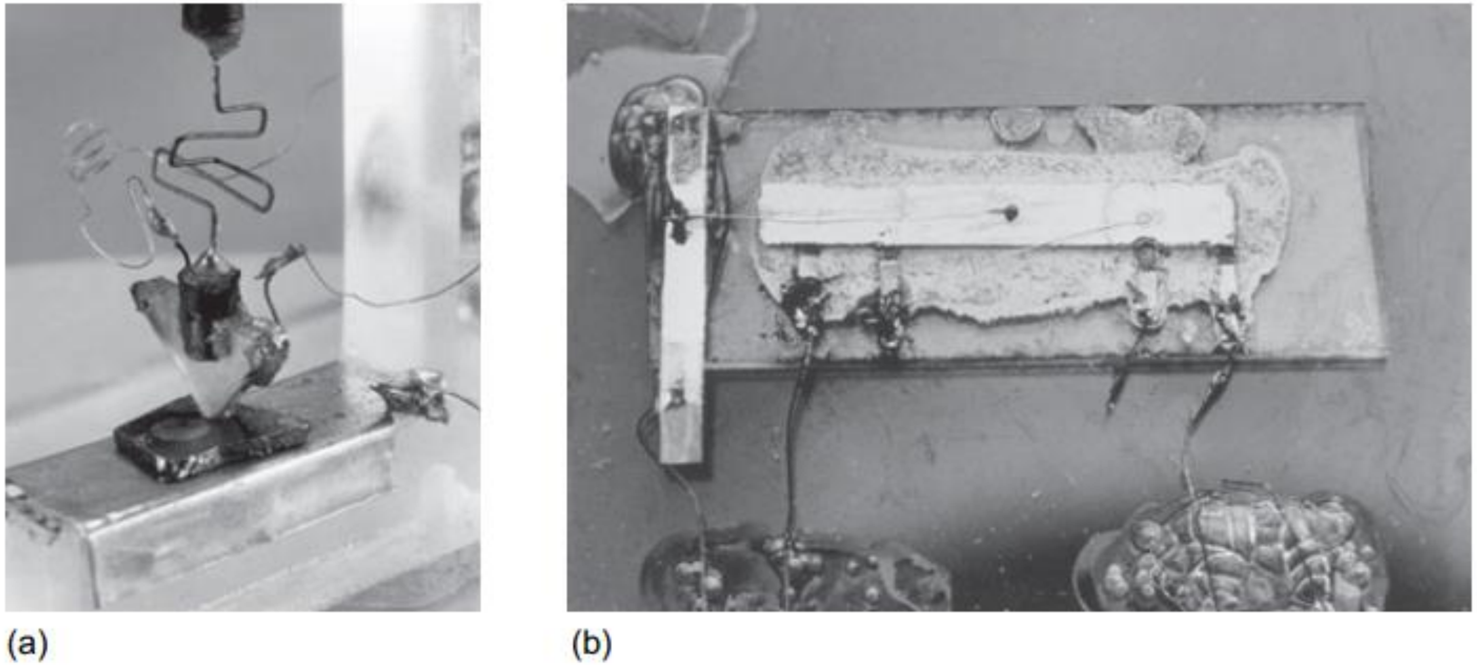


FIGURE 1.2 (a) First transistor (Property of AT&T Archives. Reprinted with permission of AT&T.) and (b) first integrated circuit (Courtesy of Texas Instruments.)

The first microprocessor – Intel 4004

Intel 4004 Microprocessor was the first commercial microprocessor produced by Intel Corporation. It was originally a product for Busicom Corp., aimed to be part of an electronic calculator. It is a 3mm x 4mm, with 16 pins and 2,300 transistors. The max CPU clock rate is 740-750 kHz. Figure 4 shows this component that has similar performance as ENIAC, which is a computing machine that occupied a whole room.

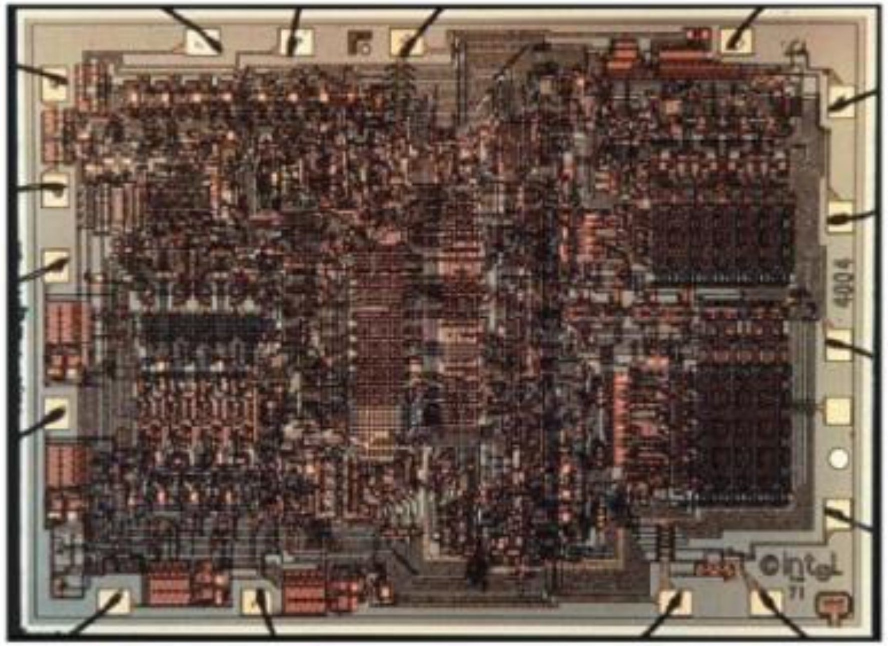
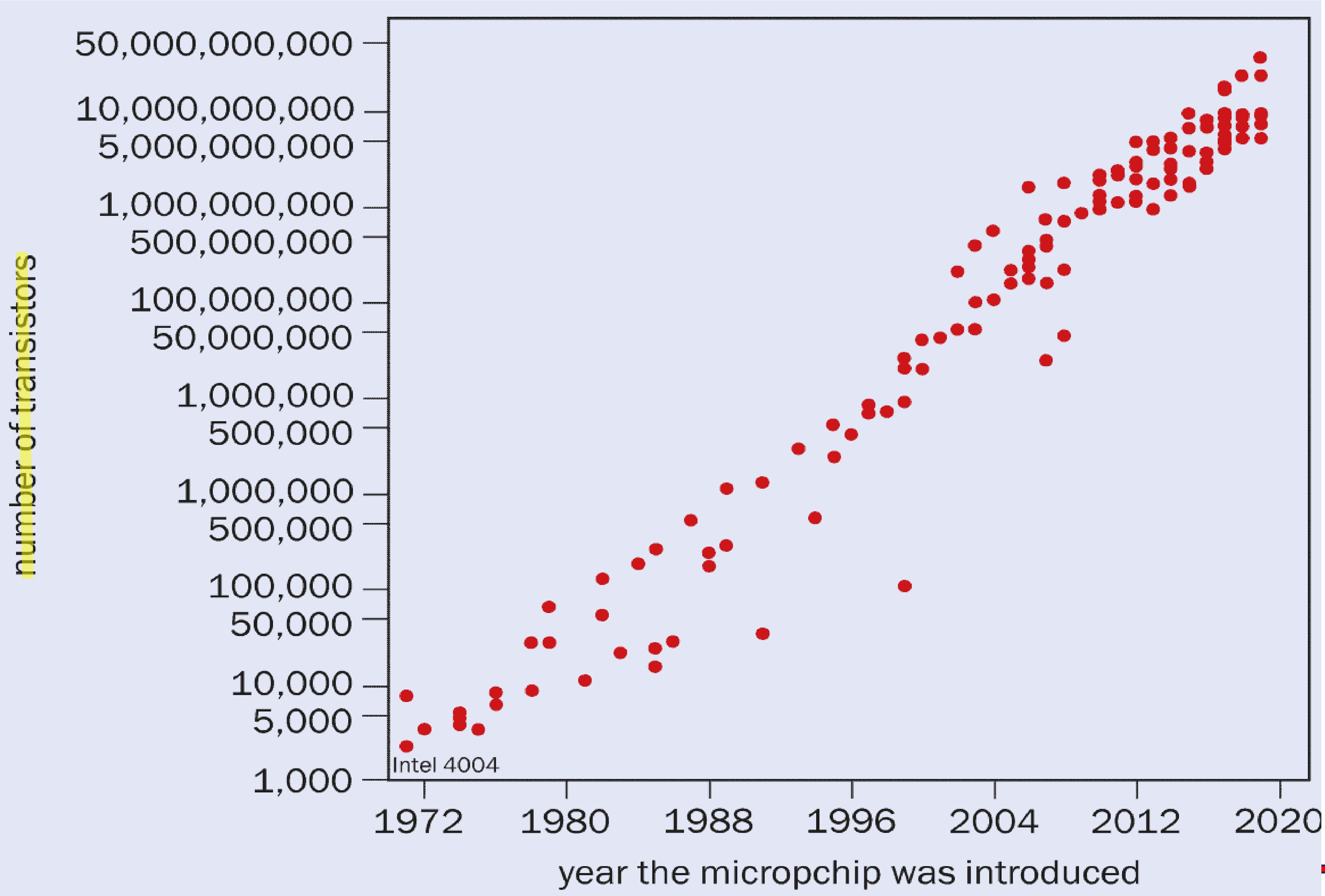
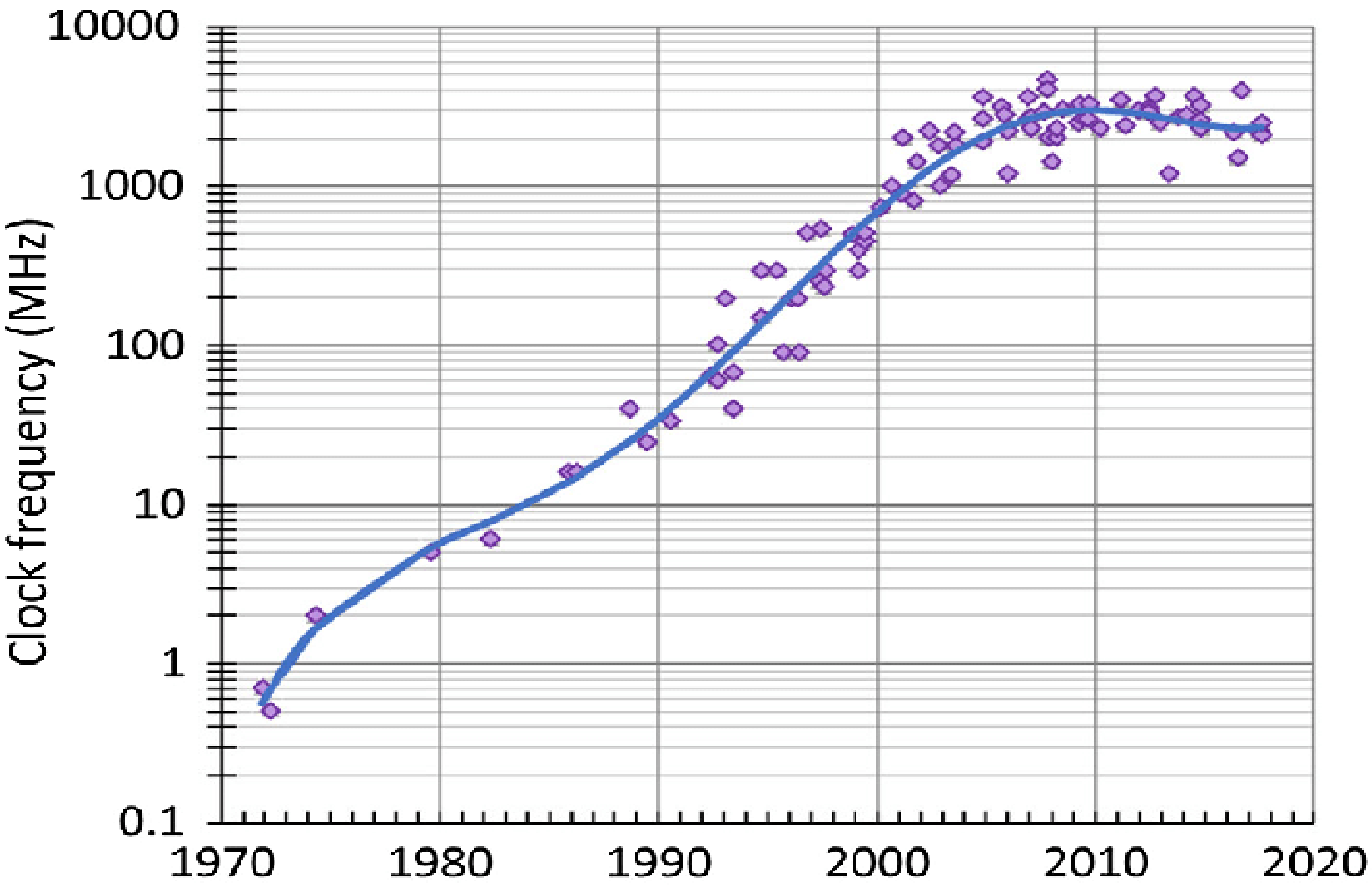


Figure 4. The Structure of Intel 4004

Number of transistors in modern chips



Clock Frequency of modern chips



VLSI Fabrication technology over the years

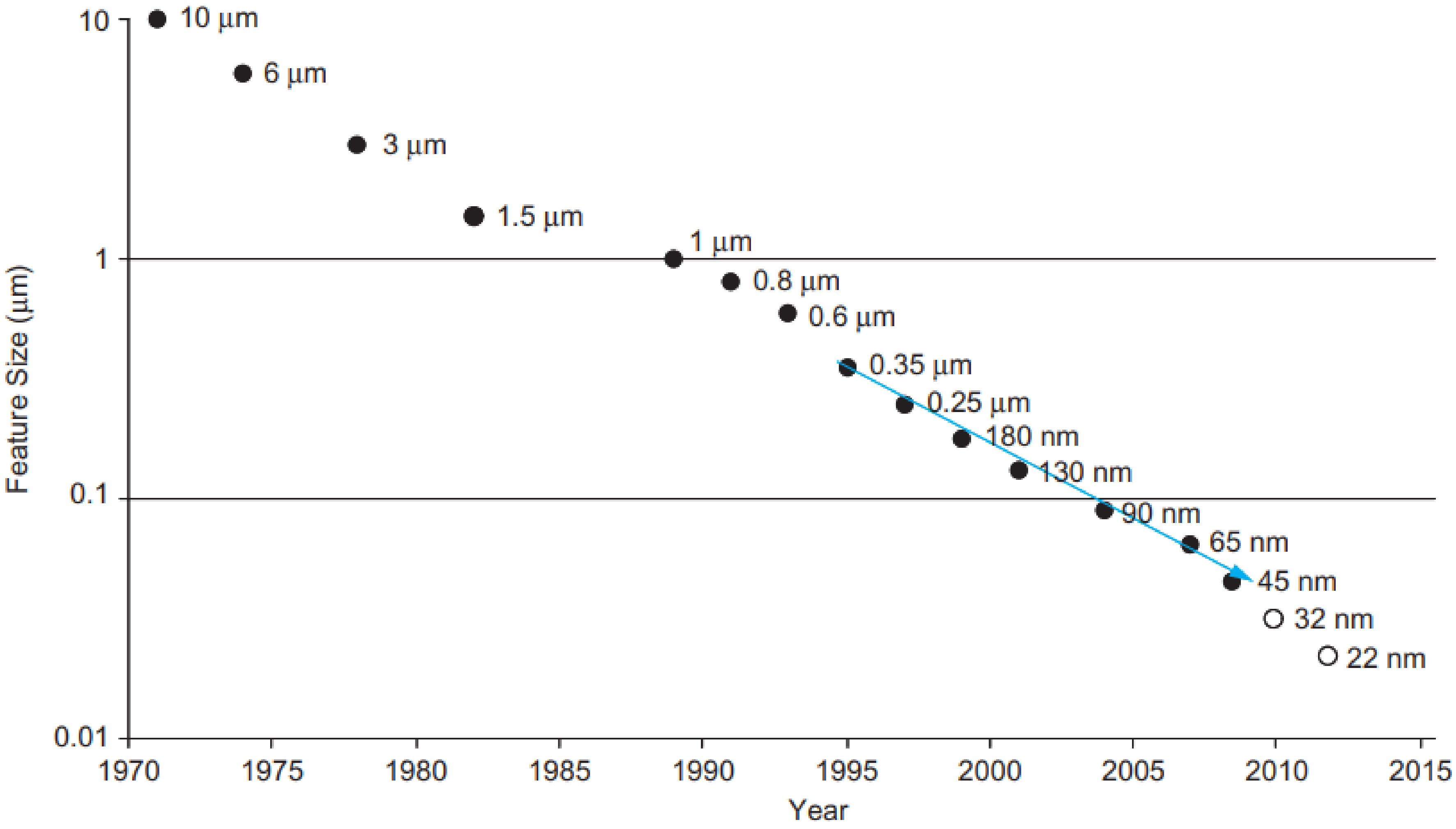


FIGURE 1.6 Process generations. Future predictions from [SIA2007].

Some latest chip examples

How Complex are todays Designs?

Chip	IBM $P9^{TM}$	IBM $P10^{TM}$
Technology	14nm FinFET SOI	7nm Bulk
No. Cores	24	60
Area(mm^2)	695	602
No. of Transistors (B)	8	18
No. Vias(B)	-	110
No. Metal Levels	17	18
M1-M3 Pitch (nm)	64	-
M4-M5 Pitch (nm)	80	-
MX-M(X-1) (nm)	2400	2160

1. C. Gonzalez et al., "3.1 POWER9: A processor family optimized for cognitive computing with 25Gb/s accelerator links and 16Gb/s PCIe Gen4," 2017 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, 2017, pp. 50-51.

2. R. M. Rao et al., "POWER10: A 16-Core SMT8 Server Processor With 2TB/s Off-Chip Bandwidth in 7nm Technology," 2022 IEEE International Solid- State Circuits Conference (ISSCC), 2022, pp. 48-50, doi: 10.1109/ISSCC42614.2022.9731594.

Semiconductor Technology and its Future

Periodic table – semiconductor, p and n type

DONOR IMPURITIES

VERSUS

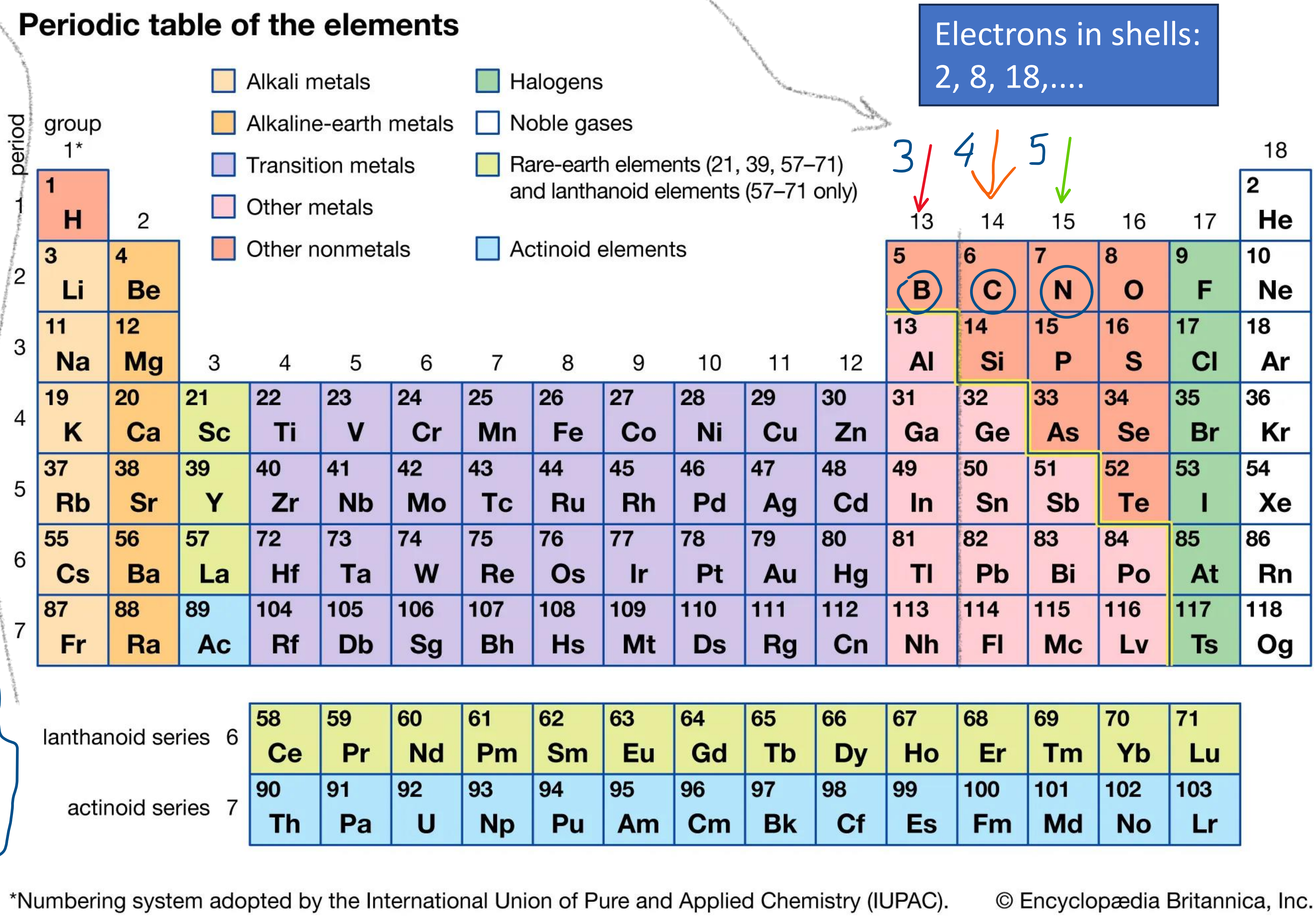
ACCEPTOR IMPURITIES

Visit www.PEDIAA.com

DONOR IMPURITIES	ACCEPTOR IMPURITIES
Donor impurities inject extra electrons into the semiconductor crystal lattice due to having an excess of valence electrons compared to the host material	Acceptor impurities generate "holes" or gaps within the valence band of the semiconductor lattice by possessing fewer valence electrons than the host material
Introduce excess electrons that can move through the material	Create holes that can also carry a charge
Introduce energy levels within the band gap near the conduction band	Introduce energy levels near the valence band
Elements found in group V of the periodic table commonly function as donor impurities	Elements in group III usually serve as acceptor impurities

- P type semiconductor (holes) is doped with B, Al, or In; 3 el in Outermost valence shell
- N type seminconductor (electrons) is doped with P, As, Sb (antimony) 5 el in outermost valence shell

Electrons in shells: 2, 8, 18,....



Basic CMOS building blocks

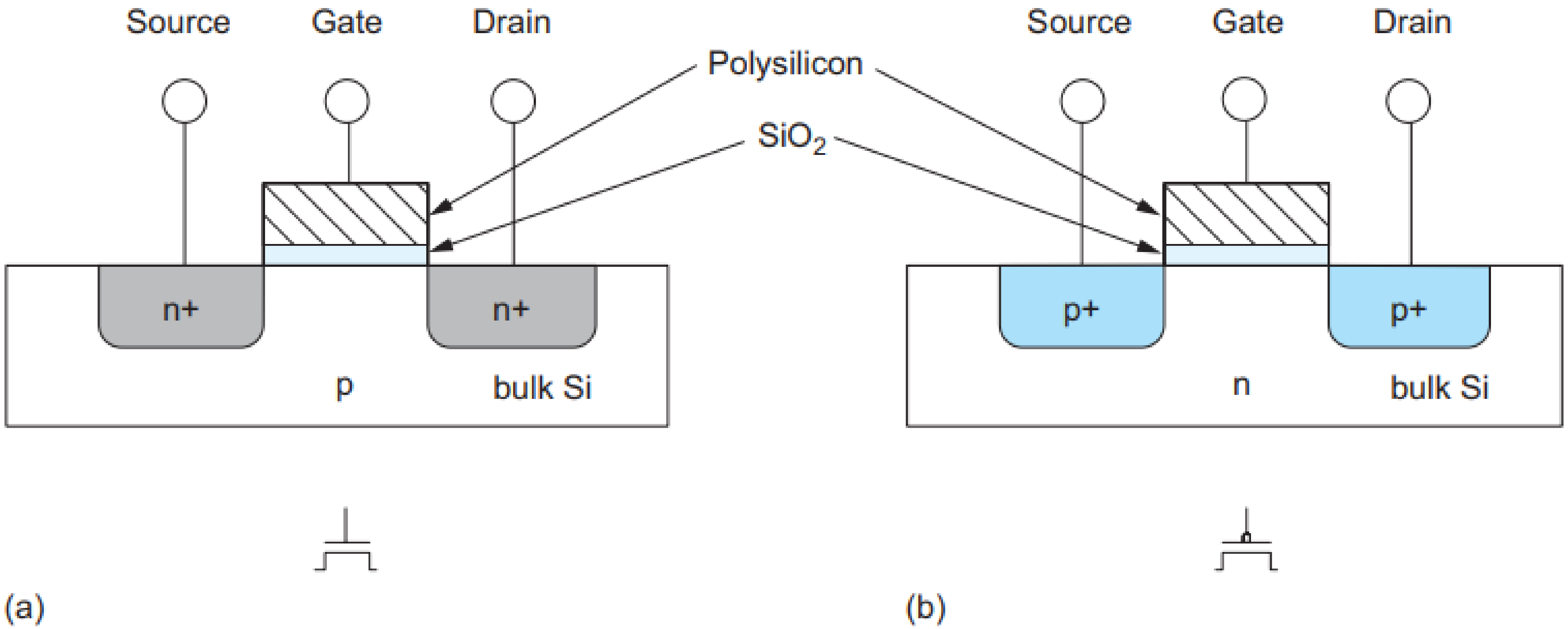
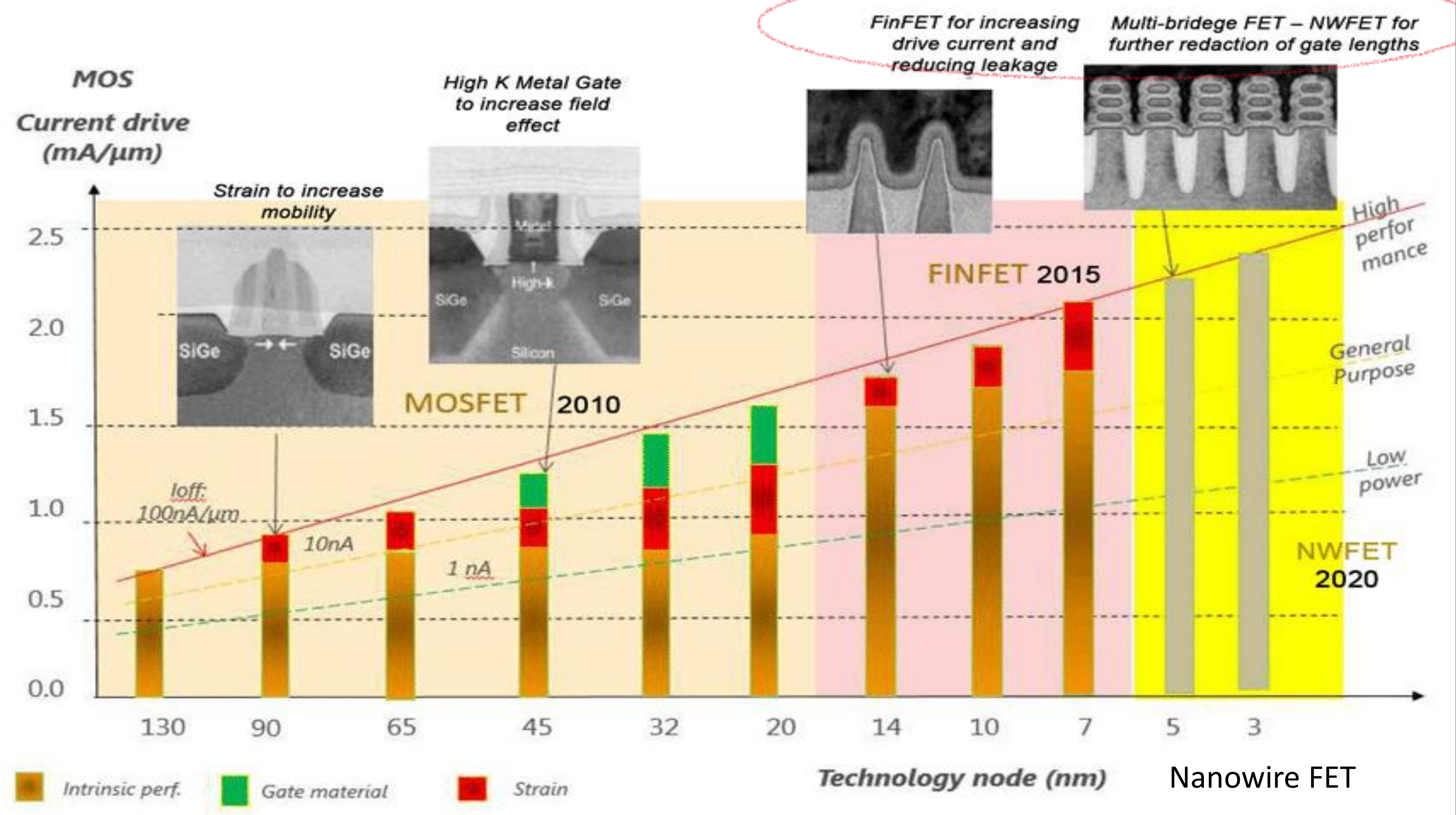


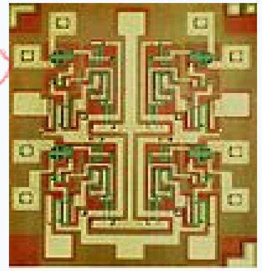
FIGURE 1.9 nMOS transistor (a) and pMOS transistor (b)

Semiconductor Technology Roadmap



Nanowire FET

Semiconductor device fabrication



MOSFET scaling (process nodes)

- 20 µm – 1968
- 10 µm – 1971
- 6 µm – 1974
- 3 µm – 1977
- 1.5 µm – 1981
- 1 µm – 1984
- 800 nm – 1987
- 600 nm – 1990
- 350 nm – 1993
- 250 nm – 1996
- 180 nm – 1999
- 130 nm – 2001
- 90 nm – 2003
- 65 nm – 2005
- 45 nm – 2007
- 32 nm – 2009
- 22 nm – 2012
- 14 nm – 2014
- 10 nm – 2016
- 7 nm – 2018
- 5 nm – 2020
- 3 nm – 2022

Future

- 2 nm ~ 2024

The scaling competition

Only Three Companies Have Survived the Scaling Competition

Let's look at the trends in semiconductor companies from the scaling viewpoint. Because process development costs and capital investment costs kept skyrocketing as circuit patterns were shrunk, semiconductor companies began to leave the competition one after another. Around 2002/2003, there were 26 semiconductor companies worldwide capable of manufacturing 130-nm devices. However, the number of companies continuing with scaling competition decreased. For example, there were only 18 companies at 90 nm and only 14 companies at 45 nm. Beyond 10 nm, only Intel, Samsung, and TSMC remained. In 7-nm processes[*5], it seems that Intel and Samsung had been having manufacturing yield problems in their cutting-edge processes, including EUV lithography, for a long time, but industry sources say that Samsung has pulled ahead and is monopolizing outsourced production from cutting-edge fabless semiconductor companies.

Most Japanese companies stopped scaling at around 45/40 nm, and even Panasonic, which kept going with scaling until it became the only remaining company, also decided that scaling beyond 28 nm was meaningless because performance could not be improved[Reference 3]. This way of thinking might have been correct if the transistor structure and constituent materials had stayed the same. However, transistor materials, as well as structure, have changed completely, and more recently, EUV lithography, which had been considered impossible to implement, was put into practical use in some cases, dramatically improving the resolution of aligners and opening the path to further scaling.

Future of Integrated Circuits

The Future of Integrated Circuits: A Survey of Nanoelectronics

Publisher: IEEE Cite This PDF

Michael Haselman ; Scott Hauck All Authors

Abstract

Authors

References

Citations

Keywords

Metrics

Abstract:
While most of the electronics industry is dependent on the ever-decreasing size of lithographic transistors, this scaling cannot continue indefinitely. Nanoelectronics (circuits built with components on the scale of 10 nm) seem to be the most promising successor to lithographic based ICs. Molecular-scale devices including diodes, bistable switches, carbon nanotubes, and nanowires have been fabricated and characterized in chemistry labs. Techniques for self-assembling these devices into different architectures have also been demonstrated and used to build small-scale prototypes. While these devices and assembly techniques will lead to nanoscale electronics, they also have the drawback of being prone to defects and transient faults. Fault-tolerance techniques will be crucial to the use of nanoelectronics. Lastly, changes to the software tools that support the fabrication and use of ICs will be needed to extend them to support nanoelectronics. This paper introduces nanoelectronics and reviews the current progress made in research in the areas of technologies, architectures, fault tolerance, and software tools.

IC Design future

The future of IC design

JULY 14, 2016

BY **R COLIN JOHNSON**

To celebrate 60 years of EDN, we're looking into the future to predict what advancements will be made in IC Design in the next 60 years. By 2076 3-D room-temperature, superconducting, quantum, neuromorphic, and photonic mixed-signal devices will be the common denominator for all integrated circuit designs. Design tools will be so sophisticated that even novice designers will be able to mix and match these technologies into system-in-package designs that solve all application problems behind the scenes. Users will be so used to extensions to their innate brain capabilities that the technologies which perform the tasks will be taken for granted, leaving the engineering community—and its robotic assistants—on a unique echelon of society that actually understands how the world works.

CHIPS Alliance for chip design and fab

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Current State of the Art CMOS Design and Fabrication

TSMC has 2nm fab technology

TSMC reportedly achieves smooth implementation of GAA for 2nm process

Monica Chen, Hsinchu; Judy Lin, DIGITIMES Asia | Monday 15 January 2024 | 0 Like 1

Credit: DIGITIMES

Taiwan Semiconductor Manufacturing Company (TSMC) is on schedule to implement its 2-nanometer node with the Gate-All-Around (GAA) technology, according to its supply chain

TSMC Latest

As of today, January 13, 2026, the global semiconductor landscape has officially shifted on its axis. Taiwan Semiconductor Manufacturing Company (NYSE: TSM) has announced that its Fab 22 facility in Kaohsiung has reached high-volume manufacturing (HVM) for its long-awaited 2nm (N2) process node. This milestone marks the definitive end of the FinFET transistor era and the beginning of a new chapter in silicon architecture that promises to redefine the limits of performance, efficiency, and artificial intelligence.

The transition to 2nm is not merely an incremental step; it is a foundational reset of the "Golden Rule" of Moore's Law. By successfully ramping up production at Fab 22 alongside its sister facility, Fab 20 in Hsinchu, TSMC is now delivering the world's most advanced semiconductors at a scale that its competitors—namely Samsung and Intel—are still struggling to match. With yields already reported in the 65–70% range, the 2nm era is arriving with a level of maturity that few industry analysts expected so early in the year.
The technical centerpiece of the N2 node is the transition from FinFET (Fin Field-Effect Transistor) to Gate-All-Around (GAA) Nanosheet transistors. For over a decade, FinFET served the industry well, but as transistors shrank toward the atomic scale, current leakage and electrostatic control became insurmountable hurdles. The GAA architecture solves this by wrapping the gate around all four sides of the channel, providing a degree of control that was previously impossible. This structural shift allows for a staggering 25% to 30% reduction in power consumption at the same performance levels compared to the previous 3nm (N3E) generation.

Beyond power savings, the N2 process offers a 10% to 15% performance boost at the same power envelope, alongside a logic density increase of up to 20%. This is achieved through the stacking of horizontal silicon ribbons, which allows for more current to flow through a smaller footprint. Initial reactions from the semiconductor research community have been overwhelmingly positive, with experts noting that TSMC has effectively bypassed the "yield valley" that often plagues such radical architectural shifts. The ability to maintain high yields while implementing GAA is being hailed as a masterclass in precision engineering.

Transistor Scaling Through Innovation in CMOS

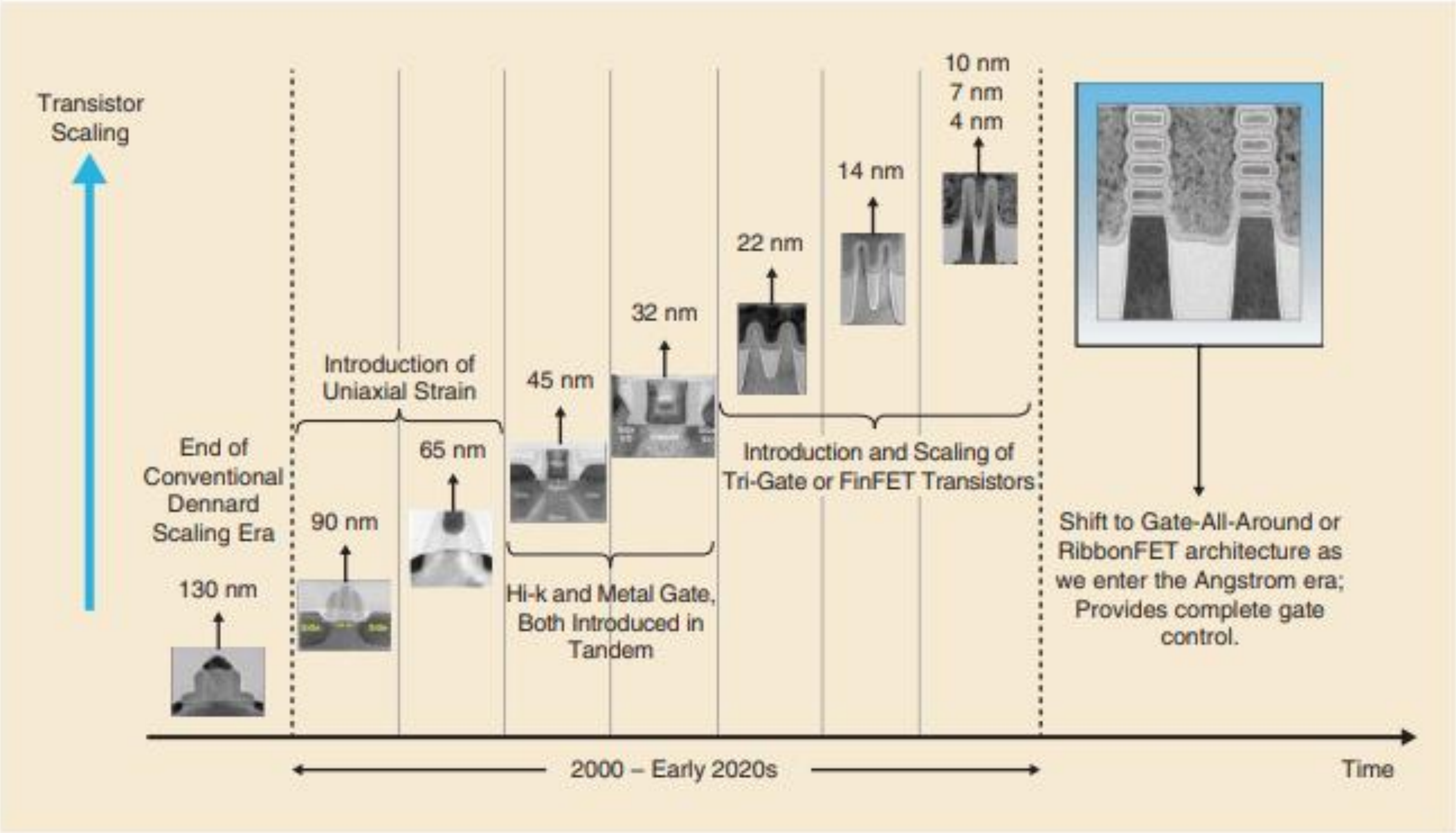
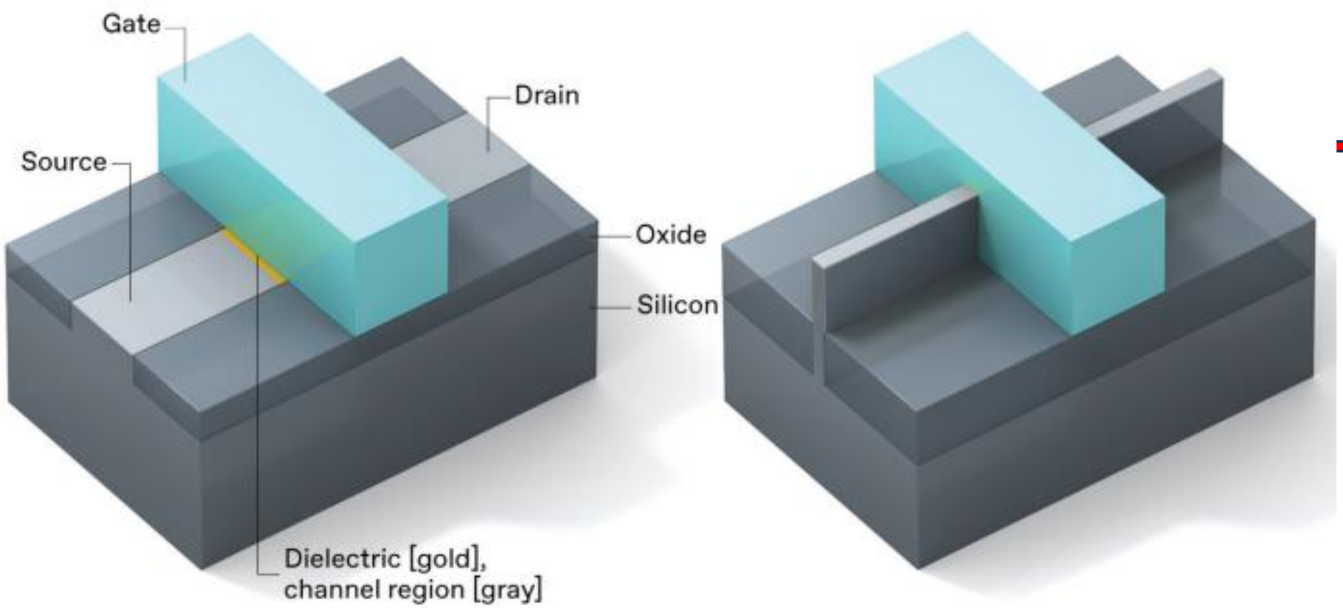
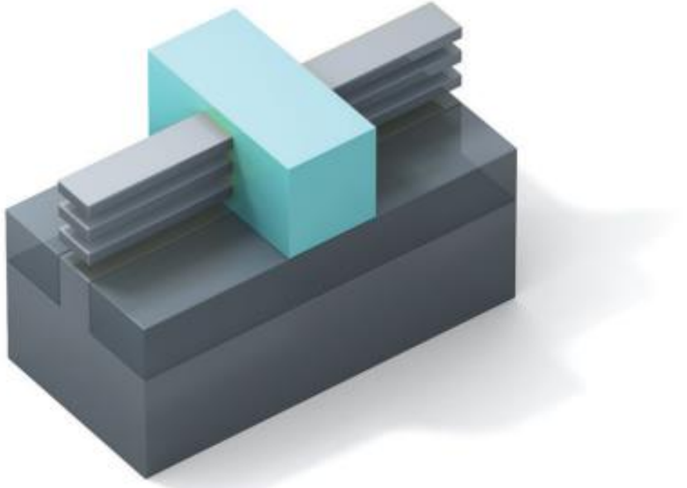


FIGURE 7: The evolution of transistor technology since the 130-nm node, as we enter the postconventional scaling era or the "golden" era of transistor evolution.

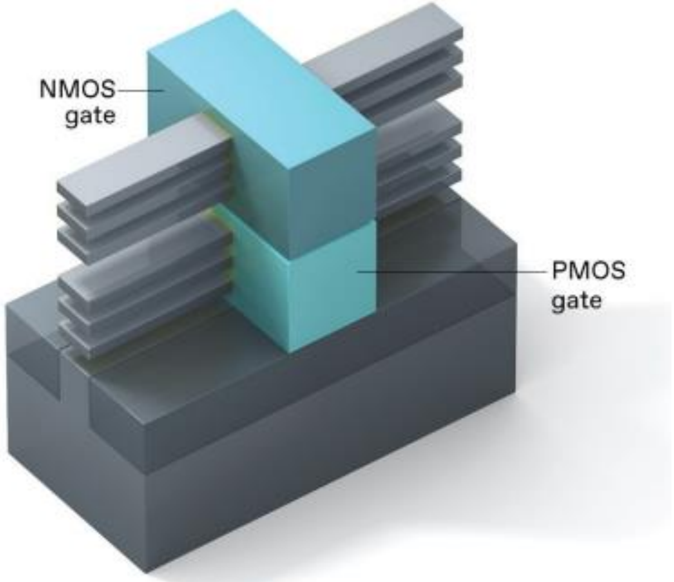
Transistor Evolution

TRANSISTOR EVOLUTION
The shift from a planar transistor architecture [left] to the FinFET [right] provided greater control of the channel [covered by blue block], resulting in a reduction in power consumption of 50 percent and an increase in performance of 37 percent.





In the RibbonFET, the gate wraps around the transistor channel region to enhance control of charge carriers. The new structure also enables better performance and more refined optimization.



3D-stacked CMOS puts a PMOS device on top of an NMOS device in the same footprint a single RibbonFET would occupy. The NMOS and PMOS gates use different metals.

FinFET vs Nanowire Transistor

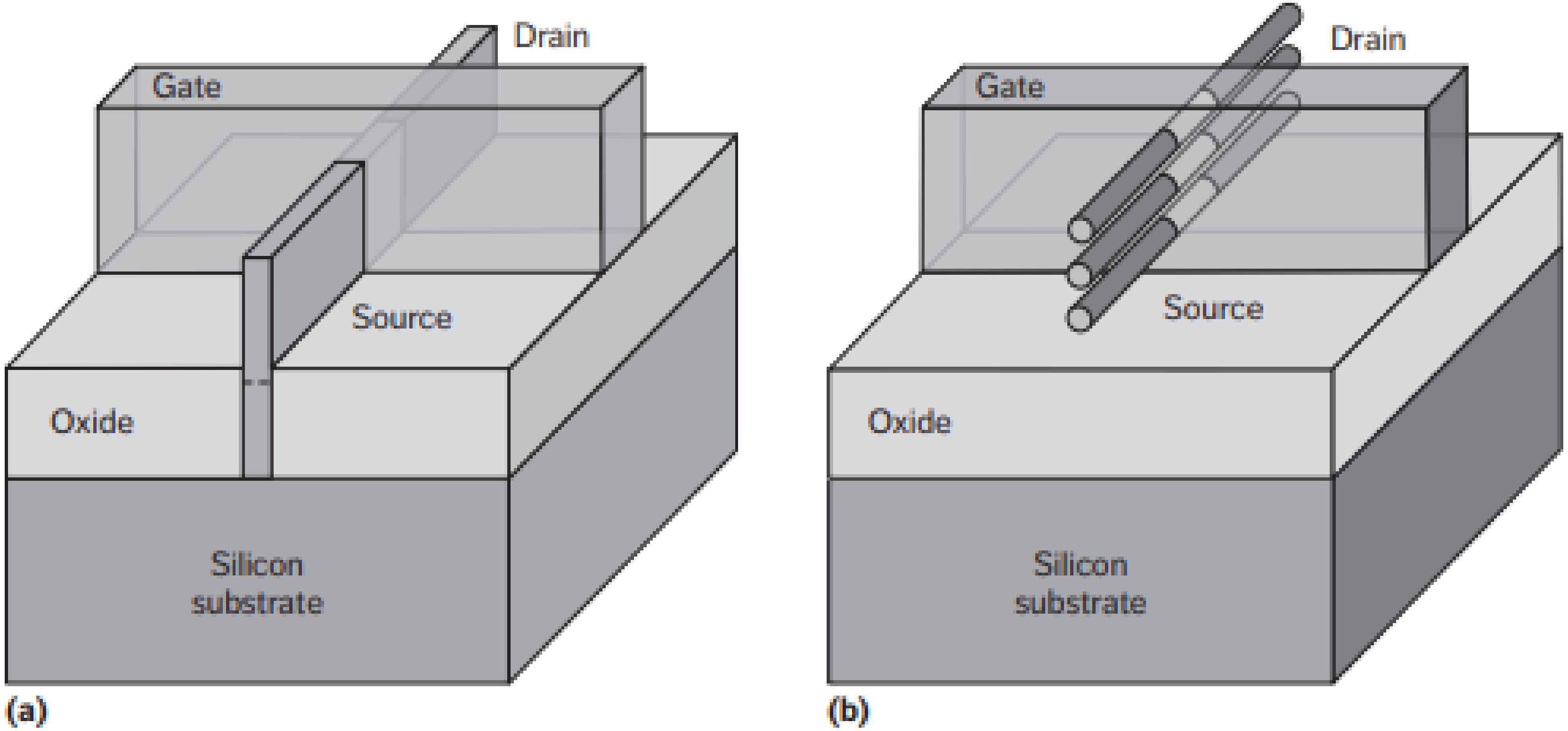


Figure 11. Comparison of transistor structures. (a) FinFET transistor. (b) Nanowire transistor.

Nanowire FET

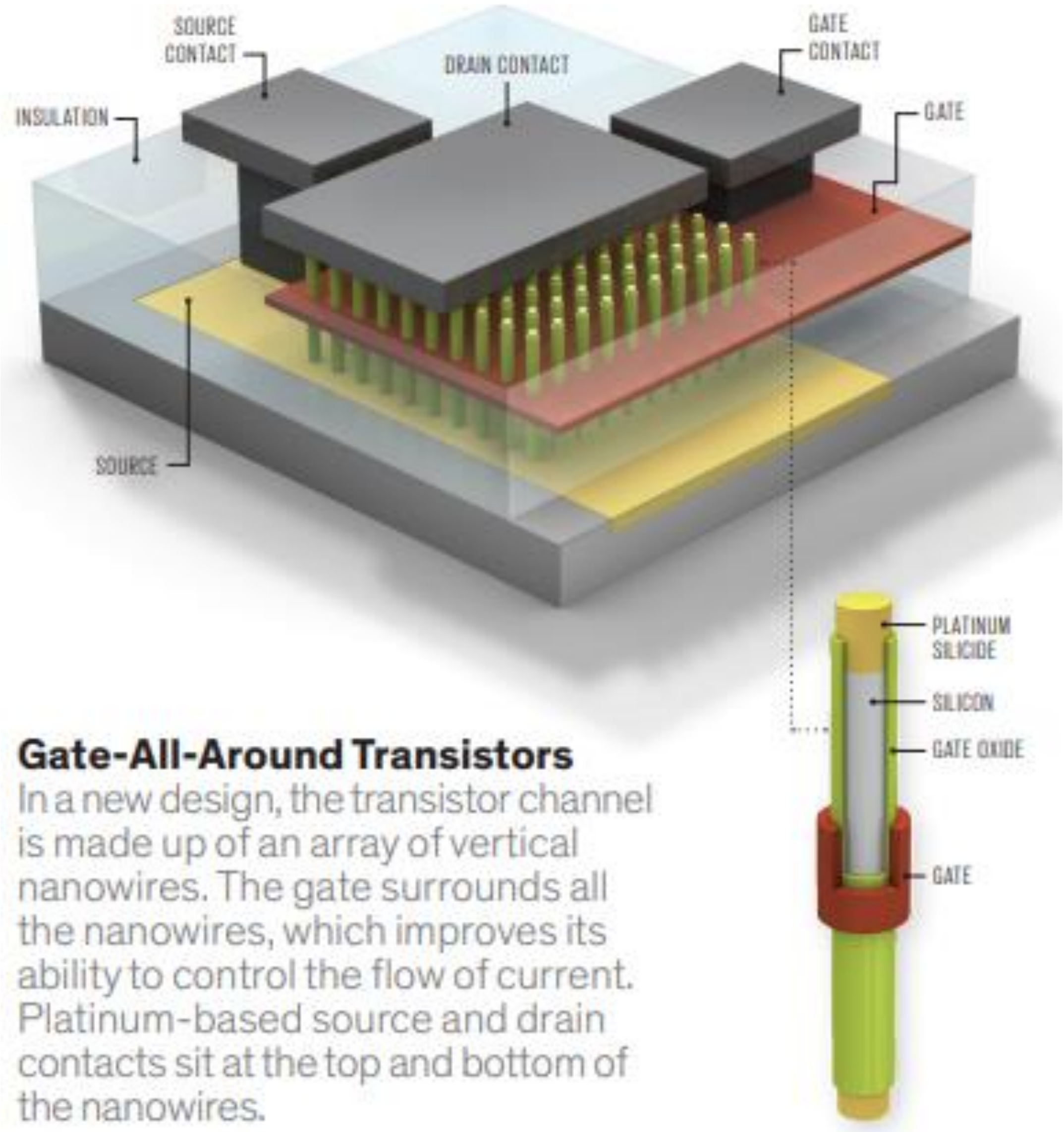
RING AROUND THE NANOWIRE

Researchers are perfecting ways to produce gate-all-around devices

THE END OF Moore's Law has been predicted again and again. And again and again, new technologies, most recently FinFETs, have dispelled these fears. Engineers may already have come up with the technology that will fend off the next set of naysayers: nanowire FETs (field-effect transistors).

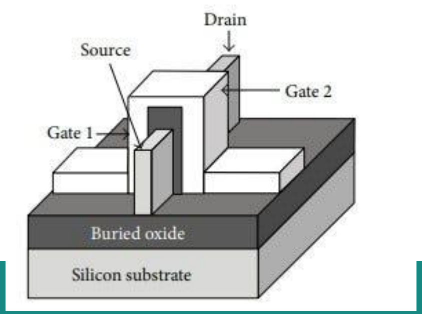
In these nanodevices, current flows through the nanowire or is pinched off under the control of the voltage on the gate electrode, which surrounds the nanowire. Hence, nanowire FETs' other name: "gate-all-around" transistors. However, because of their small size, single nanowires can't carry enough current to make an efficient transistor.

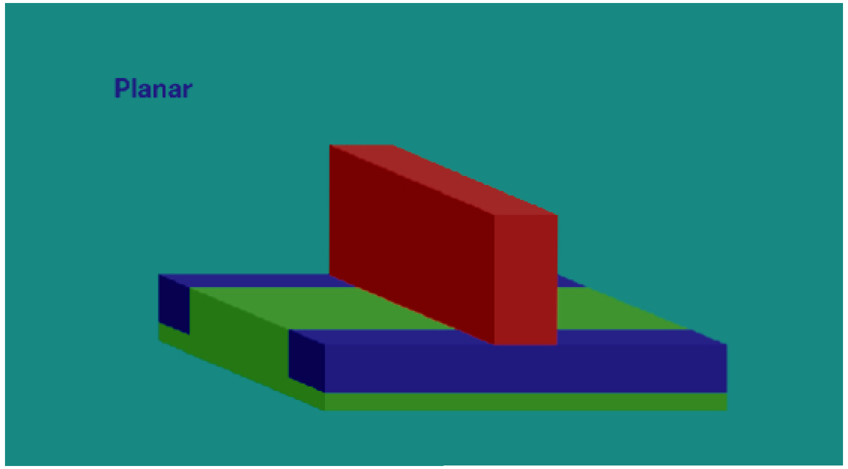
The solution, recent research shows, is to make a transistor that consists of a small forest of nanowires that are under the control of the same gate and so act as a single transistor. For example, researchers at Hokkaido University and from the Japan Science and Technology Agency reported last year in *Nature* a gate-all-around nanowire transistor consisting of 10 vertical indium gallium arsenide nanowires grown on a silicon substrate. Although the device's electrical properties were good, the gate length–a critical dimension–was 200 nanometers, much too large for the tiny transistors needed to power the microprocessors of the 2020s. »

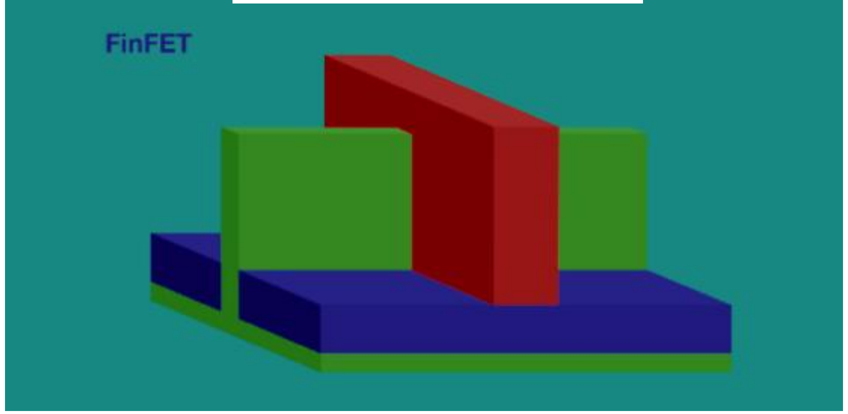


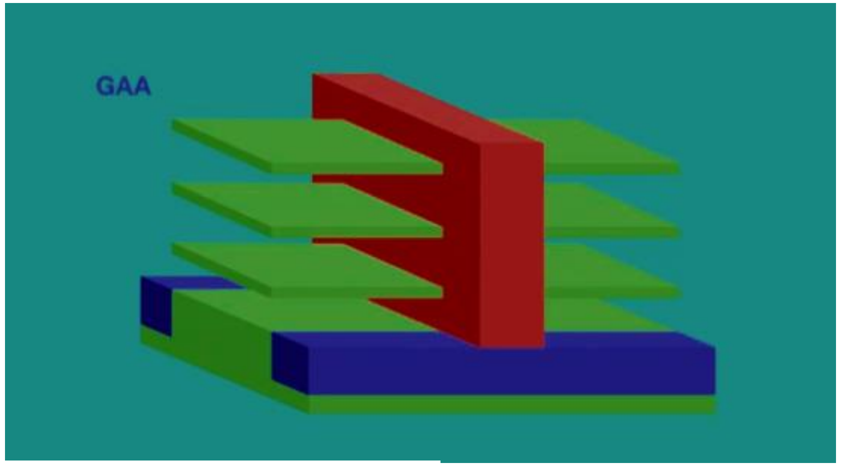
Gate-All-Around Transistors
In a new design, the transistor channel is made up of an array of vertical nanowires. The gate surrounds all the nanowires, which improves its ability to control the flow of current. Platinum-based source and drain contacts sit at the top and bottom of the nanowires.

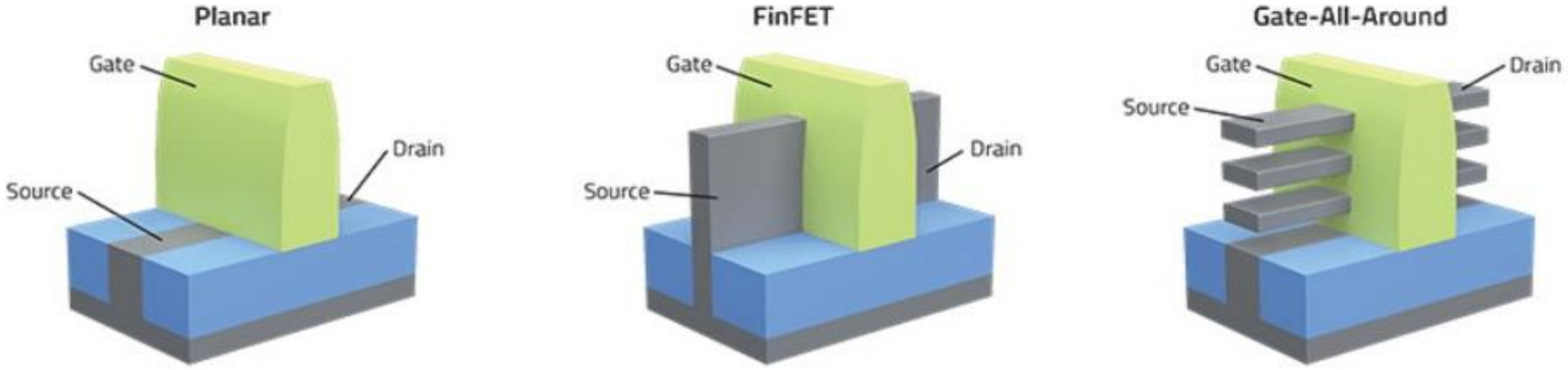
Planar, FINFET, Gate All Around



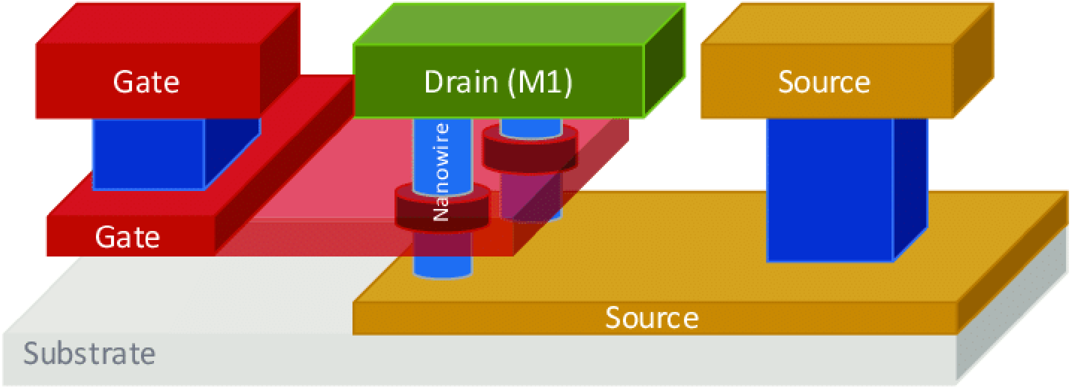




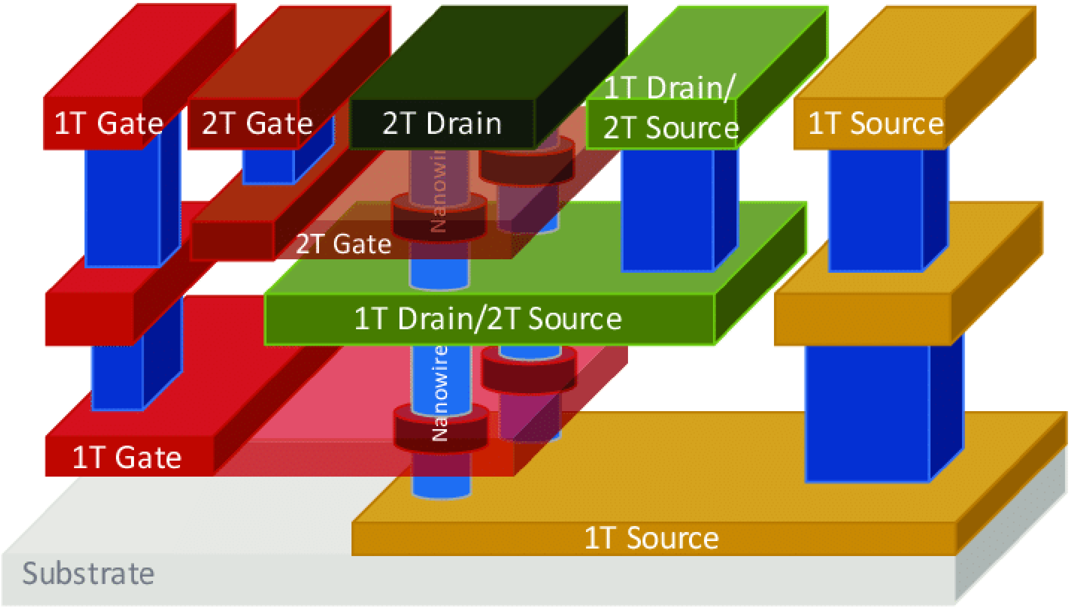




Vertical FET

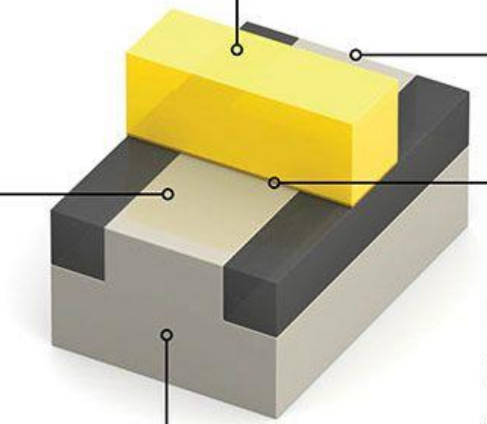


(a) 1-tier Vertical FET (1T V-FET)

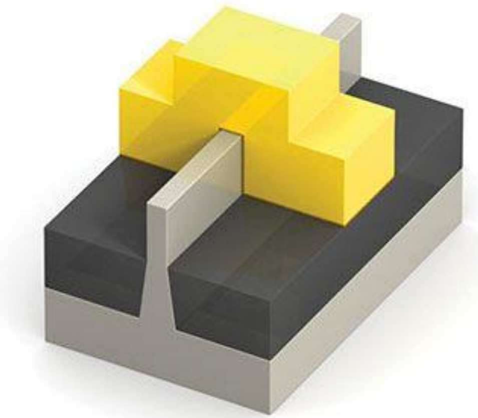


(b) 2-tier Vertical FET (2T V-FET)

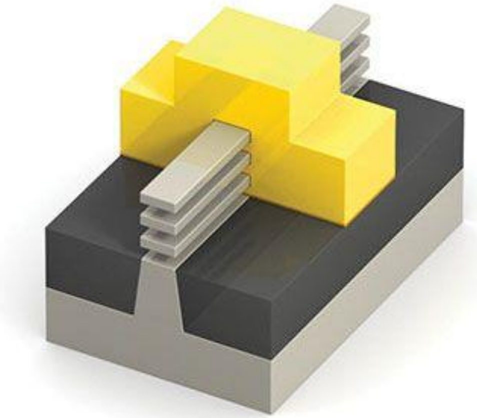
Nanosheet FET



Planar FET
Up until about 2011, planar transistors were the best devices available.

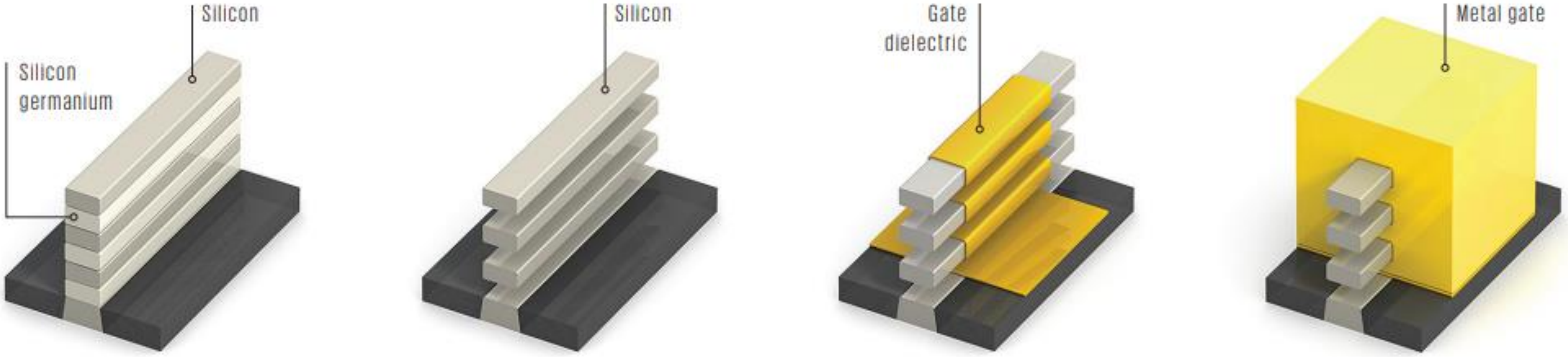


FinFET
Surrounding the channel region on three sides with the gate gives better control and prevents current leakage.



Stacked nanosheet FET
The gate completely surrounds the channel regions to give even better control than the FinFET.

How to make Nanosheets



A superlattice of silicon and silicon germanium are grown atop the silicon substrate.

A chemical that etches away silicon germanium reveals the silicon channel regions.

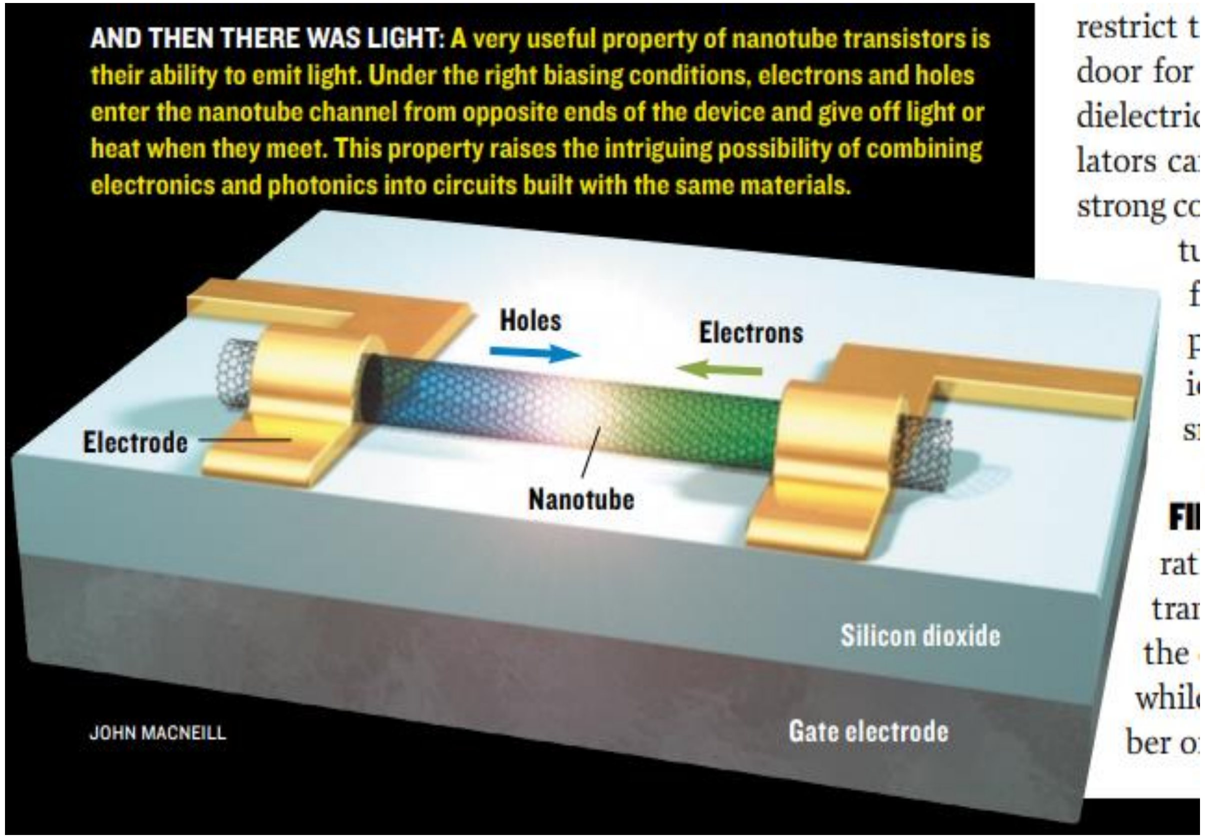
Atomic layer deposition builds a thin layer of dielectric on the silicon channels, including on the underside.

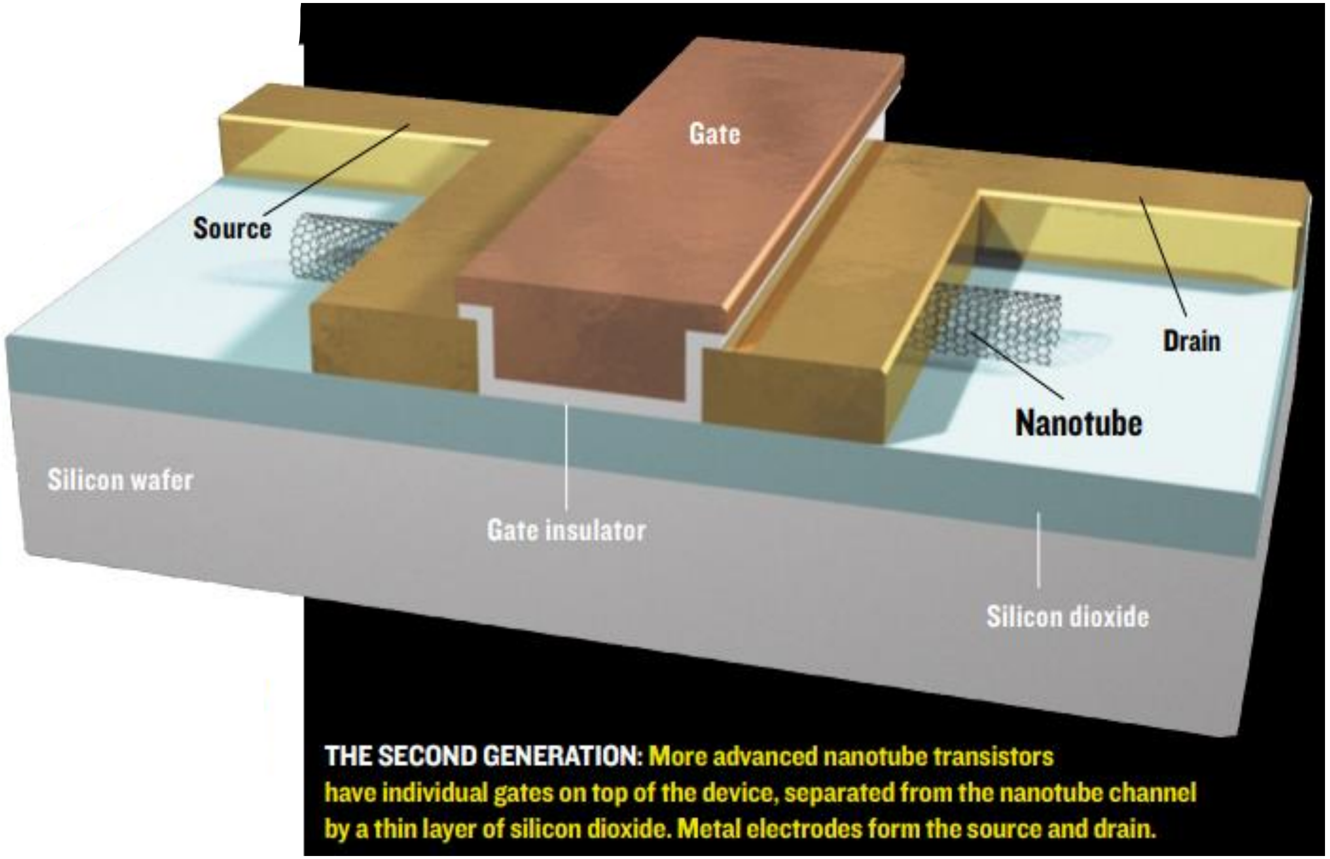
Atomic layer deposition builds the metal gate so that it completely surrounds the channel regions.

HOW TO MAKE NANOSHEETS

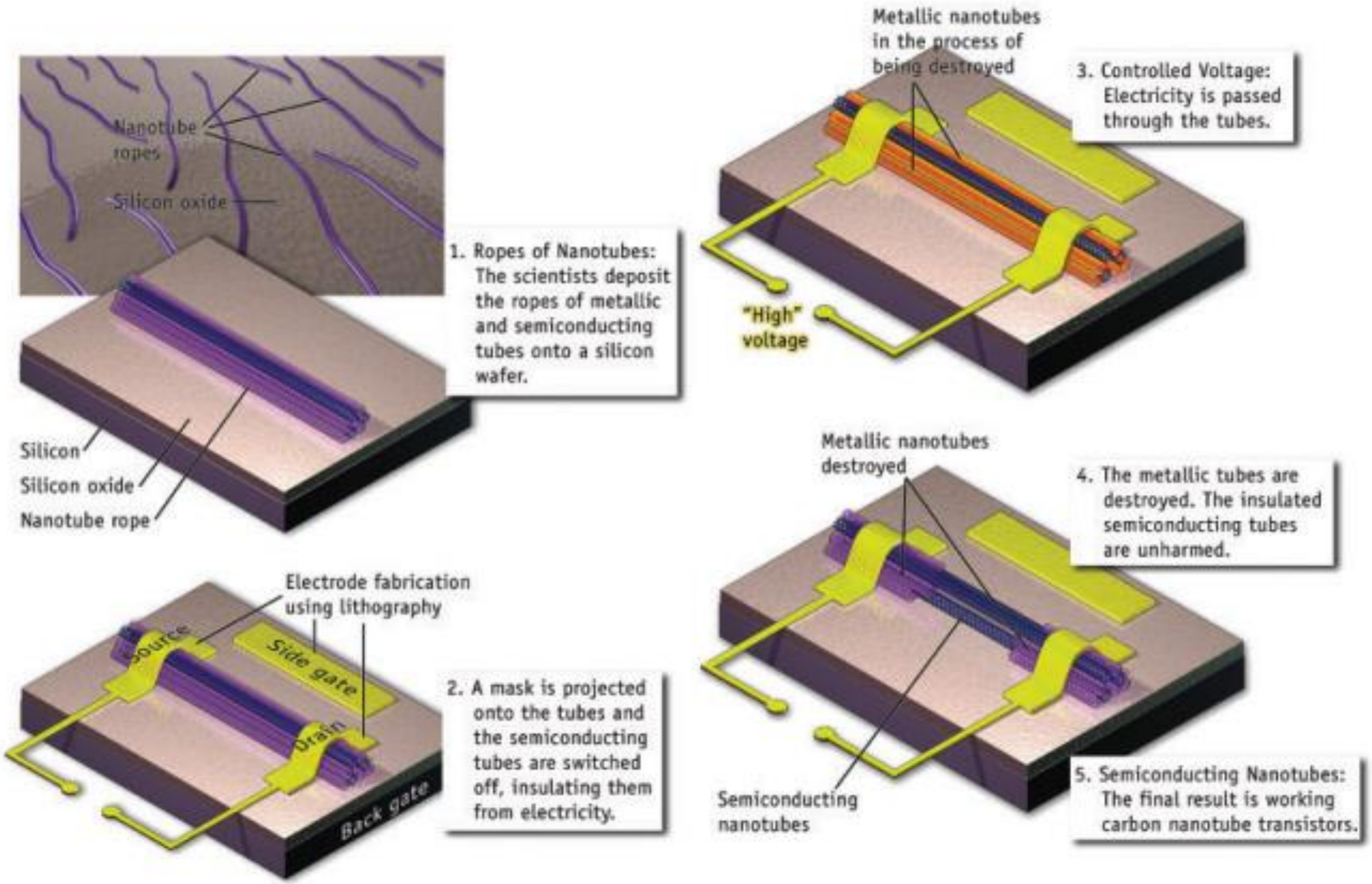
Sacrificial layers, selective chemical etchants, and advanced atomically precise deposition technology are needed to make nanosheets.

Basics of Carbon Nanotubes





IBM Carbon Nanotube Process



IBM has developed a process that puts the right kind of nanotube in the right place

CAN WE BUILD THEM?

There is some scepticism as to the possibility of building complex circuits using CNT technology. CNT circuits face at least two of the same issues as silicon circuits. The first is that the physical dimensions of these circuits are now well below the wavelengths of the light used in the lithography systems that pattern the circuitry on to each chip, leading to increasingly complex and expensive workarounds. The second is that because CNTs are so small, the characteristics of CNTFETs will vary dramatically from device to device, making circuit design much more difficult.

However, Avouris says IBM and other companies have already been able to fabricate not just single CNTFETs but also simple circuits such as logic gates. His team has also built more complex structures such as ring oscillators. He says these structures show how to integrate a number of CNT devices to achieve a specific function, and that they are compatible with conventional CMOS circuitry.

A Canadian team says it has tackled the other major issue – making large amounts of nanotubes reliably. The team, from the National Research Council Steacie Institute for Molecular Sciences (NRC-SIMS)

Beyond 1nm

Emergence of high-NA EUV and 2D materials extending Moore's Law beyond 1 nm

Furthermore, two-dimensional materials are being researched as transistor channel materials in 1-nm processes[Reference 5]. These are two-dimensional (2D) atomic layer, inorganic nanomaterials, such as graphene and transition metal dichalcogenides. Imec, a cutting-edge semiconductor research organization in Belgium, maintains that these new technologies and materials can now be expected to extend Moore's Law beyond 1 nms[References 4, 5].

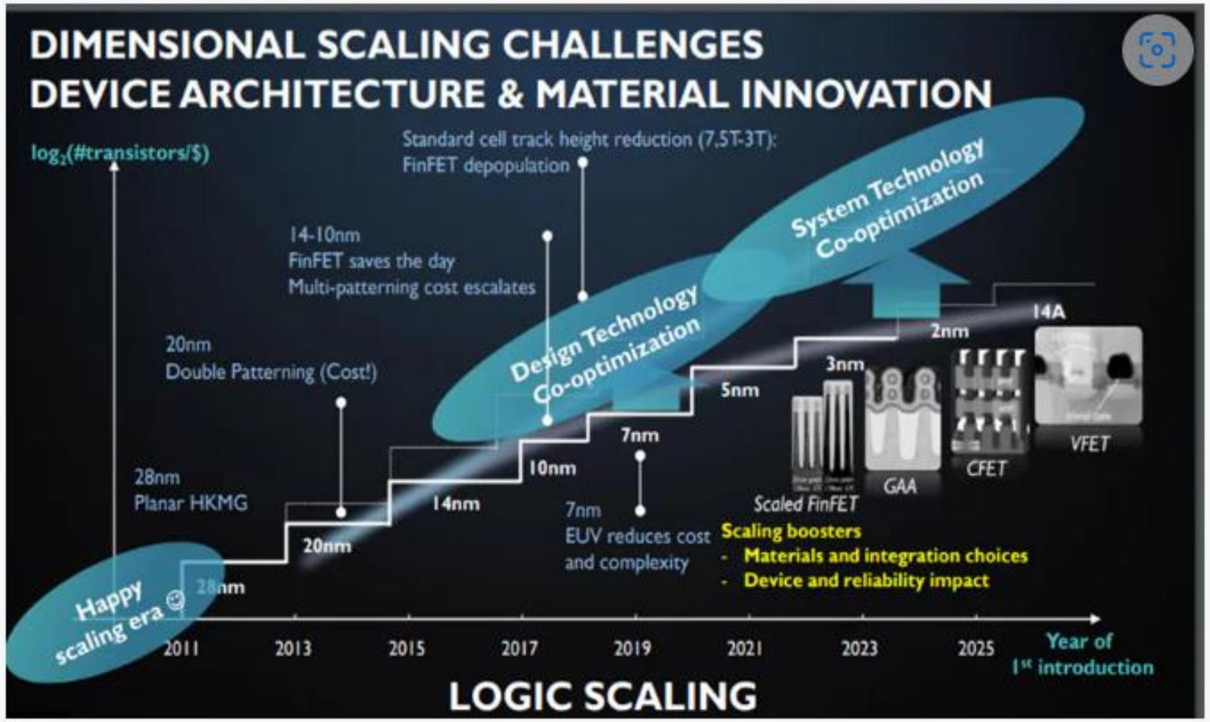


Figure 7. Imec's scaling roadmap for semiconductor logic devices

GAA = Gates All Around
VFET = Vertical FET
CFET = Complementary FET – a type of VFET
FINFET = has thin vertical fin, gate is wrapped around channel on 3 sides
Carbon Nanotube Transistor – has carbon nano tubes as channels
HKMG = High k metal gate

Future Integrated Circuits

Future 3D Chips

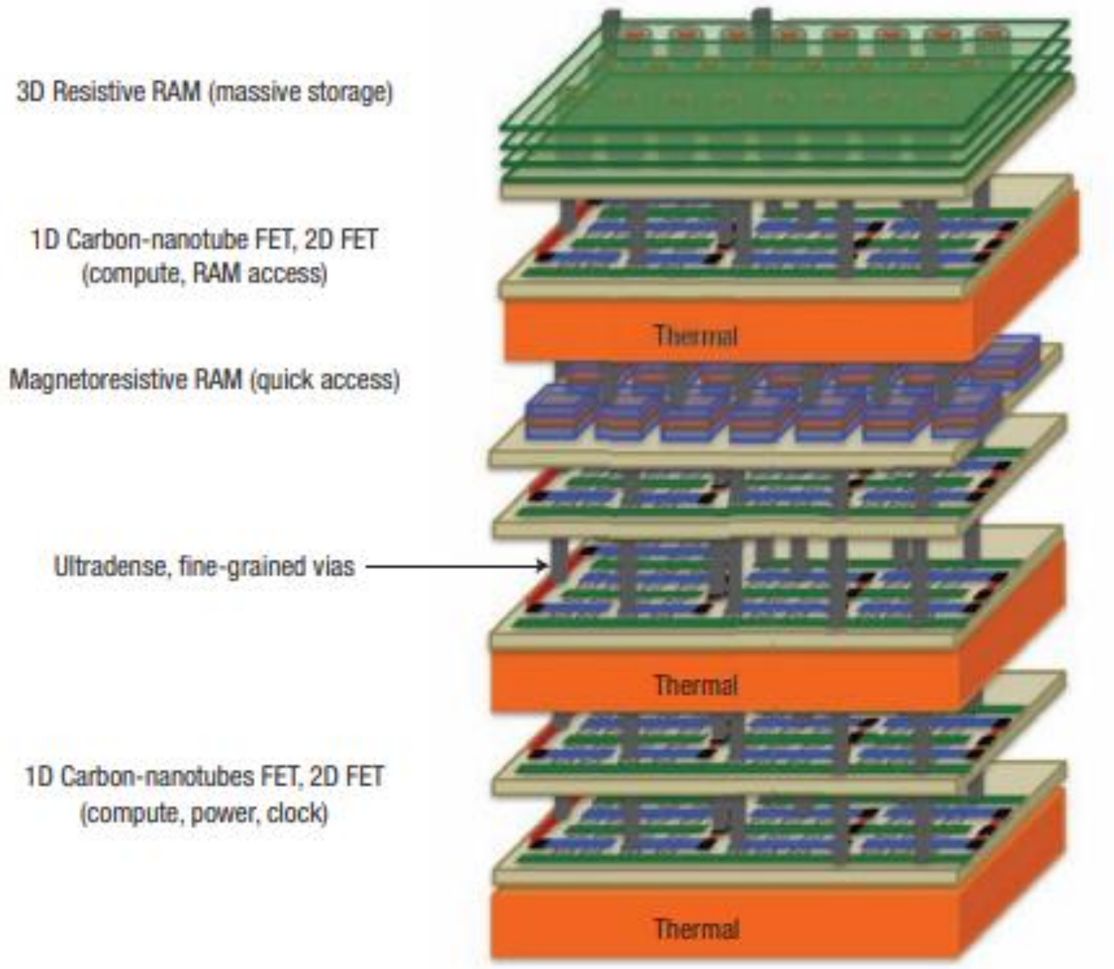


Figure 2. 3D chip. University researchers propose building chips in three dimensions, with multiple layers of logic and memory, including field-effect transistors (FETs), connected by ultradense vias.

Different Types of 3D Stacking

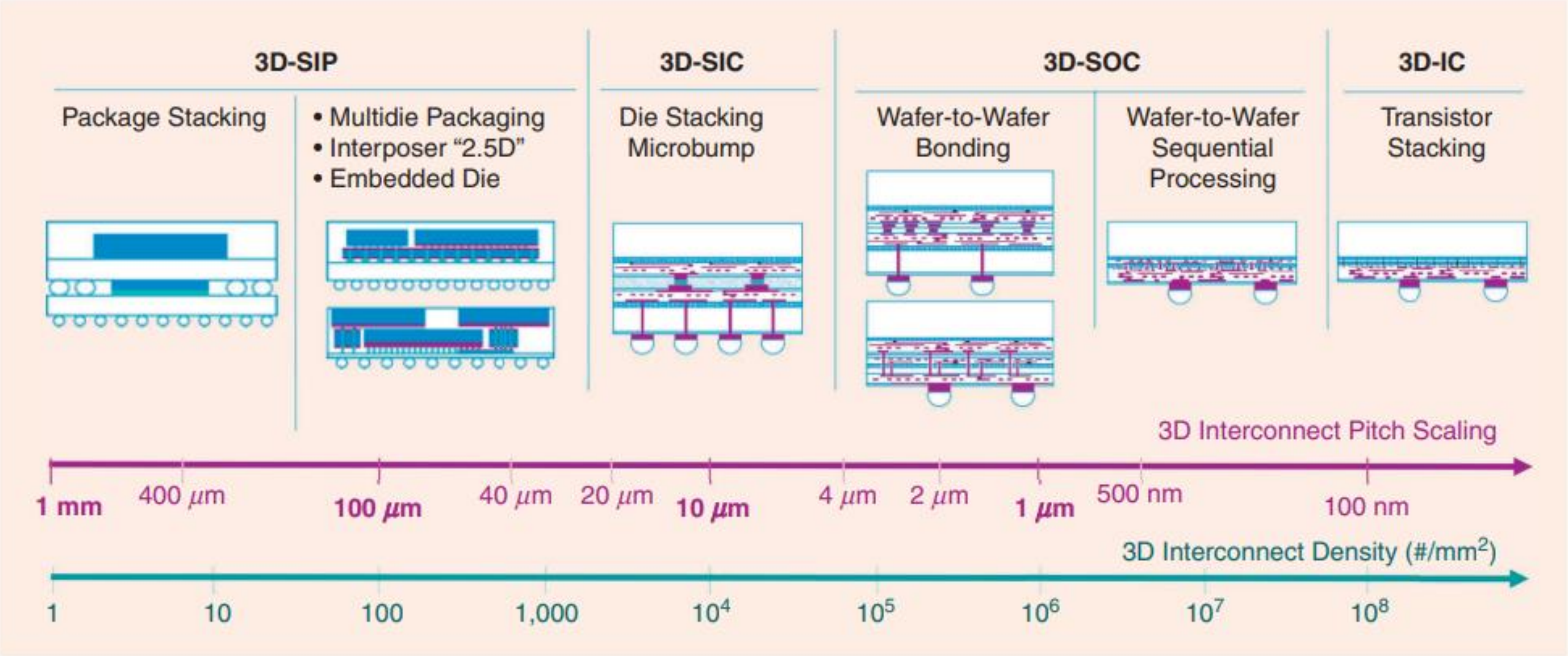


FIGURE 2: The landscape of 3D interconnect technologies can be categorized based on their increasing 3D interconnect density capability. System-in-package (SIP) integration technologies and stacked-IC (SIC) technology with die-to-die interconnects offer relatively lower-density capabilities. On the other hand, system-on-chip (SOC) integration enabled by advanced codesign EDA tools, wafer-to-wafer bonding technologies, and sequential 3D stacking offer higher-density capabilities. The highest density is offered by transistor-level stacking of devices, allowing for 3D integration at the standard cell level, which is referred to as *3D-IC* [11]. Reprinted, with permission, from [7] S. B. Samavedam et al., "Future logic scaling: towards Atomic Channels and Deconstructed Chips," *IEDM Tech. Digest*, 2020.

What about new Materials?

WILL SILICON STILL BE THE ACTIVE PART OF MOST TRANSISTORS IN 2047?

Experts say that the heart of most devices, the transistor channel region, will still be silicon, or possibly silicon-germanium—which is already making inroads—or germanium. But in 2047 many chips may use semiconductors that are considered exotic today. These could include oxide semiconductors like indium gallium zinc oxide; 2D semiconductors, such as the metal dichalcogenide tungsten disulfide; and one-dimensional semiconductors, such as carbon nanotubes. Or even "others yet to be invented," says Imec's Samavedam.

Silicon-based chips may be integrated in the same package with chips that rely on newer materials, just as processor makers are today integrating chips using different silicon manufacturing technologies into the same package, notes IEEE Fellow Gabriel Loh, a senior fellow at AMD.

Which semiconductor material is at the heart of the device may not even be the central issue in 2047. "The choice of channel material will essentially be dictated by which material is the most compatible with many other materials that form other parts of the device," says Salahuddin. And we know a lot about integrating materials with silicon.

WHERE WILL TRANSISTORS BE COMMON WHERE THEY ARE NOT FOUND TODAY?

Everywhere. No, seriously. Experts really do expect some amount of intelligence and sensing to creep into every aspect of our lives. That means devices will be attached to our bodies and implanted inside them; embedded in all kinds of infrastructure, including roads, walls, and houses; woven into our clothing; stuck to our food; swaying in the breeze in grain fields; watching just about every step in every supply chain; and doing many other things in places nobody has thought of yet.

Transistors will be "everywhere that needs computation, command and control, communications, data collection, storage and analysis, intelligence, sensing and actuation, interaction with humans, or an entrance portal to the virtual and mixed reality world," sums up Stanford's Wong.

To look for - in the future

Future of transistor – FinFET, NWFET, NSFET, Gate All Around

Future of CMOS technology – around 1 nm or lower

Future of Integrated Circuits – 3D Stacked, Quantum Computing

Future of VLSI Design – Manage Complexity, Speed, Energy, Performance

Go over course outline