VLSI Design EE 523
Spring 2026

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Lecture 3

Topics for lecture 3

- Some solved examples from Lecture 2
- Simple working models for NMOS and PMOS transistors as switches
- Making logic gates from simple CMOS models
  - Inverter
  - Nand
  - Nor
  - AND-NOR combined gate
- Pass Transistor Logic using simple CMOS models
  - Non-restoring and Restoring switches

Reading from Weste and Harris ‘CMOS VLSI Design’ textbook: Chapter 1

Basic Diode Shockley Equations

It can be demonstrated through the use of solid-state physics that the general characteristics of a semiconductor diode can be defined by the following equation, referred to as Shockley's equation, for the forward- and reverse-bias regions:

$$I_D = I_s(e^{V_D/nV_T} - 1) \quad \text{(A)} \tag{1.2}$$

where I_s is the reverse saturation current
V_D is the applied forward-bias voltage across the diode
n is an ideality factor, which is a function of the operating conditions and physical construction; it has a range between 1 and 2 depending on a wide variety of factors ($n = 1$ will be assumed throughout this text unless otherwise noted).

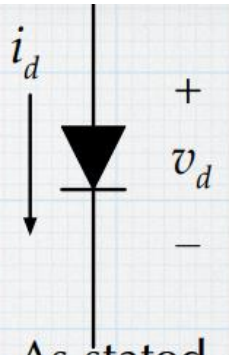
The voltage V_T in Eq. (1.1) is called the *thermal voltage* and is determined by

$$V_T = \frac{kT_K}{q} \quad \text{(V)} \tag{1.3}$$

where k is Boltzmann's constant $= 1.38 \times 10^{-23}$ J/K
T_K is the absolute temperature in kelvins = 273 + the temperature in °C
q is the magnitude of electronic charge $= 1.6 \times 10^{-19}$ C

Diode i-v characteristics

diode i-v characteristic



The ideal diode equation: $i_D = I_S \left[\exp\left(\frac{v_D}{kT/q} \right) - 1 \right]$

where i_D is the diode current and v_D voltage across the diode. As stated earlier, the relationship is extremely non-linear, and it will cause us a some grief when analyzing diodes. But the non-linear behavior offers opportunities for new applications.

- I_S is the current parameter of the diode, often known as the *saturation current* or *scale current*. It is like "R" for a resistor. Each diode will have a unique value for I_S. A typical value is $I_S \approx 10^{-14}$ A.
- kT/q is the *thermal voltage*. k is Boltzmann's constant (recall thermodynamics from physics) with a value of 1.38×10^{-23} J/K. T is the absolute temperature of the diode, expressed in kelvin (K). Then the product kT is the thermal energy and represents the average energy of an electron in the semiconductor. If we divide the electron the electron charge — $q = 1.6 \times 10^{-19}$ C — we get the thermal voltage. At 300 K (= 27°C, approximately room temperature), $kT/q = 25.8$ mV.

Diode Calculation

Example 3.1

Determine the built-in potential, depletion width, and zero-bias depletion capacitance for an n^+–p Si diode at 300 K, with $N_d = 10^{18}\ \text{cm}^{-3}$, $N_a = 10^{16}\ \text{cm}^{-3}$, and a junction area of $10^{-5}\ \text{cm}^2$.

Solution. The built-in potential is

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_a N_d}{n_i^2}\right) = (0.0259\ \text{V})\ln\left(\frac{(10^{16}\ \text{cm}^{-3})(10^{18}\ \text{cm}^{-3})}{(1.45\times10^{10}\ \text{cm}^{-3})^2}\right) = 0.816\ \text{V}.$$

The depletion width is almost entirely on the p-type side and is

$$W = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN_a}} = \sqrt{\frac{2(11.9)(8.85\times10^{-14}\ \text{F/cm})(0.816\ \text{V})}{(1.602\times10^{-19}\ \text{C})(10^{16}\ \text{cm}^{-3})}}$$

$$= 0.33\times10^{-4}\ \text{cm} = 0.33\ \mu\text{m}.$$

The zero-bias depletion capacitance is

$$C_T = \frac{\varepsilon_s A}{W} = \frac{(11.9)(8.85\times10^{-14}\ \text{F/cm})(10^{-5}\ \text{cm}^2)}{0.33\times10^{-4}\ \text{cm}} = 0.32\times10^{-12}\ \text{F} = 0.32\ \text{pF}.$$

Die Yield

$$\text{die yield} = \left(1 + \frac{\text{defects per unit area} \times \text{die area}}{\alpha}\right)^{-\alpha} \quad (1.4)$$

α is a parameter that depends upon the complexity of the manufacturing process, and is roughly proportional to the number of masks. $\alpha = 3$ is a good estimate for today's complex CMOS processes. The defects per unit area is a measure of the material and process induced faults. A value between 0.5 and 1 defects/cm^2 is typical these days, but depends strongly upon the maturity of the process.

Example 1.3 Die Yield

Assume a wafer size of 12 inch, a die size of 2.5 cm^2, 1 defects/cm^2, and $\alpha = 3$. Determine the die yield of this CMOS process run.

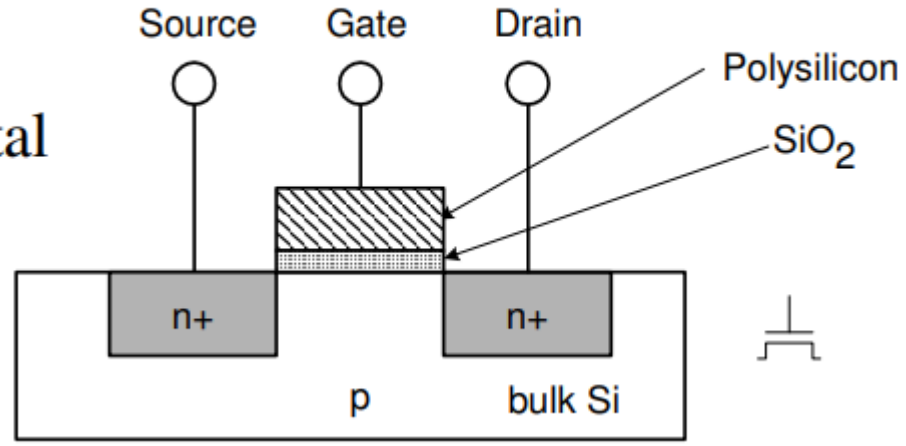
The number of dies per wafer can be estimated with the following expression, which takes into account the lost dies around the perimeter of the wafer.

$$\text{dies per wafer} = \frac{\pi \times (\text{wafer diameter}/2)^2}{\text{die area}} - \frac{\pi \times \text{wafer diameter}}{\sqrt{2 \times \text{die area}}}$$

This means 252 (= 296 - 44) potentially operational dies for this particular example. The die yield can be computed with the aid of Eq. (1.4), and equals 16%! This means that on the average only 40 of the dies will be fully functional.

nMOS Transistor

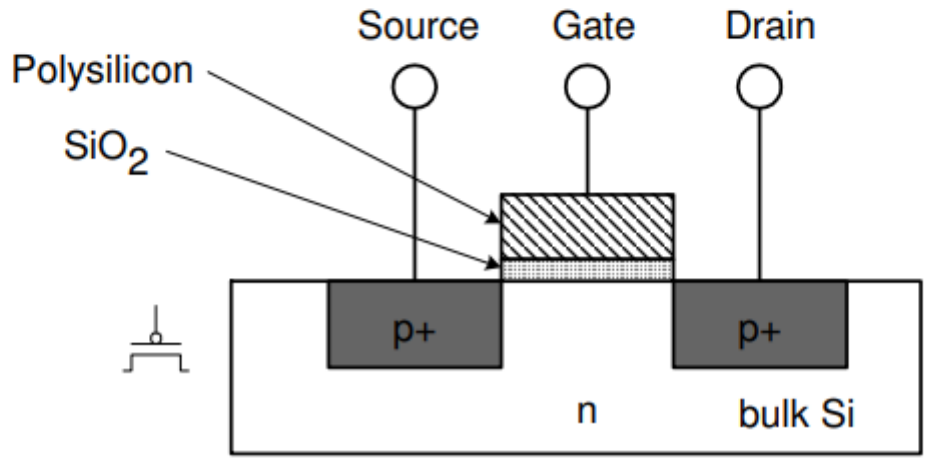
- Four terminals: gate, source, drain, body
- Gate – oxide – body stack looks like a capacitor
  - Gate and body are conductors
  - SiO_2 (oxide) is a very good insulator
  - Called metal – oxide – semiconductor (MOS) capacitor
  - Even though gate is no longer made of metal



PMOS Transistor Fabrication

pMOS Transistor

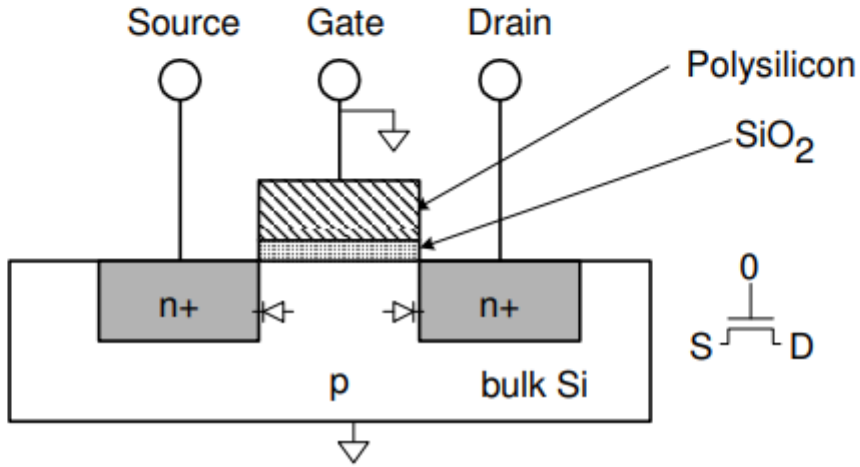
- Similar, but doping and voltages reversed
  - Body tied to high voltage (V_{DD})
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior



Basic NMOSFET with no Bias

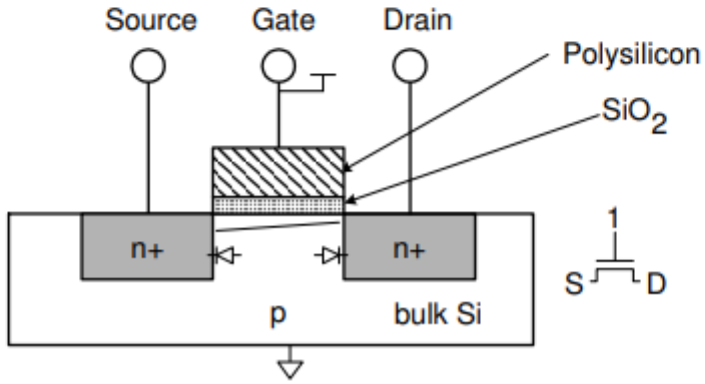
nMOS Operation

- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF



nMOS Operation Cont.

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON

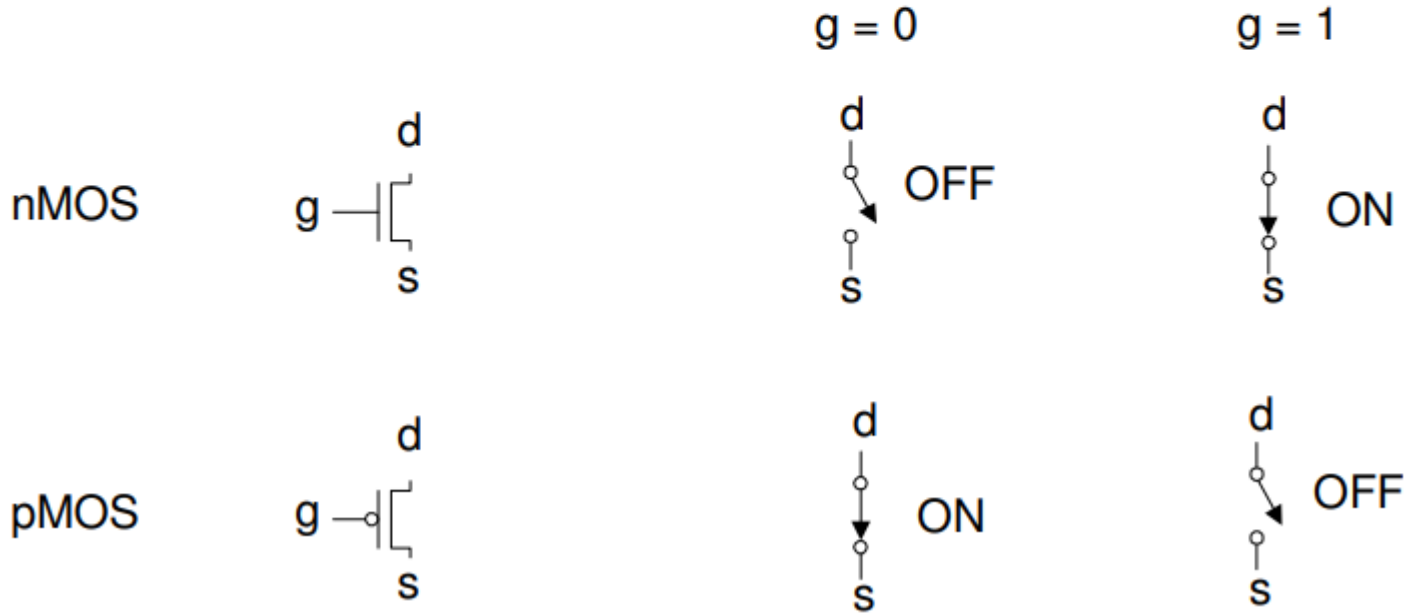


Basic Switching Operation of MOSFET

Transistors as Switches

- We can view MOS transistors as electrically controlled switches
- Voltage at gate controls path from source to drain

What is CMOS?
vs
NMOS or PMOS



Logic Circuits made from CMOS Switches

Switch Behaviour of MOSFET

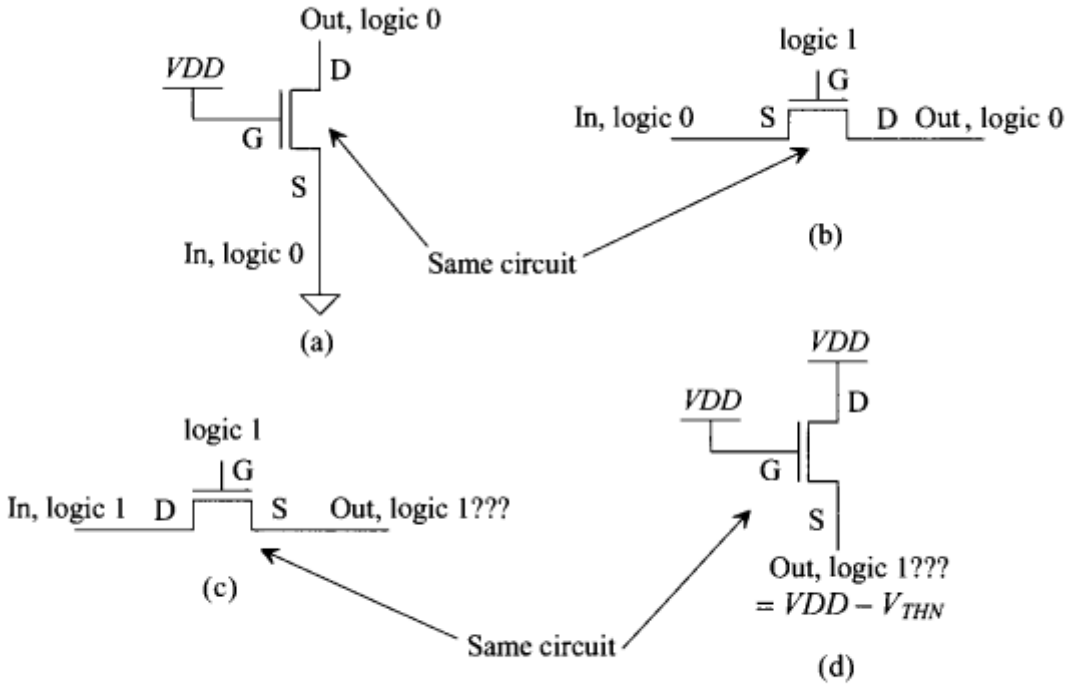


Figure 10.13 Using the NMOS switch as a pass gate.

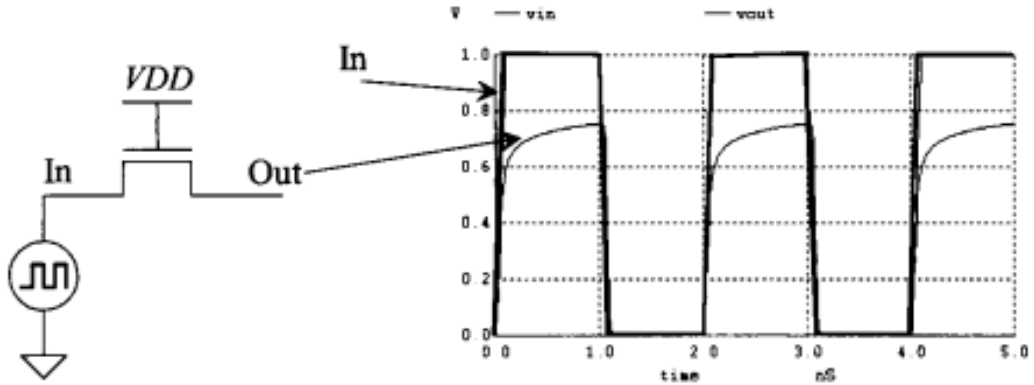


Figure 10.14 The input and output of an NMOS pass gate.

The Pass Transistor Gate

The PMOS Pass Gate

Figure 10.15 shows the operation of the PMOS PG. As expected the operation of the PMOS device is complementary to the NMOS's operation. The PMOS device turns on when its gate is driven to ground. If its gate is pulled to *VDD*, the device is off (and the output is in the Hi-Z state). In Fig. 10.15a the PG is passing a "1" to the output (the V_{SG} is *VDD*). In (b) a "0" is passed to the output. However, noting that the terminals we label drain and source are swapped from (a), the output only gets pulled down to V_{THP}. In (b) the V_{SG} of the MOSFET is V_{THP}. It can be said that a *PMOS PG is good at passing a 1 and bad at passing a 0.*

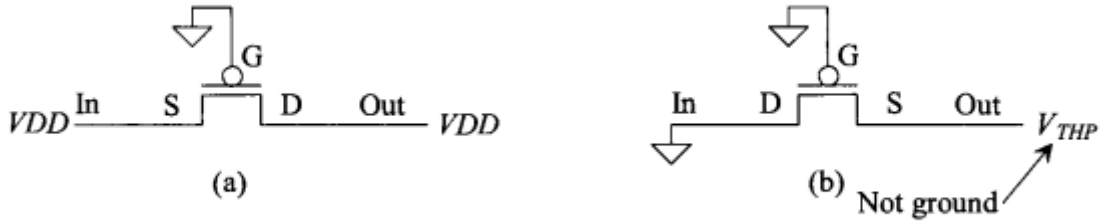


Figure 10.15 How the PMOS device does not pass a logic 0 well.

NMOS vs PMOS as Switch

Example 10.3
Estimate the output voltages in the circuits seen in Fig. 10.16.

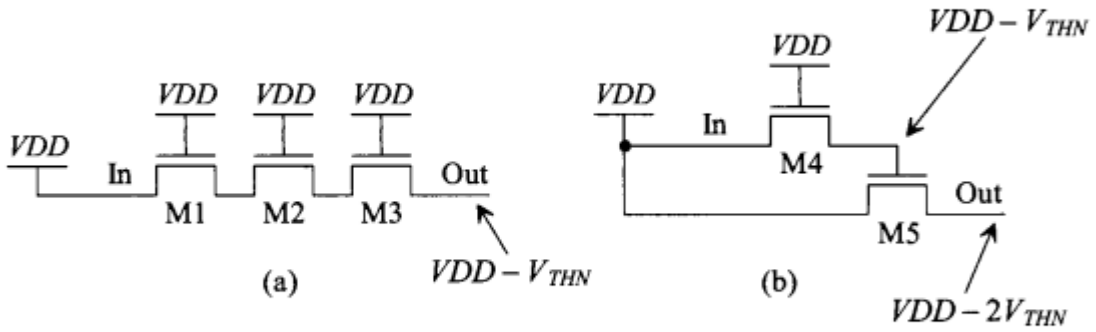


Figure 10.16 Circuits used in Ex. 10.3.

In (a) the output of M1 is $VDD - V_{THN}$. To keep M2 and M3 on, each MOSFET must have a V_{GS} of at least V_{THN}. Because the gates of M2 and M3 are already at VDD, the output of M1 gets passed through M2 and M3 to the final output of the circuit. As seen in the figure this means the overall output is also $VDD - V_{THN}$. We only take one threshold voltage hit.

In (b) the output of the M4 is $VDD - V_{THN}$. This is the gate voltage of M5. For M5 to be on its gate-source voltage must be greater than V_{THN}. The final output is then $VDD - 2V_{THN}$ (again as seen in the figure). ■

Some Examples of Pass-Transistor Logic

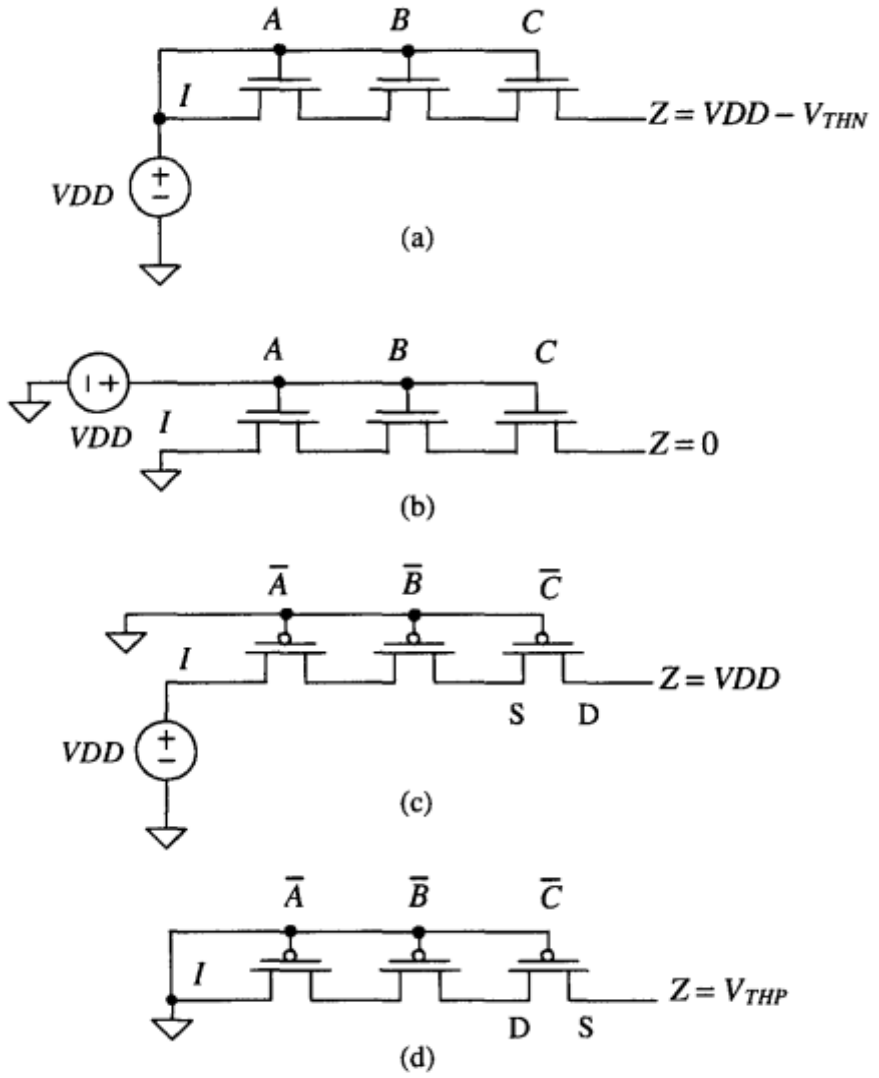


Figure 10.12 DC operation of series-connected MOSFETs.

Readings

- Chapter 1
- Textbook 3rd Edition, CMOS VLSI Design A Circuits and Systems Perspective, Weste and Harris