VLSI Design EE 523
Spring 2026

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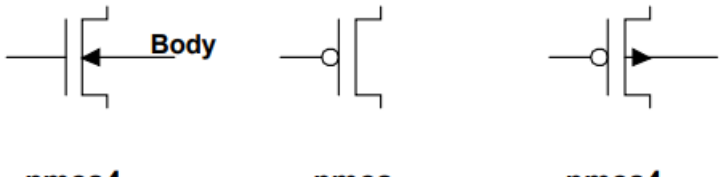
Lecture 7

LTSpice Examples

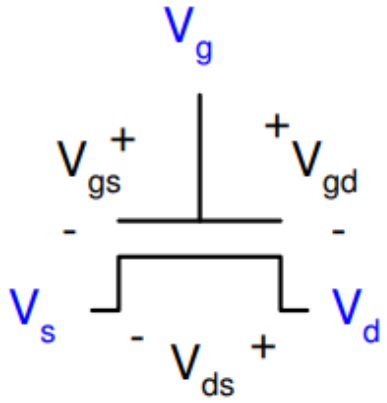
Topics for lecture 6

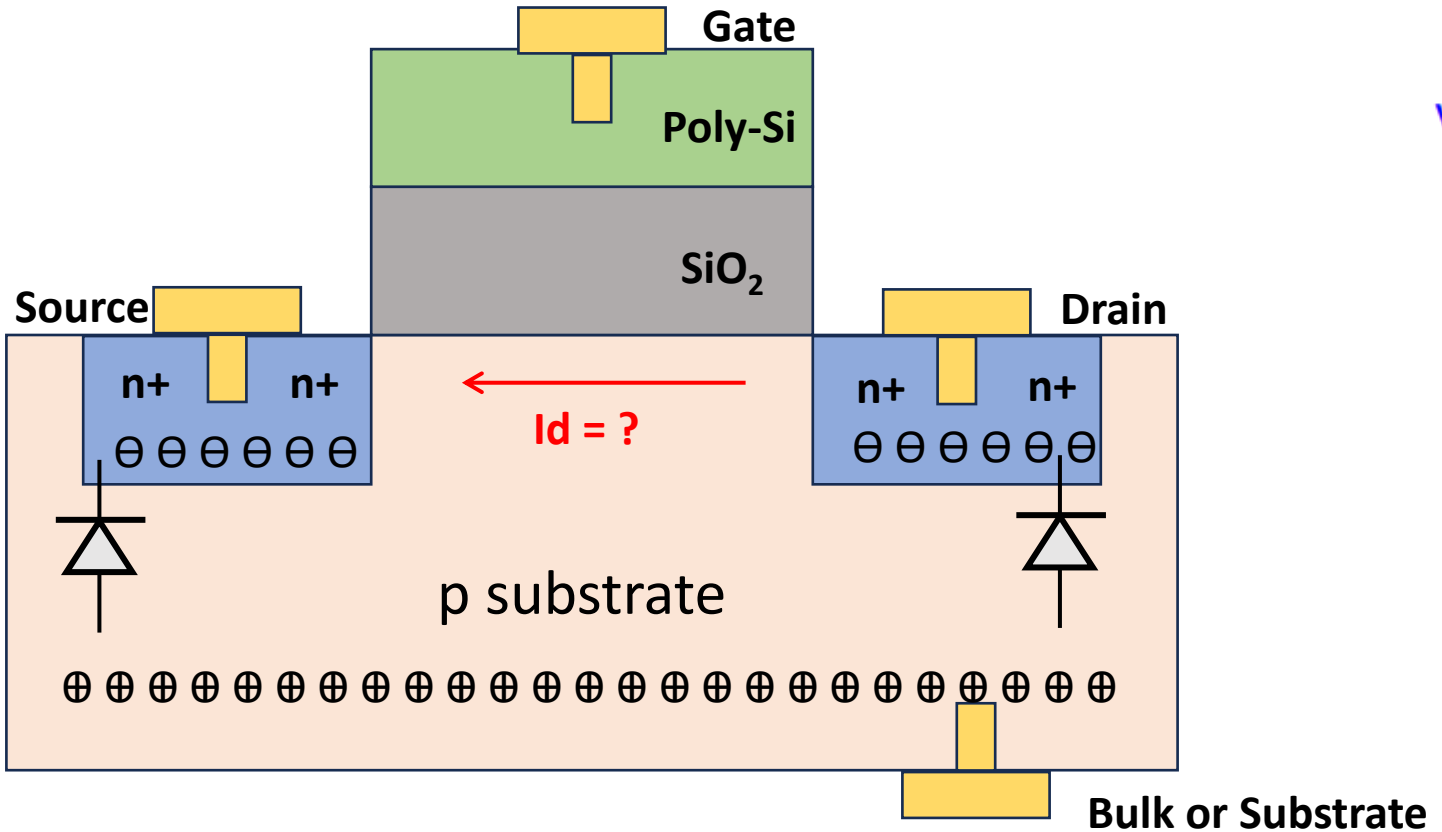
- MOS transistor theory and operation
- Mathematical Equations for:
  - Gate Capacitance, and charge stored
  - Velocity of electron forming current flow
  - W, L ratios in MOS
- Schokley model of MOSFET:
  - Equation for current Ids in three regions of operation
- Quiz 1 today
- Readings: Chapter 2 of textbook

MOS Transistor with Zero Bias Voltages



symbols





Shockley Model for CMOS Transistor

where

$$\beta = \mu C_{ox} \frac{W}{L};\ V_{GT} = V_{gs} - V_t \qquad \textbf{(2.6)}$$

EQ (2.10) summarizes the current in the three regions:

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t & \text{Cutoff} \\ \beta\left(V_{GT} - V_{ds}/2\right)V_{ds} & V_{ds} < V_{dsat} & \text{Linear} \\ \dfrac{\beta}{2}V_{GT}^2 & V_{ds} > V_{dsat} & \text{Saturation} \end{cases} \qquad \textbf{(2.10)}$$

CMOS Output Characteristics

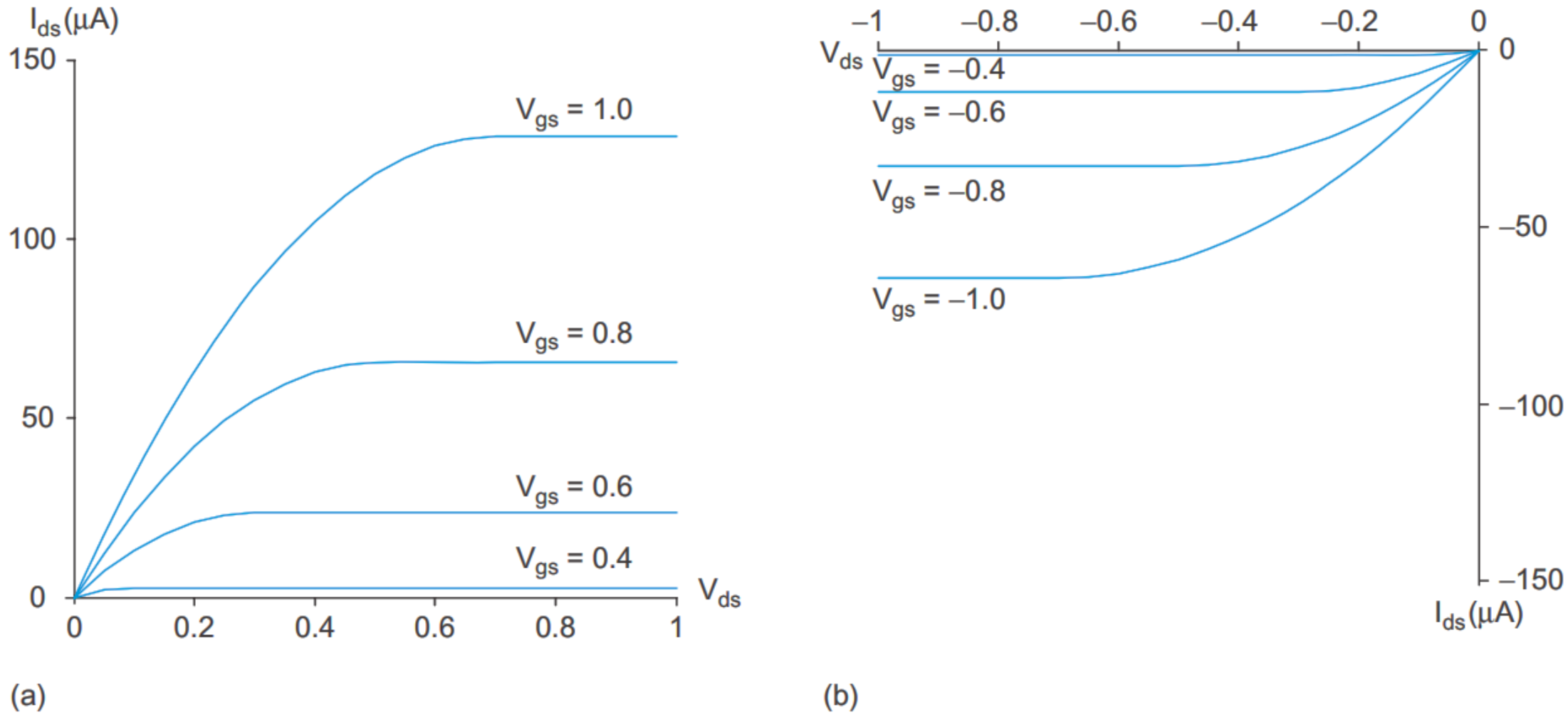


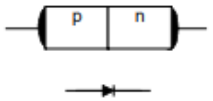
FIGURE 2.7 I-V characteristics of ideal 4/2 λ (a) nMOS and (b) pMOS transistors

Detailed Device Models

Diode at a glance

DIODE QUICK REFERENCE

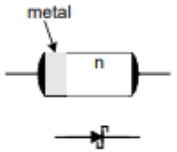
p-n junction diode



$I_S \approx 10^{-15} A$

$V_D \approx 0.7V$

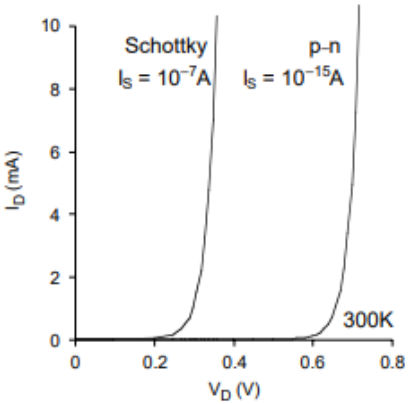
Schottky diode



$I_S \approx 10^{-7} A$

$V_{SBD} \approx 0.3V$

Diode Forward Bias Characteristics



P-n junction diodes are rectifying and can be used as switches in logic gates. Schottky (metal-semiconductor) diodes are also rectifying but are faster switching due to the absence of minority carrier storage effects. Schottky diodes exhibit lower turn-on voltages than p-n junctions (~0.3V versus ~0.7V for silicon devices).

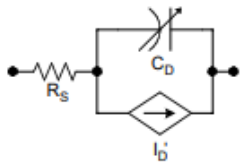
Zero Bias Characteristics

$$V_{bi} = \frac{kT}{q}\ln\left(\frac{N_a N_d}{n_i^2}\right) \qquad W = \sqrt{\frac{2\varepsilon_s V_{bi}}{q}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)} \qquad C_T = \frac{\varepsilon_s A}{W} = A\sqrt{\frac{q\varepsilon_s}{2V_{bi}}\left(\frac{1}{N_a}+\frac{1}{N_d}\right)^{-1}}$$

Forward Bias Characteristics

$$I = I_0\left(e^{qV/kT}-1\right) \qquad I_0 \approx \frac{qAD_n n_i^2}{N_a W_B} \text{ (short-base diode)}$$

SPICE Model



$$I_D' = IS\left[\exp\left(\frac{V_D'}{NV_T}\right)-1\right] \qquad V_D = V_D' + I_D RS$$

$$C_D = TT\frac{IS}{NV_T}\exp\left(\frac{V_D'}{NV_T}\right)+\frac{CJO}{\left(1-\frac{V_D'}{VJ}\right)^M}$$

Charge Control Model and Large Signal Switching Behavior

$$-i_n(0,t) = \frac{dQ_B}{dt}+\frac{Q_B}{\tau_F}-C_t\frac{dv}{dt} \qquad t_s = \tau_F\left[\left(1+\frac{I_F}{I_R}\right)-\left(1+\frac{\tau_R}{\tau_F}\right)\right]$$

$f = 10^{-15}$ $p = 10^{-12}$ $n = 10^{-9}$ $\mu = 10^{-6}$ $m = 10^{-3}$ $k = 10^{3}$ $M = 10^{6}$ $G = 10^{9}$

NMOS Transistor W and L and Biasing

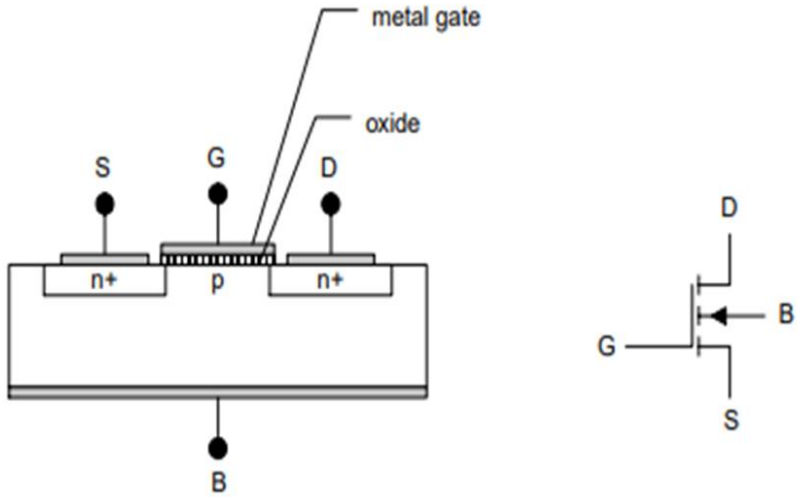


FIGURE 7.1
Enhancement-type n-channel metal oxide–semiconductor field-effect transistor (MOSFET) and circuit symbol.

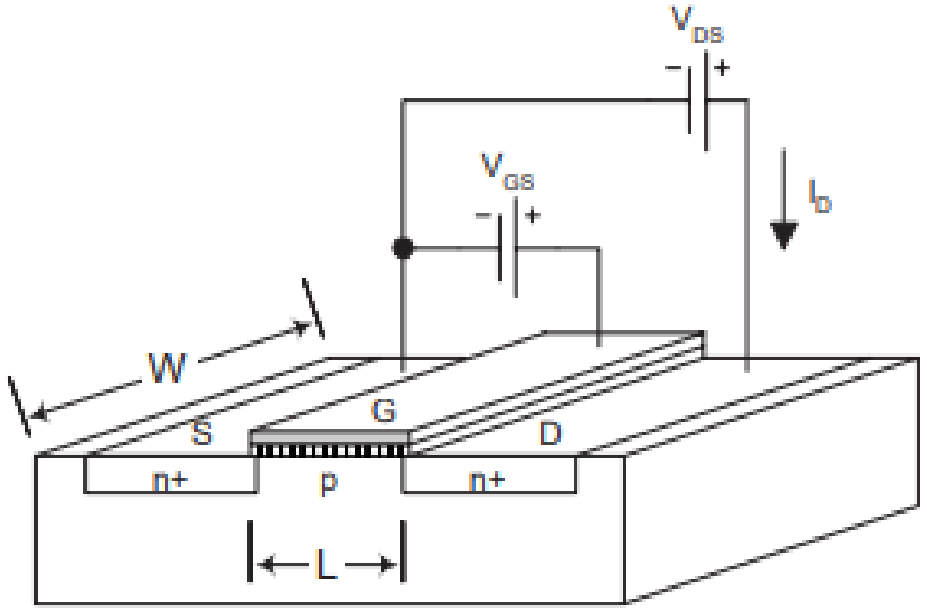


FIGURE 7.7
N-channel enhancement-type MOSFET with bias.

Characteristic curves of MOS

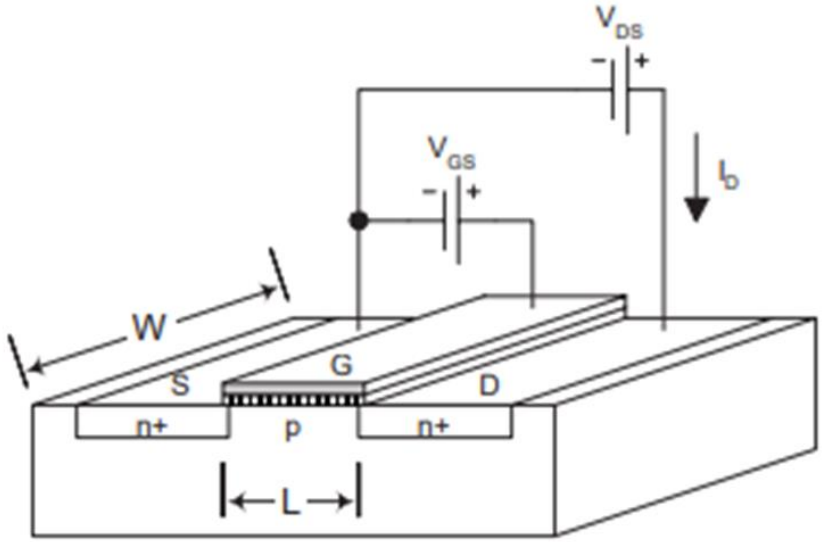


FIGURE 7.7
N-channel enhancement-type MOSFET with bias.

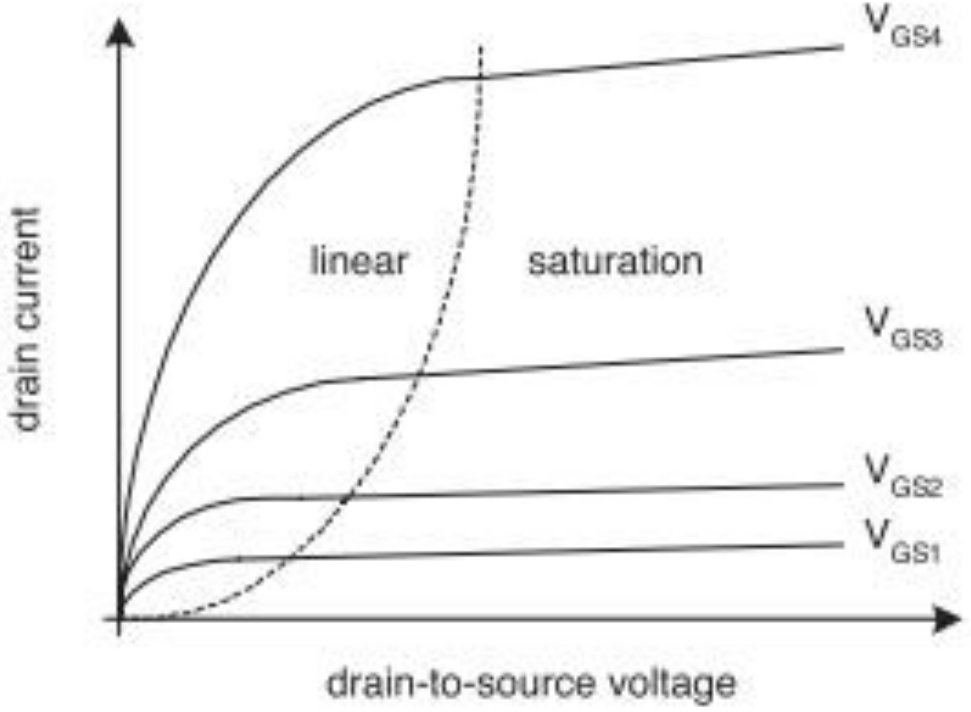


FIGURE 7.8
Characteristic curves for a MOSFET.

Spice Model of MOS transistor

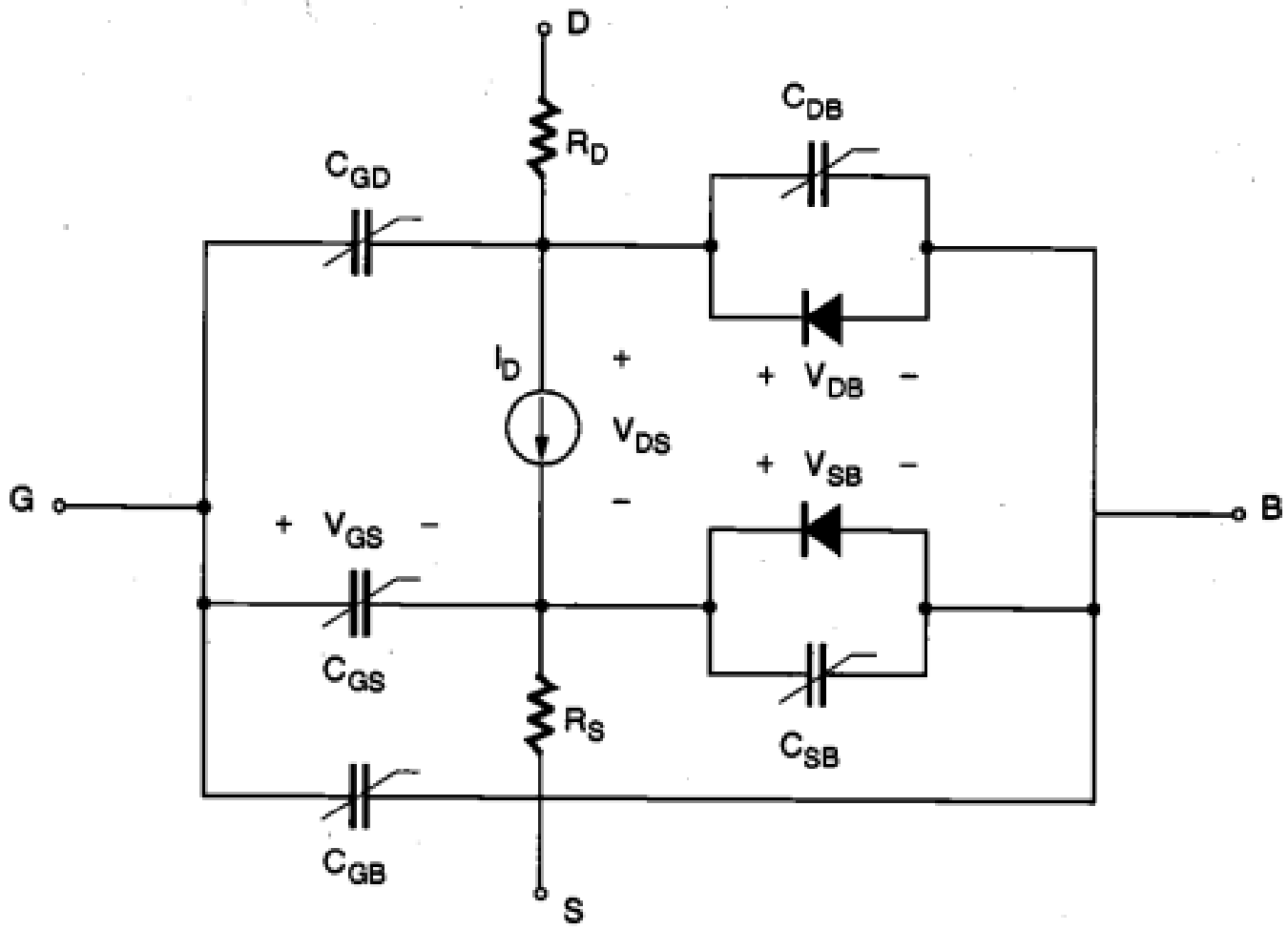


Figure 4.1. Equivalent circuit structure of the LEVEL 1 MOSFET model in SPICE.

NMOS Model Equations – near to real behavior

4.2. The LEVEL 1 Model Equations

The LEVEL 1 model is the simplest current-voltage description of the MOSFET, which is basically the GCA-based quadratic model originally proposed by Shichman and Hodges. The equations used for the LEVEL 1 n-channel MOSFET model in SPICE are as follows.

Linear Region

$$I_D = \frac{k'}{2}\cdot\frac{W}{L_{eff}}\cdot\left[2\cdot(V_{GS}-V_T)V_{DS}-V_{DS}^2\right]\cdot(1+\lambda V_{DS}) \quad \text{for} \quad V_{GS}\geq V_T \quad \text{and} \quad V_{DS}<V_{GS}-V_T \tag{4.1}$$

Saturation Region

$$I_D = \frac{k'}{2}\cdot\frac{W}{L_{eff}}\cdot(V_{GS}-V_T)^2\cdot(1+\lambda\cdot V_{DS}) \quad \text{for} \quad V_{GS}\geq V_T \quad \text{and} \quad V_{DS}\geq V_{GS}-V_T \tag{4.2}$$

Some parameters of NMOS Level 1 model

SPICE Level 1 Model Parameters for the MOSFET

Symbol	SPICE Name	Description	Units	Default	Typical
k'	KP	Process transconductance parameter	A/V^2	1E-4	1E-4
V_{TO}	VTO	Threshold voltage with $V_{BS} = 0$	V	0	0.5
γ	GAMMA	Body effect coefficient	$V^{1/2}$	0	1E-4
$2\phi_F$	PHI		V	1.0	1.0
C_{GSO}	CGSO	Gate–source capacitance per unit gate width	F/m	0	
C_{GDO}	CGDO	Gate–source capacitance per unit gate width	F/m	0	
C_{GBO}	CGBO	Gate–source capacitance per unit gate width	F/m	0	
C_{BSO}	CBSO	Gate–source capacitance per unit gate width	F/m	0	

Some parameters of MOS Level 2 model

SPICE Level 2 model parameters for a typical 0.8 μm CMOS process:

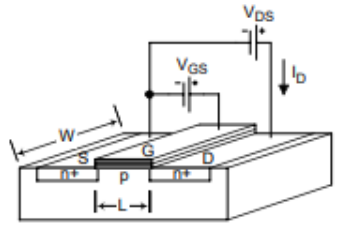
```
.MODEL MODN NMOS LEVEL=2
+NLEV=0
+CGSO=0.350e-09   CGDO=0.350e-09   CGBO=0.150e-09
+CJ=0.300e-03     MJ=0.450e+00     CJSW=0.250e-09
+MJSW=0.330e+00   IS=0.000e+00     N=1.000e+00
+NDS=1.000e+12    VNDS=0.000e+00
+JS=0.010e-03     PB=0.850e+00     RSH=25.00e+00
+TOX=15.50e-09    XJ=0.080e-06
+VTO=0.850e+00    NFS=0.835e+12    NSUB=64.00e+15
+NEFF=10.00e+00   UTRA=0.000e+00
+UO=460.0e+00     UCRIT=38.00e+04  UEXP=0.325e+00
+VMAX=62.00e+03   DELTA=0.250e+00  KF=0.275e-25
+LD=0.000e-06     WD=0.600e-06     AF=1.500e+00
+BEX=-1.80e+00    TLEV=1.000e+00   TCV=1.400e-03
```

```
.MODEL MODP PMOS LEVEL=2
+NLEV=0
+CGSO=0.350e-09   CGDO=0.350e-09   CGBO=0.150e-09
+CJ=0.500e-03     MJ=0.470e+00     CJSW=0.210e-09
+MJSW=0.290e+00   IS=0.000e+00     N=1.000e+00
+NDS=1.000e+12    VNDS=0.000e+00
+JS=0.040e-03     PB=0.800e+00     RSH=47.00e+00
+TOX=15.00e-09    XJ=0.090e-06
+VTO=-.725e+00    NFS=0.500e+12    NSUB=32.80e+15
+NEFF=2.600e+00   UTRA=0.000e+00
+UO=160.0e+00     UCRIT=30.80e+04  UEXP=0.350e+00
+VMAX=61.00e+03   DELTA=0.950e+00  KF=0.470e-26
+LD=-.075e-06     WD=0.350e-06     AF=1.600e+00
+BEX=-1.50e+00    TLEV=1.000e+00   TCV=-1.80e-03
```

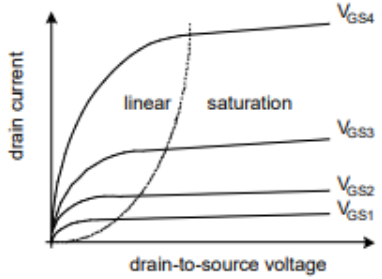
MOS reference

FIELD-EFFECT TRANSISTORS QUICK REFERENCE

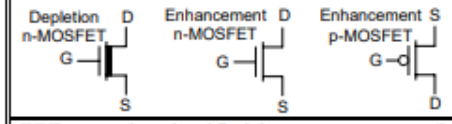
Enhancement n-MOSFET



n-MOSFET characteristics



MOSFET Symbols



FETs may be classified by gate structure (MOSFETs, MESFETs, JFETs), as enhancement-type or depletion type, and by channel carrier (n-channel or p-channel). FETs are majority carrier devices. FETs have three modes of operation: cutoff, linear (or ohmic), and saturation.

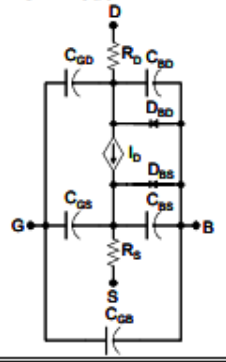
n-MOSFET Modes of Operation

cutoff	$V_{GS} < V_T$		$I_D = 0$
linear	$V_{GS} > V_T$	$V_{GS} - V_T > V_{DS}$	$I_D = K\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$ $V_{DS} = (V_{GS} - V_T) - \sqrt{(V_{GS} - V_T)^2 - \frac{2I_D}{K}}$
saturation	$V_{GS} > V_T$	$V_{GS} - V_T < V_{DS}$	$I_D = \frac{K}{2}(V_{GS} - V_T)^2$

Device Transconductance Parameters

$$K_N = \frac{W_N}{L_N} k_N' \qquad k_N' = \frac{\mu_n \varepsilon_{OX}}{t_{OX}} \qquad K_P = \frac{W_P}{L_P} k_P' \qquad k_P' = \frac{\mu_p \varepsilon_{OX}}{t_{OX}}$$

SPICE Model



$$V_T = VTO + GAMMA\left(\sqrt{PHI + V_{SB}} - \sqrt{PHI}\right)$$

$$I_D = \frac{KP}{2}\frac{width}{length}(V_{GS} - V_T)^2(1 + V_{DS}LAMBDA)$$

$$I_D = \frac{KP}{2}\frac{width}{length}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right](1 + V_{DS}LAMBDA)$$

$C_{GS} = width \times CGSO$ $\quad C_{GD} = width \times CGDO$ $\quad C_{GB} = width \times CGBO$

$C_{BD} = width \times CBDO$ $\quad C_{BS} = width \times CBSO$

Design Rules

$\mu_n = 580 cm^2 V^{-1} s^{-1}$ $\quad \mu_p = 230 cm^2 V^{-1} s^{-1}$ $\quad \varepsilon_{OX} = 3.9\varepsilon_0$ $\quad$ Å $= 10^{-8}$ cm

f $= 10^{-15}$ $\quad$ p $= 10^{-12}$ $\quad$ n $= 10^{-9}$ $\quad$ μ $= 10^{-6}$ $\quad$ m $= 10^{-3}$ $\quad$ k $= 10^{3}$ $\quad$ M $= 10^{6}$ $\quad$ G $= 10^{9}$

CMOS Inverter characteristics

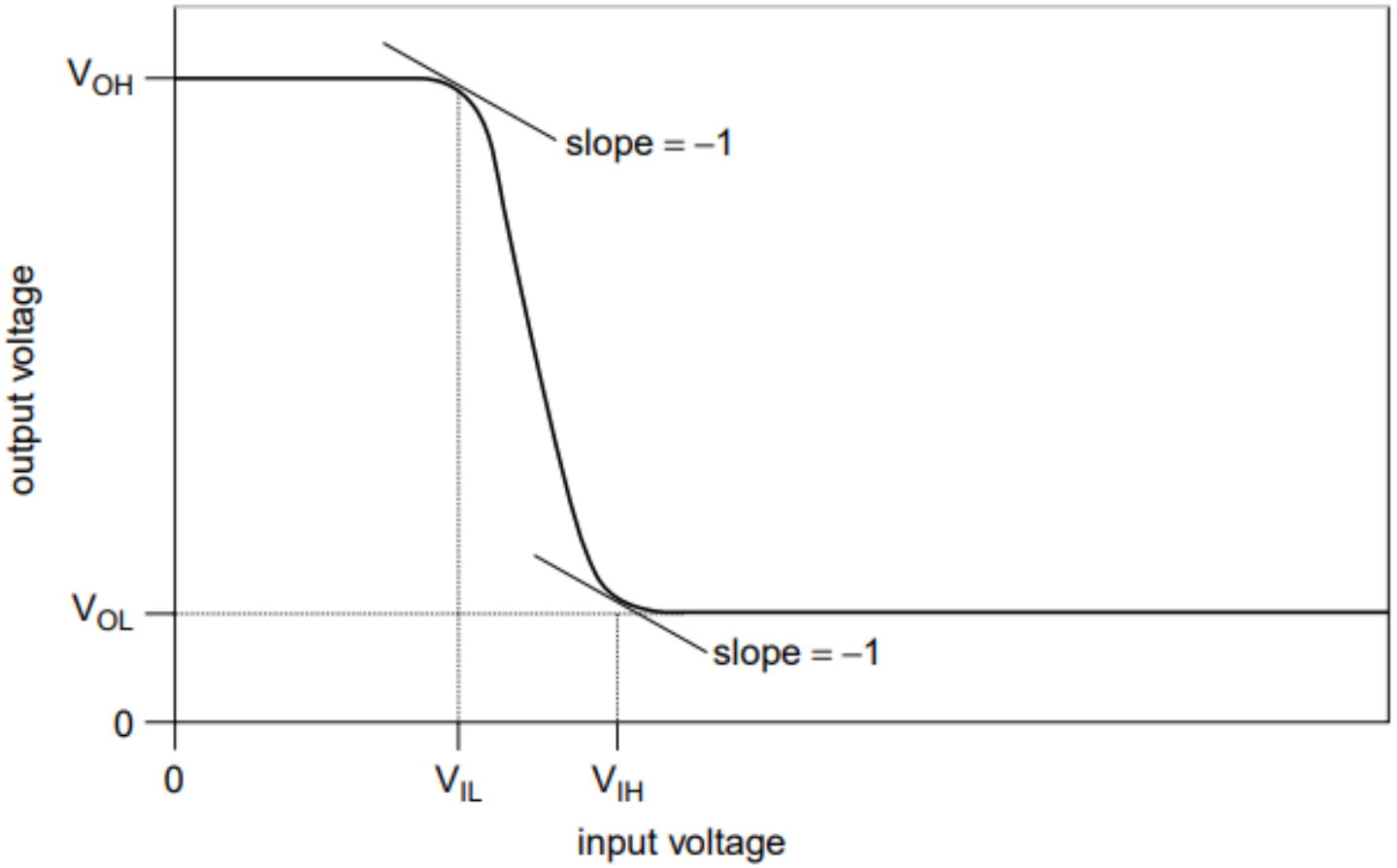
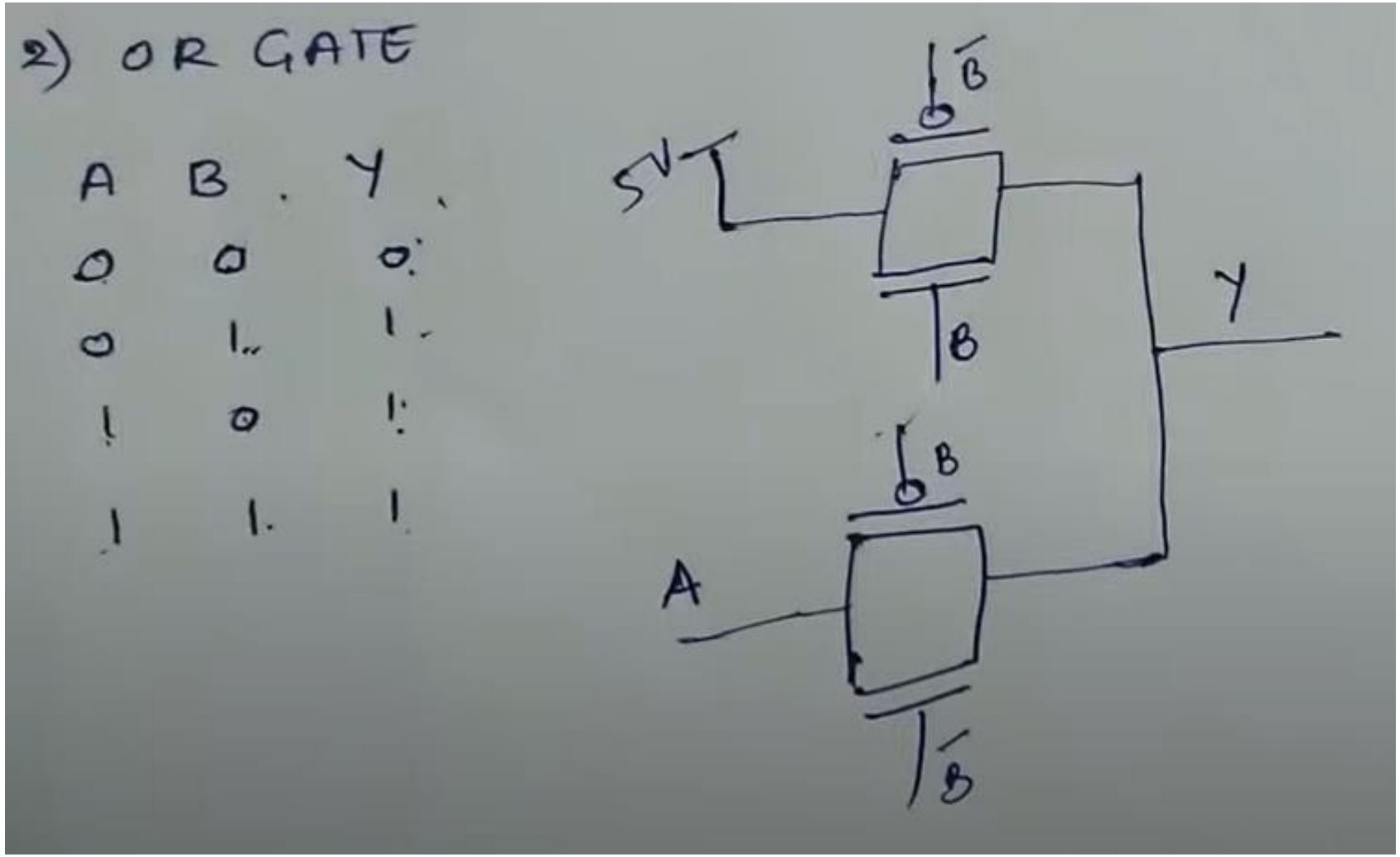


FIGURE 1.12
Voltage transfer characteristic for an inverter.

OR gate using transmission gate logic



Make a CMOS Inv based Oscillator

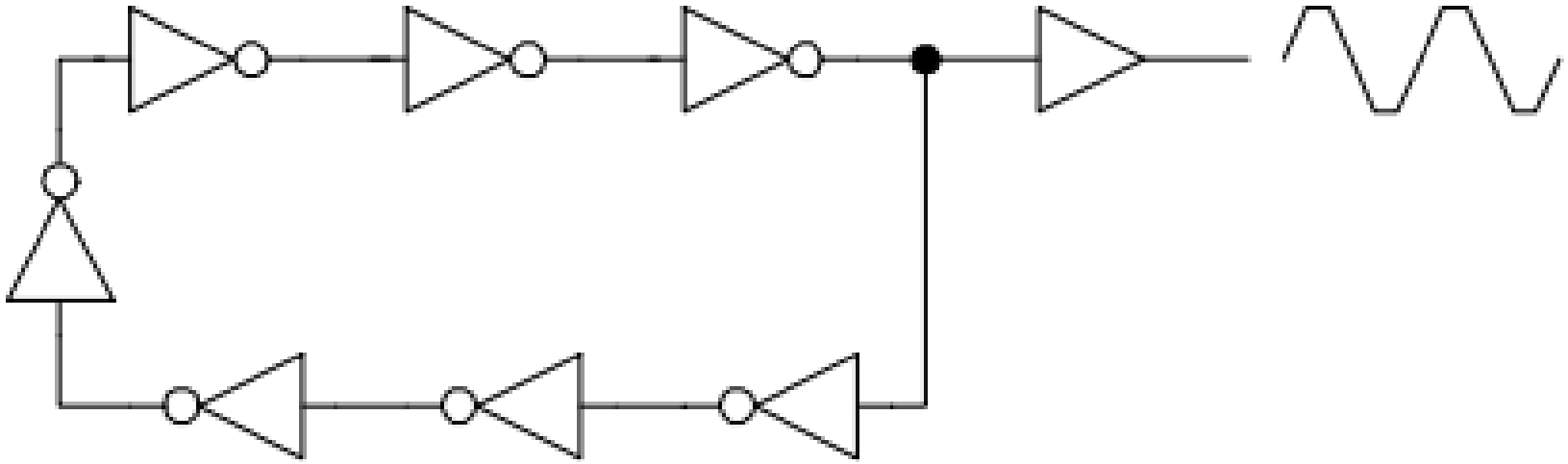


FIGURE 1.16
Seven-stage ring oscillator with a buffered output.

Important Parameters 0.18u

4.10 Summary

Useful technology parameters for 0.18 μm CMOS:

$$\mu_n = 270\ \text{cm}^2/\text{V-s}, \quad \mu_p = 70\ \text{cm}^2/\text{V-s}, \quad t_{ox} = 35\ \text{Å},$$

$$C_{ox} = 1.0\ \mu\text{F/cm}^2, \quad V_{TN} = 0.5\ \text{V}, \quad V_{TP} = -0.5\ \text{V}$$

$$E_{CN}L = 1.2\ \text{V}, \quad E_{CP}L = 4.8\ \text{V}, \quad v_{\text{sat}} = 8 \times 10^6\ \text{cm/s},$$

$$V_{DD} = 1.8\ \text{V}, \quad 2|\phi_F| = 0.85\ \text{V}, \quad \gamma = 0.3V^{1/2}, L = 2\lambda = 200\ \text{nm}$$

Useful technology parameters for 0.13 μm CMOS:

$$\mu_n = 270\ \text{cm}^2/\text{V-s}, \quad \mu_p = 70\ \text{cm}^2/\text{V-s}, \quad t_{ox} = 22\ \text{Å},$$

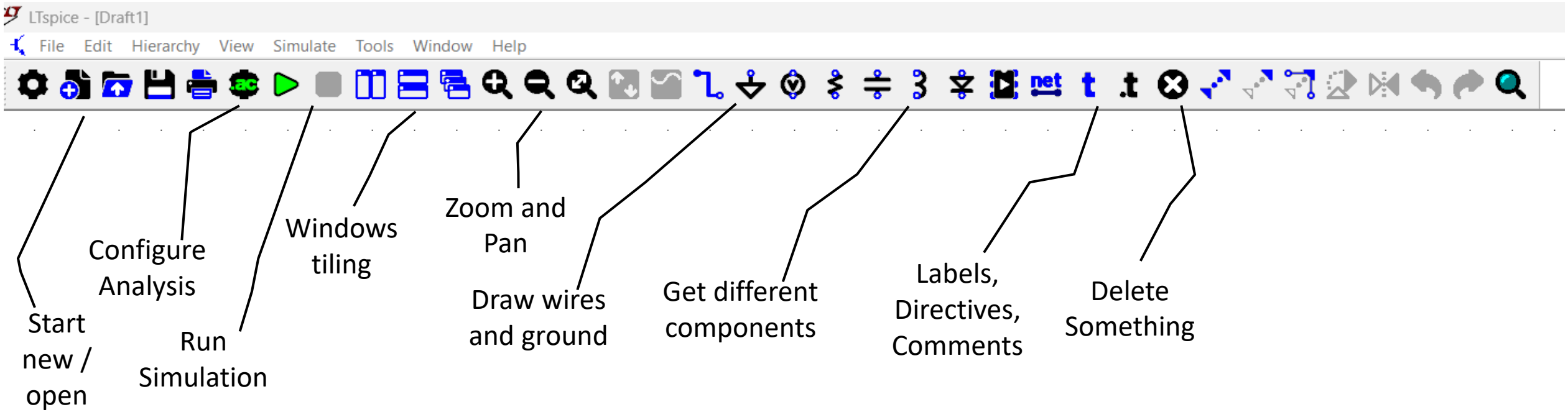
$$C_{ox} = 1.6\ \mu\text{F/cm}^2, \quad V_{TN} = 0.4\ \text{V}, \quad V_{TP} = -0.4\ \text{V}$$

$$E_{CN}L = 0.6\ \text{V}, \quad E_{CP}L = 2.4\ \text{V}, \quad v_{\text{sat}} = 8 \times 10^6\ \text{cm/s},$$

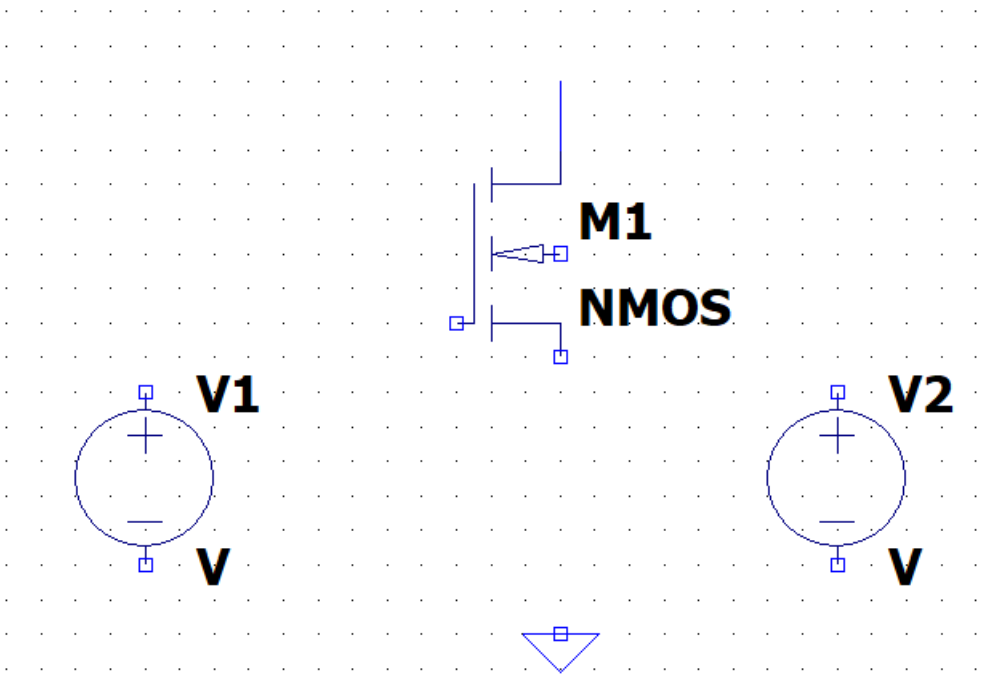
$$V_{DD} = 1.2\ \text{V}, \quad 2|\phi_F| = 0.88\ \text{V}, \quad \gamma = 0.2V^{1/2}, L = 2\lambda = 100\ \text{nm}$$

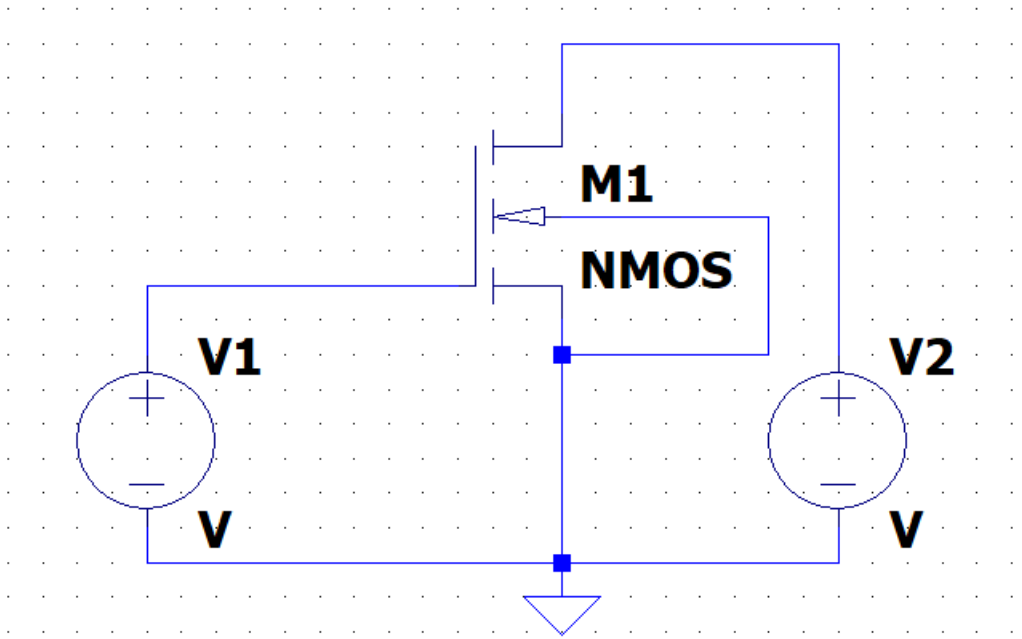
Getting Started with LTSpice

LTSpice Interface Startup Screen



Make NMOS Circuit





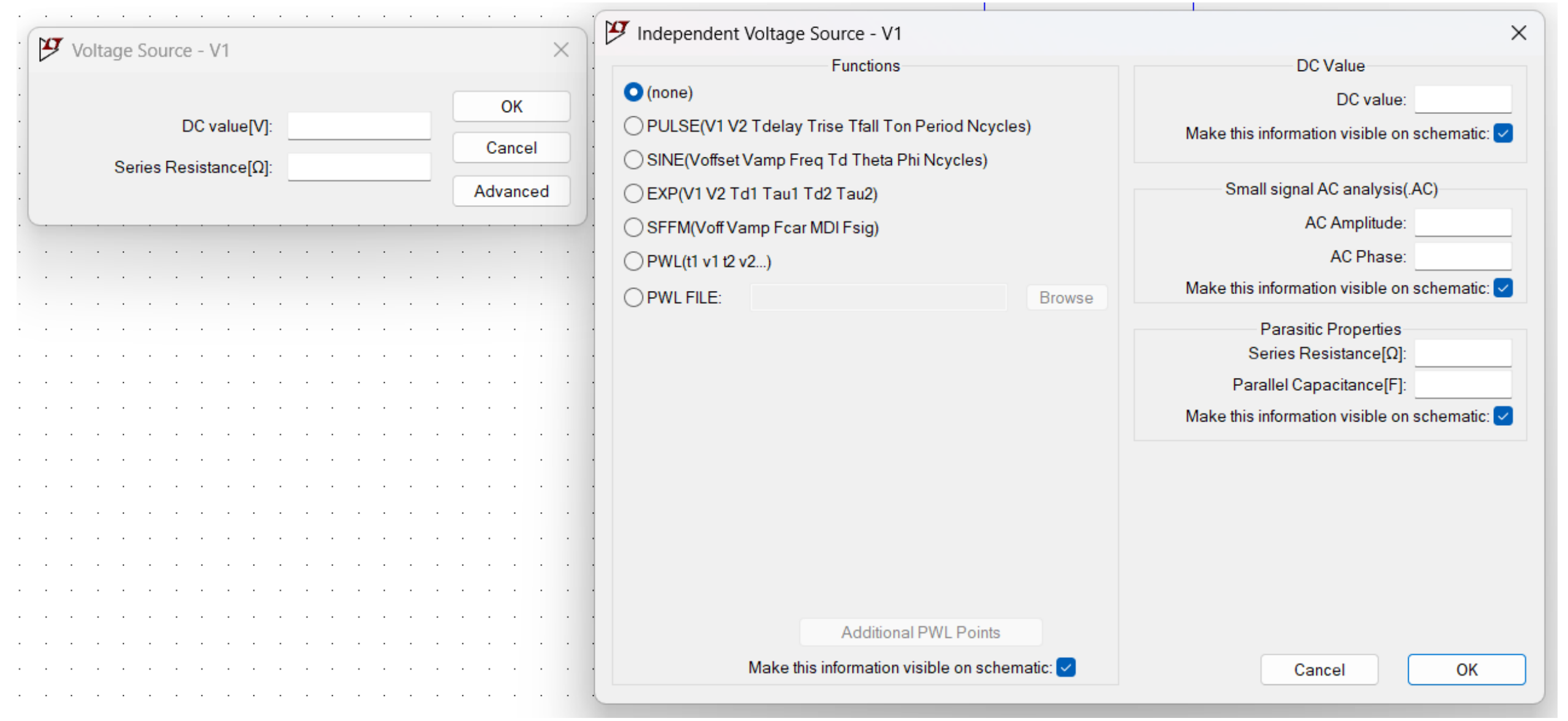
We can find NMOS (3 Terminal) and NMOS4 (4 Terminal) in the Default Component Library

Before Analysis

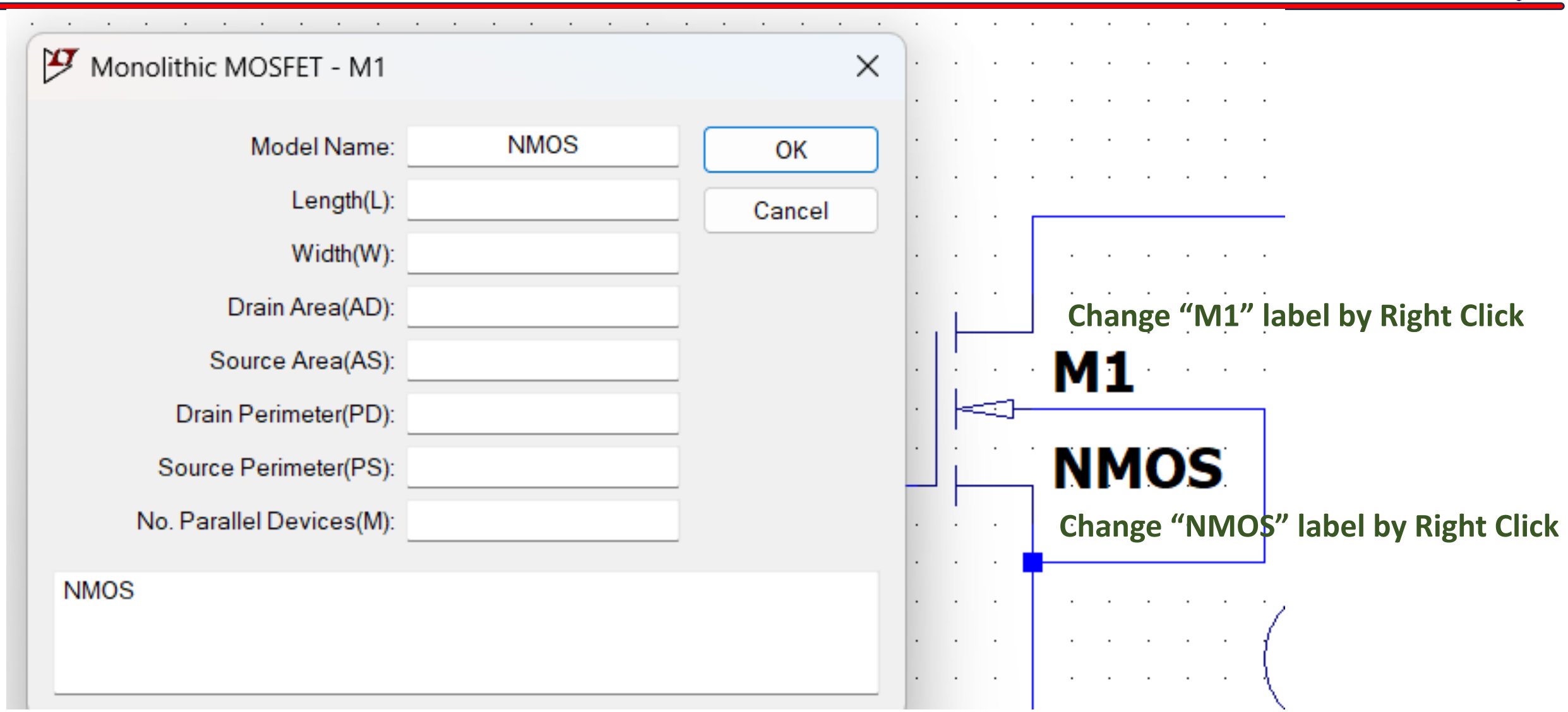
Case 1: Default Component Library

Configure all voltage sources
Configure all devices e.g. transistors

Right Click on Voltage Source → Advanced



Right Click on NMOS Transistor to Configure



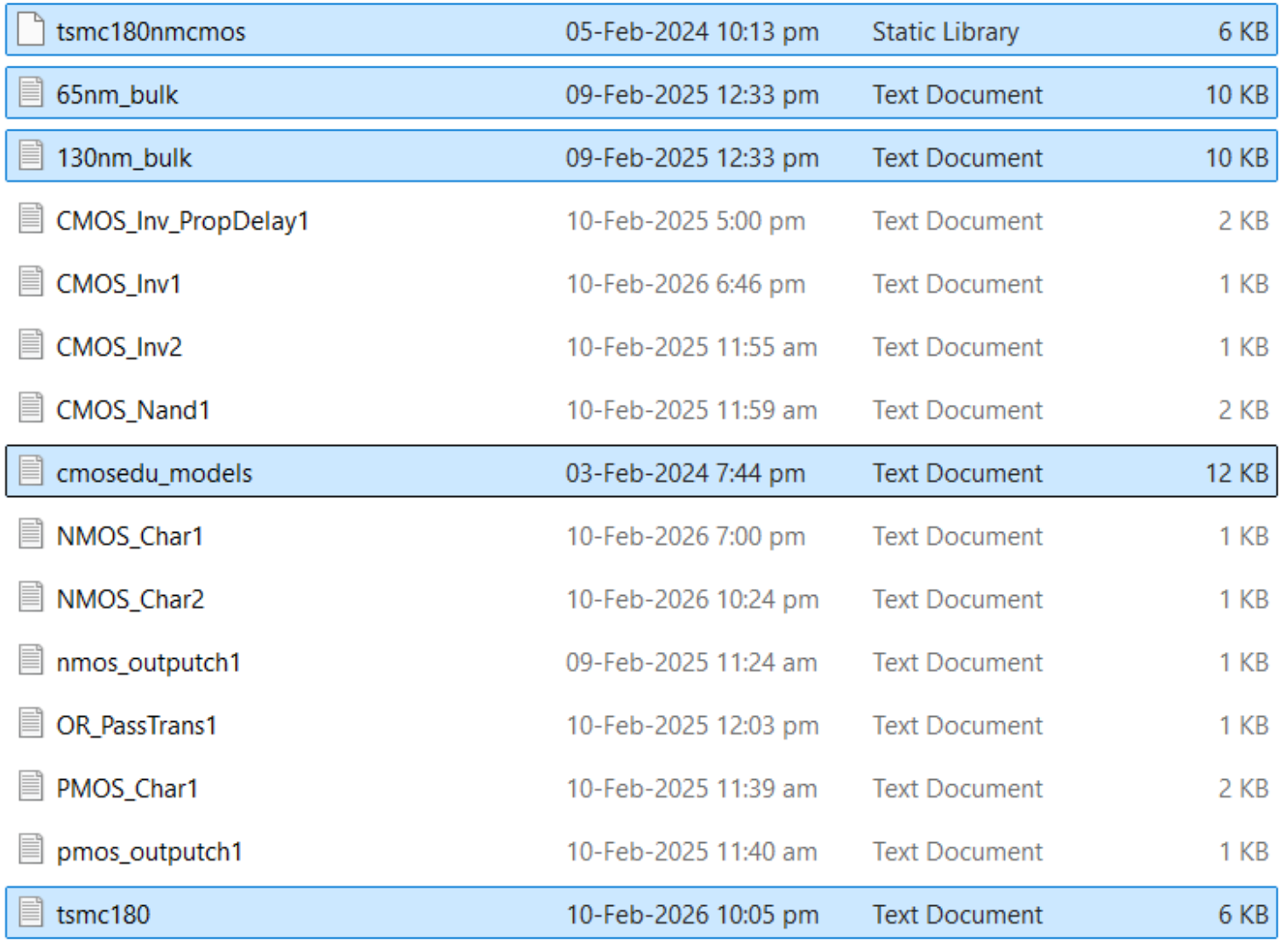
Adding Device Models for VLSI

- **Make a working folder on Desktop**
- **Put model files in this folder**

- **You can configure paths and colours in Tools → Settings**

- **Some model file needs to be included In the Spice Deck**

Model files Highlighted text files in folder



How do Device Model files look like

Examine cmosedu_models.txt file

We find following models:

.MODEL N_1u NMOS LEVEL = 3

.MODEL P_1u PMOS LEVEL = 3

.model N_50n nmos level = 54

.model P_50n pmos level = 54

Examine tsmc180.txt file

We find following models:

.MODEL NMOS NMOS (LEVEL = 49

.MODEL PMOS PMOS (LEVEL = 49

.model N_50n nmos level = 54

.model P_50n pmos level = 54

Examine other model files:

tsmcnmcmos.lib

130nm_bulk.txt

.....

So on

How to add in LTSpice and Do Basic Simulations

- Use Spice Directive

.inc cmosedu_models.txt

- FOR Transistor Characteristics
- We need to SWEEP VDS and VGS and get NMOS operating curves
- Use either these Spice Directives:
- **Approach 1:** Give DC Sweep to both voltages

.dc VDS 0 2.5 0.1 VGS 0 2.5 0.25

- **Approach 2:** Give a variable name {VGIN} to VGS, use .STEP and .dc

.dc VDS 0 1.8 0.1

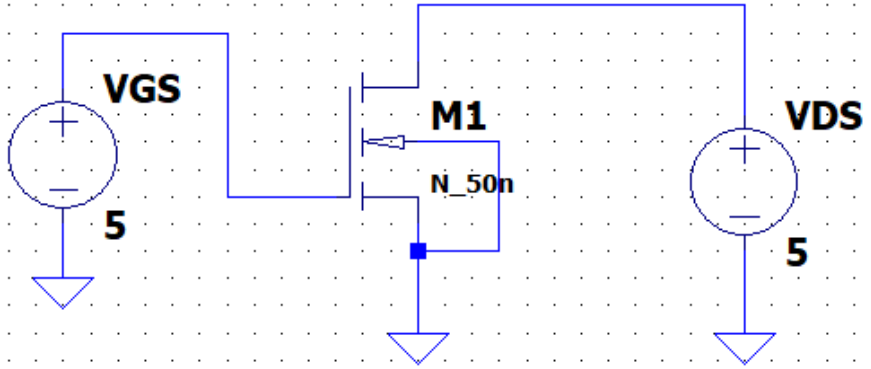
.STEP PARAM VGIN 0.0 1.8 0.2

Examples of Sweeping Voltages

Blue text is ‘Comment’

.inc cmosedu_models.txt

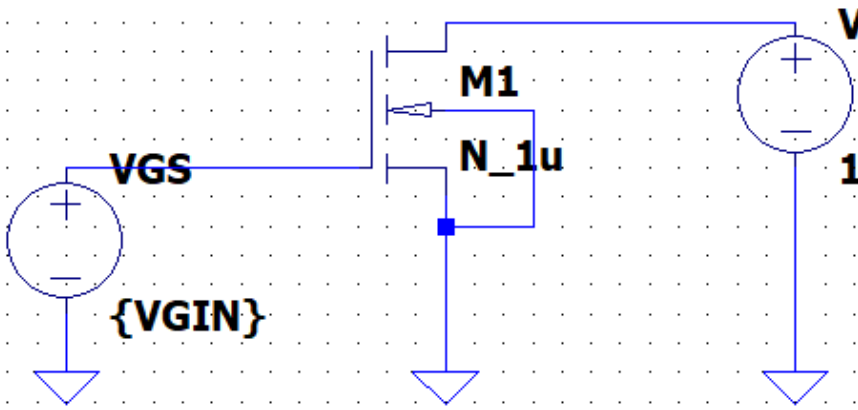
.dc VDS 0 2.5 0.1 VGS 0 2.5 0.25



Use .STEP Param {voltage name} to vary both VGS and VDS

models in cmosedu_models.txt are N_1u N_50n P_1u P_50n

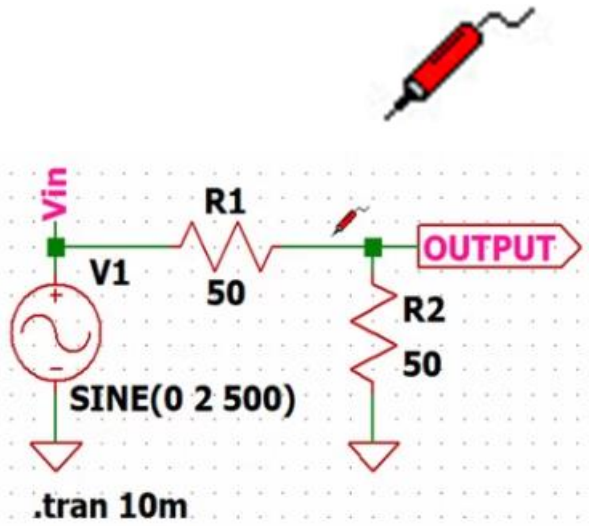
NMOS Characterization with different model files

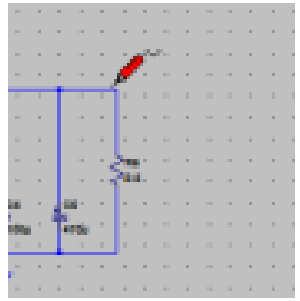


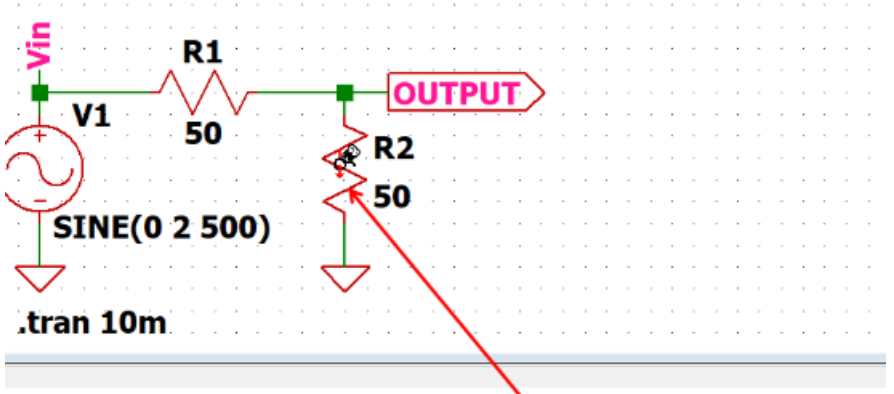
.inc cmosedu_models.txt
.dc VDS 0 1.8 0.1
.STEP PARAM VGIN 0.0 1.8 0.2
tsmc180nmcmos.lib contains .MODEL TSMC180nmN NMOS
.inc tsmc180nmcmos.lib

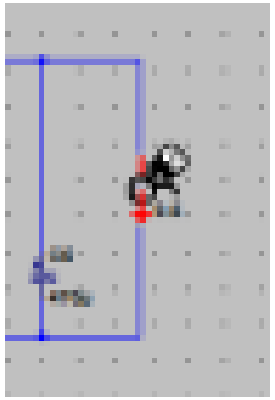
How to Simulate and View Waveforms

- Press Green Triangle to ‘RUN’ simulation
- A blank window will appear over the circuit
- Bring cursor over a wire or a source
- Either voltage probe or current probe will show
- Pressing mouse will select that value for display







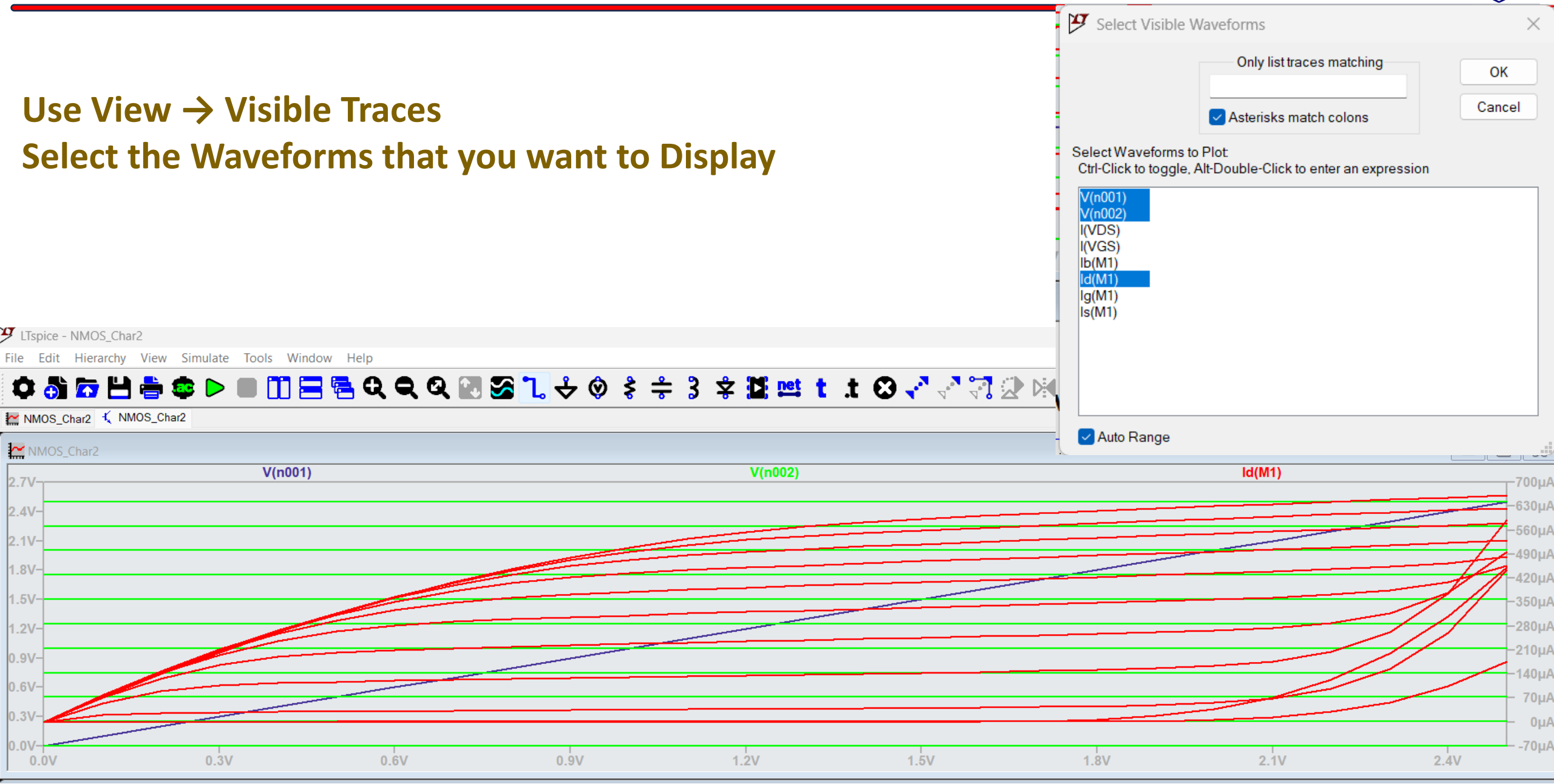


Move the cursor to R2 to change to a current probe

Waveform Display – As selected by Probes

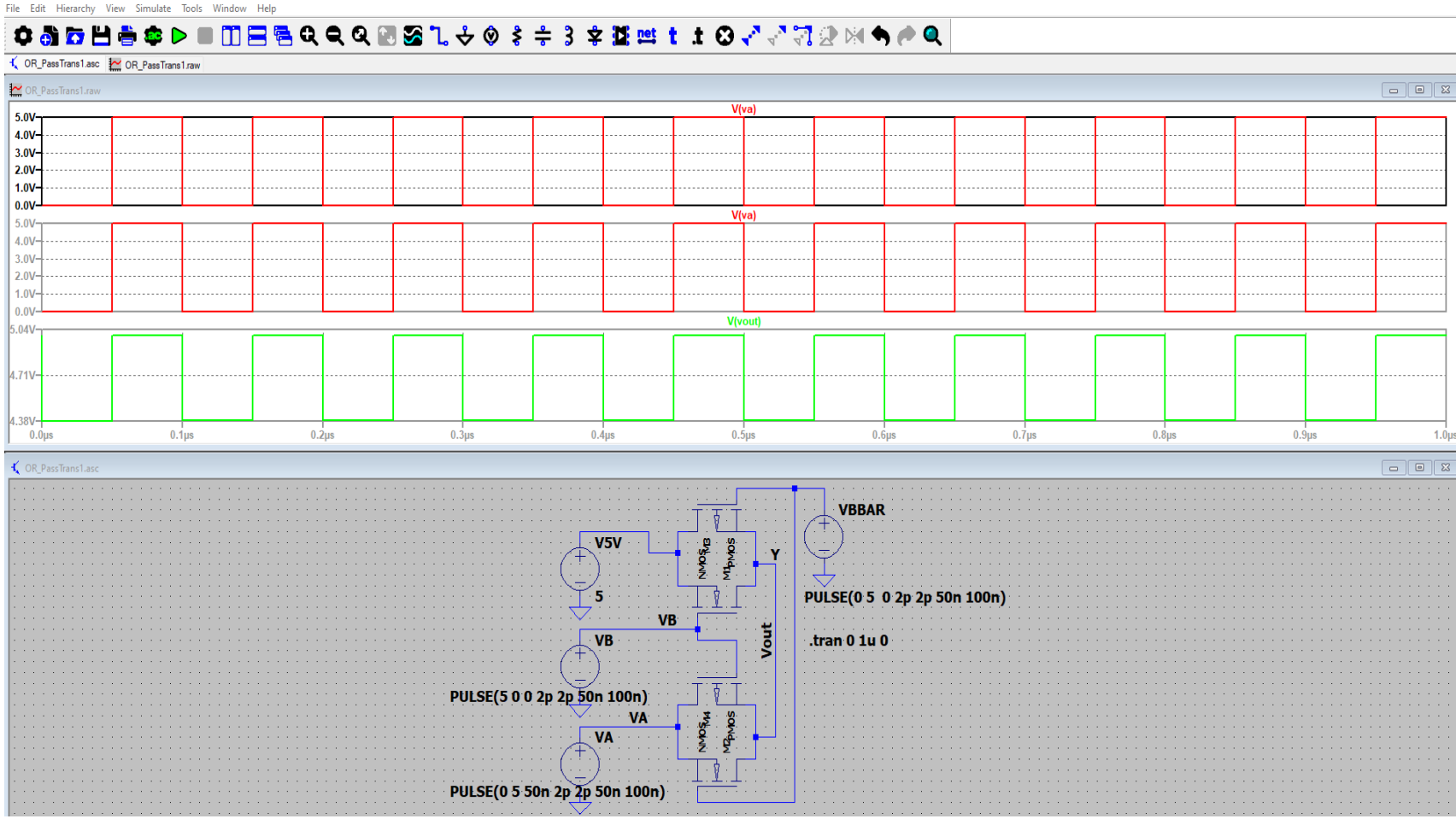
Use View → Visible Traces

Select the Waveforms that you want to Display

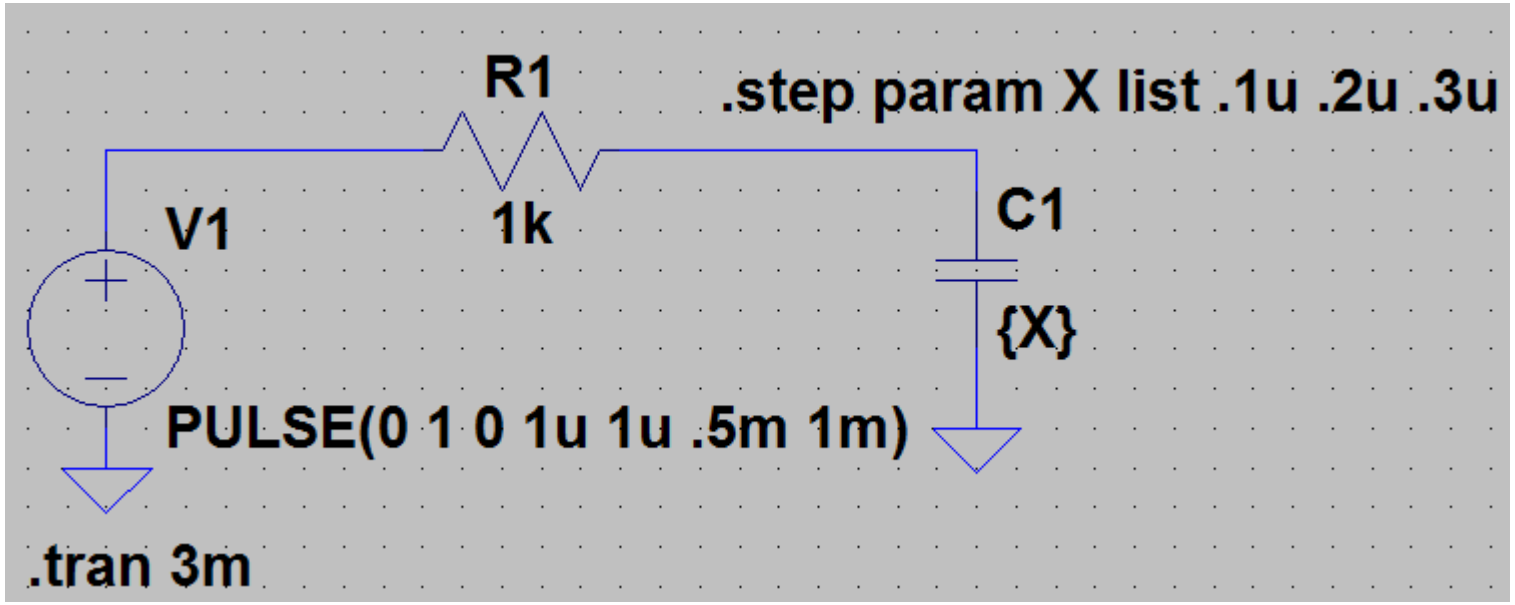


View Plots in Separate Window Panes

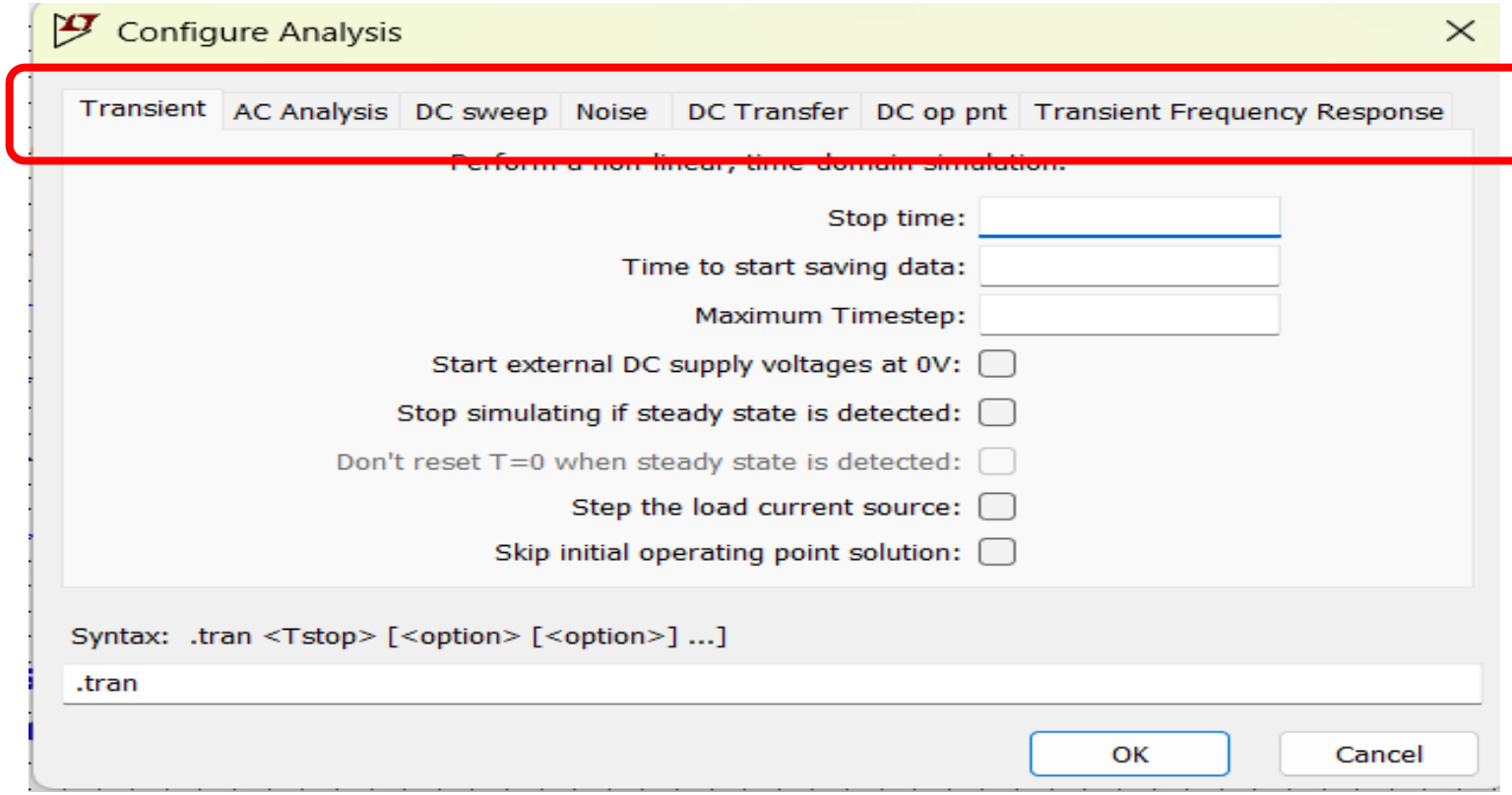
After Running Simulation:
Right Click on Waveform Window
There is option to Add new pane
First click on new pane and then
Add wave through probe on circuit



Different Values can be Stepped using .STEP



Different types of Circuit Analysis



https://www.allaboutcircuits.com/technical-articles/how-to-perform-transient-analysis-noise-simulation-LTspice/
https://www.cxi1.co.uk/ltspice/transient.htm
https://www.allaboutcircuits.com/technical-articles/intermediate-ltspice-tutorial/
https://www.allaboutcircuits.com/technical-articles/basic-circuit-simulation-with-ltspice/
LTspice XVII Tutorial | Spiceman

.meas statement for waveforms

[.measure/.meas : LTspice -- Evaluate User-Defined Electrical Quantities | Spiceman]

.meas Command in LTSpice [1]

The `.meas` command in LTSpice is used to measure specific parameters or values during a simulation, such as voltages, currents, or time intervals. It allows you to extract and analyze results programmatically.

Example: Measuring Rise Time

To measure the rise time of a signal `V(out)` when it crosses 0.5V:

```
meas trise when v(out)=0.5 rise=1
```

This command calculates the time at which `V(out)` first rises to 0.5V.

Example: Measuring Time Period

To measure the time period of a clock signal:

```
meas trise1 when v(clk)=0.5 rise=1
meas trise2 when v(clk)=0.5 rise=2
meas T param trise2 - trise1
```

Here, `T` represents the time period of the clock signal by subtracting the first rise time from the second.

Example: Finding Voltage at Specific Time

To find the voltage at a specific point in time (e.g., at `tfall`):

```
meas tfall when v(out)=0.5 fall=1
meas Vout find v(out) at tfall
```

This measures the voltage `V(out)` at the falling edge of the signal.

Key Considerations:

- **Syntax**: `.meas <name> <operation> <signal> [conditions]`
- **Operations**: `find`, `param`, etc.
- **Conditions**: Use `when`, `rise=n`, or `fall=n` to specify criteria.
- Ensure proper signal naming and conditions for accurate measurements.
- Use `.step` with `.meas` for parameter sweeps across multiple simulations.

The `.meas` command is versatile and essential for automating measurements in LTSpice simulations.

Reading and Book

- Textbook Chapter