Lahore University of Management Sciences

CS / EE 320 – Computer Organization and Assembly Language

Spring 2024 - 25

Instructor	Dr. Shahid Masud
Room No.	9-223A, Level 2, SBASSE
Office Hours	To be announced
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Secretary/TA	
TA Office Hours	
Course URL	on LMS
Support Services	LUMS offers a range of academic and other services to support students. These are mentioned below, and you are encouraged to use these in addition to in-class assistance from course staff. For a complete list of campus support services available for you click here (https://advising.lums.edu.pk/#supportservices)

Course Teaching Methodology (Please mention following details in plain text)
• On-campus lectures and computer-based labs

Course Basics				
Credit Hours	4 (3 Theory + 1 Programming Lab)			
Lecture(s)	Nbr of Lec(s) Per Week	2	Duration	75 minutes
Recitation/Lab (per week)	Nbr of Lec(s) Per Week	1	Duration	75 – 100 minutes
Tutorial (per week)	Nbr of Lec(s) Per Week	As required	Duration	As required

Course Distribution	
Core	**CS → Can be used as Core in CS undergraduate curriculum (in lieu of Fundamentals of Computer Systems CS 225*)**
Elective	Computer Science / Electrical Engineering / Computer Systems / and related majors
Open for Student Category	Sophomore / Junior / Senior
Close for Student Category	Freshman

COURSE DESCRIPTION
The first course in the Computer Systems series helps students understand the basic design and operation of computing hardware, how to evaluate its performance, and how the hardware interfaces to software. When designing or selecting a computer system, it is important to understand the tradeoff among various components and functional blocks. This course will cover the basic concepts of Computer Organization including the design of single-cycle and multi-cycle CPU control and data-path, memory systems including hierarchy, caches and virtual memory, and input/output subsystems. Instruction set architecture of a RISC processor is studied in detail. Some aspects of pipelining and parallel processing are also covered. Performance estimation is used to appreciate different operations and choices.

The Labs will have focus on learning and experimenting with (i) MIPS Assembly Level Programming, and (ii) Architecture Exploration through Pipelining.

COURSE PREREQUISITE(S)	
•	Introduction to Computer Programming (SSE Core) CS 100

COURSE OBJECTIVES	
	To understand basic building blocks and appreciate design choices in a modern computer system including hardware, microprocessor, software and the interface between hardware and software. Learn to program in Assembly Language

Course Learning Outcomes	
	The students will be able to:
CLO 1	Demonstrate understanding of basic building blocks and performance measurement in a computer system
CLO 2	Demonstrate knowledge of methods and techniques to build datapath of a modern microprocessor
CLO 3	Write Assembly Language programs to carry out basic arithmetic and data-handling operations

Relation to CS / EE Program Outcomes				
CLOs	Related PLOs	Levels of Learning	Teaching Methods	CLO Attainment checked in
CLO 1	PLO 1 (Engg. Knowledge)	Cog 3	Lectures	Quizzes, Exams
CLO 2	PLO 3 (Development of Solutions)	Cog 3	Lectures	Quizzes, Exams
CLO 3	PLO 5 (Modern Tool Usage)	Cog 3, PsyMo 2	Programming	Lab Tasks and Assignments

Grading breakup: Component Details and weightages
Assignment(s): 5% (2 to 3) Home Work: 0% Quiz(s): 15% (5 to 6, one quiz will be dropped) Labs: 20% (Attendance 4%, Task Completion 12%, Lab Quiz/s 4%) Class Participation: 0% Midterm Examination: 25% Project: Final Examination: 35%

Examination Detail	
Midterm Exam	Yes/No: Yes Combine Separate: Combine Duration: 75 minutes Preferred Date: Lecture 15 or 16 Exam Specifications: Closed Book / Closed Notes / Calculator Allowed

Final Exam	Yes/No: Yes Combine Separate: Combine Duration: 3 hours Exam Specifications: Closed Book / Closed Notes / Calculators Allowed

Week/ Lecture	Topics	Readings	Related CLOs & Remarks
Weeks 1, 2	**Introduction to Computer Organization, Building blocks, performance issues**	**Chap 1**	**CLO 1**
1	Course Introduction, Basic blocks of a Computer System	**Chap 1**	**CLO 1**
2	Emerging trends in computer systems, Microprocessor Technology, software processing on hardware	**Chap 1**	**CLO 1**
3	Computer throughput and response time, Performance of a computer system, Power Wall	**Chap 1**	**CLO 1**
4	Performance of Uniprocessor and Multiprocessor, MIPS, Quantitative Performance Benchmarks	**Chap 1**	**CLO 1**
Weeks 3, 4	**Operation of Computer Hardware, Instructions, logical and arithmetic operations, addressing modes**	**Chap 2**	**CLO 3**
5	Operations of Computer Hardware, Representing Instructions in Computers	**Chap 2**	**CLO 3**
6	Instruction fields, Logical and Decision Instructions,	**Chap 2**	**CLO 3**
7	Procedures and Sub-Routines, Stack operations	**Chap 2**	**CLO 3**
8	Addressing Modes, Instruction Execution	**Chap 2**	**CLO 3**
Weeks 5, 6	**Computer Arithmetic, addition, subtraction, multiplication, floating point, parallelism in SIMD, vector instructions**	**Chap 3**	**CLO 2**
9	Computer Arithmetic, Addition, Multiplication, Signed numbers	**Chap 3**	**CLO 2**
10	Division, Introduction to Floating Point numbers	**Chap 3**	**CLO 2**
11	IEEE 754 standard, Floating Point Addition and Subtraction	**Chap 3**	**CLO 2**
12	Floating Point Multiplication, Rounding, Truncation, Guard Bits, MIPS example, Parallelism and Computer Arithmetic	**Chap 3**	**CLO 2**
Week 7, 8, 9	**Processor design, building a datapath, multicycle implementation, pipelined datapath and control, data and control hazards**	**Chap 4**	**CLO 2**
13	Basic MIPS Processor, Major Functional Units	**Chap 4**	**CLO 2**
14	Building a Datapath, R-format Instructions, Register file, ALU Control	**Chap 4**	**CLO 2**
15	**Midterm week**		
16	Load / Store Instructions, BEQ Instructions, Single Cycle vs Multicycle Implementation	**Chap 4**	**CLO 2**
17	Introduction to Pipelining, Data Hazards	**Chap 4**	**CLO 2**
18	Forwarding, Stalling, Control Hazards, Impact of Pipelining on Branch Instructions, Branch Prediction	**Chap 4**	**CLO 2**
Midterm week 8 or 9	**Midterm examination**		
19	Exception Handling, Parallelism via Instructions, Concept of Speculation, Multiple-Issue Processor	**Chap 4**	**CLO 2**
Weeks 10, 11, 12	**Memory technologies, memory hierarchy, caches, virtual memory**	**Chap 5**	**CLO 1**
20	Memory Technology, RAM, ROM, Flash	**Chap 5**	**CLO 1**

21	Memory Technology DISK, DVD, RAID Array (Stallings)	**Stallings**	**CLO 1**
22	Introduction to Caches, Tag Field, Cache Access Direct, Associative, Set-Associative	**Chap 5 / Stallings**	**CLO 1**
23	Cache Misses, Cache Performance, Multi-Level Caches	**Chap 5**	**CLO 1**
24	Virtual Memory, Page Faults, Fast Address Translation using TLB	**Chap 5**	**CLO 1**
25	Virtual Machines, Integrating VM, TLB and Caches, Cache Coherence	**Chap 5**	**CLO 1**
Week 13, 14	**Parallel processing, multithreading, multicore processors**	**Chap 6**	**CLO 2**
26	Challenges in creating parallel processing programs, SISD, MIMD, SIMD, SPMD, Vector Processing	**Chap 6**	**CLO 2**
27	Hardware Multithreading, Multicore and Shared-Memory Multiprocessors	**Chap 6**	**CLO 2**
28	GPU, Domain Specific Architecture (DSA)	**Chap 6**	**CLO 2**

Textbook(s)/Supplementary Readings
Text Book: Computer Organization and Design (MIPS Edition) The Hardware / Software Interface by David Patterson and John Hennessy, 6th Edition **Supplementary Reading:** Computer Organization and Architecture Designing for Performance by William Stallings, 10th Edition

Lab Topics	
Lab 1	Introduction to Assembly Language Programming, QtSpim (MARS) environment, MIPS Reference Card
Lab 2	Writing simple Assembly language programs in QtSpim, MIPS Registers and Memory map
Lab 3	Write programs to add, subtract, logical operations using different addressing modes
Lab 4	Write program to multiply and divide using different registers and addressing modes
Lab 5	Write program to use array operations in different addressing modes
Lab 6	Control Instructions and Procedure calls in Assembly Language
Lab 7	Exceptions, Interrupts and I/O in Assembly Language
Lab 8	Special instructions in RISC assembly language (eg. floating point)
Lab 9	Lab Assignment 1
Lab 10	Lab Assignment 2
Lab 11	Introduction to Computer Architecture Simulators, study pipeline behavior
Lab Exam	Lab Exam

Complex Engineering Problem/Activity:	
Complex Engineering Problem Details	Included: No Nature and details of Complex Engineering Problem: Assessment in
Complex Engineering Activity Details	Included: No Nature and details of Complex Engineering Activity: Assessment in:

Rubric Based Assessment of CLO:NIL
Assessment based on written quizzes, assignments, exams and laboratory tasks.

Lab tasks involve writing, debugging and executing Assembly Language Code for MIPS processor.

Rights and Code of Conduct for Online Teaching
The misuse of online modes of communication is unacceptable. TAs and Faculty will seek consent before the recording of live online lectures or tutorials. Please inform if you do not wish to be recorded during a session to inform the faculty member. Please also ensure that you prioritize formal means of communication (email, lms) over informal means to communicate with course staff.
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