CS222:
Processor Design: Control Unit Design, Multi-Cycle Design

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Outline

- Design Strategy of Data path
- Control Path Implementation
- Multi-cycle Design
- Pipeline: Concept

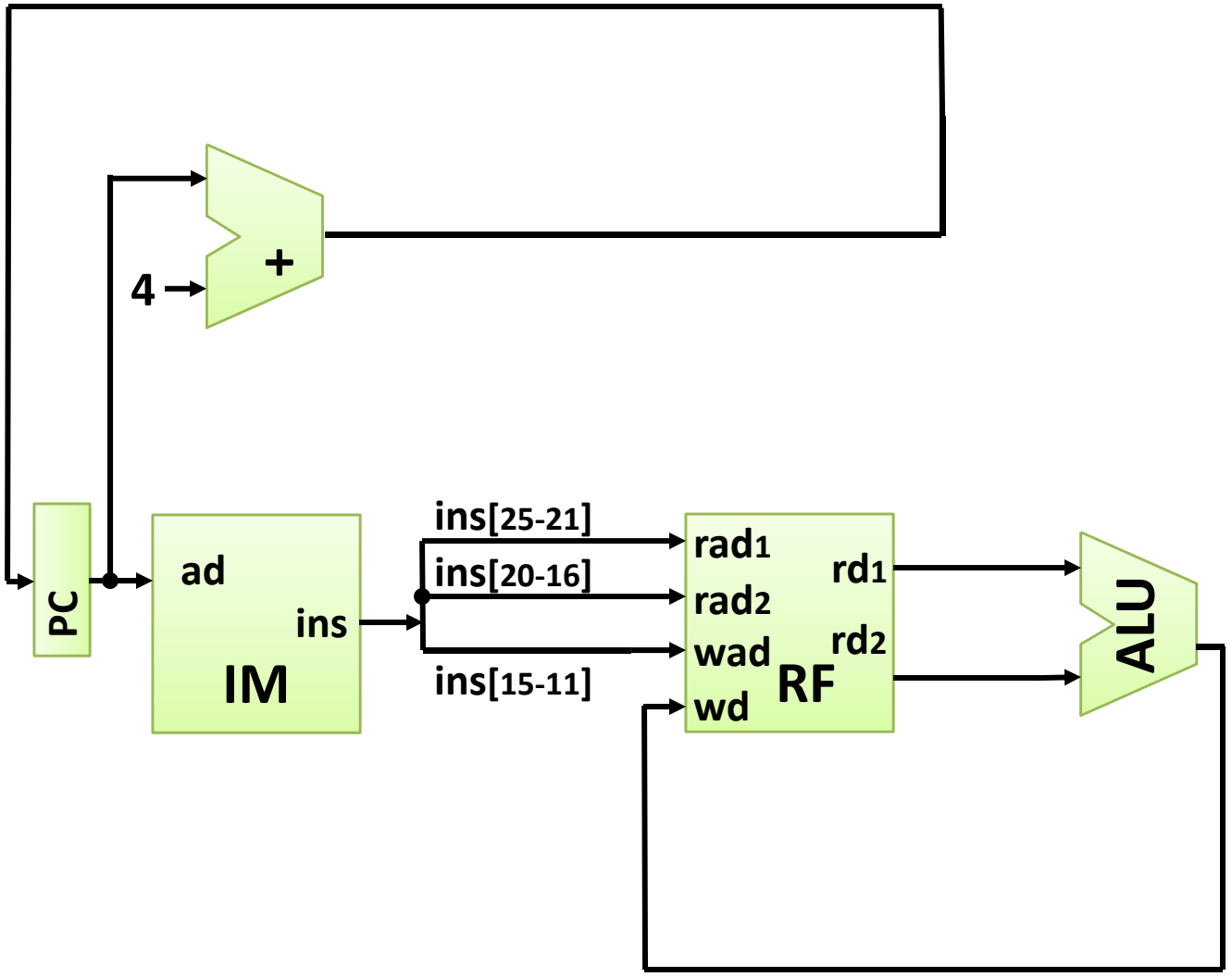
MIPS subset for implementation

- Arithmetic - logic instructions
  - **add, sub, and, or, slt**
- Memory reference instructions
  - **lw, sw**
- Control flow instructions
  - **beq, j**

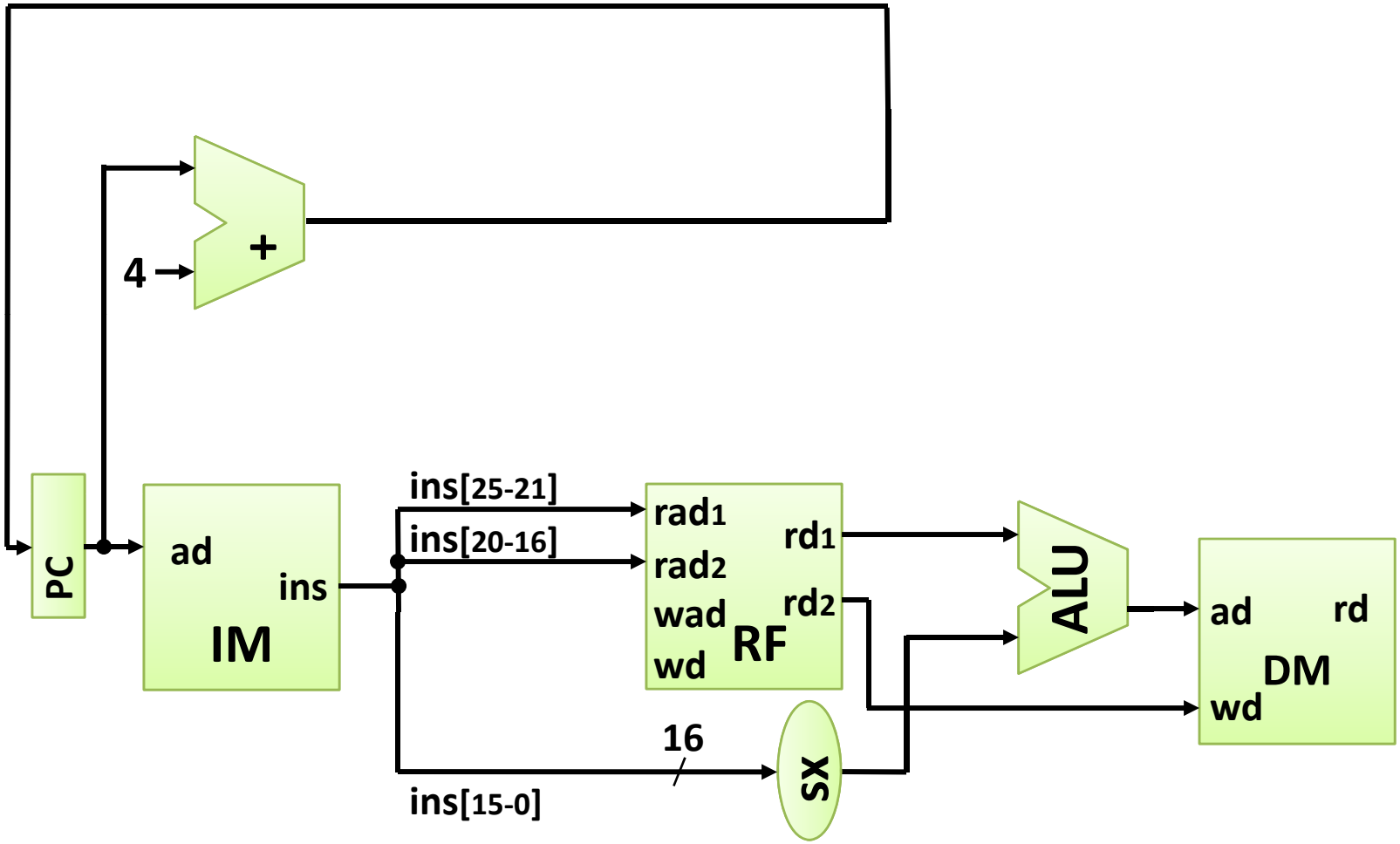
Datapath design approaches

- Grow the design incrementally
  - D1: {add, sub, and, or, slt}
  - D2: {add, sub, and, or, slt, sw}
  - D3: {add, sub, and, or, slt, sw, lw}
  - D4: {add, sub, and, or, slt, sw, lw, beq}
  - D5: {add, sub, and, or, slt, sw, lw, beq, j}
- Do sub-designs and then merge
  - D1: {add, sub, and, or, slt}
  - D2: {sw}
  - D3: {lw}
  - D4: {beq}
  - D5: { j}
  - D6: D1$\cup$D2 $\cup$ D3 $\cup$ D4 $\cup$ D5

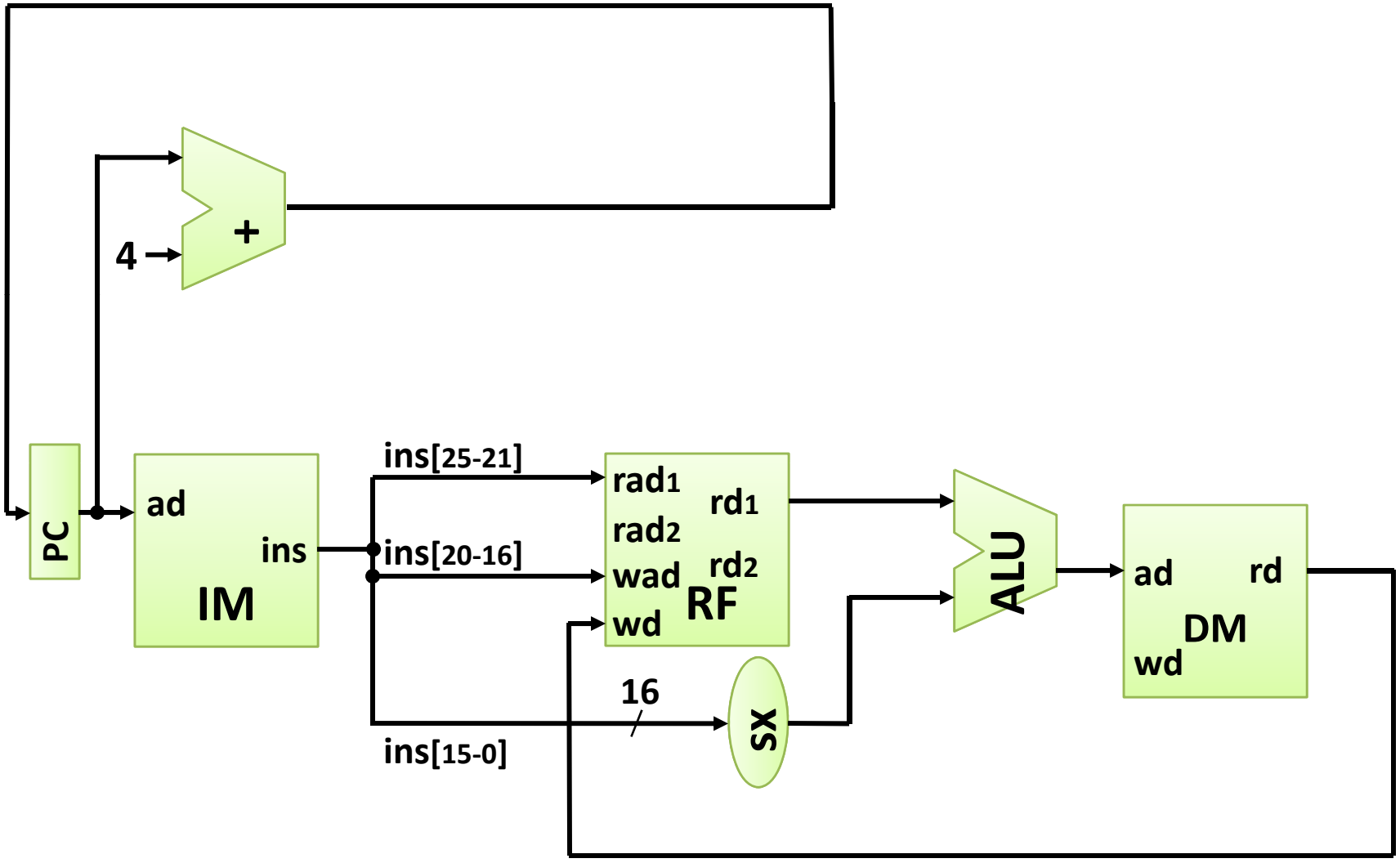
Design for {add, sub, and, or, slt}



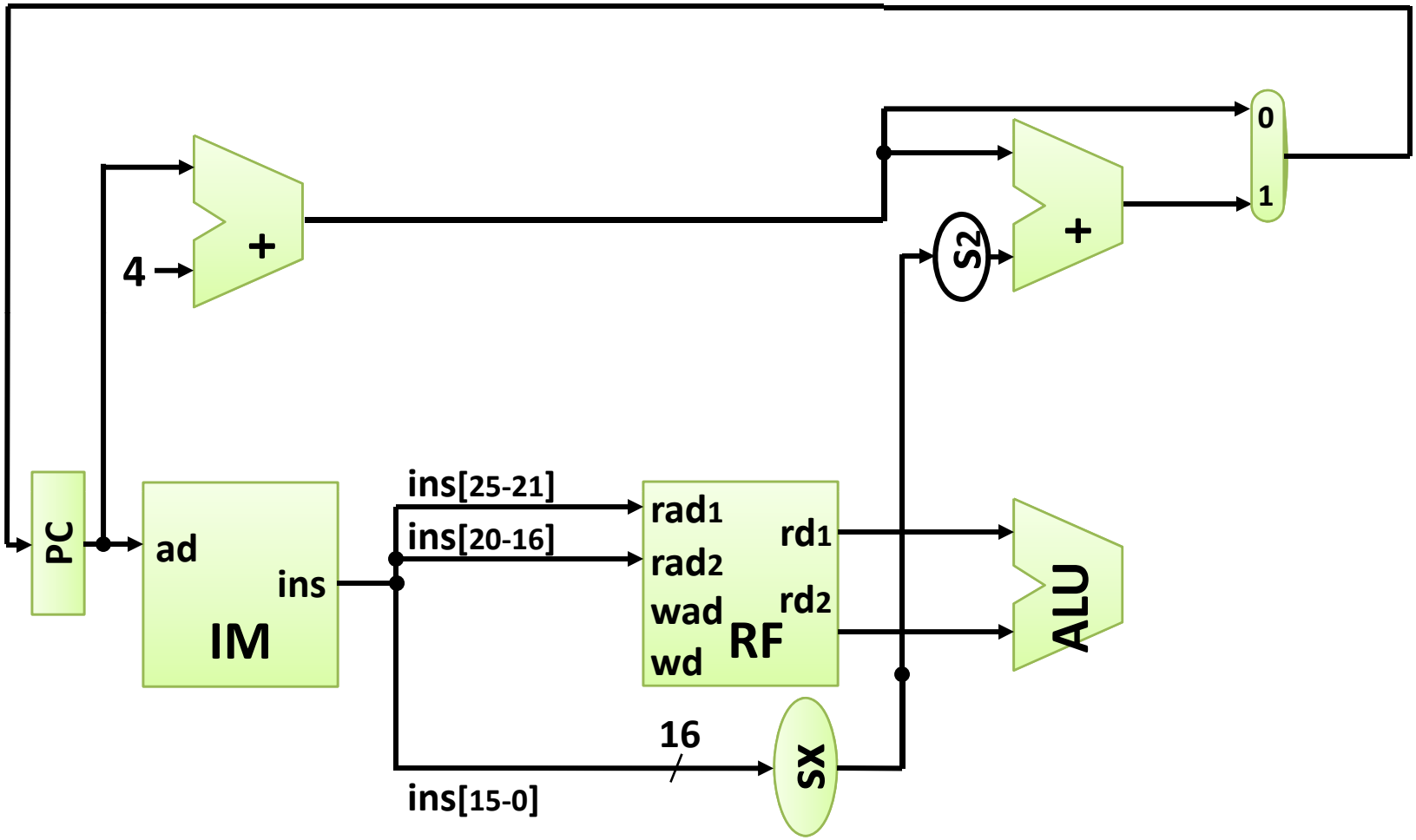
Design for {sw}



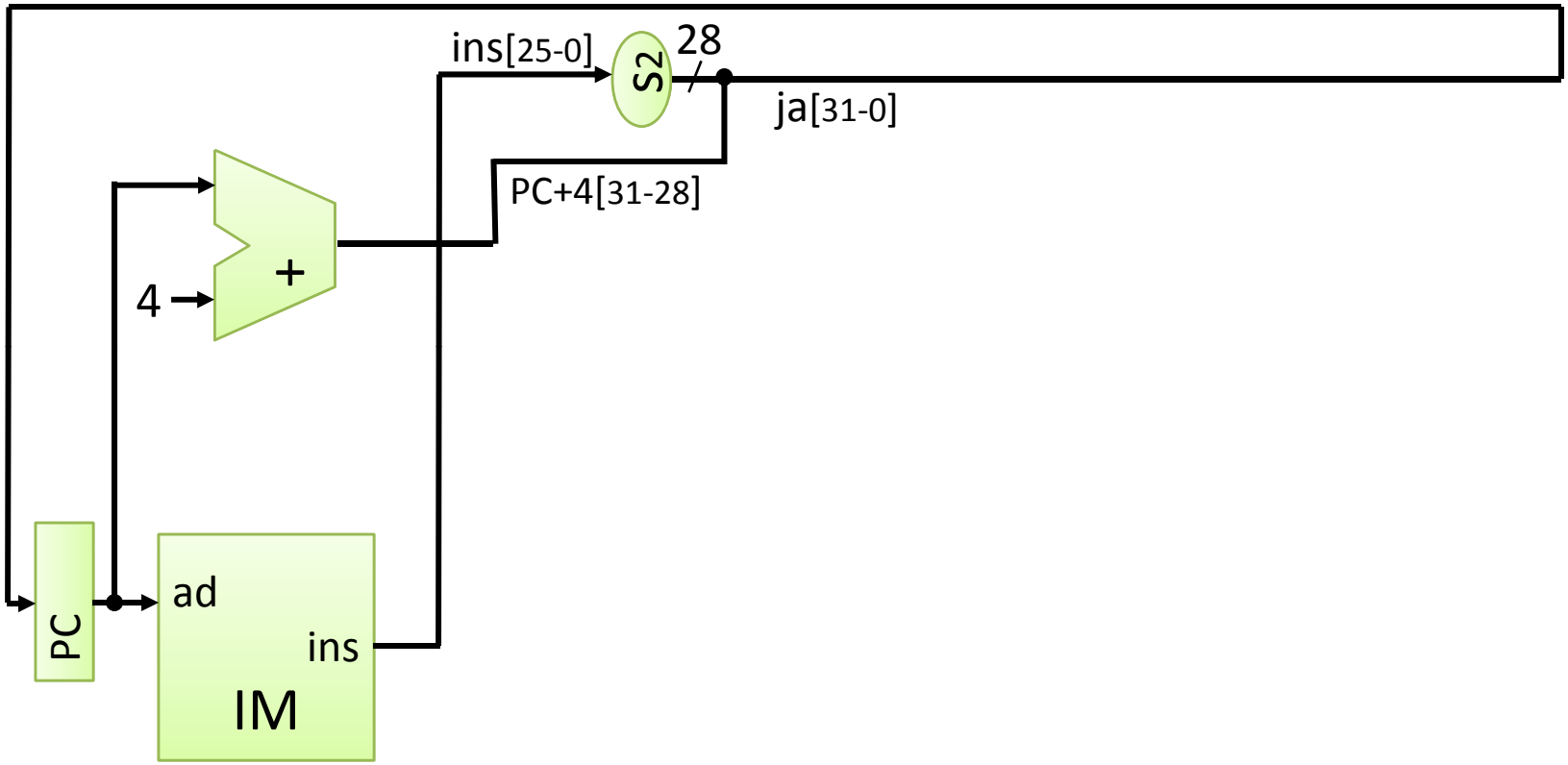
Design for {lw}



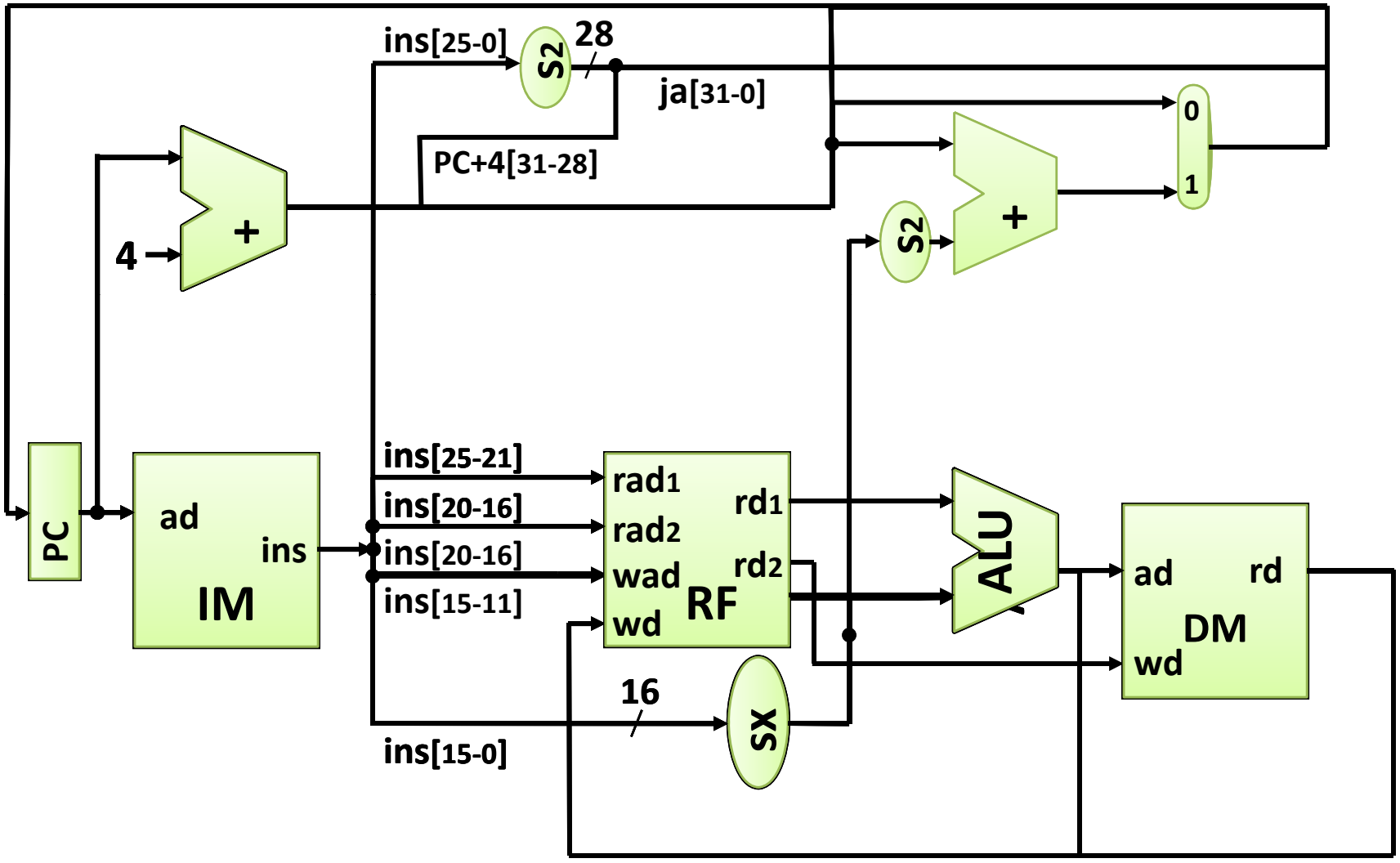
Design for {beq}



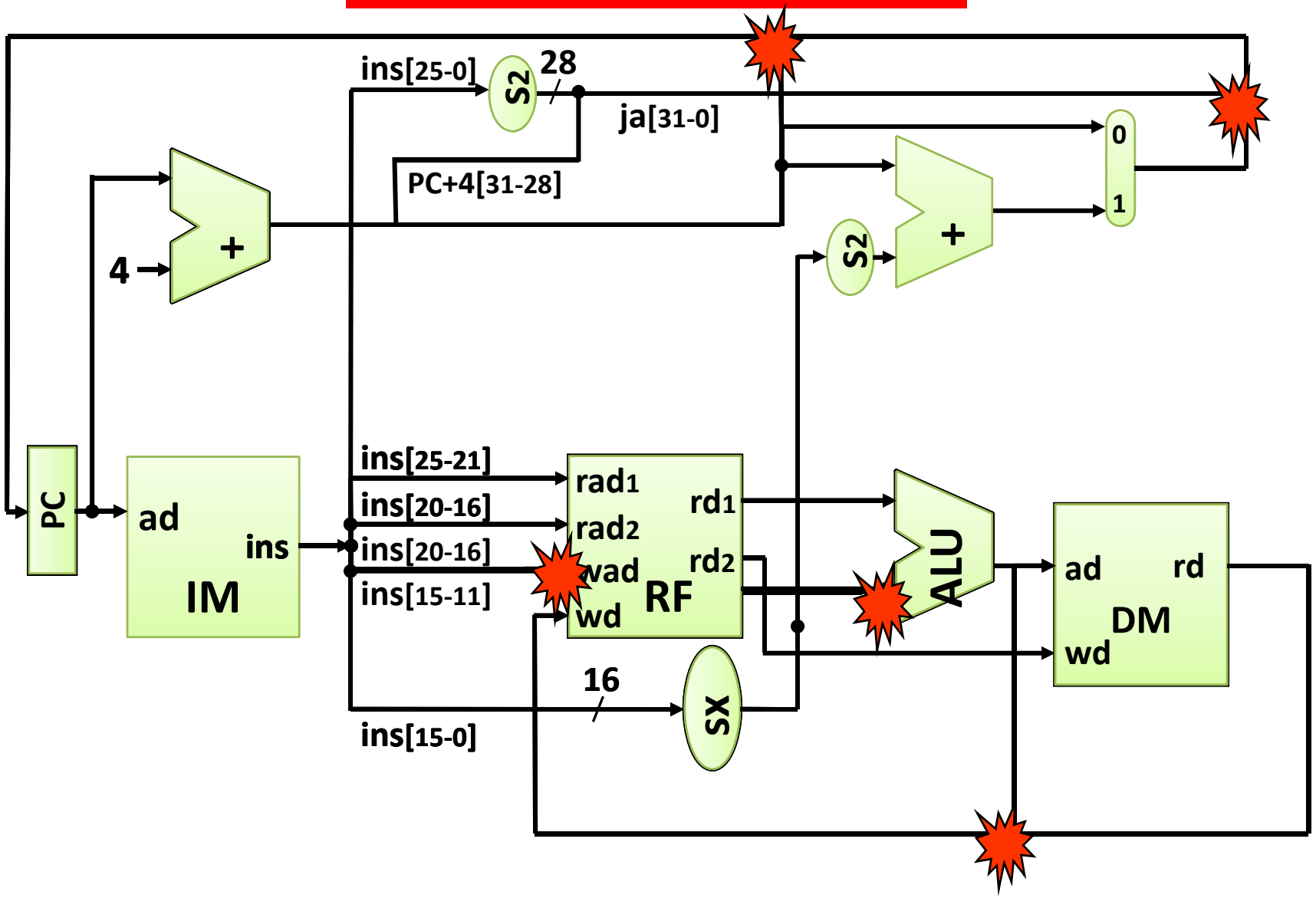
Design for { j}



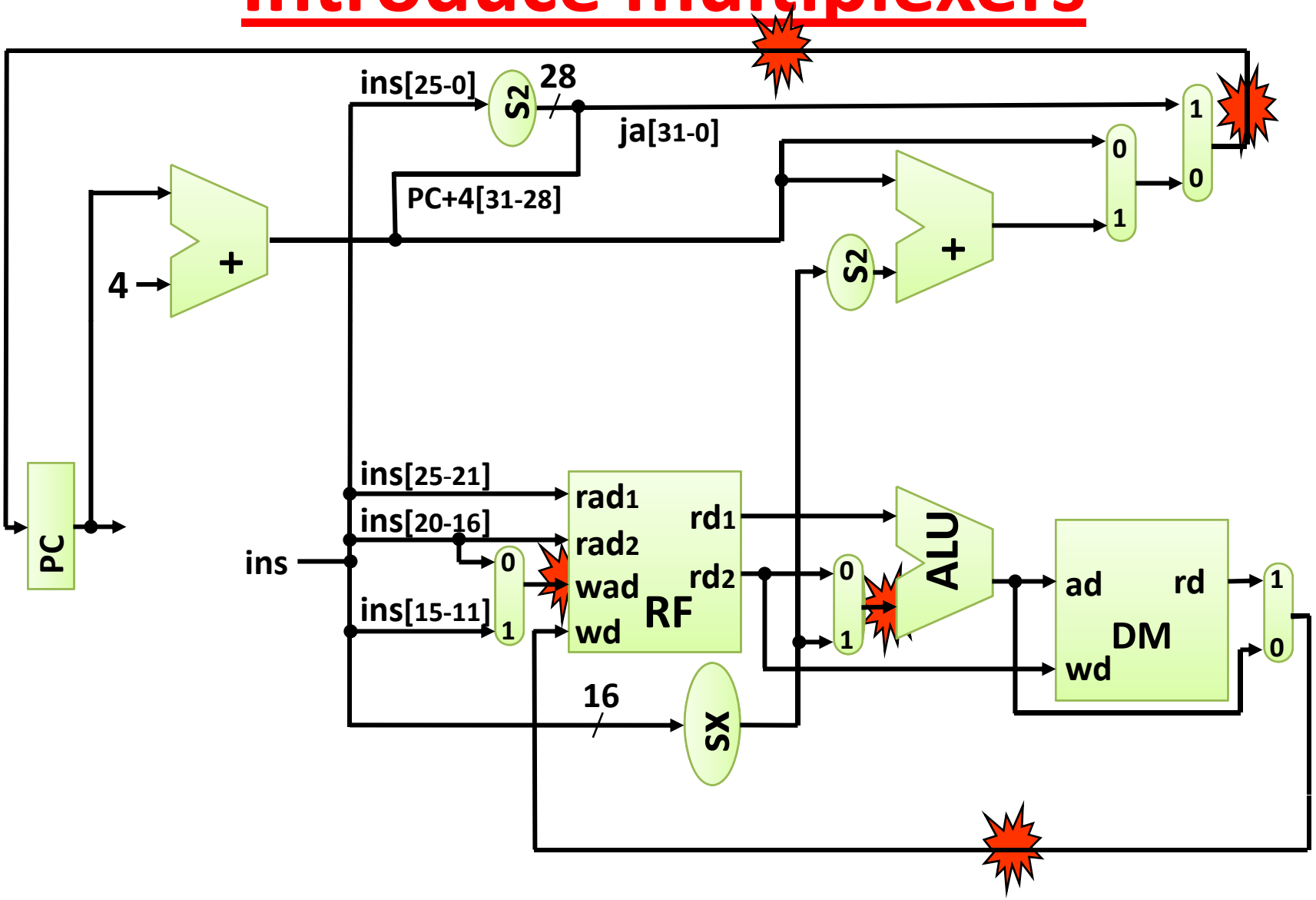
Merging sub-designs



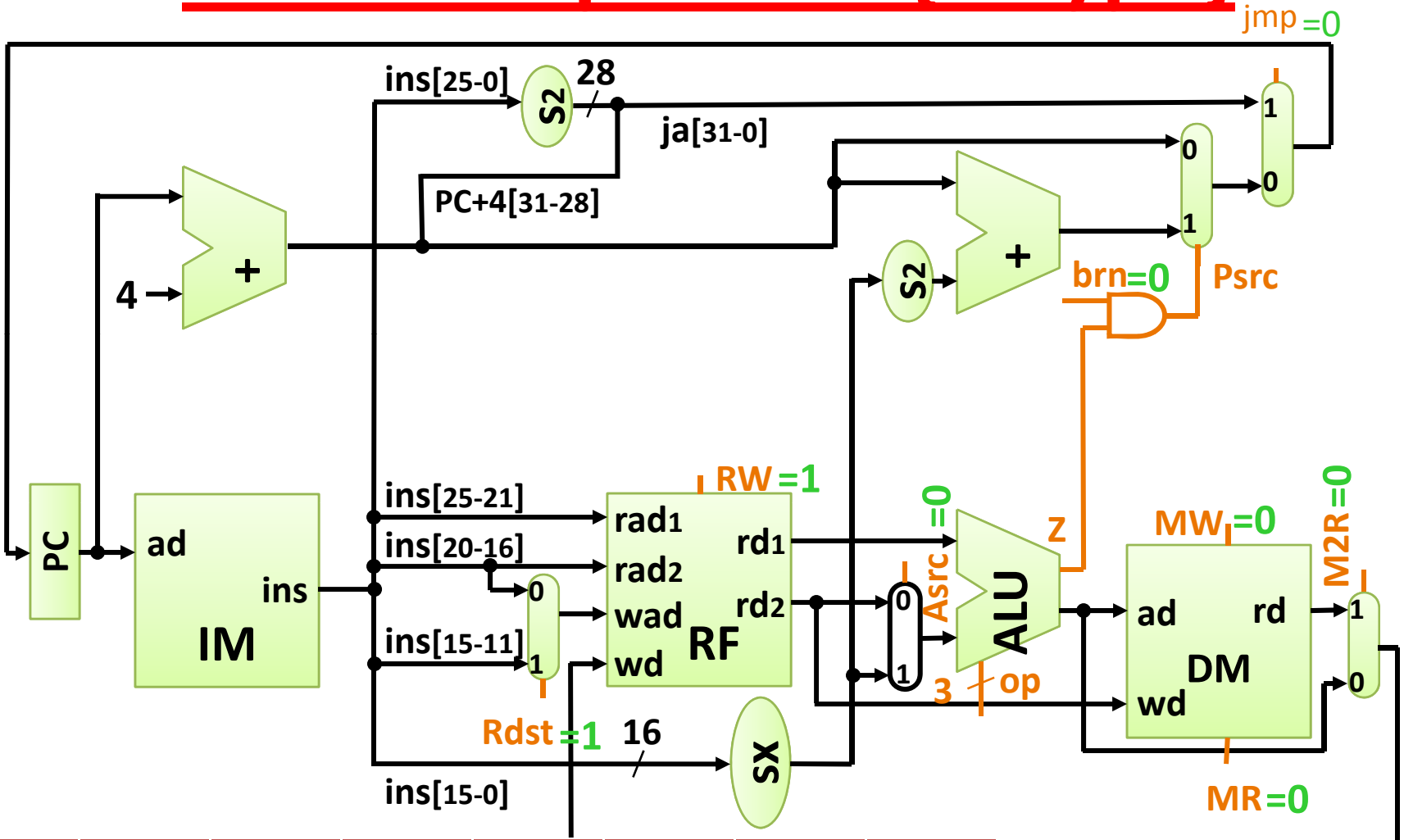
Identify conflicts



Introduce multiplexers

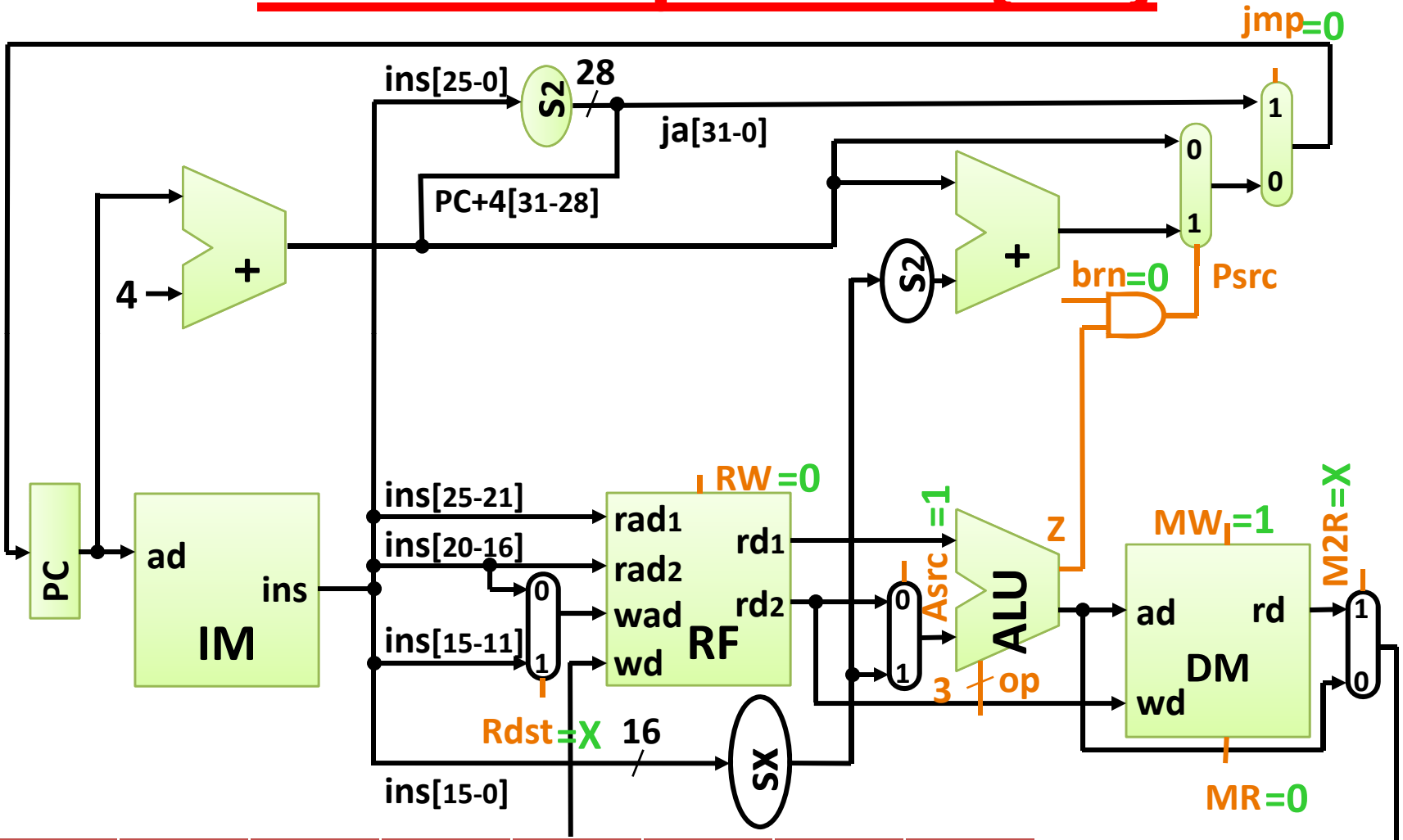


Control inputs for {R-type}



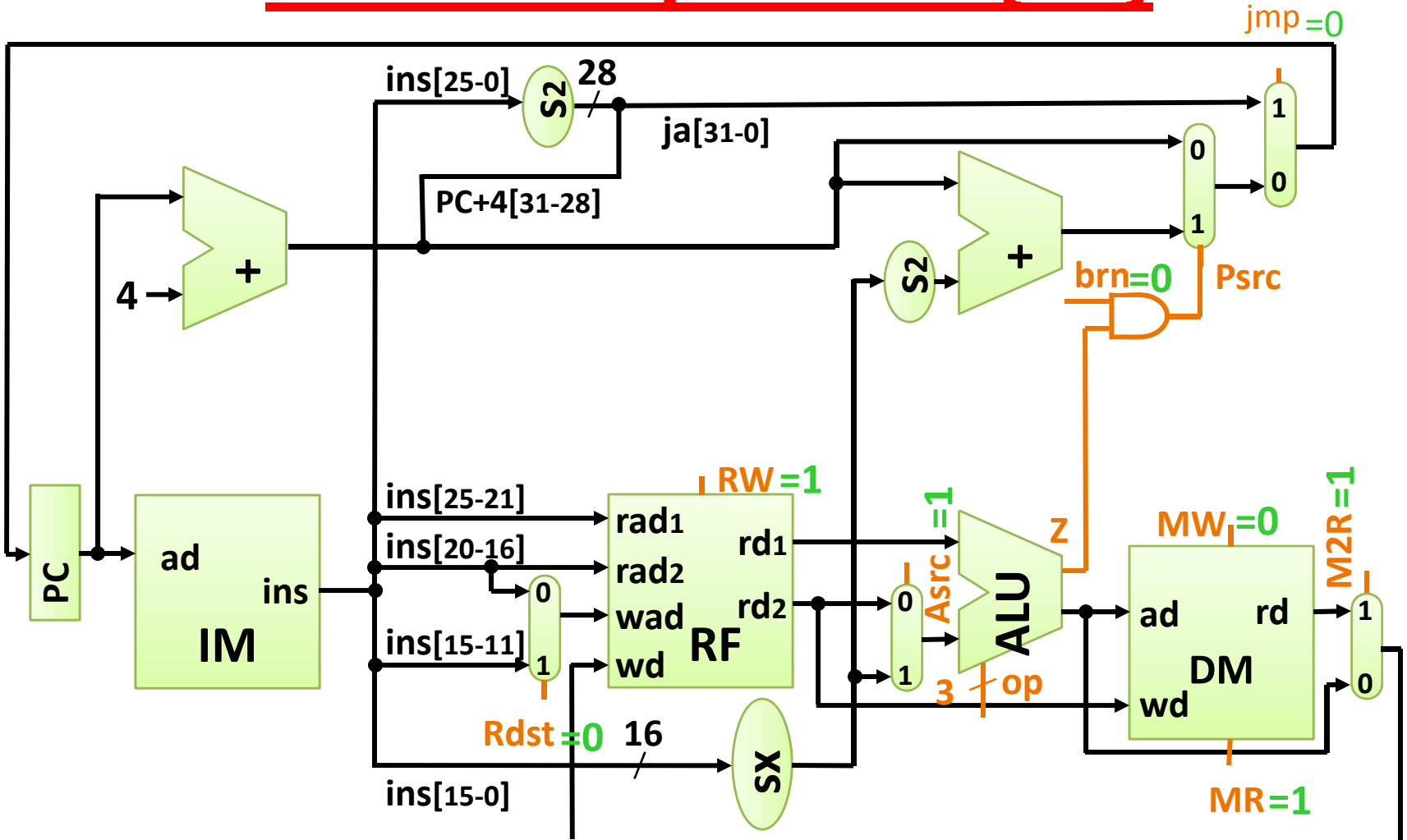
Rdst	RW	Asrc	MW	MR	M2R	Brn	Jmp
1	1	0	0	0	0	0	0

Control inputs for {sw}



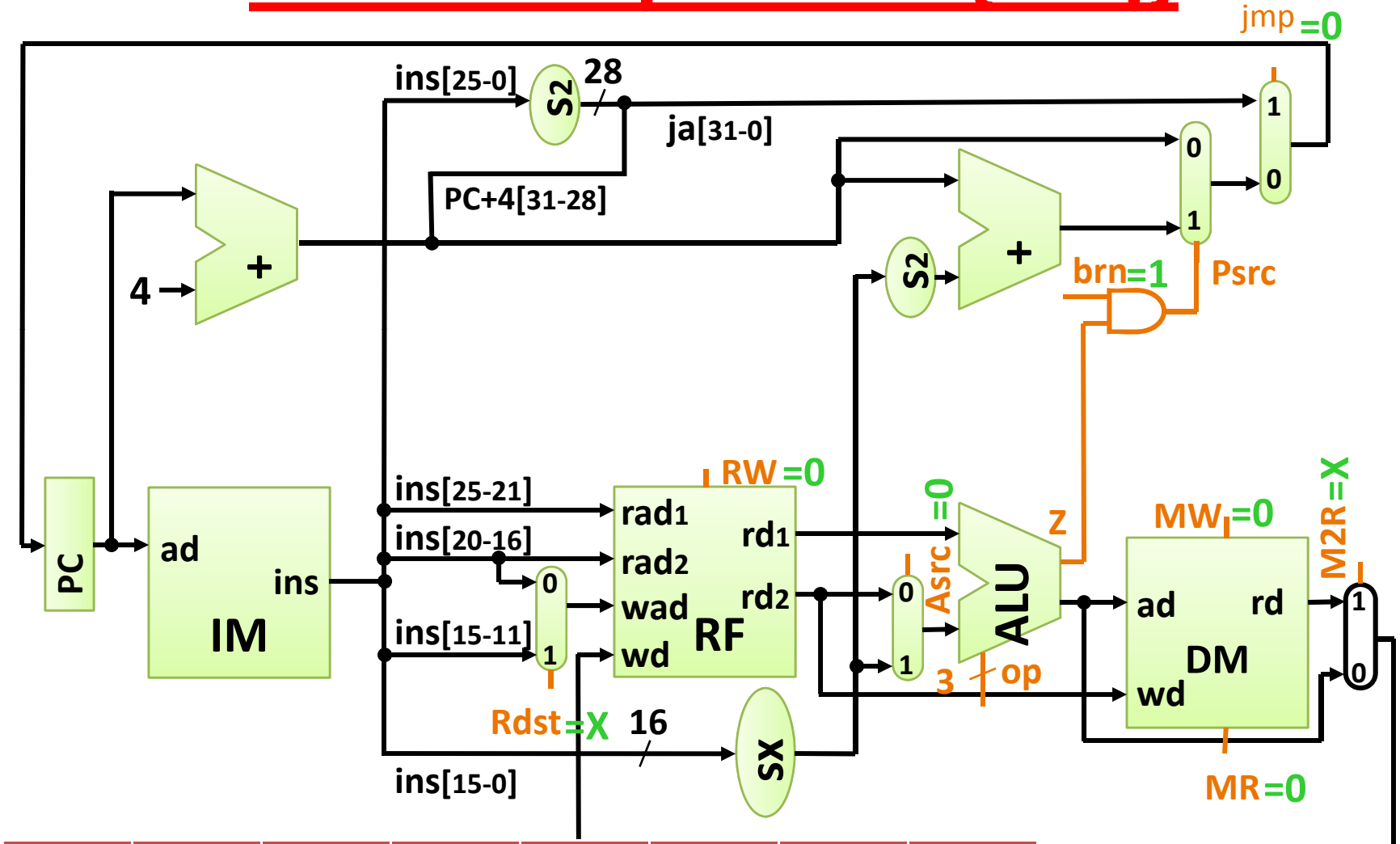
Rdst	RW	Asrc	MW	MR	M2R	Brn	Jmp
X	0	1	1	0	X	0	0

Control inputs for {lw}



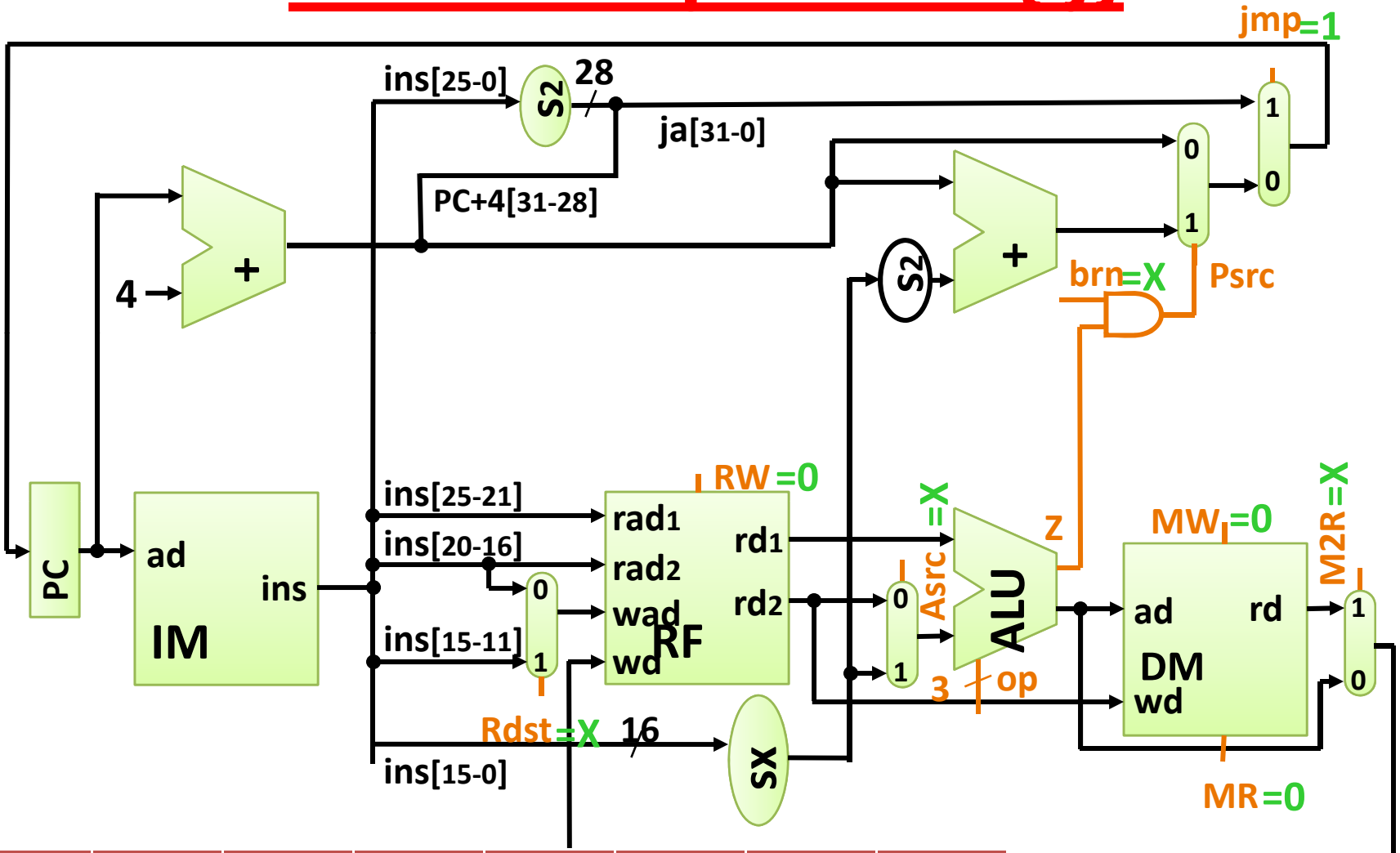
Rdst	RW	Asrc	MW	MR	M2R	Brn	Jmp
0	1	1	0	1	1	0	0

Control inputs for {beq}



Rdst	RW	Asrc	MW	MR	M2R	Brn	Jmp
X	0	0	0	0	X	1	0

Control inputs for { j}



Rdst	RW	Asrc	MW	MR	M2R	Brn	Jmp
X	0	X	0	0	X	X	1

All control inputs

Instruction	Opcode	Rdst	RW	Asrc	MW	MR	M2R	Brn	Jmp
Rtype	000000	1	1	0	0	0	0	0	0
Sw	101011	X	0	1	1	0	X	0	0
Lw	100011	0	1	1	0	1	1	0	0
Beq	000100	X	0	0	0	0	X	1	0
J	000010	X	0	X	0	0	X	X	1

Encoding opc

Ins	Opc ode	OPC	Rdst	RW	Asrc	MW	MR	M2R	Brn	Jmp
R	000000	10	1	1	0	0	0	0	0	0
Sw	101011	00	X	0	1	1	0	X	0	0
Lw	100011	00	0	1	1	0	1	1	0	0
Beq	000100	01	X	0	0	0	0	X	1	0
J	000010	XX	X	0	X	0	0	X	X	1

Thanks