REVIEW

# Carbon nanotube transistors: Making electronics from molecules

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**Semiconducting carbon nanotubes are robust molecules with nanometer-scale diameters that can be used in field-effect transistors, from larger thin-film implementation to devices that work in conjunction with silicon electronics, and can potentially be used as a platform for high-performance digital electronics as well as radio-frequency and sensing applications. Recent progress in the materials, devices, and technologies related to carbon nanotube transistors is briefly reviewed. Emphasis is placed on the most broadly impactful advancements that have evolved from single-nanotube devices to implementations with aligned nanotubes and even nanotube thin films. There are obstacles that remain to be addressed, including material synthesis and processing control, device structure design and transport considerations, and further integration demonstrations with improved reproducibility and reliability; however, the integration of more than 10,000 devices in single functional chips has already been realized.**

Transistors are electronic switching devices that enable digital computation based on their on-state (binary 1) and off-state (binary 0) operation. In the earliest days of integrated circuits, it became clear that scaling down the size of the transistors would drive better chip-level performance, which is now known as Moore's law. One of the most important dimensions for such scaling is the semiconducting channel length, which is the distance that electrical current flows or is controlled by a gate electric field to turn the device on and off. Although the initial channel lengths were many microns in size, proposals to scale the semiconducting channel to the ultimate limit of molecular dimensions (fractions of a nanometer) date to the mid-1970s (*1*). Decades of study on the transfer of electrons through conjugated organic molecules, considered to replace the silicon channel, highlighted several important challenges for such molecular transistors. The foremost issues included low stability and the difficulty of effectively gating, and making reliable electrical contact to, the molecules (*2*).

To meet or exceed the performance of silicon electronics, it became clear that new channel materials must have similar stability. Among the molecular options, semiconducting single-walled carbon nanotubes (CNTs) have several advantages (*3*, *4*). Nested multiwalled CNTs are effectively metallic at room temperature and thus have limited utility as transistor channels (*5*). Throughout this review, CNTs will imply single-walled nanotubes. Semiconducting CNTs are composed of a cylindrical shell of hexagonally arranged carbon with a diameter of ~1 nm. Electrons travel only forward or backward with a wave function wrapping around the nanotube to create a one-dimensional (1D) semiconductor with an energy bandgap of a few hundred milli–electron volts (*5*). These materials are stable in air and can be manipulated through a variety of processing methods that are commonly used in the semiconductor industry. The early demonstrations of field-effect transistors (FETs) by draping a semiconducting CNT over metal electrodes (*3*, *4*) have led to continued research activity with the goal of creating reproducible, scalable, and high-performance devices integrated into dense circuitry using processing steps similar to those used to create silicon electronics.

The widespread interest in semiconducting CNTs has also inspired intense and ongoing exploration of other nanomaterials, including semiconducting nanowires (*6*), 2D graphene (*7*), transition metal dichalcogenides (*8*), and Xenes (*9*). Despite the growing number of nanomaterial options, CNTs stand out in offering stability, bandgap, and superb electrical and thermal properties that are unmatched by other candidates. Here, we review recent material, device, and technology advances for CNT transistors, establishing both the substantial promise and the remaining challenges for this molecular transistor. Progress in the field will be related to the foremost potential applications for CNT transistors, highlighted in Fig. 1. Two of the most prominent potential applications are high-performance (HP) computing chips and thin-film transistors (TFTs) for display backplanes and the internet of things (IoT); a few of the target performance metrics for these applications are summarized in Table 1.

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## Advances in materials for CNT transistors

Exploiting the advantages of semiconducting CNTs requires overcoming several materials science hurdles. Just as silicon must be purified and doped to be a useful channel material, as-synthesized CNTs can be either metallic or semiconducting and must be purified into semiconducting-only for use in transistors. Whether CNTs are metallic or semiconducting depends on how the hexagonal lattice wraps into a tube. This structure is most easily visualized by rolling a rectangular section of the $sp^2$-bonded hexagonal carbon lattice of atomically thin graphene into a 1D cylinder, where the resulting diameter is ~1 nm and the length is $10^2$ to $10^8$ nm. The vector that defines the width of the rectangular section with respect to the graphene lattice is commonly referred to as the chiral vector and ultimately determines the diameter, helicity, and conductivity properties of the CNT (*5*).

In addition to specifying the physical structure of the CNT, the chiral vector also imposes well-defined quantum-mechanical boundary conditions on the electronic band structure, which implies that for random tube closure, ~33% of CNT chiralities are metallic and ~67% are semiconducting. Moreover, among the semiconducting chiralities, the bandgap is approximately inversely proportional to the CNT diameter. Because CNT transistors require semiconducting channels, preferably with a well-defined and uniform bandgap, the ability to scalably synthesize and isolate CNTs with atomically precise chiral vector control is the ultimate goal for high-performance CNT integrated circuits.

### *Controlled synthesis of CNTs*

CNTs can be synthesized by introducing a carbonaceous feedstock with a metal catalyst (usually Fe or Ni) into a growth chamber, where energy is added through heat, light, or plasma excitation. Because CNT growth typically occurs at temperatures at which these catalysts undergo substantial restructuring, it is difficult to control the chiral vector, and a range of CNT diameters and both electronic types are produced; much effort has been expended to gain control over CNT chirality (*10*). These approaches include the use of refractory catalyst particles such as W-Co alloys with well-defined size and shape that remain structurally invariant at the growth temperature and thus can drive predictable nucleation of targeted CNT chiralities (Fig. 2A) (*11*), the addition of molecular seeds that have a structure that closely matches the targeted CNT chirality (*12*), or the deployment of CNTs themselves as seeds in "CNT cloning" (*13*). Although tailored catalysts or seeds help control synthetic outcomes, many other growth parameters also play a role—including temperature, pressure, flow rates, and applied electric fields (*14*)—and

thus growth optimization entails the search of a broad parameter space. In an effort to accelerate this exploration, autonomous growth using closed-loop iterative experimentation is showing promise for rapid identification of synthesis conditions that minimize CNT structural polydispersity (*15*).

### *Separation of semiconducting CNTs*

Because the most-optimized CNT growth procedures still lack sufficient monodispersity for wafer-scale transistor applications, post-synthetic separation methods are required to sort as-grown CNTs by diameter, chirality, and electronic type. Fortunately, CNTs have sizes and shapes that are comparable to those of biological macromolecules, which has allowed many CNT separation methods to be adapted from ones that have already been developed for biochemistry. In density gradient ultracentrifugation (DGU), CNTs are first dispersed and encapsulated with mixtures of surfactants that show selectivity for different CNT separation targets (including chiral vector, chiral handedness, electronic type, and diameter) and then separated by buoyant density in aqueous density gradients (*16*). Although DGU has sufficient scalability to be viable commercially, other strategies from biochemistry have also been heavily developed, including gel chromatography (*17*) and dielectrophoresis. The latter method has the added benefit of enabling aligned assembly of CNTs between prepatterned electrodes (*18*).

Methods from polymer chemistry have also been used for CNT separations, including aqueous two-phase extraction (*19*) and selective dispersion of targeted CNT chiralities with structure-discriminating polymers that wrap the nanotubes (Fig. 2B) (*20*). In all cases, purities of semiconducting CNTs have reached the detectable limits of optical spectroscopic characterization (~99.9%) and begun to provide sufficient monodispersity for many CNT transistor applications. The ultimate goal for high-performance digital transistors is to achieve >99.9999% pure semiconducting CNTs (see Table 1)—the higher the purity, the better the corresponding performance. In addition, any molecular wrapper (e.g., surfactant or polymer) should ideally be completely removed after deposition of the CNTs because this presents an unwanted residue that can hamper electrical contact, gating efficiency, and transport in the CNT transistor.

### *Other material considerations*

A transistor also requires electrical contacts, doping, and dielectrics. Because contacts from commonly used metals (e.g., Au, Pd) tend to yield Fermi-level alignment near the valence band of CNTs, p-type behavior from the injection of holes is readily achieved for CNT transistors (*21*). However, the requirement for complementary p-type and n-type transistors in digital circuits implies that controlled n-type injection and/or doping is required. Electron-donating adsorbates, such as organorhodium compounds (*22*), coupled with atomic layer–deposited encapsulation layers (*23*), enable the fabrication of highly stable n-type CNT transistors (Fig. 2C). Charge-selective contacts based on metal work function, such as Pd for p-type injection and Sc for n-type injection, also enable complementary CNT transistors (*24*, *25*). Beyond the metal selection, interfacial material considerations and overall contact structure also play a role (see Fig. 2D for an exemplary end-bonded contact structure using Mo). Extension regions of a metal-oxide-semiconductor FET (MOSFET), which are between the source

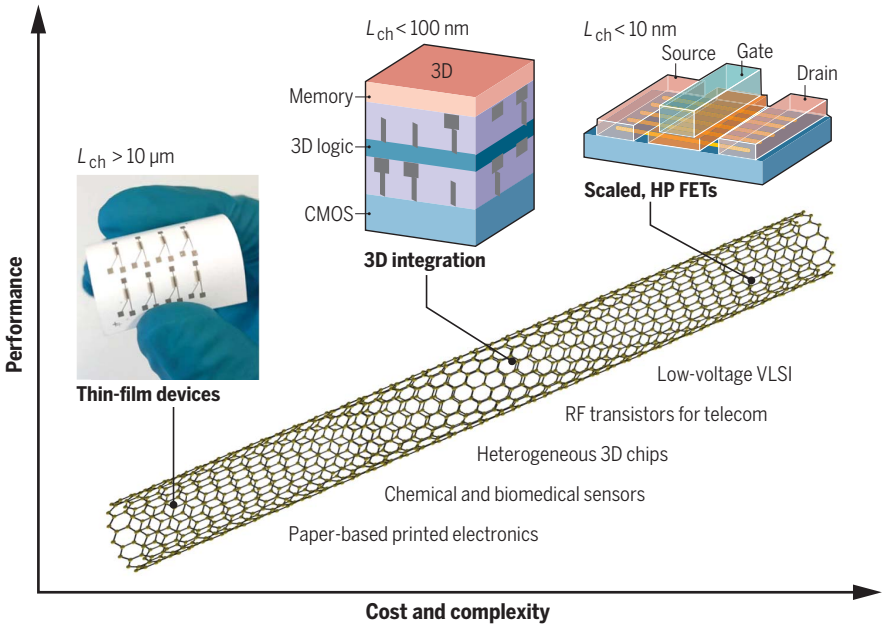


**Fig. 1. Broad range of potential applications for CNT transistors.** Illustration of device performance versus cost and complexity for some of the foremost potential applications of CNT transistors. Applications range from microscale thin-film devices (e.g., printed electronics, biosensors) to three-dimensionally integrated BEOL devices (such as heterogeneous 3D layers integrated onto silicon CMOS) and scaled high-performance (HP) FETs [such as low-voltage very-large-scale integration (VLSI)], with increasing performance corresponding with increased cost and complexity of integration. $L_{ch}$, channel length.

**Table 1. A few of the target metrics for two prominent CNT transistor applications.** Values are approximations based on achieving optimal performance. Notably, although some of these targets have been achieved, one of the foremost challenges is to achieve them simultaneously (e.g., high on-state current with low subthreshold swing, which is a measure of how much gate voltage is required to modulate the current by one decade). High-performance FETs are used in applications such as central processing units (CPUs) for servers, and TFTs are thin-film transistors such as those used in the backplane electronics of displays.

| Metric | Target for high-performance FETs | Target for TFTs |
|---|---|---|
| CNT semiconducting purity | >99.9999% | >99.9% |
| CNT array alignment | Parallel CNTs, consistent pitch | Thin-film CNTs in an unaligned network |
| CNT array density | >200 CNTs per micrometer (linear density) | >50 CNTs per square micrometer (aerial density) |
| Channel length | <12 nm | >10 µm |
| Contact length | <10 nm | >1 µm |
| On-state current | > 0.5 mA µm$^{-1}$ at 0.6 V | >100 µA mm$^{-1}$ at 3 V |
| Contact resistance | <50 ohm·µm per side | <20 kilohm·µm per side |
| Subthreshold swing | <70 mV per decade | <200 mV per decade (application dependent) |

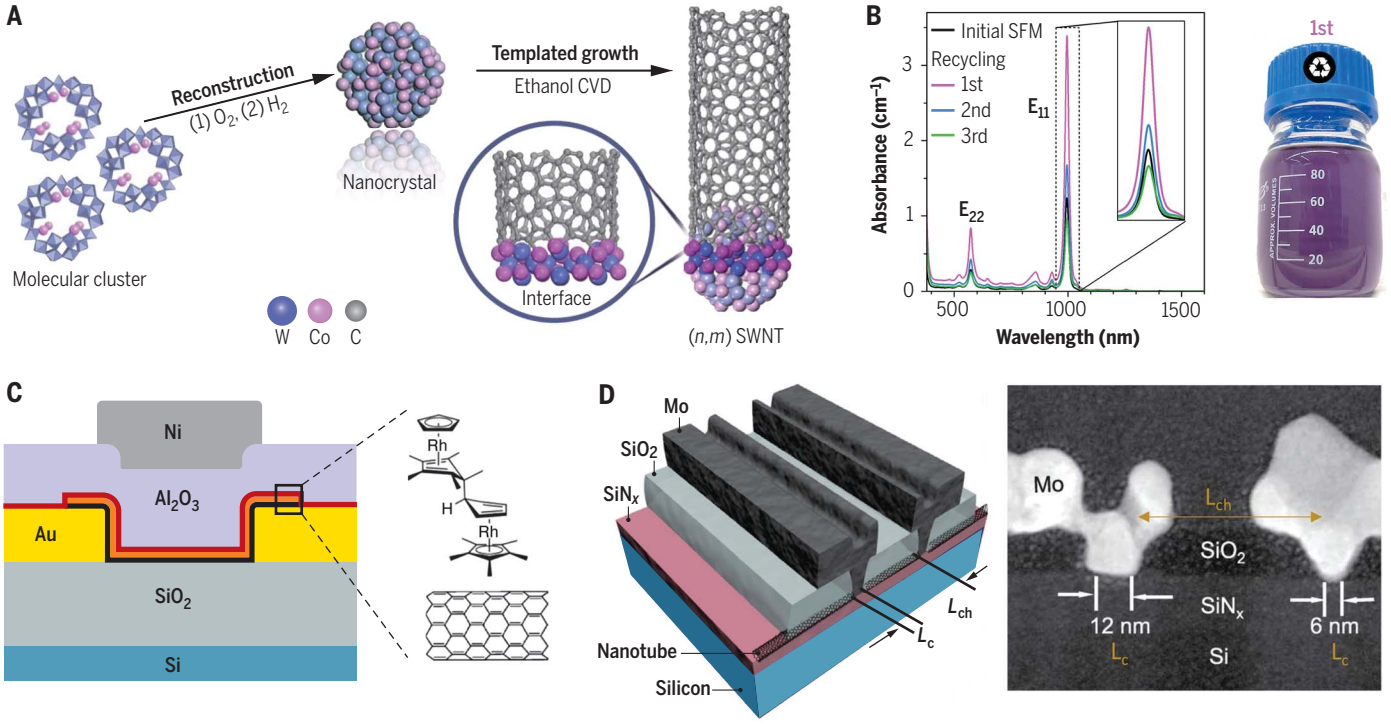


**Fig. 2. Examples of materials for high-performance CNT transistors, including synthesized CNTs, purified CNT mixtures, doping strategies, and contact metals.** (**A**) Templated CNT growth of targeted chiralities using refractory W-Co nanocrystal catalysts. CVD, chemical vapor deposition; SWNT, single-walled nanotube. [Adapted by permission from Springer Nature Customer Service Center GmbH, Springer *Nature* (*11*), copyright (2014)]. (**B**) Selective polymer dispersion enabling scalable isolation of targeted CNT chiralities from as-grown polydisperse mixtures as verified by absorption spectrum is shown on the left; a photo of the resultant bottle of sorted CNTs is shown on the right. $E_{11}$ and $E_{22}$, absorption peaks; SFM, shear force mixing. [Adapted from (*20*) with permission from Elsevier]. (**C**) Electron-donating organorhodium compounds encapsulated with atomic layer–deposited alumina enabling stable n-type CNT transistors. Black is the CNT layer, orange is the dopant layer, and red is a seeding layer for dielectric growth. [Adapted with permission from (*22*). Copyright 2016 American Chemical Society]. (**D**) When reacted to form end-bonded carbides, molybdenum contacts to CNT transistors can be scaled down to sub-10-nm dimensions in contact length ($L_c$) while retaining efficient charge injection. [Adapted with permission from (*54*)].

or drain and the gated semiconducting channel, require stable doping with well-controlled doping levels that are optimized for the trade-off between series resistance and parasitic capacitances (*26*)—a feat yet to be reliably accomplished for CNT transistors. For the gate dielectric layer, specific materials such as $Y_2O_3$ have exhibited nearly ideal properties with a high dielectric constant κ and conformal dielectric coating on CNTs after oxidation of deposited yttrium (*27*). A more conventional approach that uses atomic layer deposition of $Al_3O_3$ and $HfO_2$ bilayer dielectrics has enabled transistors that have a 10-nm gate length with a gate leakage current commensurate with state-of-the-art Si transistors (*28*). Upon integration of all these optimized materials, CNT transistors have been shown to exceed the performance of incumbent silicon integrated circuit technology, as will be discussed in the subsequent sections.

## CNT transistor design

The initial focus for CNT transistor research was on the use of a single CNT as the channel (see Fig. 3, A and B) and demonstration of ballistic transport (*21*) and digital circuit operability (*29*). Although devices with an individual nanotube channel are still of interest for sensing applications, they are no longer considered suitable for digital or radio-frequency (RF) electronics based on the need for higher current flow than a single CNT can deliver. Although the current-carrying capacity for CNTs is astonishing [~$10^9$ A cm$^{-2}$ (*30*)], they are only ~1 nm in diameter, which yields only ~10 μA per CNT. Hence, recent work has predominantly focused on having multiple CNTs in the channel.

### *Aligned arrays of CNTs*

Ideally, the CNTs in a transistor channel would be perfectly aligned in a parallel array with a controlled pitch of ~2 to 5 nm (*31*), similar to how fins of silicon are arranged in modern transistor technologies (FinFETs). Realizing such arrays continues to be a challenge. If the CNTs are too close (or bundled), it can create cross-talk (electric field screening) and effective gating issues (*32*). If the CNTs are too far apart, current density (current per transistor width) will be insufficient. For digital systems with a high density of CNT transistors, variations in the pitch between CNTs also deleteriously affects the overall energy, delay, and noise margin (*33*).

Recent progress is encouraging, including a small-scale demonstration with a controlled CNT pitch of ~10 nm using DNA-directed assembly (*34*). There are also wafer-scale, high-throughput strategies that use various forms of solution-phase assembly (also referred to as dimension-limited self-alignment or liquid crystalline interfacial assembly), which achieved a ~20-nm pitch (Fig. 3, C and D) in one report (*35*) and a 5- to 10-nm pitch in another (*36*). The primary differences in the two studies were the polymer used to wrap the CNTs and the solution-phase technique of depositing the CNTs into arrays on the substrate. Nevertheless, these approaches still require further work to remove unwanted residue from the solution-phase processing along with more consistent, controlled alignment (without bundling) in all directions with uniform spacing.

### *Thin films of CNTs*

The difficulty of achieving aligned arrays with controlled pitch has led some researchers to use unaligned CNT networks or thin films (Fig. 3, E to H). Although these unaligned films are less favorable for carrier transport, as well as for contacting and gating the nanotubes,

unaligned CNT networks have achieved high performance in nanoscale transistors (*37*, *38*). Moreover, CNT thin films can be deposited by using printing techniques, including roll-to-roll (*39*) and direct-write (*40*, *41*) approaches (Fig. 3H), which makes them attractive for TFTs. The application space for these larger (approximately tens of micrometers) TFTs is distinct from high-performance nanoscale FETs and includes sensors, flexible electronics, IoT, and display backplanes (*42*). For TFT applications, CNT thin films compete well against incumbent semiconductor options such as organics and polymers, metal oxides, and low-temperature polysilicon (LTPS) (*43*).

When CNT thin films are used in FETs with nanoscale channel lengths (<100 nm), most of the nanotubes bridge the entire channel, even if they are not perfectly aligned (Fig. 3F). In the microscale lengths of TFTs, nanotubes in the thin-film channel are not long enough to transverse the channel and instead operate as percolating networks in which electrons travel from CNT to CNT in transit from source to drain (Fig. 3G) (*44*, *45*). Compared with long-studied organic semiconductor TFTs (*46*), CNT-TFTs have considerably higher mobilities (10 to 100 $cm^2 V^{-1} s^{-1}$) and stability under bias, in air, or both.

### *Advanced gating structures*

In addition to the density and arrangement of nanotubes in the channel, the gate configuration in a CNT transistor has advanced in many ways. For nanoscale FETs, the primary goal is to maximize the gate control of the CNT energy bands in the channel, which is achieved through strong gate coupling that is typically expressed as a small scale length, λ (*47*). The scale length depends on the gate geometry and on the thickness and permittivity of both the gate dielectric and the semiconducting channel. A generally accepted approximation is that a channel length greater than 3λ will ensure that deleterious short-channel effects are avoided.

Given their intrinsically small size, CNTs offer advantages for aggressively scaled devices. Although it is ideal for an FET to have a gate-all-around geometry to minimize λ, and demonstrations of such gate structures for CNTs have been reported (*48*, *49*), studies have shown that channel lengths that are much less than 10 nm (as short as 5 nm) can be achieved in either bottom-gate (*50*, *51*) or top-gate (*51*, *52*) geometries. Although gate geometry does vary for TFTs, it is less critical and mostly limited by the gate dielectric material and the application needs.

### *Source-drain contact structures*

For highly scaled CNT transistors with small footprints, not only does the channel length need to be at the nanometer scale but the source and drain contacts also need to have minimal dimensions while still providing efficient ohmic charge injection. Palladium contacts have achieved the quantum limit of 6.5 kilohm per CNT at a 10-nm contact length for a p-type side contact, where the metal rests on top of a CNT without any chemical bonding (*53*), though this needs to be realized with higher yield and reproducibility. Alternatively, an edge-contact structure would offer ideal scalability and has been demonstrated by reacting Mo with CNTs to yield a carbide end-bonded contact with sub-10-nm contact lengths (Fig. 2D) (*54*). Regardless of the geometry, contacts to CNTs are a leading factor in determining overall performance, and the combination of material, structure, and processing must be further refined to yield contacts for both p- and n-type carrier injection with high consistency and low resistance.

## Technology demonstrations

### *High-performance, energy-efficient digital logic*

Although many applications can benefit from the properties of CNTs, digital logic applications have received the greatest attention (Fig. 4) because they have the potential to surpass incumbent Si technology in performance and energy efficiency. Such exemplary high-performance devices from aligned arrays of CNTs can achieve high on-state currents at relatively low voltages (Fig. 4, A to C). As shown in Fig. 4D, gate-all-around CNT transistors with doped extensions and multiple layers of high-density CNTs are projected to show up to seven times the energy-delay product (EDP) benefits compared with Si nanosheets at the 2-nm technology node (the EDP, or switching energy, is the product of the time and the power consumption for an on-off cycle, and a measure of energy efficiency) (*26*). As noted

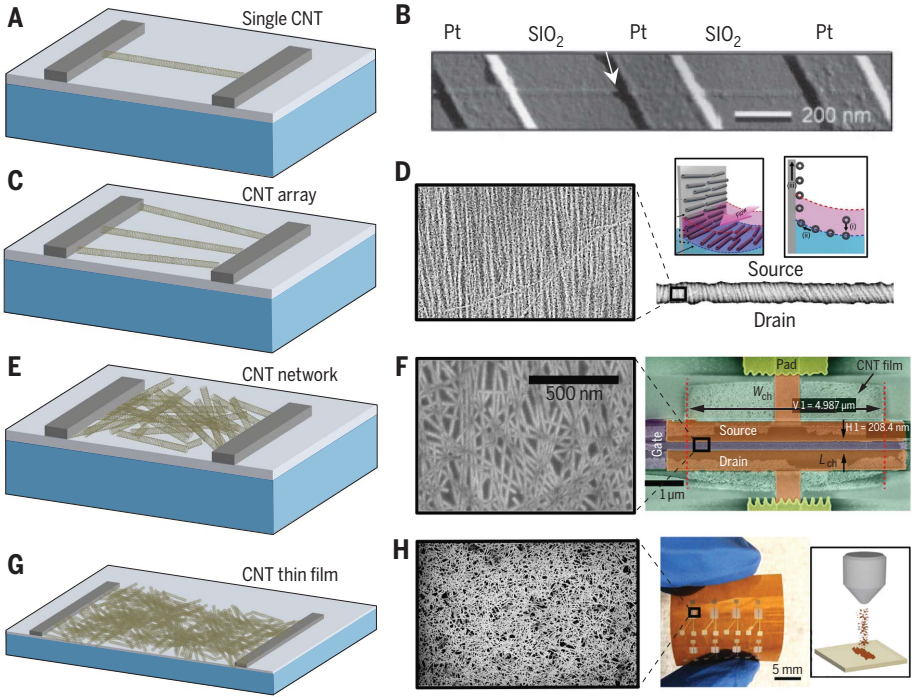


**Fig. 3. Variations in CNT transistor structures.** (**A**) Illustration of a single CNT channel with metallic source and drain contacts. (**B**) Atomic force microscopy image of the first-reported CNT transistor, which had a single nanotube. [Reprinted by permission from Springer Nature Customer Service Center GmbH, Springer *Nature* (*3*), copyright (1998)]. (**C** and **D**) Illustration of an aligned array of CNTs as the channel (C) and a corresponding recent example of a transistor with such an array (D), including a scanning electron microscopy (SEM) image of the aligned CNTs (left) and schematic of the solution-phase assembly process (right). [(D) is reprinted with permission from (*35*); Distributed under a Creative Commons Attribution NonCommercial License 4.0 (CC BY-NC). https://creativecommons.org/licenses/by-nc/4.0/]. (**E** and **F**) Illustration of a CNT network (not aligned) used as channel for nanoscale FET (E) with a corresponding recent example of a high-performance transistor (F), including a SEM image of the high-density film (left) and a top-view schematic of the device structure (right). Note that most nanotubes directly bridge the source and drain in this nanoscale configuration. H1 and V1, measurement markers of CNT film area height and channel length, respectively; $W_{ch}$, width of CNT channel region. [(F) is adapted by permission from Springer Nature Customer Service Center GmbH, Springer *Nature* (*38*), copyright (2018)]. (**G** and **H**) Illustration of a CNT thin film used in a thin-film transistor (dimensions of tens of micrometers) (G) with a corresponding recent example of an aerosol-jet printed CNT-TFT on a flexible plastic substrate (H), including a SEM image of the printed thin film (left) and a picture of the printed CNT-TFTs with a schematic of the printing technique (right). [(H) is reprinted with permission from (*41*). Copyright 2019 American Chemical Society].

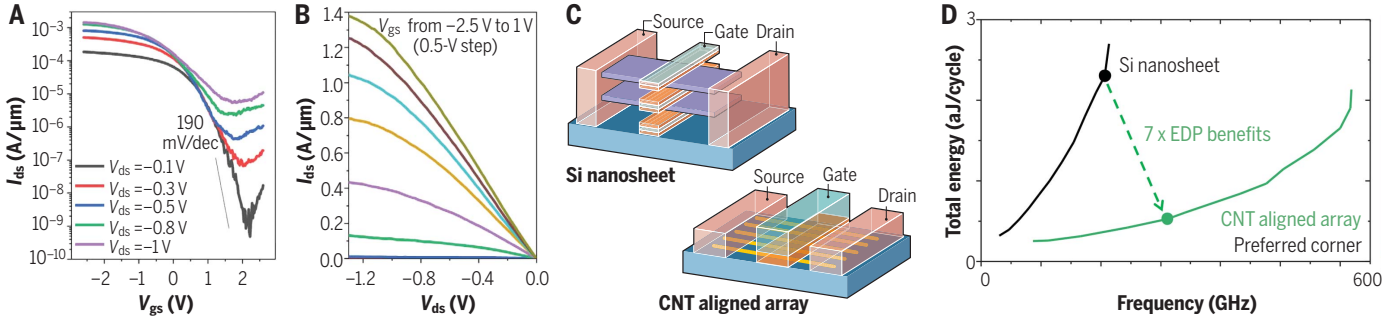


**Fig. 4. High-performance CNT transistors for digital logic applications.** (**A** and **B**) Subthreshold (A) and output characteristics (B) of CNT transistors fabricated with aligned arrays of ~150 CNTs per micrometer that achieve an on-state current of >1 mA μm$^{-1}$. $I_{ds}$, drain current; $V_{ds}$, drain-source voltage; $V_{gs}$, gate-source voltage. [Adapted with permission from (*36*)]. (**C**) Device schematics for a Si nanosheet transistor with two stacked channels and a CNT aligned array transistor. (**D**) Projected energy versus frequency pareto curves for Si nanosheet and CNT transistors at the 2-nm technology node for an inverter ring oscillator. [© 2021. Adapted, with permission, from (*26*)].

earlier, because of their ultrathin body (~1 nm), CNT transistors offer excellent electrostatic control even at aggressively scaled gate lengths, limited only by direct source-to-drain tunneling. Parasitic capacitance, a key detractor of speed and energy efficiency, accounts for >70% of the total capacitance of modern Si transistors. Because of the ultrathin body, CNT transistors have substantially lower parasitic gate-to-source or gate-to-drain capacitance. These two key attributes of CNTs, along with the high transport and injection velocities, are the physical basis for high-performance, energy-efficient digital logic.

As noted earlier, many fundamental building blocks of a CNT transistor technology have already been demonstrated. At the circuit or system level, a fully functional static random-access memory (SRAM) array (*55*), a monolithic 3D imager (*56*), and a 16-bit RISC-V (where RISC is reduced instruction set computer) processor with >14,000 transistors (Fig. 5B) (*57*) have been fabricated entirely from CNT transistors. What's more, wafer-scale fabrication of CNT transistors has been demonstrated in an industrial foundry using 200-mm wafer processing techniques (Fig. 5A) (*58*). The fabrication and design of CNT transistors with the same tools and infrastructure as commercial semiconductor technologies helps lower the barrier for the introduction of CNT devices into mass production.

At the individual device level, recent work shows short gate length (10 nm), complementary p- and n-channel devices with near ideal subthreshold swing for single-CNT transistors (*59*), and high on-state current per width for aligned CNTs with a density of 50 CNTs per micrometer (*60*). In the near future, it will be possible to integrate the following elements (already shown separately) in a single device demonstration: gate-all-around geometry (*48*, *49*), >250 CNTs per micrometer in highly aligned arrays (*36*), 3-nm oxide dielectric (target oxide capacitance = $2.94 \times 10^{-10}$ F m$^{-1}$) (*28*), sub-10-nm p-type contacts with a contact resistance of 6.5 kilohm per CNT (*53*), sub-10-nm gate length (*52*), multiple stacked CNT channel layers (*61*), and doped source or drain extensions (*62*). This MOSFET-like CNT structure with 35-nm contacted gate pitch and 20-nm active width is projected to have a performance that far exceeds that of Si transistors for a 2-nm node logic technology.

### *3D integration*

Future semiconductor chips will go beyond 2D device miniaturization and instead will have 3D layers of active devices (*63*). Because logic device layers in 3D must be thin and fabricated at temperatures that are compatible with back-end-of-line (BEOL) wiring layers (typically <400°C), CNT transistors are particularly well-suited for 3D integration because of the low device-fabrication temperature and thin device layer. Starting from the first demonstration of an all-CNT transistor computer almost a decade ago (*64*), progress has occurred not only in the level of integration but also in the variety of devices as well as maturation of the technology from university laboratories to industry.

A four-layer monolithically integrated chip comprising a silicon transistor layer, a CNT transistor memory read-out circuit layer, a resistive switching metal-oxide random-access memory (RRAM) layer, and a CNT transistor sensor layer on the top illustrates the benefits of monolithic integration (Fig. 5, C to E) (*65*). This 3D chip can process information from the sensors to the memory cells to the transistors in parallel at rates of terabytes per second. Another example is an end-to-end brain-inspired hyperdimensional computing nanosystem that is effective for cognitive tasks such as language recognition, which was realized with monolithic 3D integration of CNT transistors and RRAM, enabling fine-grained and dense vertical connections between computation and storage layers using BEOL interlayer vias (*66*). The CNT transistor fabrication process not only has been shown on full 200-mm wafers (*58*) but also has 3D integration with RRAM (*67*).

### *RF electronics*

Although digital electronics remains the dominant focus in the field, CNT transistors also hold great promise for high-frequency RF transistors, which are relevant to telecommunications applications (*68*, *69*). Many of the material and device needs for digital CNT transistors also apply to RF electronics, with some relaxing of the semiconducting purity needs and an enhanced need for high transconductance and linearity, which translates to low distortion when amplifying a signal. Recent progress on RF CNT transistors from aligned arrays of nanotubes shows the ability to operate at frequencies up to hundreds of gigahertz with attractively low power consumption and high versatility for integration in system-on-chip applications (*70*).

### *Printed electronics*

The ability to purify a solution-phase dispersion of semiconducting CNTs also enables printing into thin-film devices (Fig. 2H). Many reports have shown that fully printed CNT-TFTs can be used in digital logic circuitry to illustrate the ability of these devices to deliver computational functionality (*71*–*73*). However, given the low cost of legacy-node silicon transistor technologies, the likelihood that printed CNT-TFT circuitry will be of widespread use is low. More encouraging is the use of printed CNT-TFTs for the backplane control of displays (*74*) or for custom biosensing systems (*75*). Recent studies also reveal the recyclability of CNT thin films (*76*), which shows promise for enabling a fully printed, paper-based electronic system in which all core materials are able to be recaptured and reused (*77*).

## Future developments and perspectives

### *Materials outlook*

Advances in materials are anticipated to be central to future advances in CNT transistors. Improving the purity of semiconducting CNTs is critical for all device use cases. In this regard, one of the largest impediments to minimizing

metallic CNT impurities down to concentrations of parts per million or billion is the lack of high-throughput analytical methods for detecting ultralow concentrations of metallic CNTs. Most high-throughput optical detection methods for CNTs (such as photoluminescence spectroscopy) are less sensitive, if not completely insensitive, to metallic species. Indeed, the only established method for quantifying ultralow concentrations of metallic CNTs is to fabricate massive arrays of individual CNT transistors and then electrically probe them one by one in search of short circuits. This approach is extremely time consuming and only gets worse as the semiconducting purity increases. Thus, most CNT separation methods have only been optimized to the detection limits of optical spectroscopy (~99.9%).

Another unresolved issue for semiconducting CNTs is the need for a scalable and sustainable manufacturing approach to produce sufficient quantities of ultrahigh-purity semiconducting CNTs to meet the potentially large market represented not only by high-performance integrated circuits but also by high-volume printed electronics. Most solution-based separation methods do not possess fundamental barriers to scalability, but the yields of these processes are ultimately limited by the quality of the input raw material. Improvements in synthesis that minimize impurities and maximize semiconducting purity with narrow CNT diameter distributions are needed to improve the yield of downstream separation. An enticing option would be to refine cloning (*13*) to the point that iterative separation and amplification could be achieved in a manner analogous to the polymerase chain reaction (PCR) in biochemistry.

Ultimately, growth conditions encompass such a vast parameter space that methods for efficiently searching for and identifying optimal growth conditions are needed. Emerging artificial intelligence and machine-learning optimization approaches coupled with high-throughput experimental screening hold promise for next-generation synthetic efforts (*15*). Similarly, the discovery, optimization, and integration of the many other materials in a CNT transistor (including dopants, contacts, gate electrodes, and dielectrics) can also likely be accelerated by machine learning coupled with high-throughput experimental screening.

### *Device outlook*

Although much has been learned about establishing interfaces to CNTs, including gate structure and contacts, challenges remain. The roles of material selection and purification (discussed earlier), methods of fabrication, and doping control continue to be elucidated in an expansive volume of reports. Indeed, one of the foremost challenges moving forward is determining what combination of materials and processes (of the thousands reported) is most appropriate to use. More systematic studies are needed that explore certain contact and gate-stack material configurations for their impact on device performance, yield, reproducibility, and stability. For example, it is clear that CNT channels are scalable to sub-10-nm lengths in a variety of configurations, but it is not clear which device structure is superior (e.g., top-gate versus gate-all-around, side contact versus edge contact) and whether top-performing options also have fabrication processes that are compatible with relevant manufacturing in complementary metal-oxide-semiconductor (CMOS) fabs. Most metal-contact formation processes rely on liftoff, which is not considered a scalable process, and the liftoff-free alternatives also tend to rely on slow patterning processes (*78*).

The scalability of the contact length, which is an equally important parameter as the gate length for overall transistor scaling, needs further consideration. Some studies show severe degradation at sub-30-nm contact lengths (*52*), whereas others have shown less degradation at scaled lengths but have not yet realized them at high yield (*53*). Such contact-length scaling challenges are common to all transistors (*79*), but discovering a solution that allows for aggressively scaled contacts without degrading the device would be a critical advance. End-bonded or edge contacts present one such possibility (*54*), although further work is required to reduce the processing temperature and to understand transport and performance limits. In addition, realizing an equally high-quality and scalable contact to n-type CNT transistors remains to be addressed.

Regarding TFTs from CNTs, much of the knowledge gained from nanoscale FET devices is applicable. The foremost exceptions are that a TFT technology should ideally be compatible with large substrate sizes and have exceptionally low cost. Because one of the primary applications for TFTs is in display backplanes, the materials and processes should be scalable to large panels. Although device-level performance and size matter, TFTs have relaxed constraints, with more emphasis given to fabrication cost because these devices will be used in commodity applications (such as backplanes) or disposable applications (such as IoT). The recent demonstration of recyclable printed



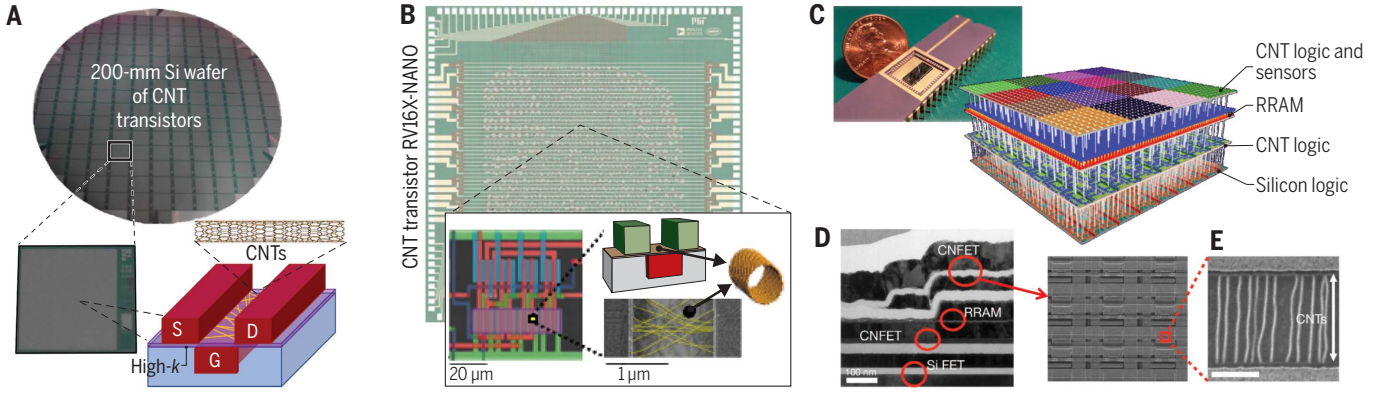


**Fig. 5. Wafer-scale and 3D integration of CNT transistors.** (**A**) A 200-mm Si wafer with CNT transistors processed in a commercial silicon foundry. An image of a single die or chip from the wafer is shown at the bottom left, and a schematic of the CNT transistor structure is shown at the bottom right. D, drain; G, gate; *k*, relative permittivity; S, source. [Adapted by permission from Springer Nature Customer Service Center GmbH, Springer *Nature* (*58*), copyright (2020)]. (**B**) Optical image of a RISC-V processor realized with CMOS CNT transistors (RV16X-NANO), including higher magnification images showing details of CNT circuits (false colors represent different metal layers) and a single CNT device (CNTs are highlighted in yellow). [Adapted by permission from Springer Nature Customer Service Center GmbH, Springer *Nature* (*57*), copyright (2019)]. (**C** to **E**) Image and schematic of a 3D N3XT chip with monolithic integration of CNT transistors and RRAM memory layers on top of silicon logic (C); cross-sectional TEM image showing the bottom Si logic layer, the RRAM memory layer, and the two CNT transistor layers [carbon nanotube field-effect transistor (CNFET), logic, and sensors] (D); and scanning electron microscopy images of a CNT circuit and devices in the top layer of the 3D N3XT chip (E) (scale bar, 500 nm). [Adapted by permission by Springer Nature Customer Service Center GmbH, Springer *Nature* (*65*), copyright (2017)].

CNT-TFTs on paper substrates suggests sustainable implementations (*77*). Improvements in CNT-TFT yield and stability will be critical, particularly the role of tube-tube contacts in percolating networks.

### *Technology outlook*

The realization of a CNT transistor technology that meets high-volume manufacturing needs has many remaining hurdles that require a concerted effort from academia and industry to surmount. Regarding semiconducting CNT purity, although the highest possible purity remains ideal for EDP, logic design techniques can be used to relax the requirement for certain applications by about 100 times (from 99.9999 to 99.99%), without imposing additional processing steps or redundancy (*65*). For high-performance digital systems, device variations play an important role in determining the overall EDP and noise margin of the system. CNT-specific sources of variation include CNT density and pitch (distance between CNTs in a multi-CNT transistor), CNT bandgap (determined by the chirality and diameter), and extreme sensitivity to random fixed charges in the surroundings (which is also the reason why CNTs are ultrasensitive sensors). The transistor width (perpendicular to the direction of current flow) of logic technologies is on the order of 20 to 40 nm. For a CNT density of 250 CNTs per micrometer, there will only be 5 to 10 CNTs in the channel; hence, variations of the CNT density and the CNT pitch will lead to substantial variations in the current drive.

Design solutions that mitigate such variations are essential as part of a co-design process for technology development (*80*). For example, CNT bandgap variation directly translates into variation in off-state leakage current through the threshold voltage and band-to-band tunneling at the drain. Band-to-band tunneling leakage varies exponentially with bandgap and sets a minimum achievable leakage current (*81*)—a boundary for trading on-state current with off-state leakage current by tuning the threshold voltage. Direct source-to-drain tunneling current also depends exponentially on the bandgap and sets the limit for gate-length scaling. The choice of the CNT diameter (bandgap) is faced with the same trade-off as other FETs. Small-bandgap CNTs have lower effective masses and higher on-state currents, and large-bandgap CNTs have lower tunneling off-state leakage currents and can scale down further in gate length and maintain higher operating voltages for high speed. The optimal choice is necessarily application-dependent and must be co-designed, given the target computing workloads (*82*).

Although the CNT transistor inherits all the limitations of a MOSFET (electrostatics and transport physics) and has all the challenges of a low-dimensional channel material (contacts and surfaces without dangling bonds), it also retains all the benefits of an FET, which include a well-developed circuit or system design ecosystem and a mature manufacturing technology, with the further potential to integrate in three dimensions for chips with increasing device count and connectivity. These benefits are projected to eventually outweigh all the limitations because the power of incumbency and scalability in three dimensions cannot be understated. Between the opportunities in high-performance digital logic with the potential for 3D integration and the possibilities for printed and even recyclable thin-film electronics, CNT transistors warrant a renewed and even redoubled effort from academic, government, and industry contributors. These molecular transistor technologies are within reach, but only if the remaining challenges are surmounted by the scientific and engineering communities.

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## ACKNOWLEDGMENTS

**Funding:** A.D.F. acknowledges support from the National Science Foundation (NSF) (NSF ECCS-1915814). M.C.H. acknowledges support from the NSF Materials Research Science and Engineering Center at Northwestern University (NSF DMR-1720139). H.-S.P.W. acknowledges support in part from the Defense Advanced Research Projects Agency (DARPA) Electronics Resurgence Initiative (ERI) Three Dimensional Monolithic System on a Chip (3DSoC), the NSF (award 1640060), and the Stanford SystemX Alliance, as well as collaboration and discussion with G. Pitner and colleagues at Taiwan Semiconductor Manufacturing Company (TSMC), M. Shulaker at MIT, and S. Mitra at Stanford. **Competing interests:** The authors declare no competing interests. 

Submitted 15 June 2022; accepted 7 September 2022
10.1126/science.abp8278

# Carbon nanotube transistors: Making electronics from molecules

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*Science* **378** (6621), . DOI: 10.1126/science.abp8278