VLSI Design EE 523
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Lecture 17

Topics for lecture 17

- Some solved examples of Power Dissipation in CMOS circuits
- Introduce Reliability, Circuit Life in CMOS chips
- Latchup problem in CMOS

Eg from text book regarding activity factor

Example 5.1

A digital system-on-chip in a 1 V 65 nm process (with 50 nm drawn channel lengths and λ = 25 nm) has 1 billion transistors, of which 50 million are in logic gates and the remainder in memory arrays. The average logic transistor width is 12 λ and the average memory transistor width is 4 λ. The memory arrays are divided into banks and only the necessary bank is activated so the memory activity factor is 0.02. The static CMOS logic gates have an average activity factor of 0.1. Assume each transistor contributes 1 fF/μm of gate capacitance and 0.8 fF/μm of diffusion capacitance. Neglect wire capacitance for now (though it could account for a large fraction of total power). Estimate the switching power when operating at 1 GHz.

SOLUTION: There are $(50 \times 10^6$ logic transistors$)(12\ \lambda)(0.025\ \mu m/\lambda)((1 + 0.8)$ fF/μm) = 27 nF of logic transistors and $(950 \times 10^6$ memory transistors$)(4\ \lambda)(0.025\ \mu m/\lambda)((1 + 0.8)$ fF/μm) = 171 nF of memory transistors. The switching power consumption is $[(0.1)(27 \times 10^{-9}) + (0.02)(171 \times 10^{-9})](1.0\ V)^2(10^9\ Hz) = 6.1$ W.

Eg related to Leakage current and Static Power

Example 5.4

Consider the system-on-chip from Example 5.1. Subthreshold leakage for OFF devices is 100 nA/μm for low-threshold devices and 10 nA/μm for high-threshold devices. Gate leakage is 5 nA/μm. Junction leakage is negligible. Memories use low-leakage devices everywhere. Logic uses low-leakage devices in all but 5% of the paths that are most critical for performance. Estimate the static power consumption.

SOLUTION: There are $(50 \times 10^6$ logic transistors$)(0.05)(12\ \lambda)(0.025\ \mu m/\lambda) = 0.75 \times 10^6$ μm of low-threshold devices and $[(50 \times 10^6$ logic transistors$)(0.95)(12\ \lambda) + (950 \times 10^6$ memory transistors$)(4\ \lambda)](0.025\ \mu m/\lambda) = 109.25 \times 10^6\ \mu$m of high-threshold devices. Neglecting the benefits of series stacks, half the transistors are OFF and contribute subthreshold leakage. Half the transistors are ON and contribute gate leakage. $I_{sub} = [(0.75 \times 10^6\ \mu m)(100\ nA/\mu m) + (109.25 \times 10^6\ \mu m)(10\ nA/\mu m)]/2 = 584$ mA. $I_{gate} = ((0.75 + 109.25) \times 10^6\ \mu m)(5\ nA/\mu m)/2 = 275$ mA. $P_{static} = (584\ mA + 275\ mA)(1\ V) = 859$ mW. This is 15% of the switching power and is enough to deplete the battery of a hand-held device rapidly.

Power Header Switch Sizing

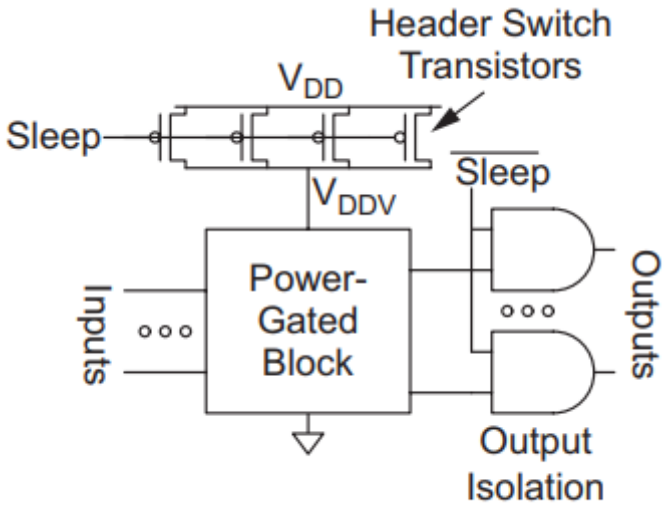

FIGURE 5.24 Power gating

Example 5.5

A cache in a 65 nm process consumes an average power of 2 W. Estimate how wide should the pMOS header switch be if delay should not increase by more than 5%?

SOLUTION: The 65 nm process operates at 1 V, so the average current is 2 W / 1 V = 2 A. The pMOS transistor has an ON resistance of $R = 2\ \text{k}\Omega \cdot \mu\text{m}$. A 5% delay increase corresponds to a droop on V_{DDV} of about 5% (check this using EQ (4.29). Thus, $R_{\text{switch}} = 0.05 \times 1\ \text{V} / 2\ \text{A} = 25\ \text{m}\Omega$. So the transistor width must be $\text{k}\Omega \cdot \mu\text{m}/25\ \text{m}\Omega = 8 \times 10^4\ \mu\text{m}$. The ON resistance at low V_{ds} is lower than R. Circuit simulation shows that a width of $3.7 \times 10^4\ \mu\text{m}$ suffices to keep droop to 5%.

4.4.6.4 Voltage Dependence Designers often need to predict how delay will vary if the supply or threshold voltage is changed. Recalling that delay is proportional to CV_{DD} / I and using the α-power law model of EQ (2.30) for I_{dsat}, we can estimate the scaling of the RC time constant and of gate delay as

$$\tau = k \frac{CV_{DD}}{\left(V_{DD} - V_t\right)^{\alpha}} \qquad (4.29)$$

where k reflects process parameters.

Readings

- Chapter 5 of textbook ‘CMOS VLSI Design’ by Weste and Harris related to Power Dissipation in CMOS circuits