CS/EE 320 Computer Organization and Assembly Language Spring 2024

Lecture 5

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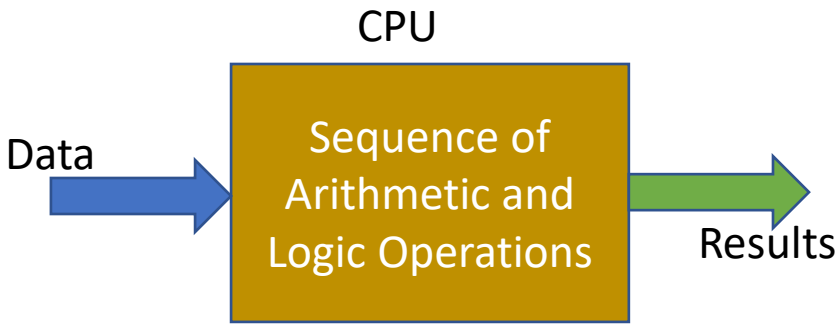
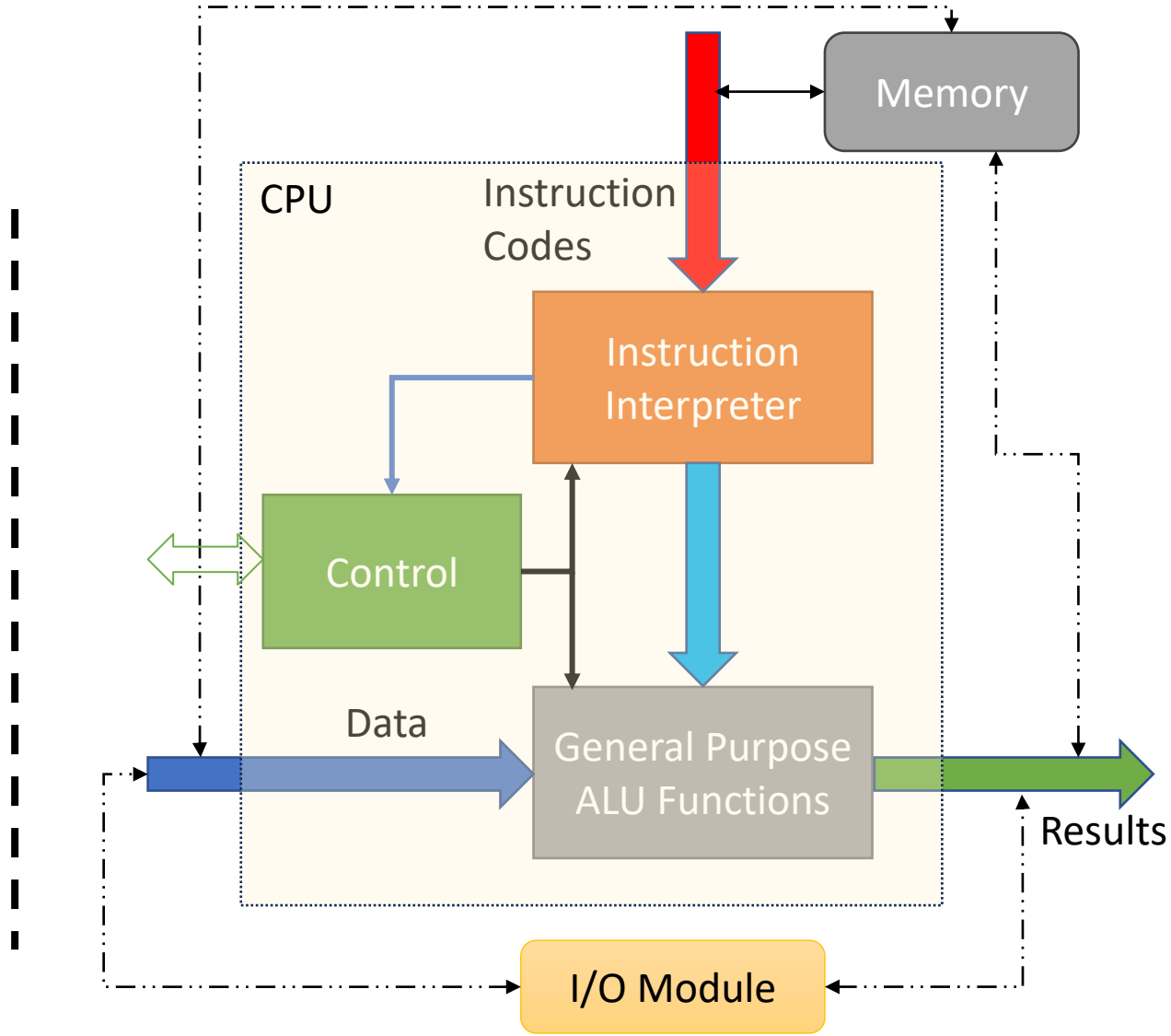
Topics

- Basic Working of Von-Neumann Stored Program Computer
- Registers Available Inside CPU: **MBR, MAR, IR, AC, PC**, etc.
- Instruction Execution Cycle Simple – Fetch, Decode, Execute
- Detailed Instruction Execution Cycle with Operand Fetch and Storage of Results, Sequential Processing
- Introducing Assembly Language Instructions
- QUIZ 1

Basic Computer Operations

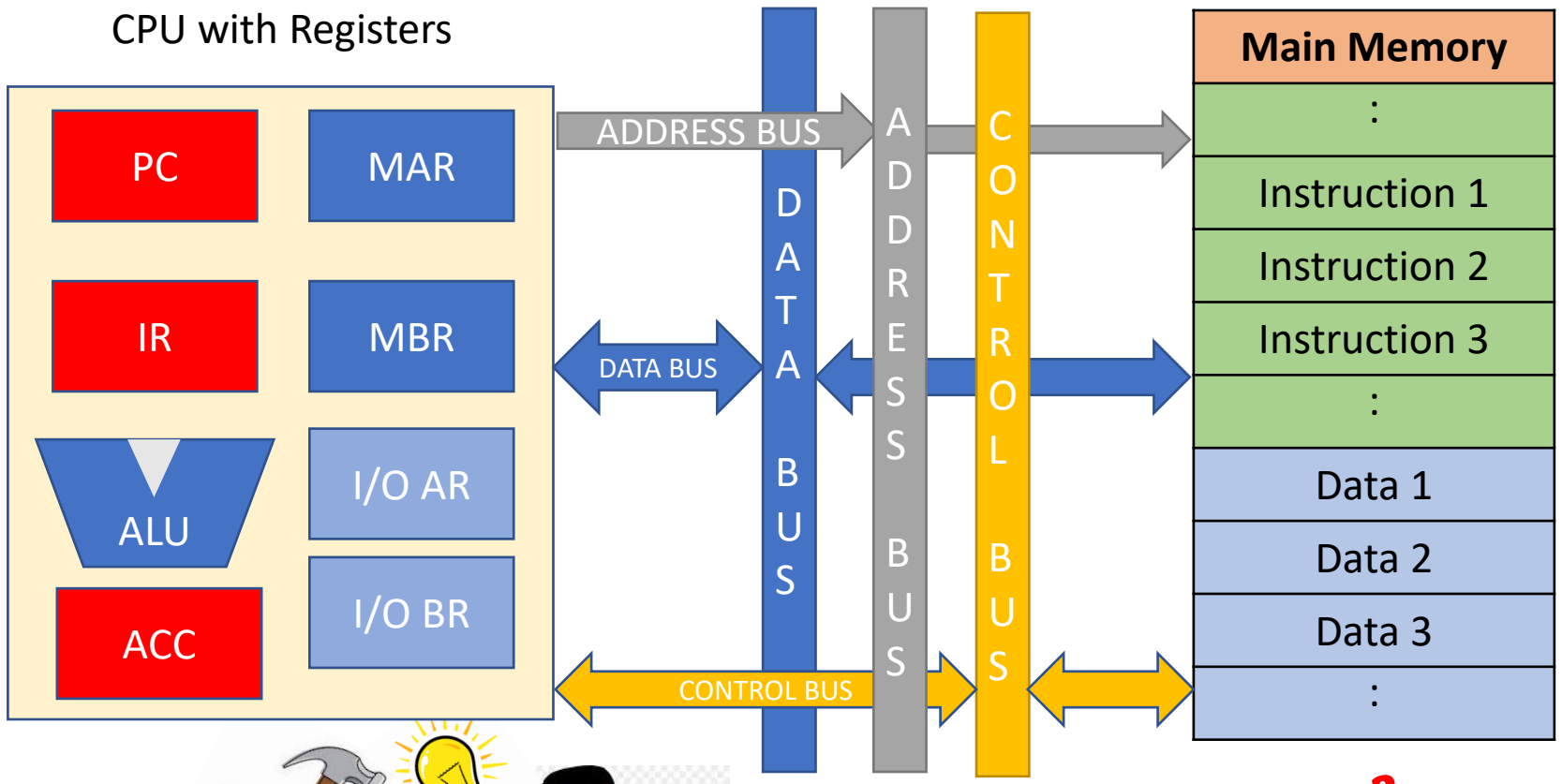




Features of Von-Neuman Architecture

- Data and Instructions are stored in a single read / write Memory
- Contents of Memory are Addressable by Location Address irrespective of stored Contents
- Execution of program occurs in a Sequential Fashion unless Modified through Branch instructions

Essential Registers in a CPU



Purpose of CPU registers?

REGISTERS IN CPU	
ABBREVIATION	**FULL NAME**
PC	Program Counter
IR	Instruction Register
ALU	Arithmetic Logic Unit
ACC	Accumulator
MAR	Memory Address Register
MBR	Memory Buffer Register
I/O AR	I/O Address Register
I/O BR	I/O Buffer Register

Buffer = temporary storage

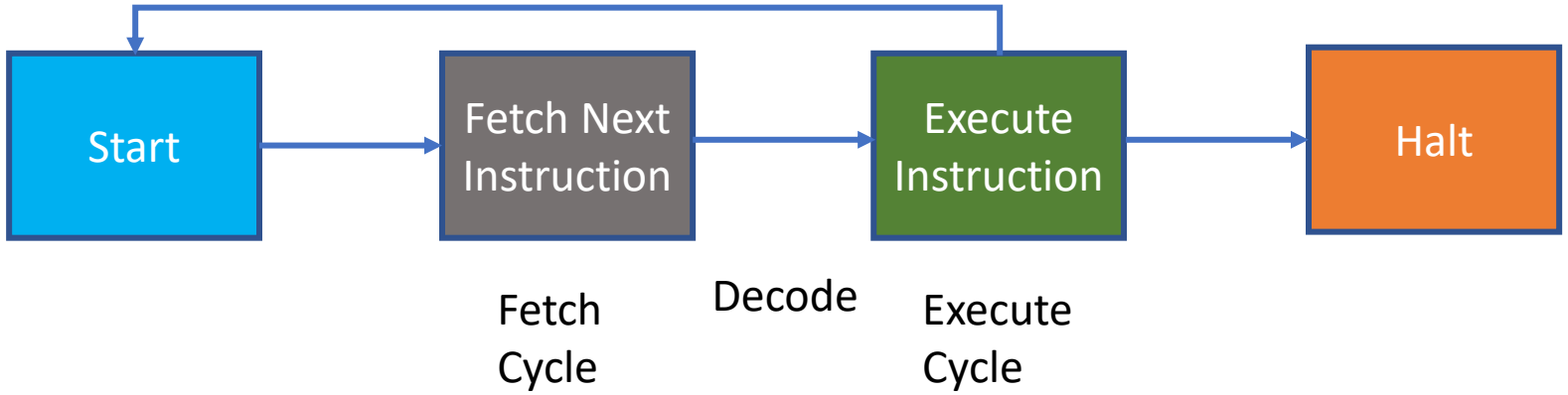
PC, IR and AC Registers

- PC (Program Counter) Register always holds the value of next instruction to be fetched
- PC is incremented by ‘1’ address after each instruction to point to next location in instruction memory
- To alter the sequence of operation, a new value is loaded into the PC
- IR (Instruction Register) Register holds the fetched instruction
- The contents of IR are examined to determine the ALU and Control operation required from this instruction
- AC (Accumulator) register stores results from ALU or other operations inside CPU

Typical Actions by CPU

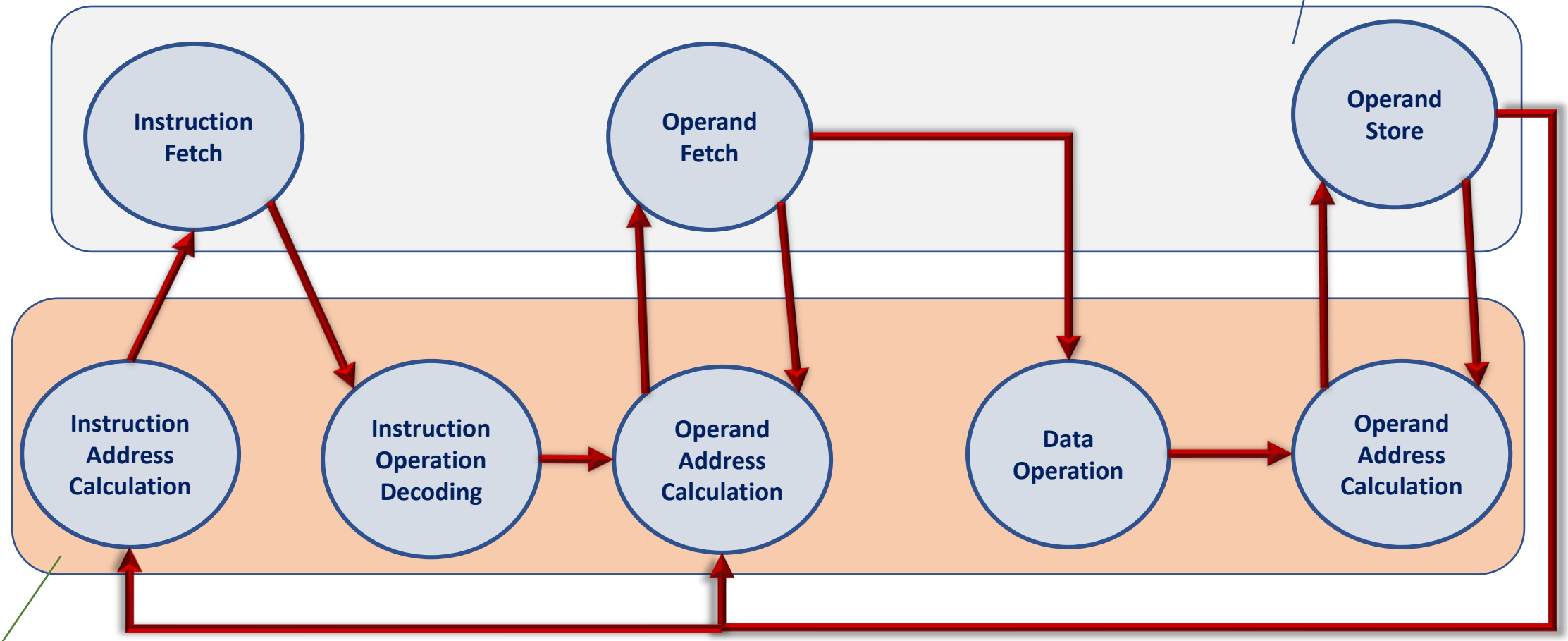
- CPU Actions fall in four categories:
  - Processor – Memory data movement
  - Processor – I/O data movement
  - Data Processing using ALU
  - Control operation to alter the sequence of program execution

Basic Instruction Cycle



- The instruction fetch and execute is repeated until the end of program
- Execution may involve several operations depending upon nature of instruction

Instruction Cycle State Diagram



Q: Why does Operand Address Calculation appear twice in state diagram:
A: A single instruction may require read, write or both operations

Instruction Execution Steps

- PC gives address of instr to be fetched from memory.
- After fetching, the instruction op code is decoded. The processor identifies number of operations. If operand is needed from memory, then its address is calculated.
- Operand fetching process is repeated until all operands are fetched from memory.
- Data operation is performed in ALU and result is produced in ACC.
- If the result is stored in a register than instruction ends here.
- If the destination of result is in memory then destination address is calculated and result moved to memory.
- In tandem, the PC is incremented by '1' **(or 4?)** to determine address of next instruction.
- Instruction cycle is repeated for further instructions.

An Example of Program Execution Cycle

Sequence of Operation

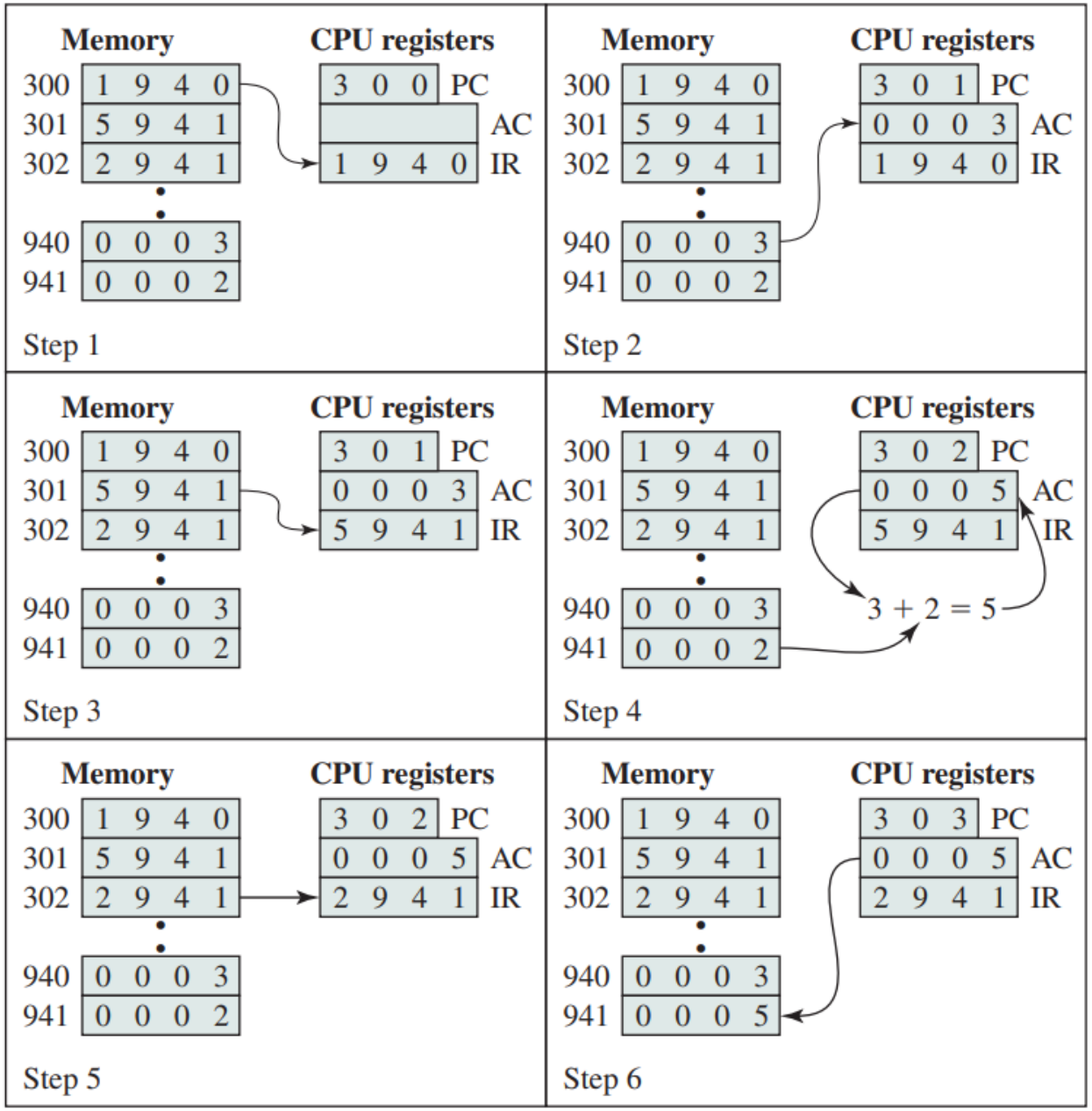
Opcode determines that

AC is to be loaded from memory

Then ADD instruction

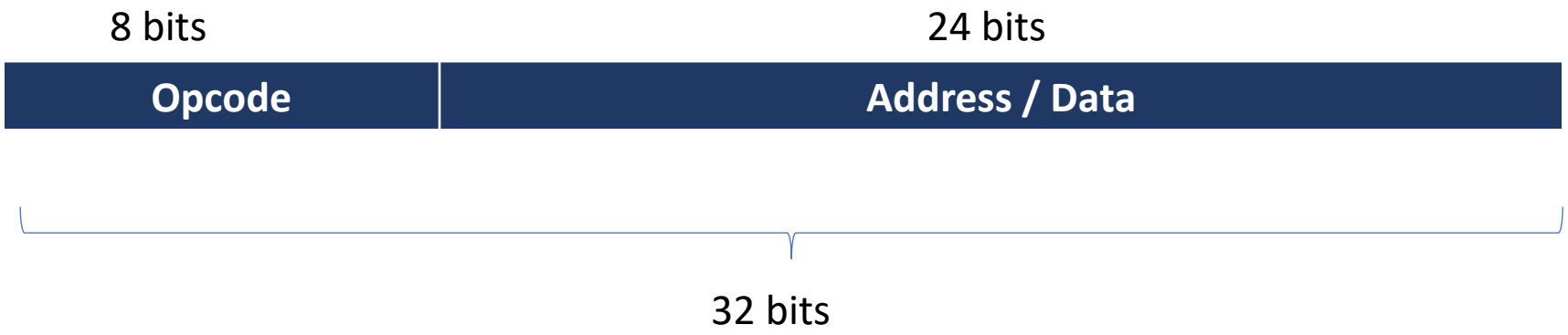
Then AC stored in location 941

? CPU needs more than one Register to store second operand



How an Assembly Instruction is Formed?

As an example:



What happens with the full range of Address or Data ?

Answer: Different Addressing Modes

Readings

- Chapter 2 of P&H Textbook