

CS/EE 320 Computer Organization and Assembly Language Spring 2024

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Topics

- Logic and Arithmetic Instructions in Assembly Language
- Binary Numbers, Logic Design and Boolean Algebra
- Basic digital logic functions Invert, AND, OR, NAND, NOR
- Half-Adder (without Carry-In)
- 1-bit Full Adder (with Carry-In)
- Making 2's Complement Subtractor from Full-Adder
- Design of 1-bit ALU containing AND gate, OR gate, Full Adder
- Quiz 2

MIPS Arithmetic Instructions



Category	Instruction	Example		Meaning	Comments
	add	add	\$s1,\$s2,\$s3	\$s1 = \$s2 + \$s3	Three operands; overflow detected
	subtract	sub	\$s1,\$s2,\$s3	\$s1 = \$s2 - \$s3	Three operands; overflow detected
	add immediate	addi	\$s1,\$s2,100	\$s1 = \$s2 + 100	+ constant; overflow detected
	add unsigned	addu	\$s1,\$s2,\$s3	\$s1 = \$s2 + \$s3	Three operands; overflow undetected
	subtract unsigned	subu	\$s1,\$s2,\$s3	\$s1 = \$s2 - \$s3	Three operands; overflow undetected
	add immediate unsigned	addiu	\$s1,\$s2,100	\$s1 = \$s2 + 100	+ constant; overflow undetected
	move from coprocessor register	mfc0	\$s1,\$epc	\$s1 = \$epc	Copy Exception PC + special regs
Arithmetic	multiply	mult	\$s2,\$s3	Hi, Lo = \$s2 × \$s3	64-bit signed product in Hi, Lo
	multiply unsigned	multu	\$ s2, \$ s3	Hi, Lo = $$s2 \times $s3$	64-bit unsigned product in Hi, Lo
	divide	div	\$ s2, \$ s3	Lo = \$s2 / \$s3, Hi = \$s2 mod \$s3	Lo = quotient, Hi = remainder
	divide unsigned	divu	\$s2,\$s3	Lo = \$s2 / \$s3, Hi = \$s2 mod \$s3	Unsigned quotient and remainder
	move from Hi	mfhi	\$ s1	\$s1 = Hi	Used to get copy of Hi
	move from Lo	mflo	\$ s1	\$s1 = Lo	Used to get copy of Lo

MIPS Logical Instructions



Logical	AND	AND	\$s1,\$s2,\$s3	\$s1 = \$s2 & \$s3	Three reg. operands; bit-by-bit AND
	OR	OR	\$s1,\$s2,\$s3	\$s1 = \$s2 \$s3	Three reg. operands; bit-by-bit OR
	NOR	NOR	\$s1,\$s2,\$s3	\$s1 = ~ (\$s2 \$s3)	Three reg. operands; bit-by-bit NOR
	AND immediate	ANDi	\$s1,\$s2,100	\$s1 = \$s2 & 100	Bit-by-bit AND with constant
	OR immediate	ORi	\$s1,\$s2,100	\$s1 = \$s2 100	Bit-by-bit OR with constant
	shift left logical	s11	\$s1,\$s2,10	\$s1 = \$s2 << 10	Shift left by constant
	shift right logical	srl	\$s1,\$s2,10	\$s1 = \$s2 >> 10	Shift right by constant

Arithmetic for Computers

- Operations on integers
 - Addition and subtraction
 - Multiplication and division
 - Dealing with overflow
- Floating-point real numbers (later)
 - Representation and operations

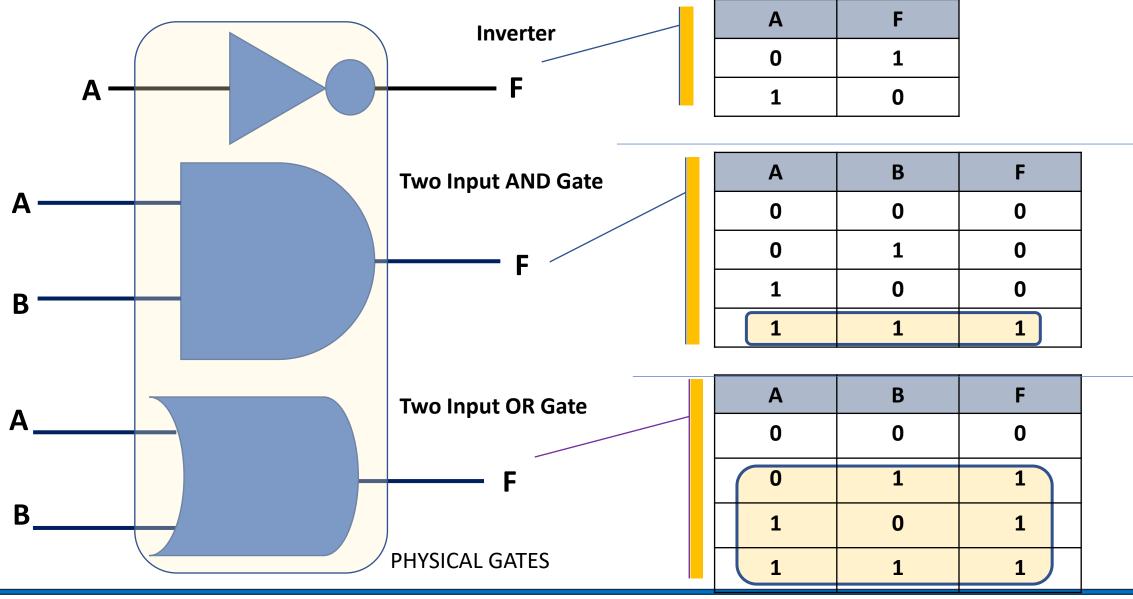
Basic Logic Operations in CPU



- Functions Through Logic Gates
 - NOT
 - AND
 - OR
 - NOR
 - NAND
 - XOR

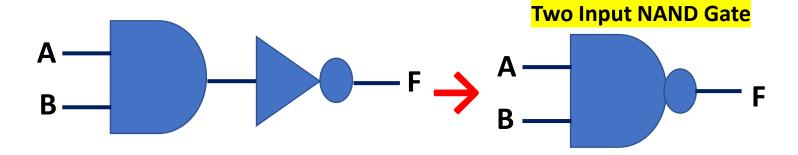
Gates (Primary Gates)





Gates (Compound Gates)





		•
0	0	1
0	1	1
1	0	1
1	1	0

AND Gate followed by Inverter

A	Two Input NOR Gate
В	F
D	OR Gate followed by Inverter
	on date followed by lifetier

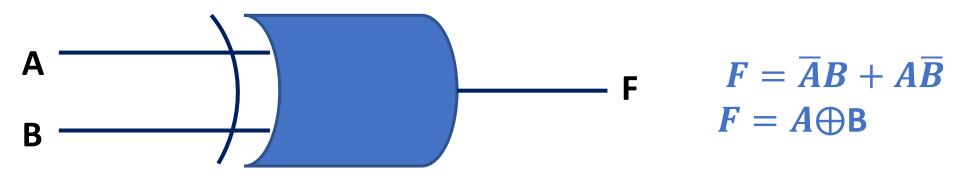
Α	В	F
0	0	1
0	1	0
1	0	0
1	1	0

Computer Organization and Assembly Language Spring 202

Complex Gates – the XOR and XNOR

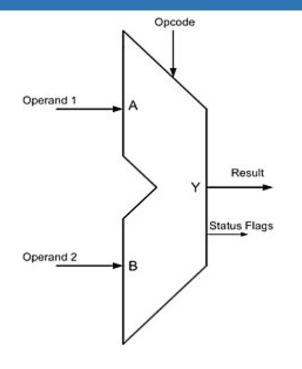


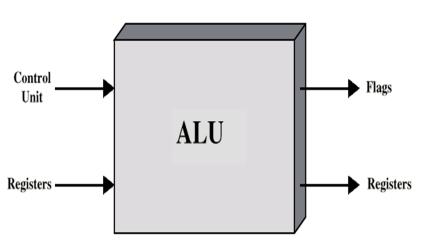
Two Input Exclusive OR Gate



Α	В	F
0	0	0
0	1	1
1	0	1
1	1	0

Arithmetic & Logic Unit

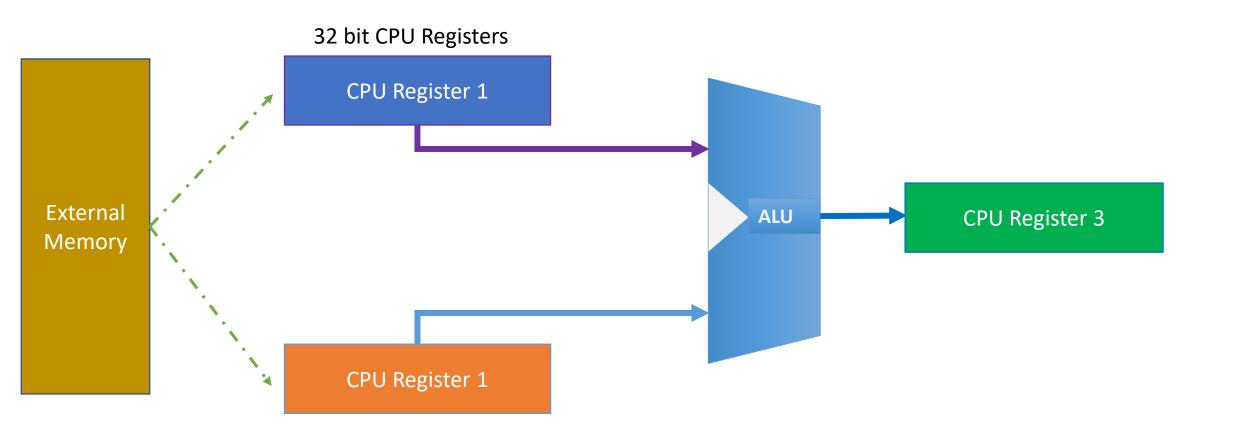




- Does all calculations
- Everything else in the computer is there to service this unit
- Handles integers
- May handle floating point (real) numbers
- May be separate FPU (maths co-processor)
- May be on chip separate FPU (Eg. 486DX)

ALU in Load/Store Architecture





Number Systems



- ALU does calculations with binary numbers
- Decimal number system
 - Uses 10 digits (0,1,2,3,4,5,6,7,8,9)
 - In decimal system, a number 84, e.g., means 84 = (8x10) + 4
 - 4728 = (4x1000) + (7x100) + (2x10) + 8
 - Base or radix of 10 → each digit in the number is multiplied by 10 raised to a power corresponding to that digit's position
 - E.g. $83 = (8x10^1) + (3x10^0)$
 - $4728 = (4x10^3) + (7x10^2) + (2x10^1) + (8x10^0)$

Binary Number System



- Uses only two digits, 0 and 1
- It is base or radix of 2
- Each digit has a **value** depending on its **position**:

•
$$10_2 = (1 \times 2^1) + (0 \times 2^0) = 2_{10}$$

•
$$11_2 = (1x2^1) + (1x2^0) = 3_{10}$$

•
$$100_2 = (1x2^2) + (0x2^1) + (0x2^0) = 4_{10}$$

•
$$1001.101_2 = (1x2^3) + (0x2^2) + (0x2^1) + (1x2^0) + (1x2^{-1}) + (0x2^{-2}) + (1x2^{-3}) = 9.625_{10}$$

Decimal to Binary conversion

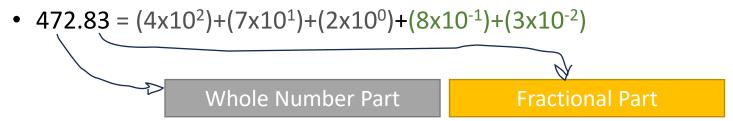


- Integer and fractional parts are handled separately,
 - Integer part is handled by repeating division by 2
 - Factional part is handled by repeating multiplication by 2
- E.g. convert decimal 11.81 to binary
 - Integer part 11
 - Factional part .81

Decimal number to Binary



• Fractional values, e.g.



- In general, for the decimal representation of
- $X = \{... x_2 x_1 x_{0.} x_{-1} x_{-2} x_{-3} ... \}$ $X = \sum_i x_i 10^i$

Decimal to Binary conversion example



- e.g. 11.81 to 1011.11001 (approx)
 - 11/2 = 5 remainder 1
 - 5/2 = 2 remainder 1
 - 2/2 = 1 remainder 0
 - 1/2 = 0 remainder 1
 - Binary number 1011
 - .81x2 = 1.62 integral part 1
 - .62x2 = 1.24 integral part 1
 - .24x2 = 0.48 integral part 0
 - .48x2 = 0.96 integral part 0
 - .96x2 = 1.92 integral part 1
 - Binary number .11001 (approximate)

Hexadecimal Notation



- Compact representation of bus information
- Use 16 digits, (0,1,3,...9,A,B,C,D,E,F)
- $1A_{16} = (1_{16} \times 16^1) + (A_{16} \times 16^0)$ = $(1_{10} \times 16^1) + (10_{10} \times 16^0) = 26_{10}$
- Convert group of four binary digits to/from one hexadecimal digit,
 - 0000=0; 0001=1; 0010=2; 0011=3; 0100=4; 0101=5; 0110=6; 0111=7; 1000=8; 1001=9; 1010=A; 1011=B; 1100=C; 1101=D; 1110=E; 1111=F;
- e.g.
 - 1101 1110 0001. 1110 1101 = DE1.DE

Integer Representation +/- numbers



- Only have 0 & 1 to represent everything
- Positive numbers stored in binary
 - e.g. 41=00101001
- No minus sign
- No period
- How to represent negative number?
 - Sign-Magnitude
 - Two's compliment

Sign-Magnitude Representation



- Add one extra bit on MSB to represent sign
- Left most bit is sign bit
- 0 means positive
- 1 means negative
- +18 = 00010010
- -18 = **1**0010010
- Problems
 - Need to consider both sign and magnitude in arithmetic
 - Two representations of zero (+0 and -0)

Two's Compliment Representation



- +3 = 00000011
- +2 = 00000010
- +1 = 00000001
- +0 = 00000000
- -1 = 11111111
- -2 = 111111110
- -3 = 11111101

2's Compliment Number System



- One representation of zero
- Arithmetic works easily, use same hardware as positive numbers
- Negating is fairly easy (2's compliment operation)
 - 3 = 00000011
 - Boolean **complement** gives 11111100
 - Add +1 to LSB 11111101

Range of 2's Compliment Numbers



- 8 bit 2's compliment
 - $+127 = 011111111 = 2^7 -1$
 - $-128 = 10000000 = -2^7$
- 16 bit 2's compliment

 - $-32768 = 1000000000000000000000 = -2^{15}$

Different word lengths in 2's Compliment

- Positive number pack with leading zeros
- +18 = 00010010 (in 8 bits)
- +18 = 00000000 00010010 (in 16 bits)
- Negative numbers pack with leading ones
- -18 = 10010010 (in 8 bits)
- -18 = 11111111 10010010 (in 16 bits, notice sign bit replication)
- i.e. pack higher bits with MSB (sign bit)

Negation Special Case 1



- 0 = 00000000
- Bitwise not 11111111
- Add 1 to LSB +1
- Result <u>1</u> 0000000
- Overflow is ignored, so:
- -0 = 0 OK!

Negation Special Case 2



- -128 = 10000000
- bitwise not 01111111
- Add 1 to LSB +1
- Result 10000000
- So:
- -(-128) = -128 **Problem here!**
- Monitor MSB (sign bit)
- It should change during negation
- >> There is no representation of +128 in this case. (no $+2^n$)

Addition and Subtraction

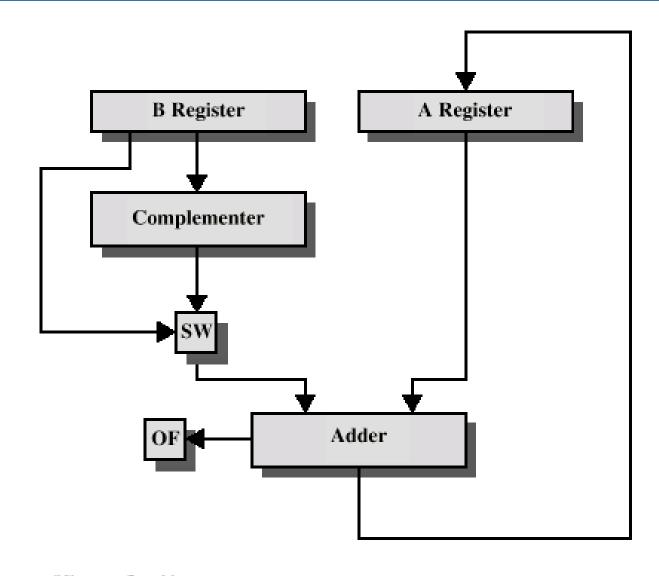


Normal binary addition

- 0011 0101 1100
- +0100 +0100 +1111
- -----
- 0111 $\underline{1}001 = \text{overflow} \ \underline{1}1011$
- Monitor sign bit for overflow (sign bit change as adding two positive numbers or two negative numbers.)
- Subtraction: Take twos compliment of subtrahend then add to minuend
 - i.e. a b = a + (-b)
- So we only need addition and complement circuits

Hardware for Addition and Subtraction



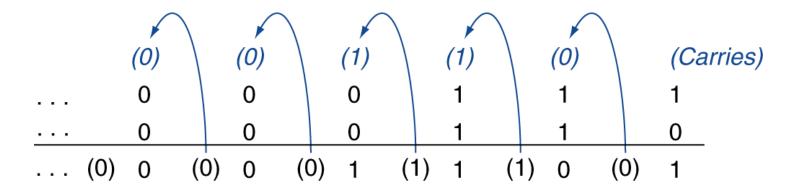


OF = overflow bit SW = Switch (select addition or subtraction)

Integer Addition - Overflow



• Example: 7 + 6



- Overflow if result is out of range
 - Adding +ve and –ve operands, no overflow
 - Adding two +ve operands
 - Overflow if result sign is 1
 - Adding two –ve operands
 - Overflow if result sign is 0

Integer Subtraction - Overflow



- Add negation of second operand
- Example: 7 6 = 7 + (-6)
 - +7: 0000 0000 ... 0000 0111
 -6: 1111 1111 ... 1111 1010
 +1: 0000 0000 ... 0000 0001
- Overflow if result is out of range
 - Subtracting two +ve or two –ve operands, no overflow
 - Subtracting +ve from –ve operand
 - Overflow if result sign is 0
 - Subtracting –ve from +ve operand
 - Overflow if result sign is 1

Overflow in Addition / Subtraction



OVERFLOW RULE: If two numbers are added, and they are both positive or both negative, then overflow occurs if and only if the result has the opposite sign.

1001 = -7 +0101 = 5 1110 = -2 (a) (-7) + (+5)	1100 = -4 +0100 = 4 10000 = 0 (b) (-4) + (+4)
0011 = 3 + 0100 = 4 0111 = 7 (c) (+3) + (+4)	1100 = -4 + 1111 = -1 11011 = -5 (d) (-4) + (-1)
0101 = 5 + 0100 = 4 1001 = Overflow (e) (+5) + (+4)	1001 = -7 + 1010 = -6 10011 = Overflow (f)(-7) + (-6)

Figure 10.3 Addition of Numbers in Twos Complement Representation

Figure 10.4 Subtraction of Numbers in Twos Complement

CPU Dealing with Overflow



- Some languages (e.g., C) ignore overflow
 - Use MIPS addu, addui, subu instructions
- Other languages (e.g., Ada, Fortran) require raising an exception
 - Use MIPS add, addi, sub instructions
 - On overflow, invoke exception handler
 - Save PC in exception program counter (EPC) register
 - Jump to predefined handler address
 - mfc0 (move from coprocessor reg) instruction can retrieve EPC value, to return after corrective action

MIPS Instructions and Overflow



The computer designer must therefore provide a way to ignore overflow in some cases and to recognize it in others. The MIPS solution is to have two kinds of arithmetic instructions to recognize the two choices:

- Add (add), add immediate (addi), and subtract (Sub) cause exceptions on overflow.
- Add unsigned (addu), add immediate unsigned (addiu), and subtract unsigned (Subu) do *not* cause exceptions on overflow.

Because C ignores overflows, the MIPS C compilers will always generate the unsigned versions of the arithmetic instructions addu, addiu, and subu, no matter what the type of the variables. The MIPS Fortran compilers, however, pick the appropriate arithmetic instructions, depending on the type of the operands.

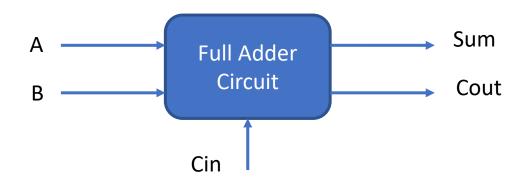


Logic Circuit of Adder / Subtractor

1 Bit Full Adder Circuit



Truth table represents behaviour of inputs and outputs



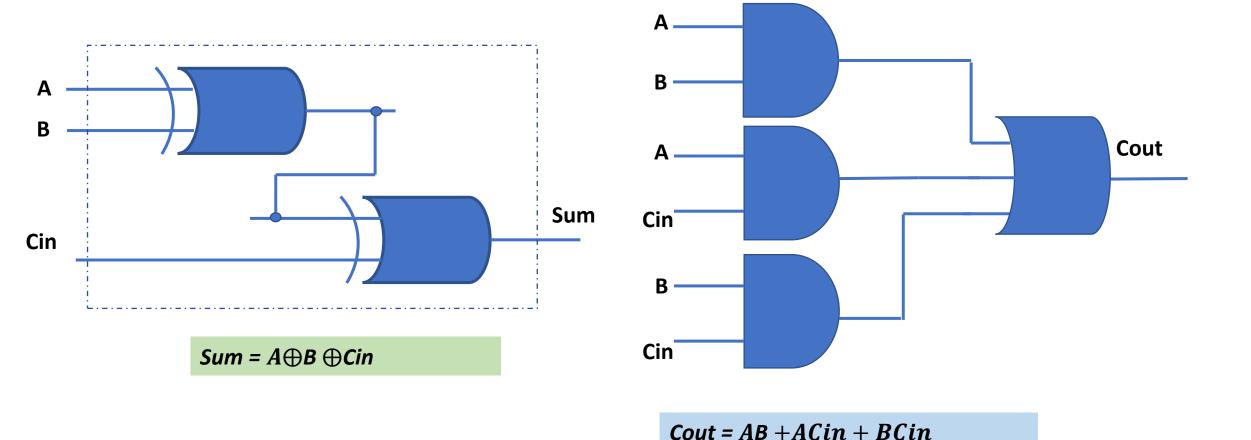
Α	В	Cin	Sum	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean Expression:

$$Ci+1 = Xi.Yi + Ci(Xi \oplus Yi)$$



Full Adder Implementation using Logic Gates

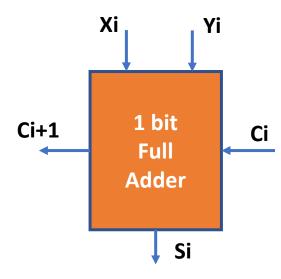




Array of Adders?

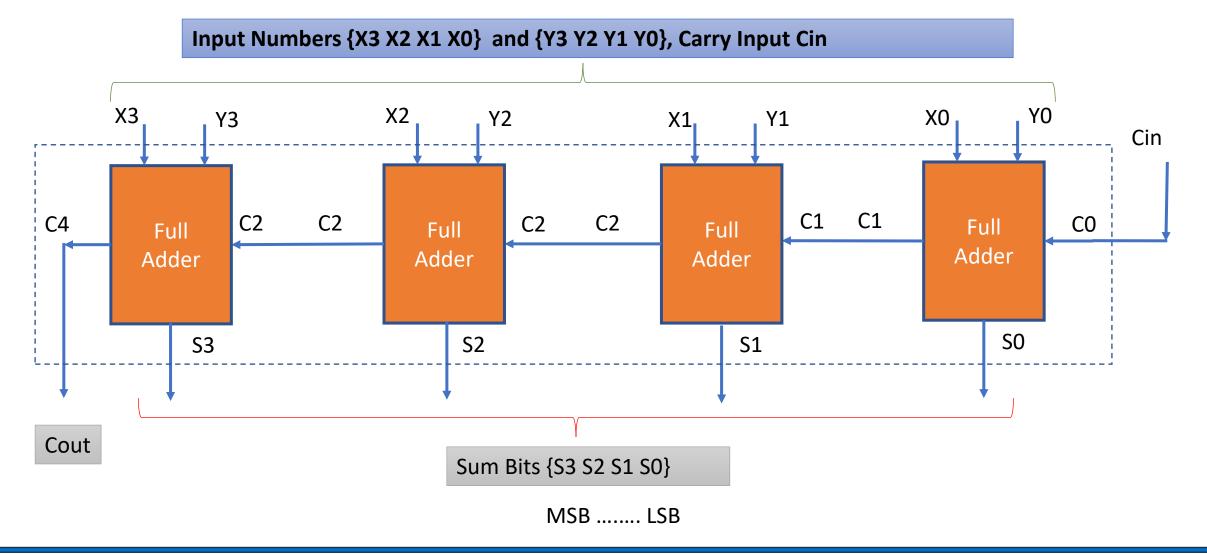
Usually, data types defined in any program are 8 bits, 16 bits or 32 bits

We need array of arithmetic and logic circuits to perform ALU operation on CPU registers





Multiple Bits – Ripple Carry Adder





Readings

- P&H Textbook Chapter 3
- Search Appendix C P&H Textbook online; this contains useful background material on digital logic, ALU and related stuff

Topics

- Computer Performance in light of
 - Power Wall
 - Complexity Wall
 - Moore's Law
 - Dennard Scaling
- Computing ideas in post-PC era
- What is meant by the Hardware / Software Interface
- Calculate Power dissipation
- Notion of Computer Performance