Lecture 20
EE 421 / CS 425
Digital System Design

Fall 2023

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Topics

- Recap – CPLD Architecture and Some Examples

- FPGA Architectures

- Configurable Logic Block

- Configurable I/O Blocks

- Distributed RAM, Block RAM, Dual Port Memory

- Special Features and DSP Slice in FPGA

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Recap from last lecture

- PLA and PAL Devices – Limited Programmability

- CPLD from Xilinx and Altera

- Architecture Differences between CPLD Families

- Important Building Blocks of CPLD

- Limitations of CPLD

- Predictable Timing Performance of CPLD

- How can logic complexity of CPLD macrocell be enhanced?
    - Expanders, etc.

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Description of Basic (Registered) Macrocell

- Each section of an SPLD is called a macrocell that contains SOP combinational logic and an optional Flipflop

- A typical SPLD has from 8 to 10 macrocells within one chip

- All Flipflops are connected to common CLK input

- All three-state buffers at Flipflop output are controlled by a common OE input

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Basic Macrocell Logic

PAL that includes a DFF is called a Registered PAL
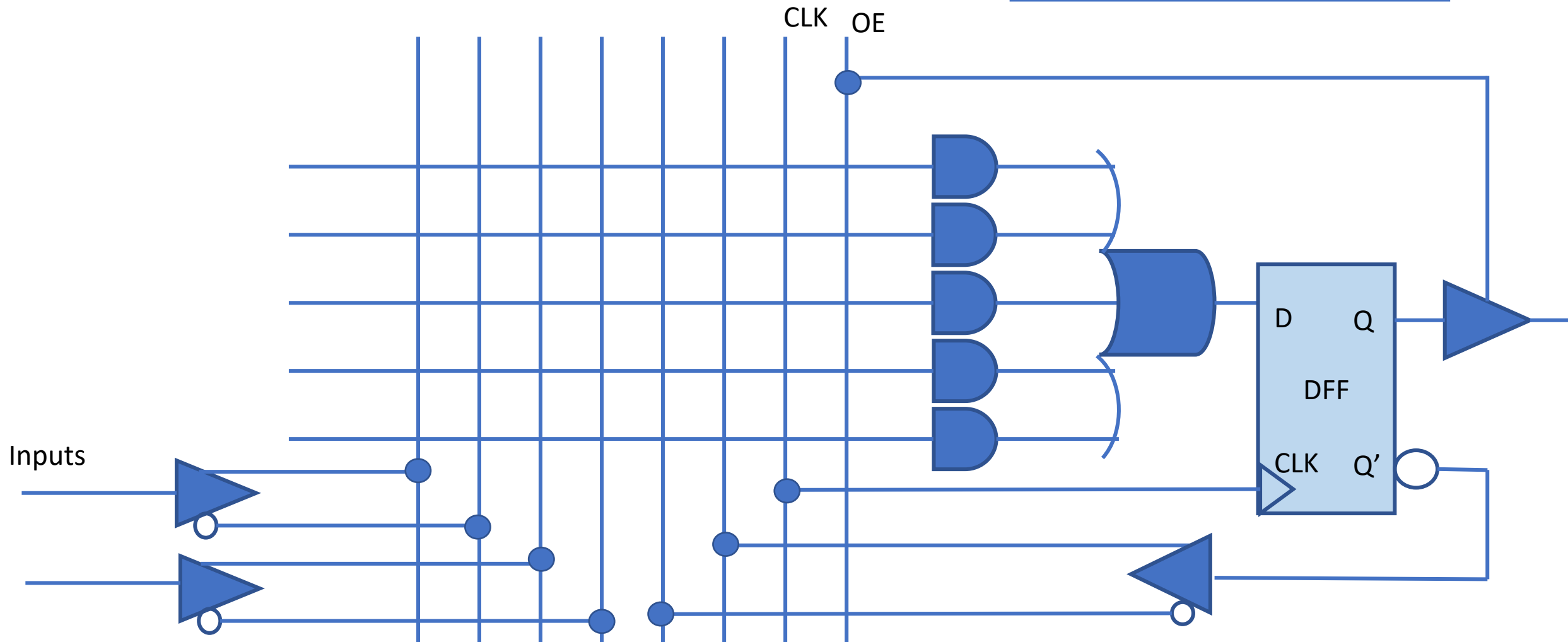
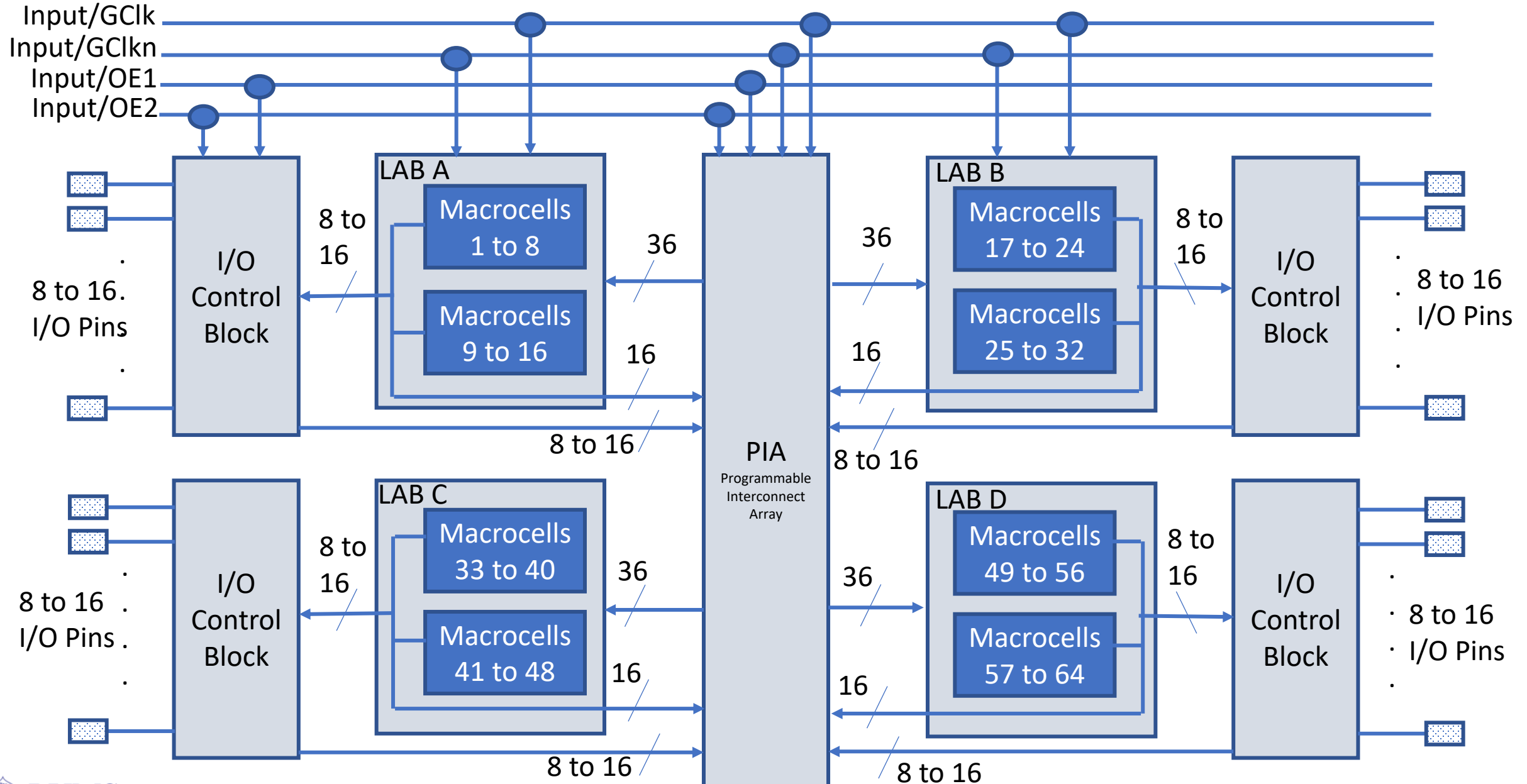# Generic CPLD Configuration
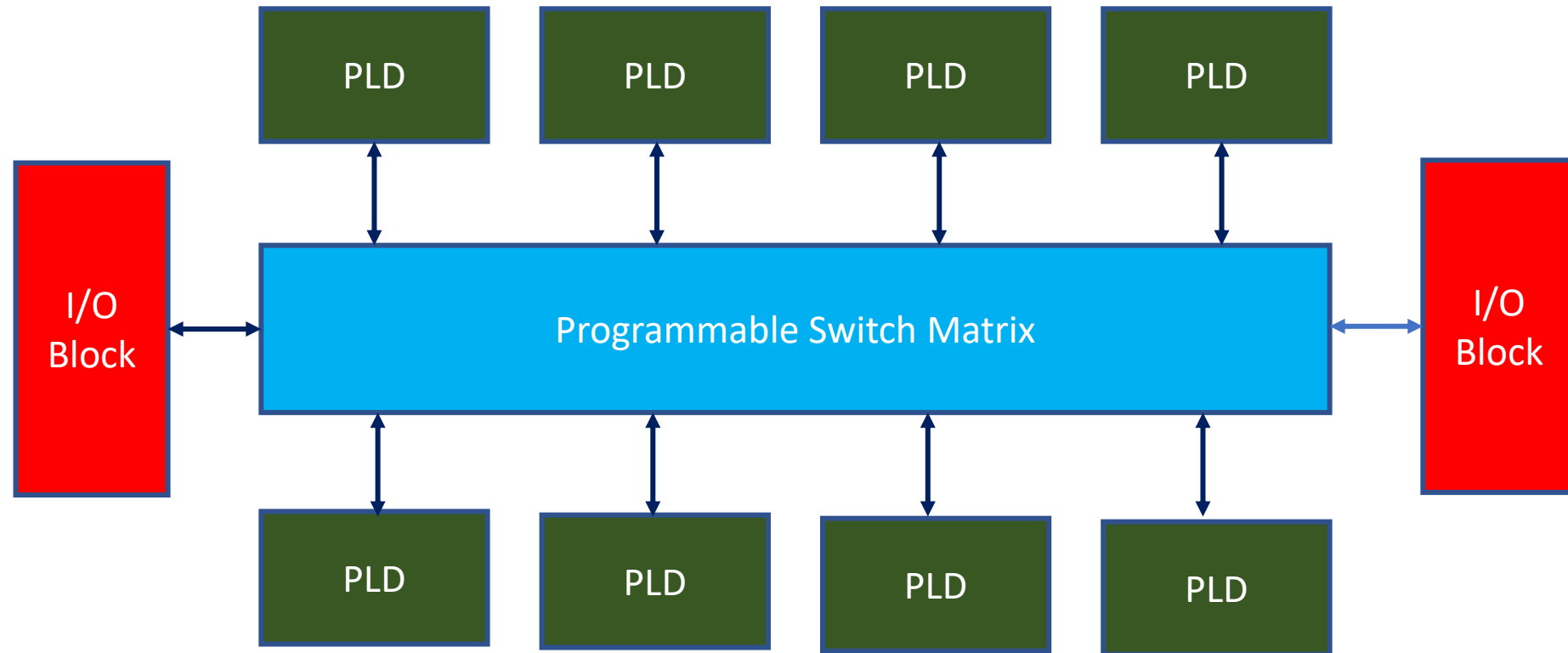
Description of CPLD

- Structured Array of PLD blocks
- Programmable On-Chip Interconnection Fabric
- Have higher number of inputs without much increase in area
- 100% connectivity between macrocells, BUT not all outputs of macrocells are connected to OUTPUT
- Wide Fan-In AND gates are used at INPUTS
- Outputs of macrocells can be routed within the chip to form more complex logic blocks
- The Interconnect Array selects signals from I/O blocks or macrocell outputs and connects them back to function block inputs
- The I/O blocks provide an interface between bidirectional physical I/O pins and the interior of the CPLD

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Details of Generic CPLD Configuration

- Collection of individual PLD gate arrays on a single integrated circuit

- Each I/O pin is driven by a 3-state buffer and can be programmed to act as Input or Output pin

- Each PLD typically contains 8 to 16 macrocells

- If a macrocell has unused product terms, they can be used by nearby macrocells

- The outputs of macrocells can be routed to inputs of other macrocells to form complex multi-level logic functions

- Different manufactures offer variations in PLD design, programmable switching matrix and different types of I/O blocks

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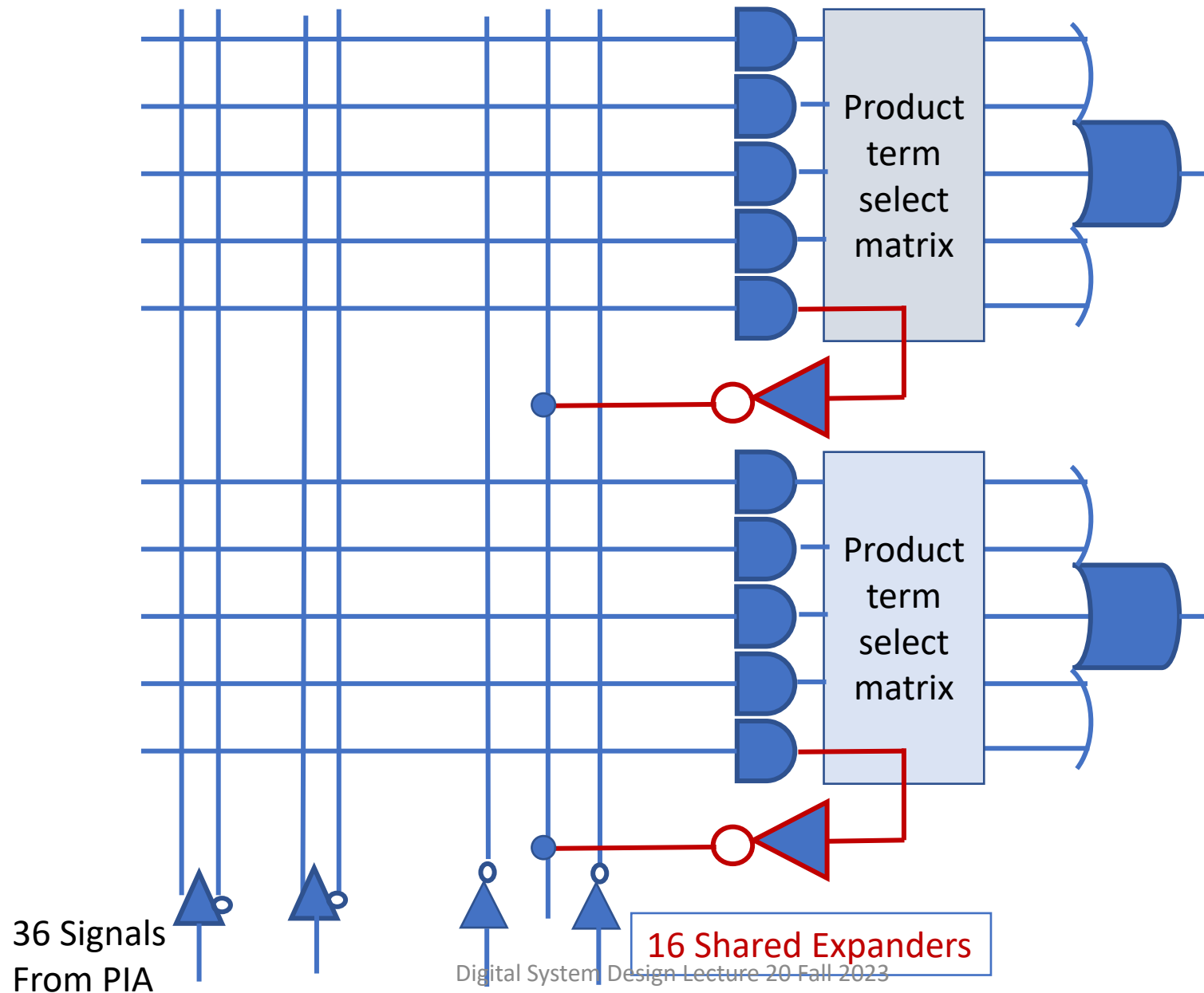# Altera 7000 Series CPLD Architecture

Input/GClk

Input/GClkn

Input/OE1

Input/OE2

I/O Control Block

8 to 16. I/O Pins

LAB A

Macrocells 1 to 8

Macrocells 9 to 16

8 to 16

36

16

8 to 16

PIA
Programmable Interconnect Array

36

LAB B

Macrocells 17 to 24

Macrocells 25 to 32

16

8 to 16

8 to 16

I/O Control Block

8 to 16 I/O Pins

LAB C

Macrocells 33 to 40

Macrocells 41 to 48

8 to 16

36

16

8 to 16

I/O Control Block

8 to 16 I/O Pins

36

LAB D

Macrocells 49 to 56

Macrocells 57 to 64

8 to 16

16

8 to 16

I/O Control Block

8 to 16 I/O Pins

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Details of Altera 7000 CPLD

- Floating gate EEPROM Configuration memory cells
- Architecture consists of an array of logic array blocks (**LAB**), programmable interconnect array (**PIA**) and an array of programmable I/O blocks
- Each LAB has 36 inputs and 16 outputs
- Each LAB consists of 16 macrocells providing both combinational and sequential logic
- PIA provides full connectivity between LAB and I/O Cells
- I/O Control block connects I/O Pins and PIA and LAB
- Global input clk (GCLK) and Global Clear (GCLR) connect to all macrocells
- Each macrocell can provide five product terms to its product-term-select matrix

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PIA and I/O

- The PIA provides full connectivity with predictable timing between LAB, dedicated inputs and I/O Pins

- The I/O Control block establishes connectivity between I/O Pins and PIA and LABs

- From 8 to 16 LAB outputs can be programmed to route through I/O Pins; and from 8 to 16 I/O Pins can be programmed to route through the I/O Control block to the PIA

- Altera architecture uses a PIA to connect LABs and I/O Pins. All signals are available throughout the device. The timing is thus predictable. The alternative is 'Channel-Routed Architecture' that is more denser but the timing is un-predictable as delays are routing-dependent

Shareable Expander in Altera 7000 CPLD

36 Signals From PIA

16 Shared Expanders

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Parallel Expander in Altera 7000 CPLD

From Previous Macrocell

Product term select matrix

Parallel Expander

Product term select matrix

To Next Macrocell

36 Signals From PIA

16 Shared Expanders

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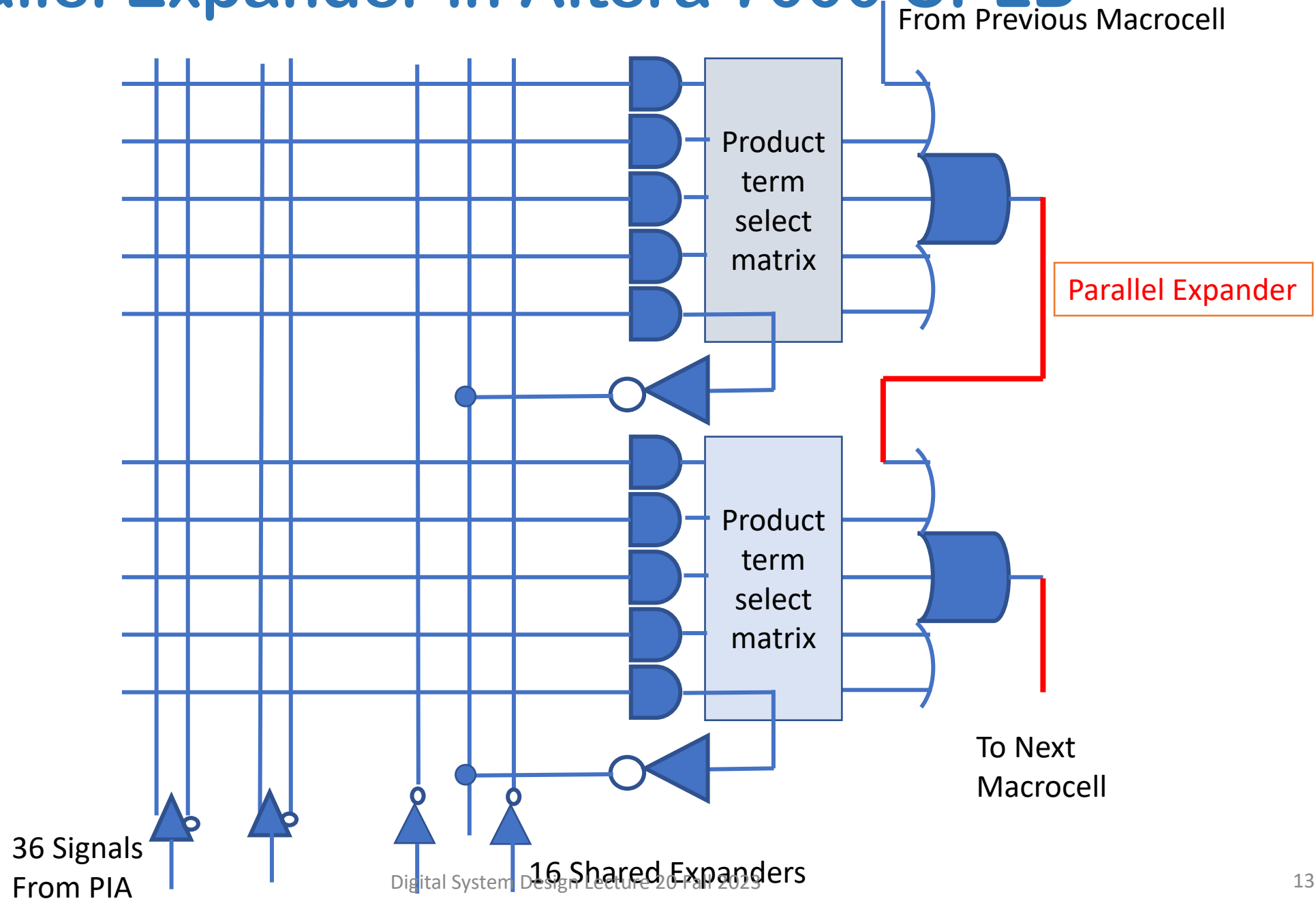
Altera 7000 Series Macrocell Architecture

Parallel Logic Expanders

Global Clear

Global Clk

Product term select matrix

Reg Byps

DFF

CLK

CLR

Clk Sel

CLR Sel

M

36 Signals From PIA

Shared Logic Expanders

To PIA

16 Expander Product Terms

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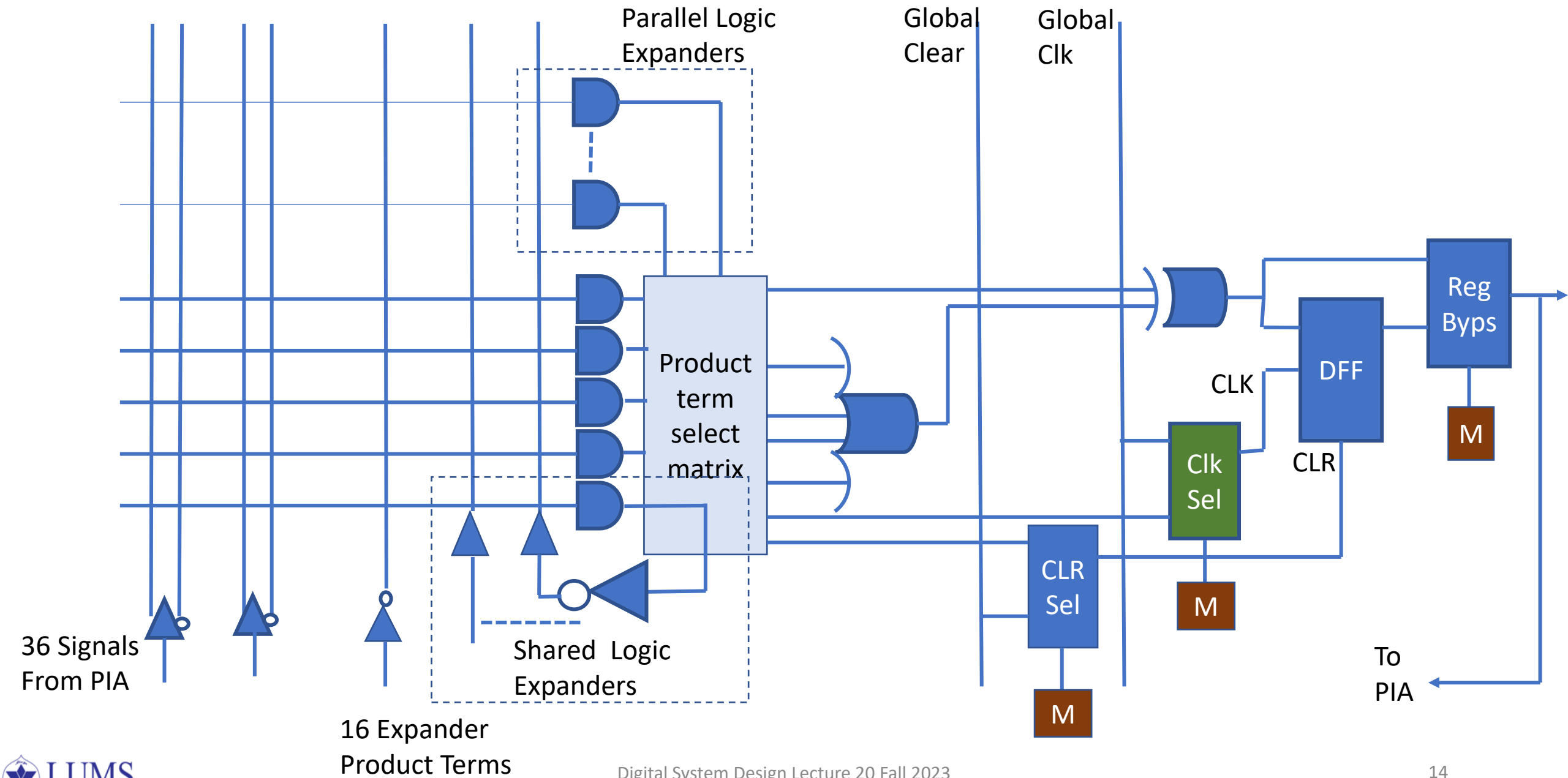
Altera 7000 Series I/O Control Block

OE Control

+VCC

OE1n

OE2n

From Macrocell

To PIA

To I/O Pin
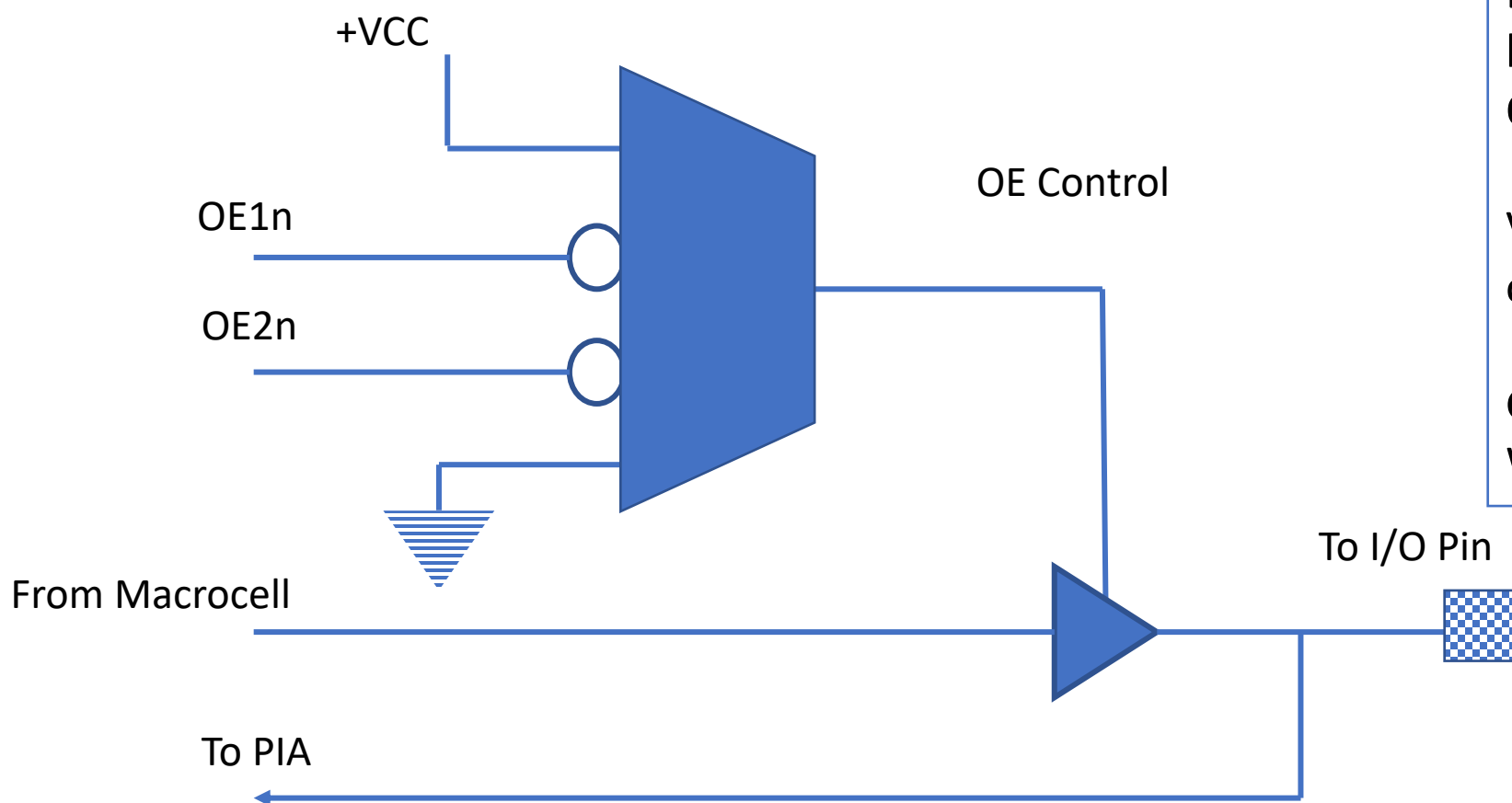
Each I/O Pin can be configured to be dedicated input pin, output pin Or bi-dir under control of OE1, OE2.

VCC will hardwire the I/O pin to output of macrocell.

GND will isolate macrocell and I/O pin Will be an input pin only.

Xilinx XC9500 CPLD Architecture
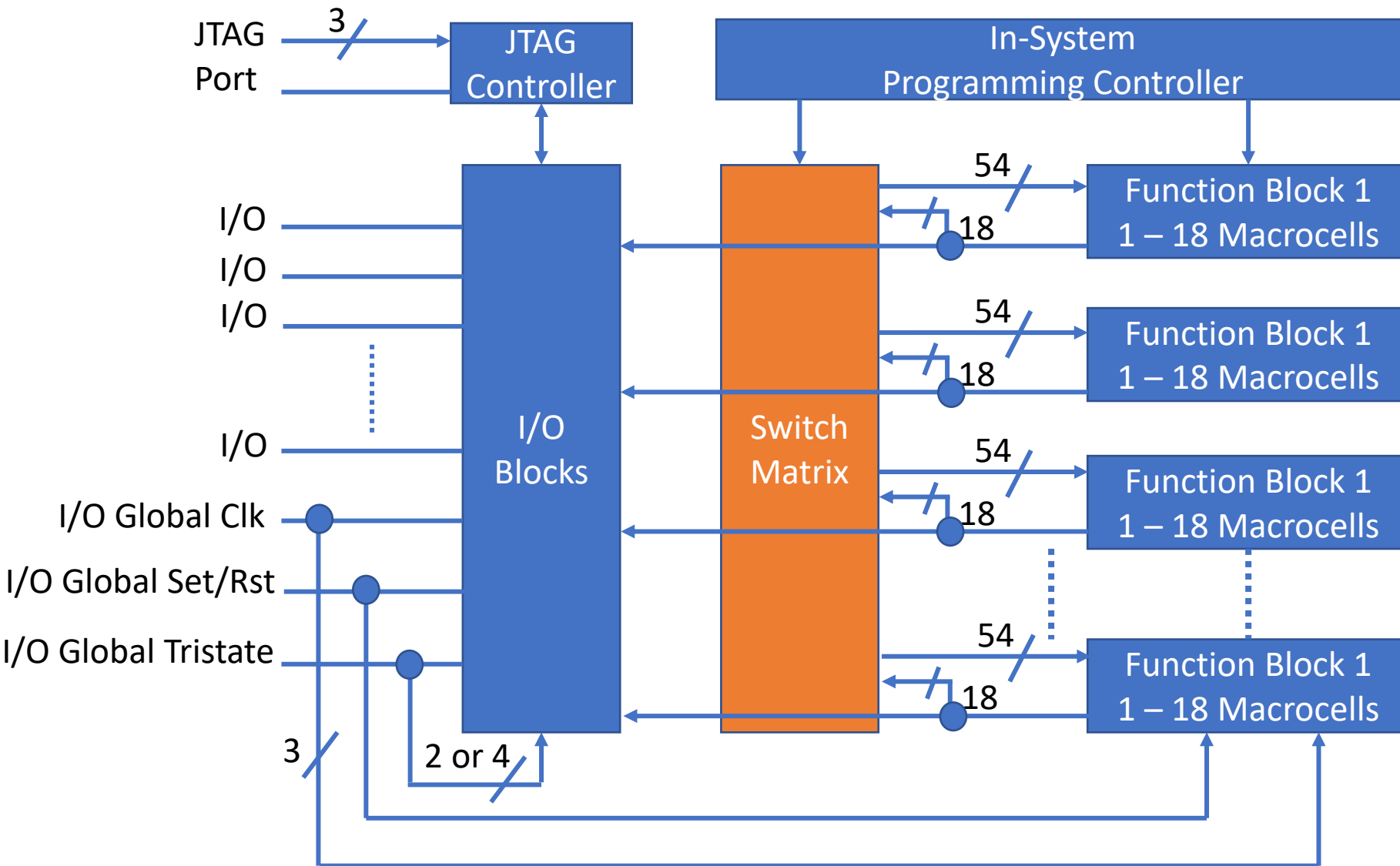
Details of Xilinx 9500 CPLD

- Flash based EEPROM Technology

- Comprises Few (4) Functional Blocks

- Each functional block contains 18 independent macrocells

- Each functional block has 54 inputs and 18 outputs

- Product-term-allocator allocates upto 90 product terms in each macrocell in a functional block to form SOP expressions

- Each macrocell can receive five direct product terms from the AND array and up to 10 more product terms can be made available from other un-committed product terms in other macrocells from same functional block

- Partial SOP terms can be combined from several macrocells

- Each macrocell can be independently configured for combinational or sequential functionality

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Xilinx XC9500 Macrocell Architecture
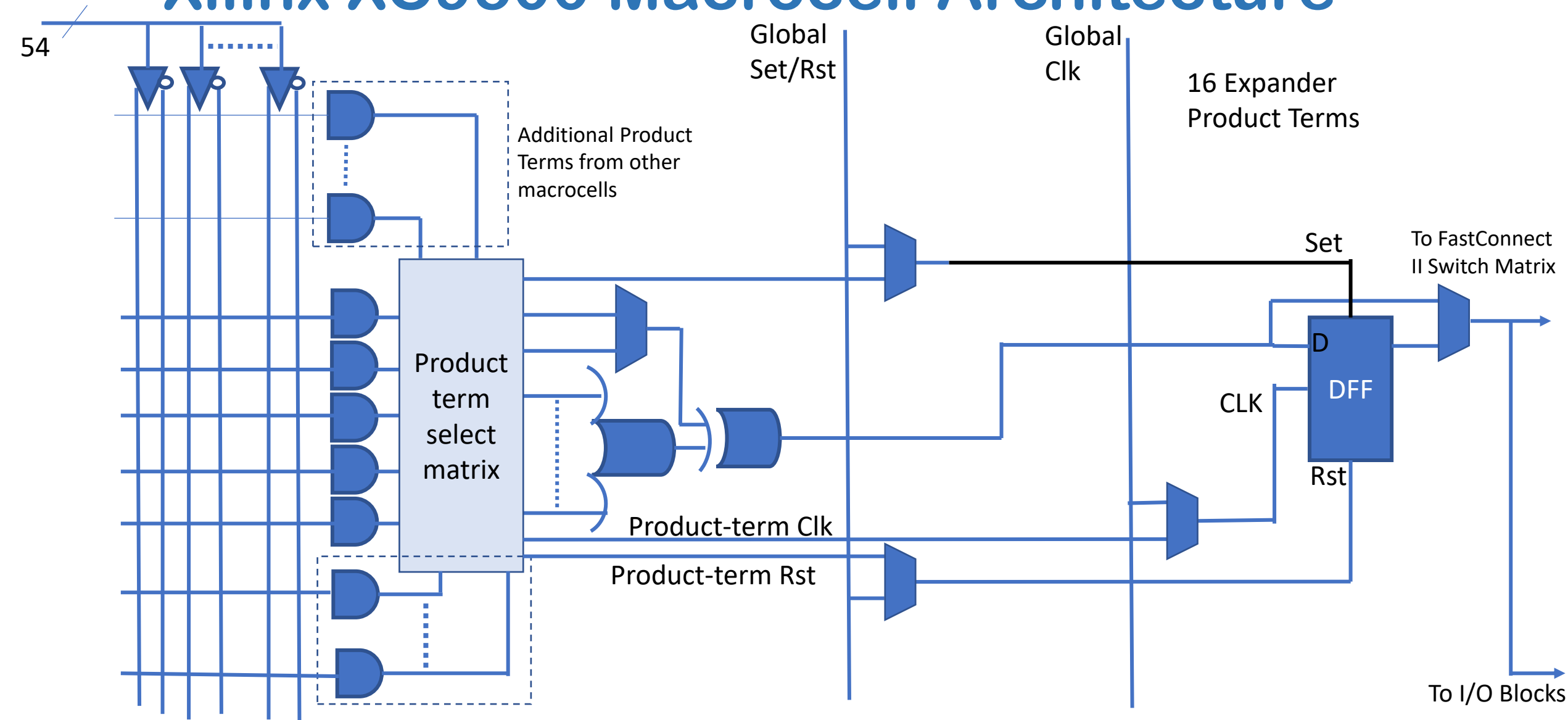
Field Programmable Gate Arrays
FPGA

Field Programmable Gate Arrays Generic Architecture
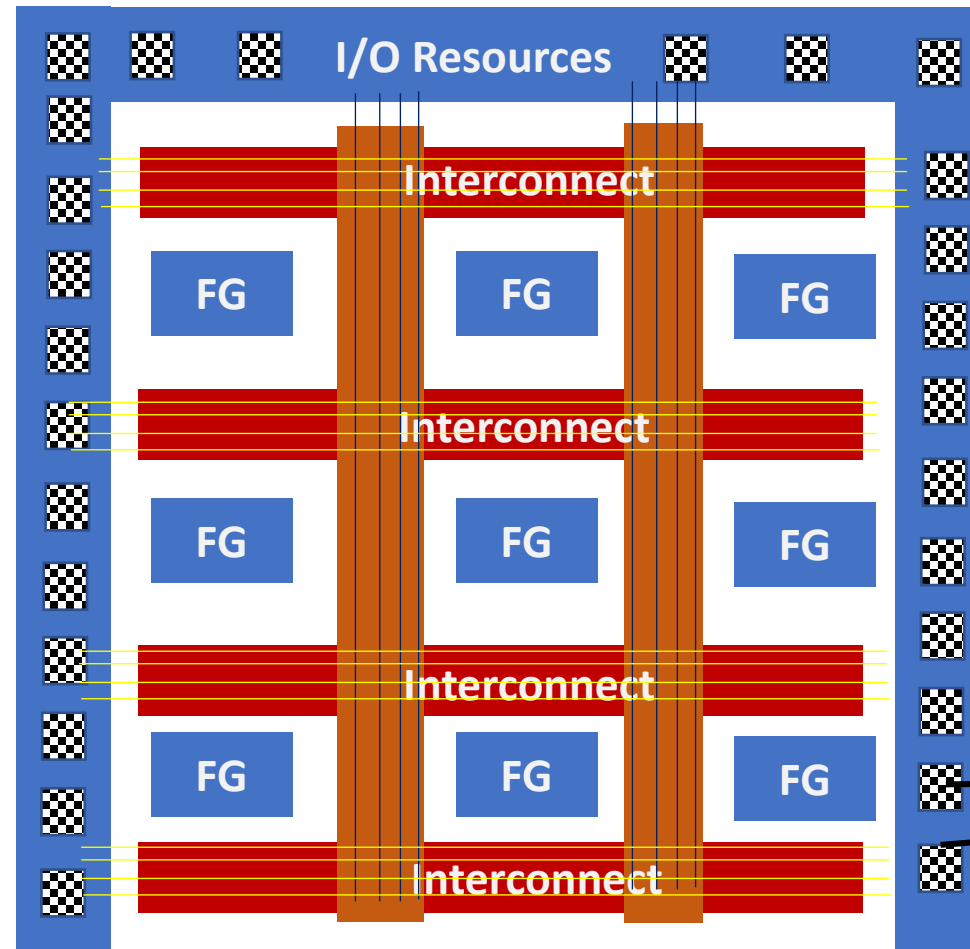
FG = function generator for Logic implementation

I/O Blocks

USB or JTAG Cable

SRAM Configuration Memory
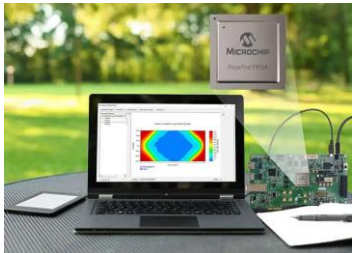
Lookup Table (LUT) based Configurable Logic Blocks
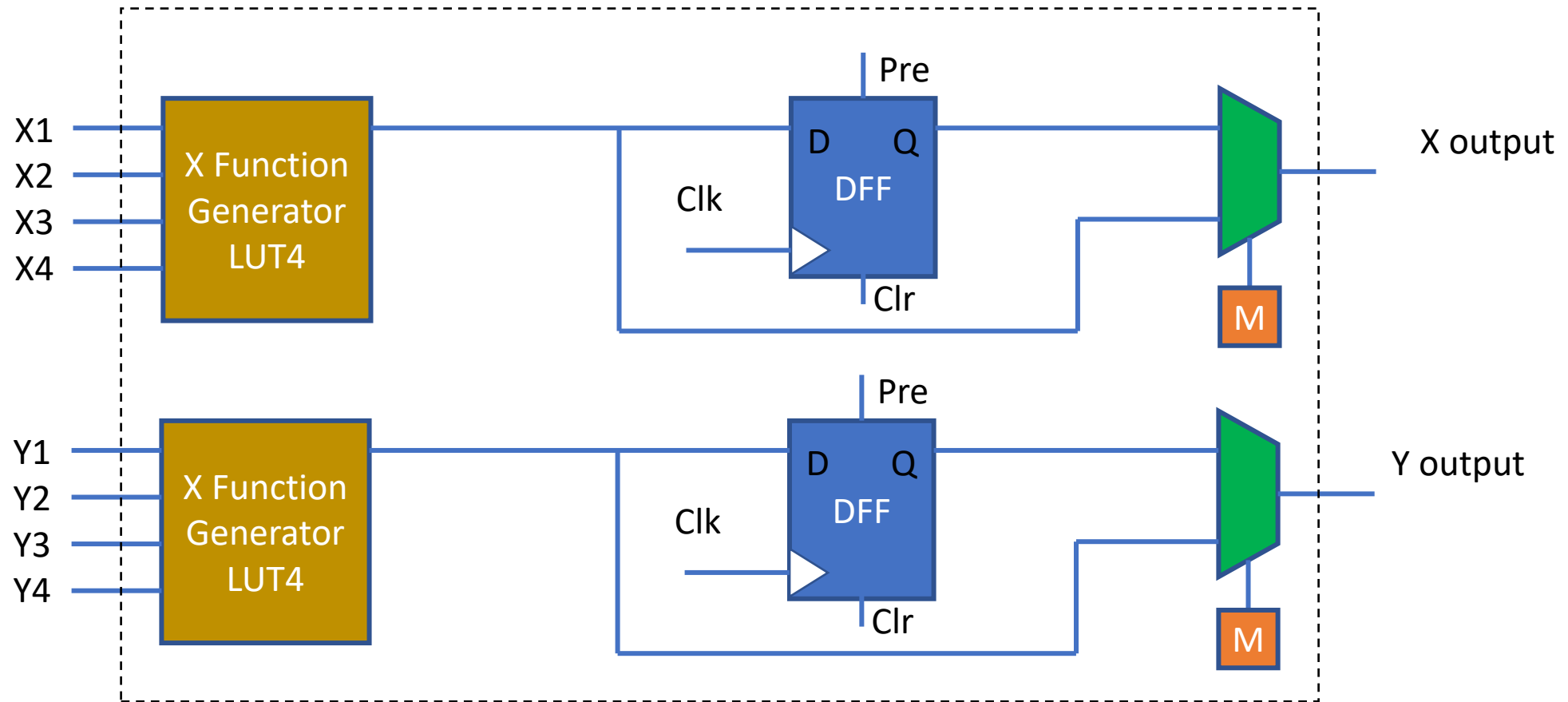
Details of LUT based CLB

- Uses a four-variable look-up table and a flipflop as the basic configurable hardware element. Several of these are combined in different families and types

- Any two functions X and Y of four variables each can be generated in the LUT

- Flipflops at the output can be used. DFF have external preset and clear as well as clock selection mechanism

- Output multiplexer selects from un-registered or registered output

Configurable Logic Blocks based on Multiplexers

Where is Distributed Memory?
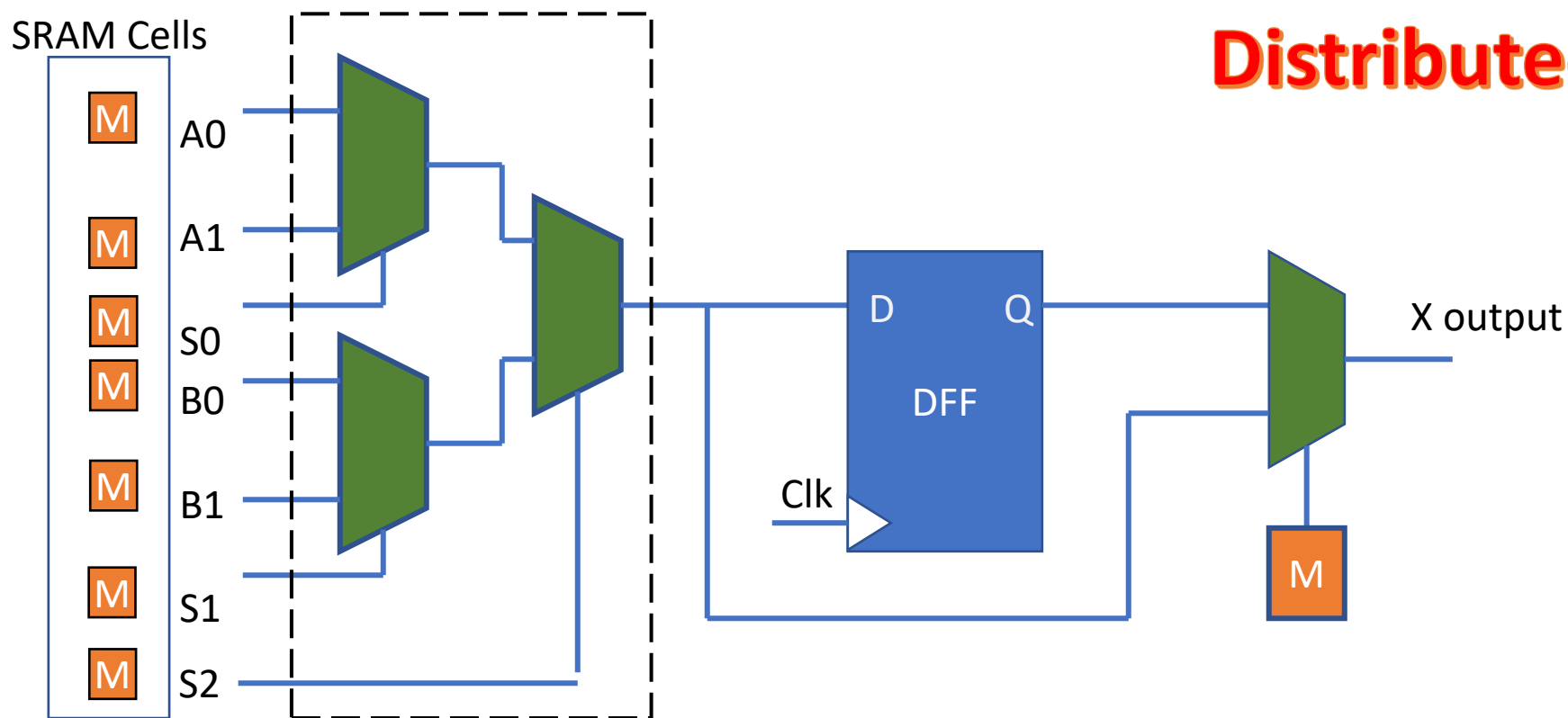
4:1 MUX to generate required SOP Expression

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Xilinx 4000 CLB
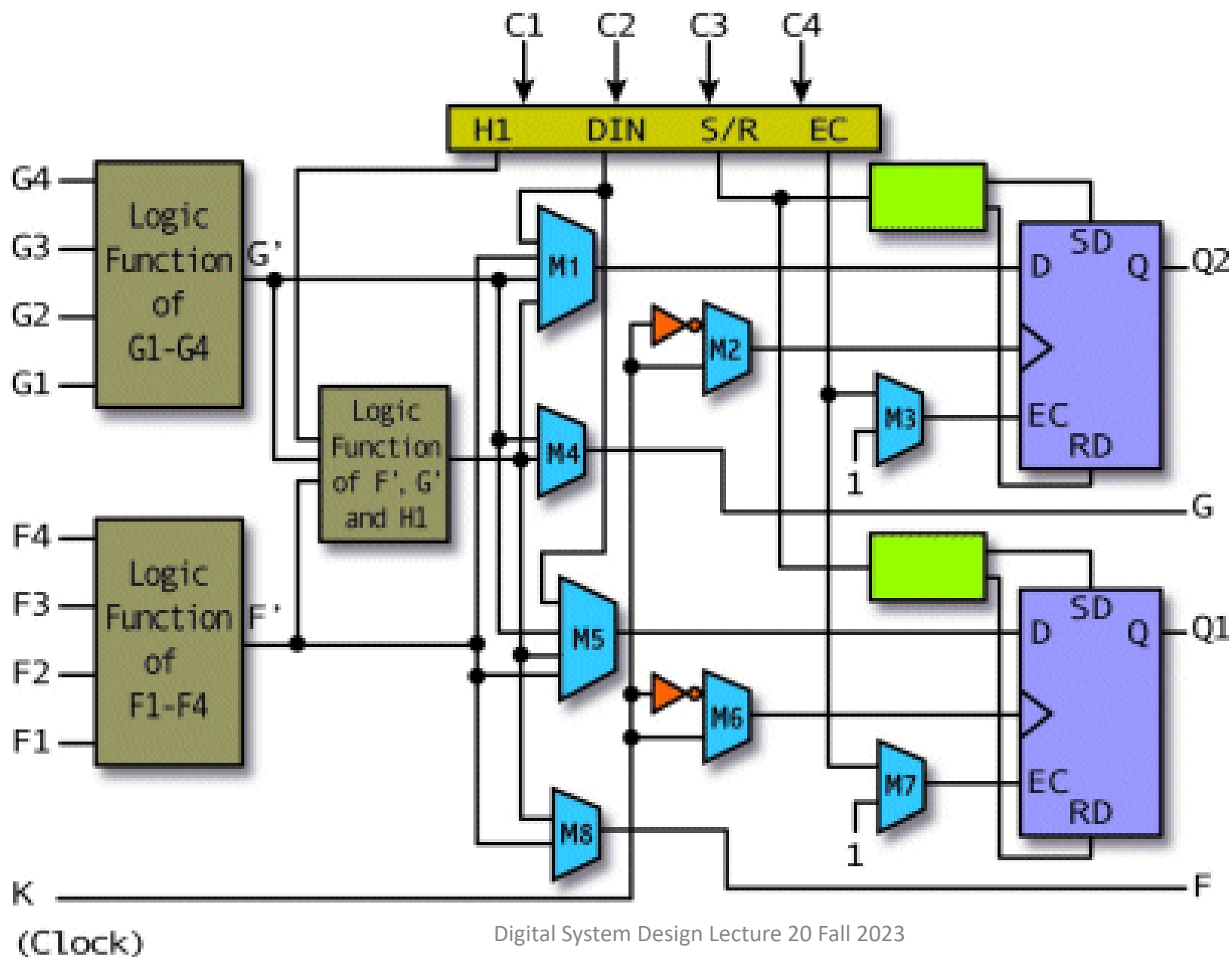
LUT Configuration and Extension

2 Four-input function generators (Look Up Tables)
1 Three-input function
2 Registers:
- Pos. or Neg. edge-trig. Synchronous and asynchr. Set/Reset Possible functions:
- any fct of 5 var.
**- two fcts of 4 var. + one fct of 3 var.**
- some fct of 9 var.
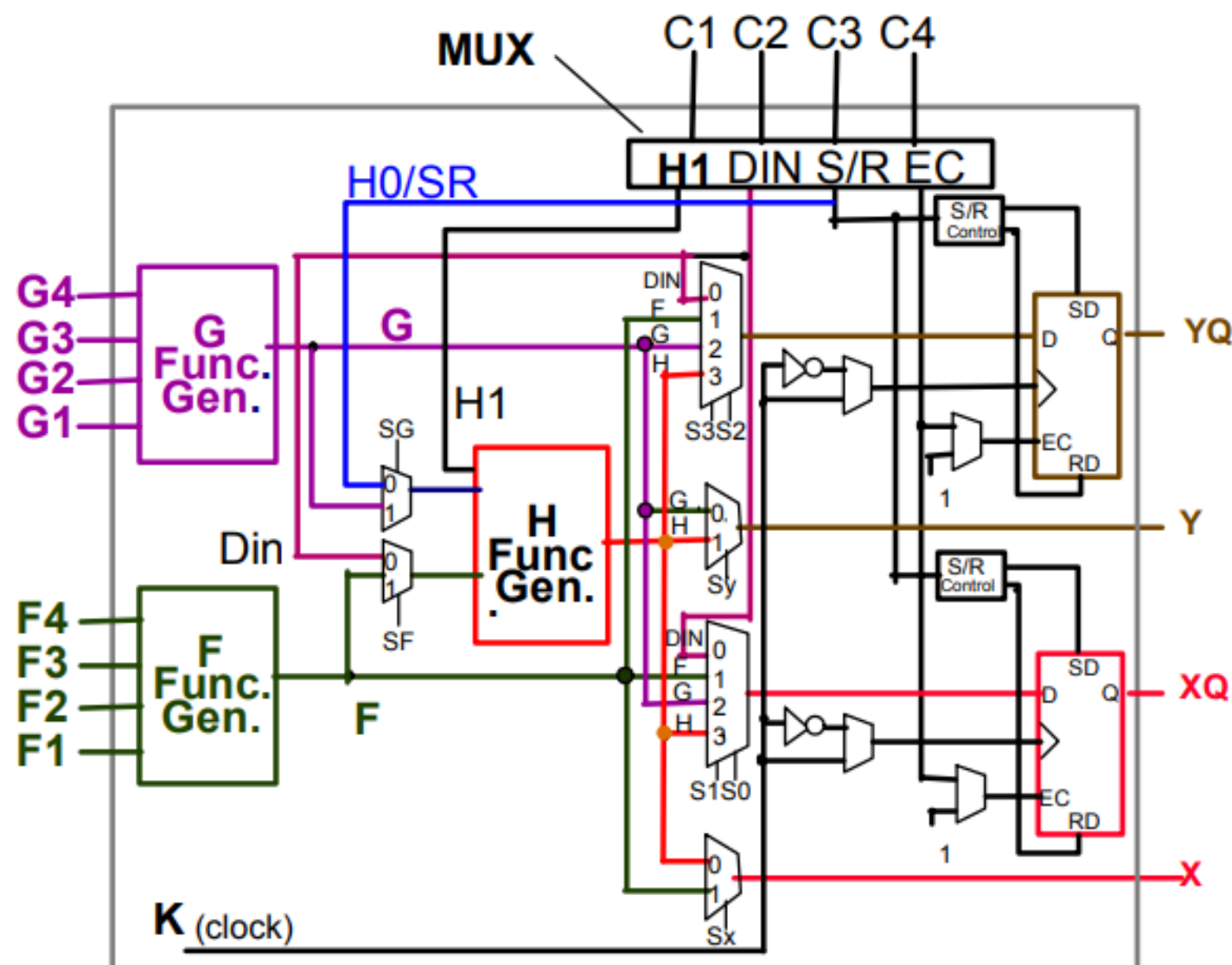
Interconnects

- FPGA in Symmetric Array Configuration (Eg Xilinx)
  - General Purpose Interconnect
  - Direct Interconnects
  - Global Lines
- FPGAs in hierarchical interconnect routing architecture (Eg Altera)
- FPGA in Row Based Configuration (Eg Actel)
- FPGAs in Sea of Gates Fine-Grained Configuration (Eg IBM)

Symmetric (Matrix) Based FPGA Configuration
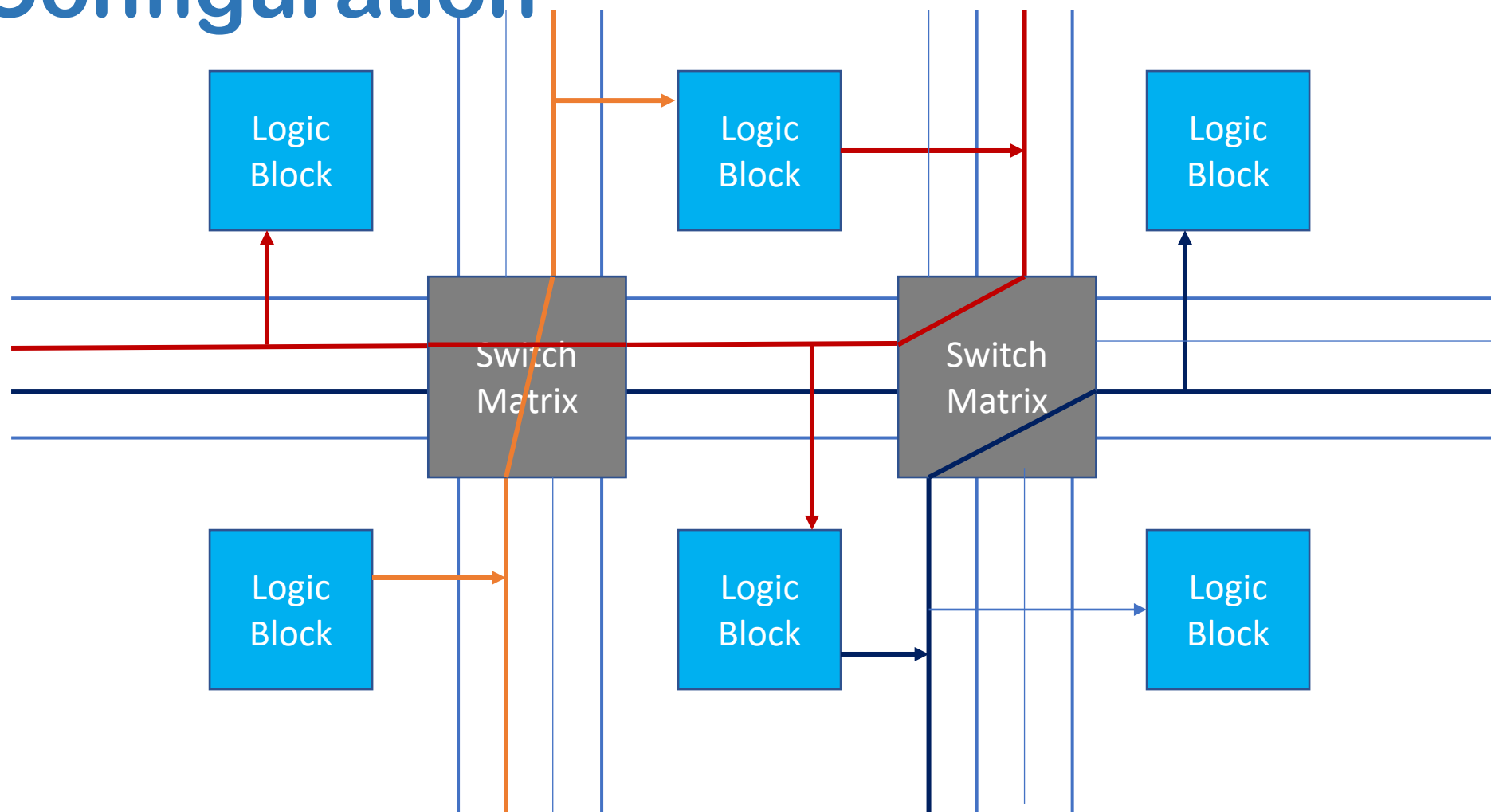
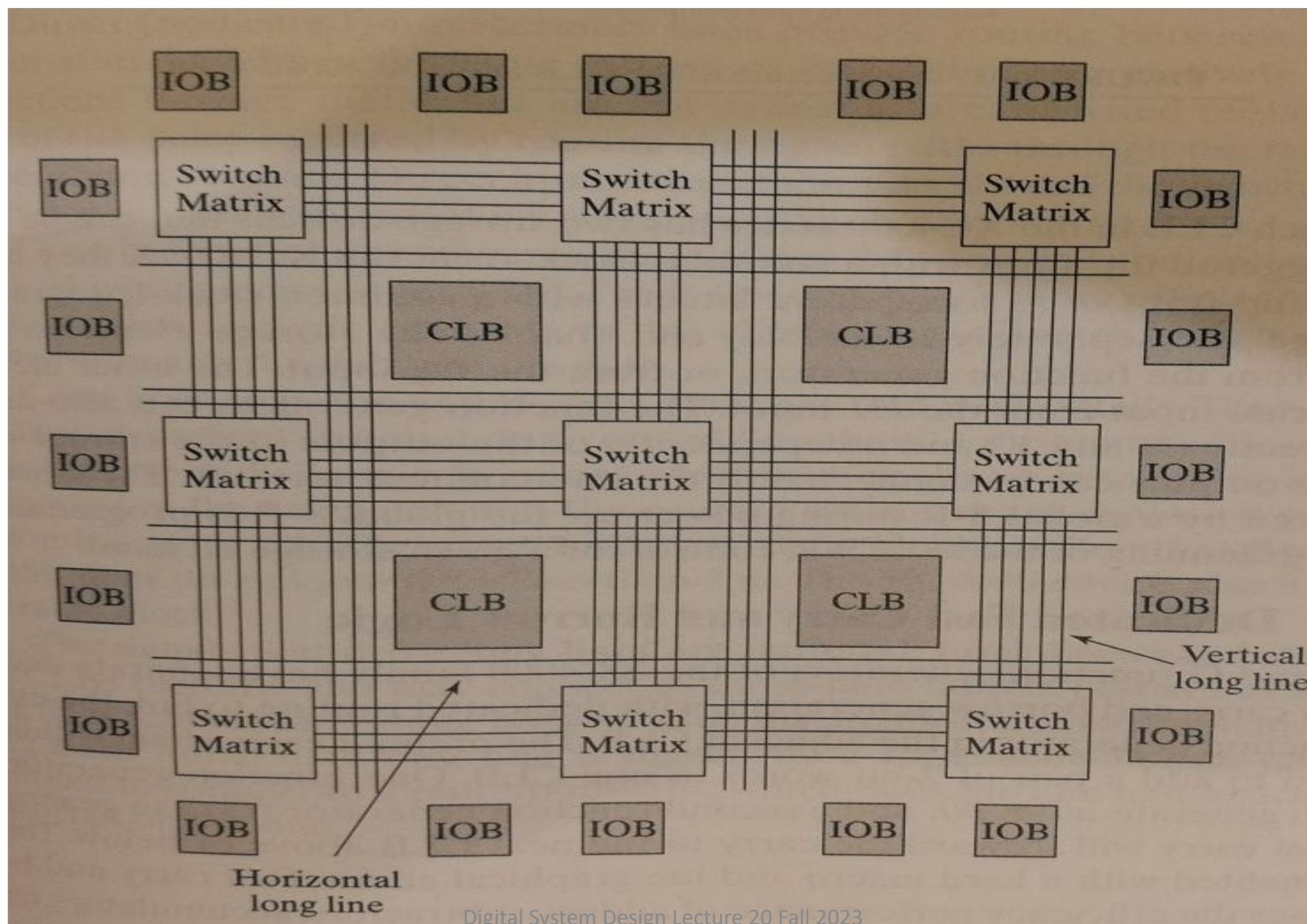# Routing Matrix for General Purpose Interconnection in FPGA
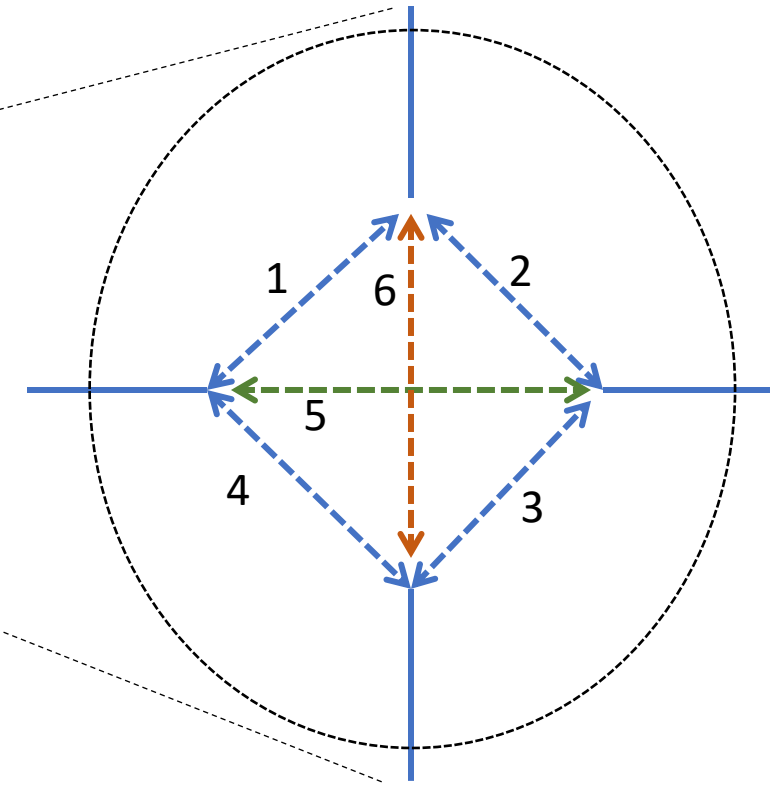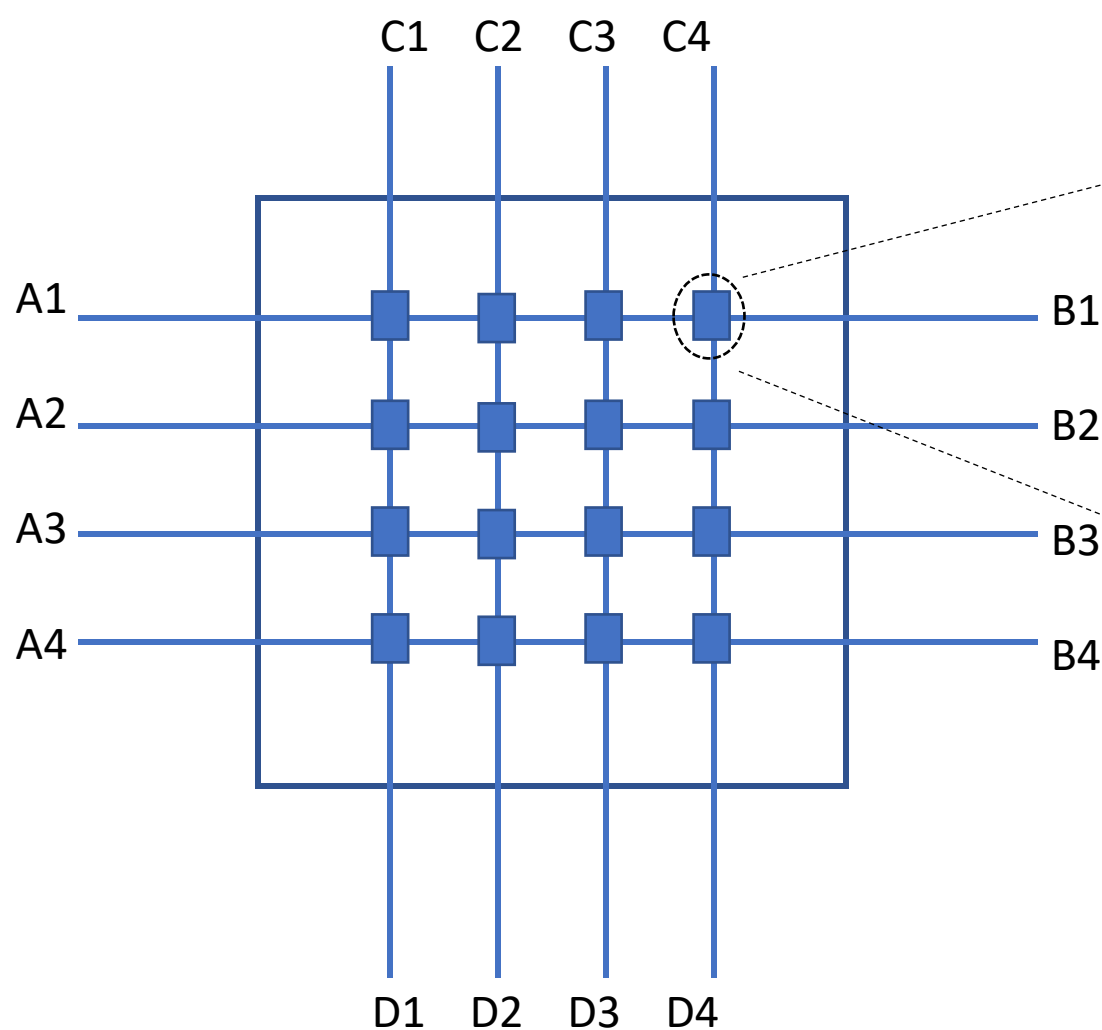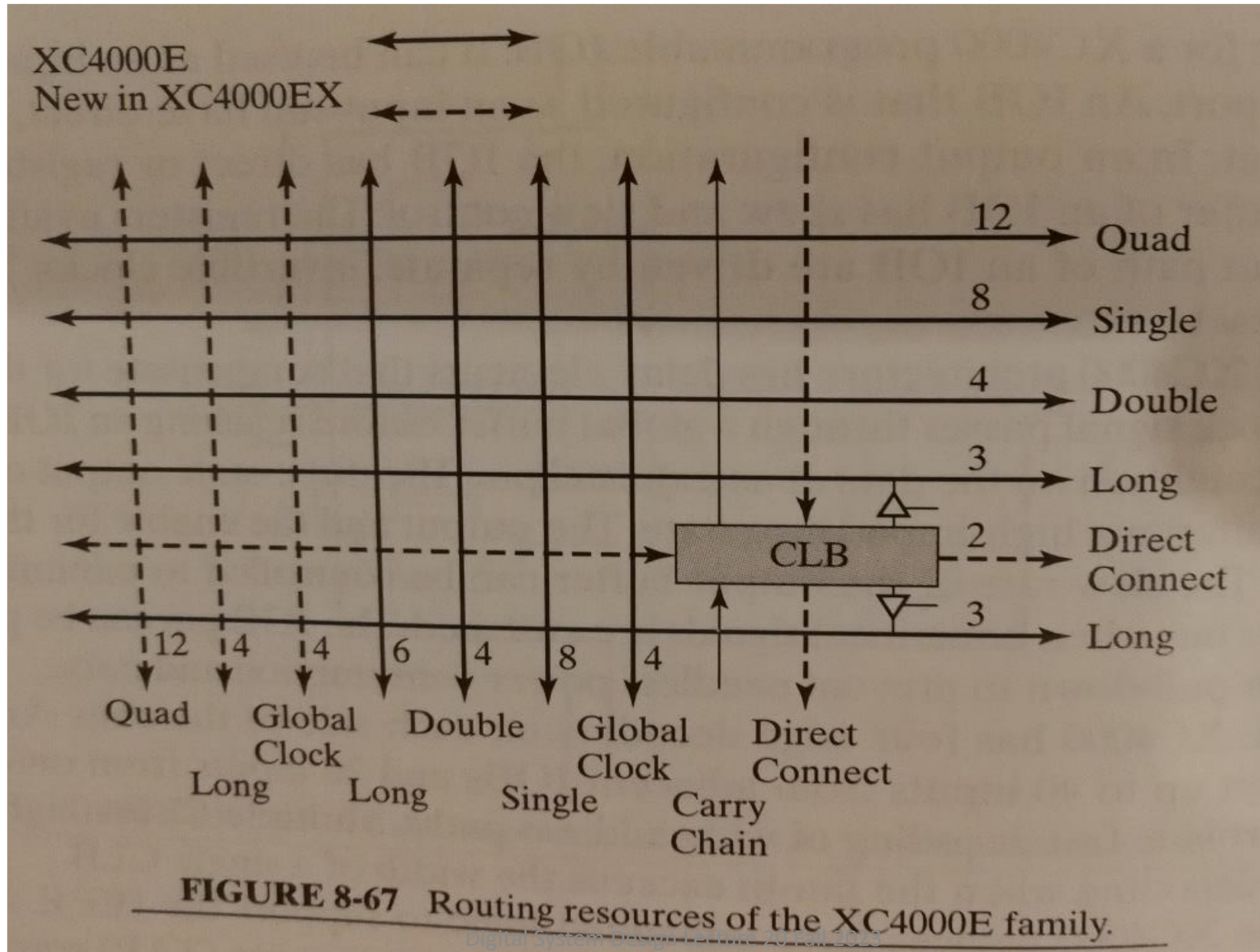

Six-way connectivity

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Direct Interconnection to Neighboring Blocks
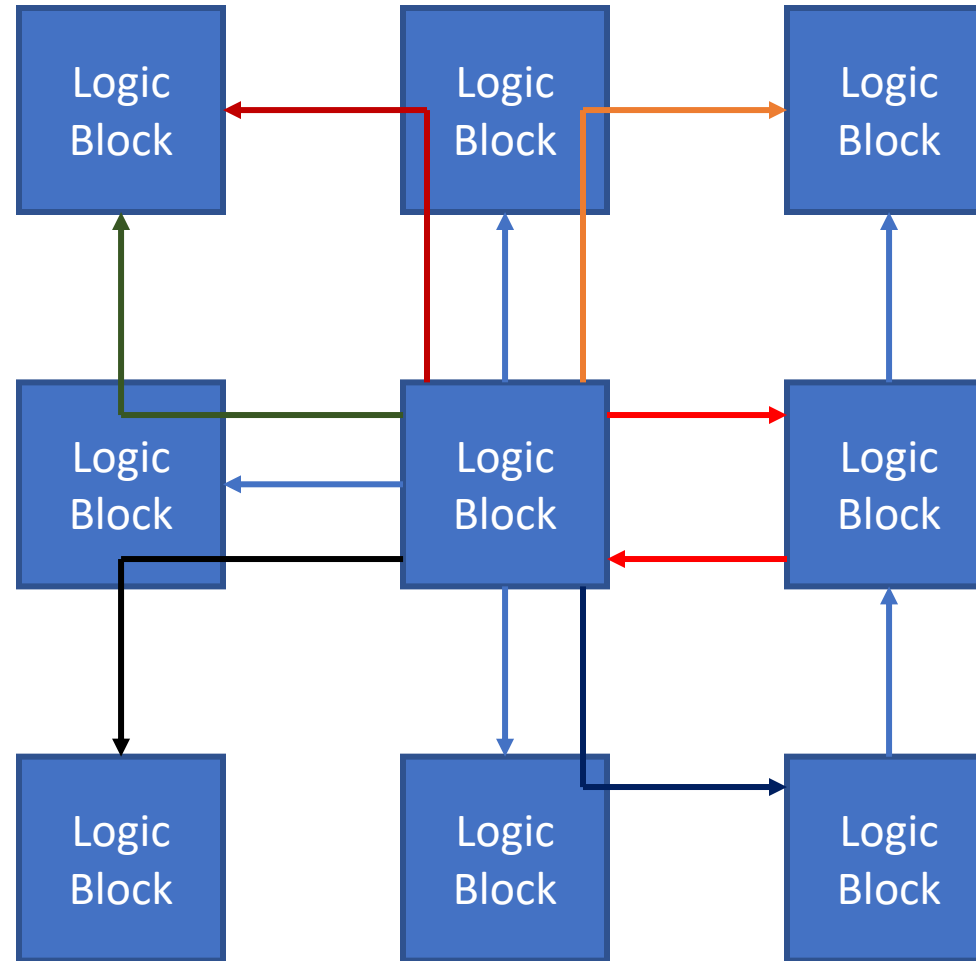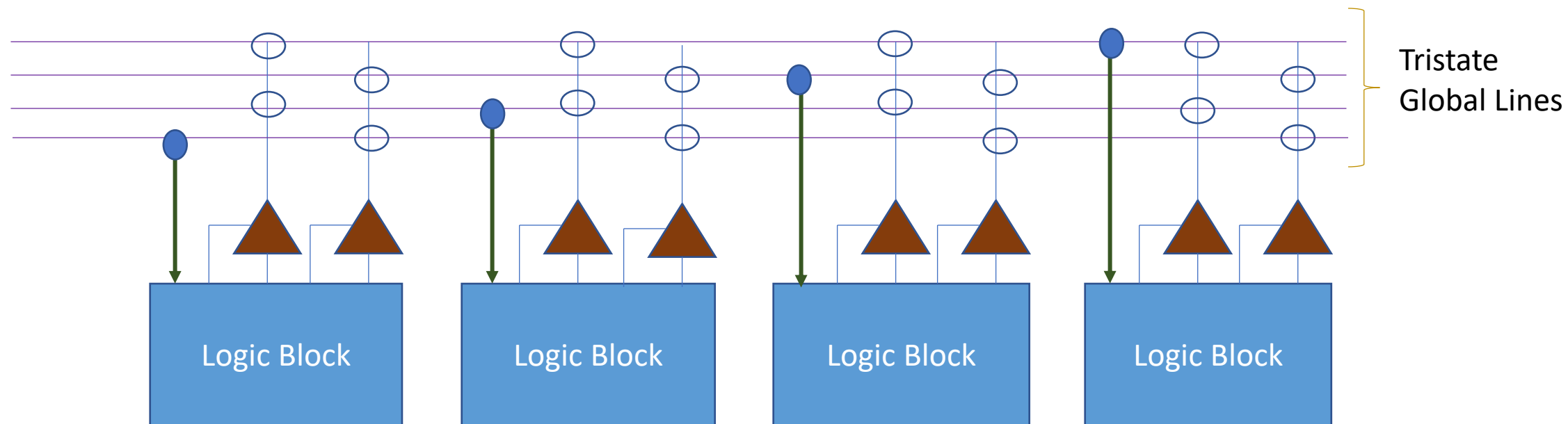
Xilinx 4000 FPGA Top Level Architecture

Xilinx 4000 Routing Resources with CLB

FIGURE 8-67 Routing resources of the XC4000E family.

Global Interconnection Lines

Tristate Global Lines
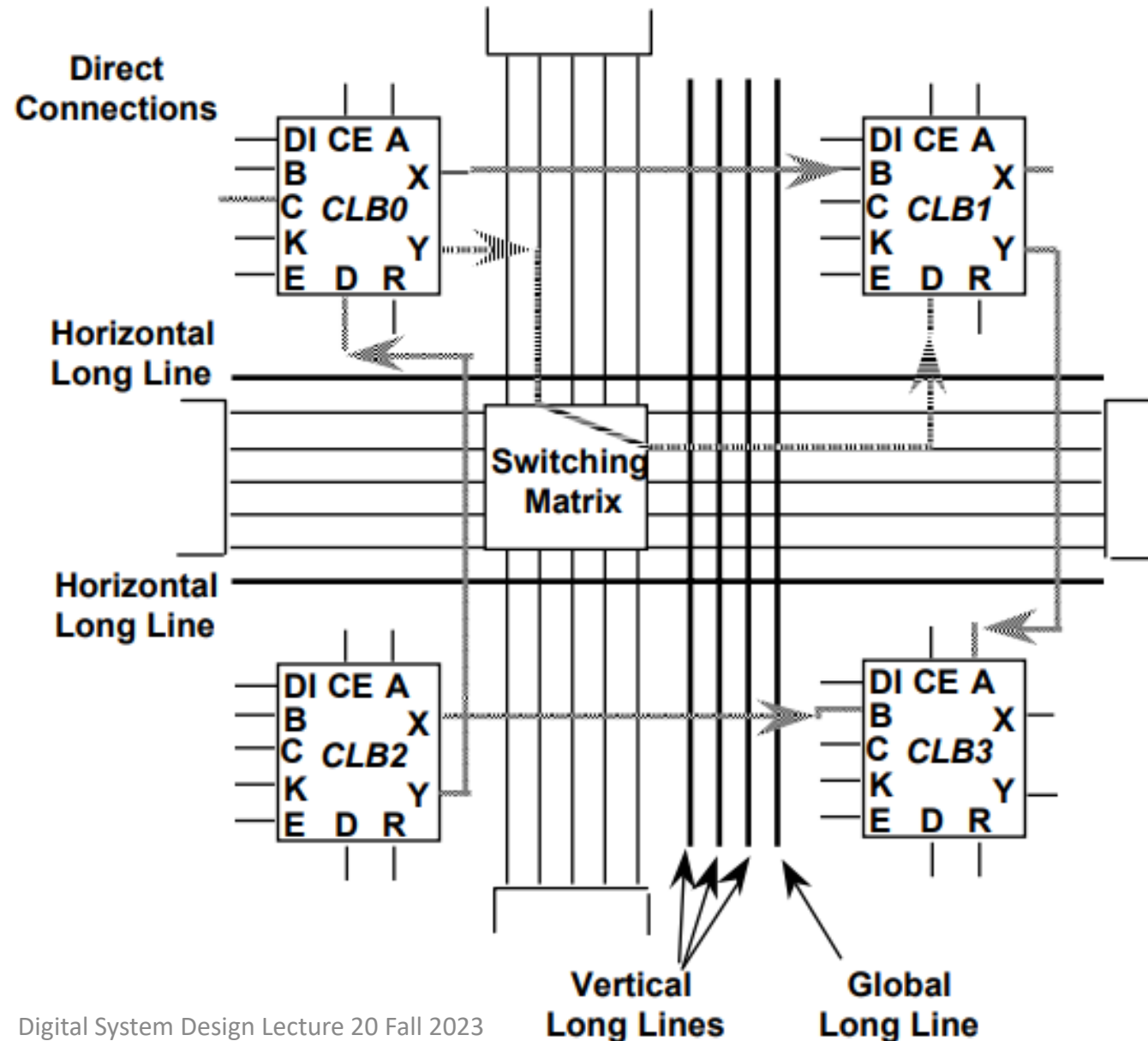
Xilinx 4000 Different types of Interconnects
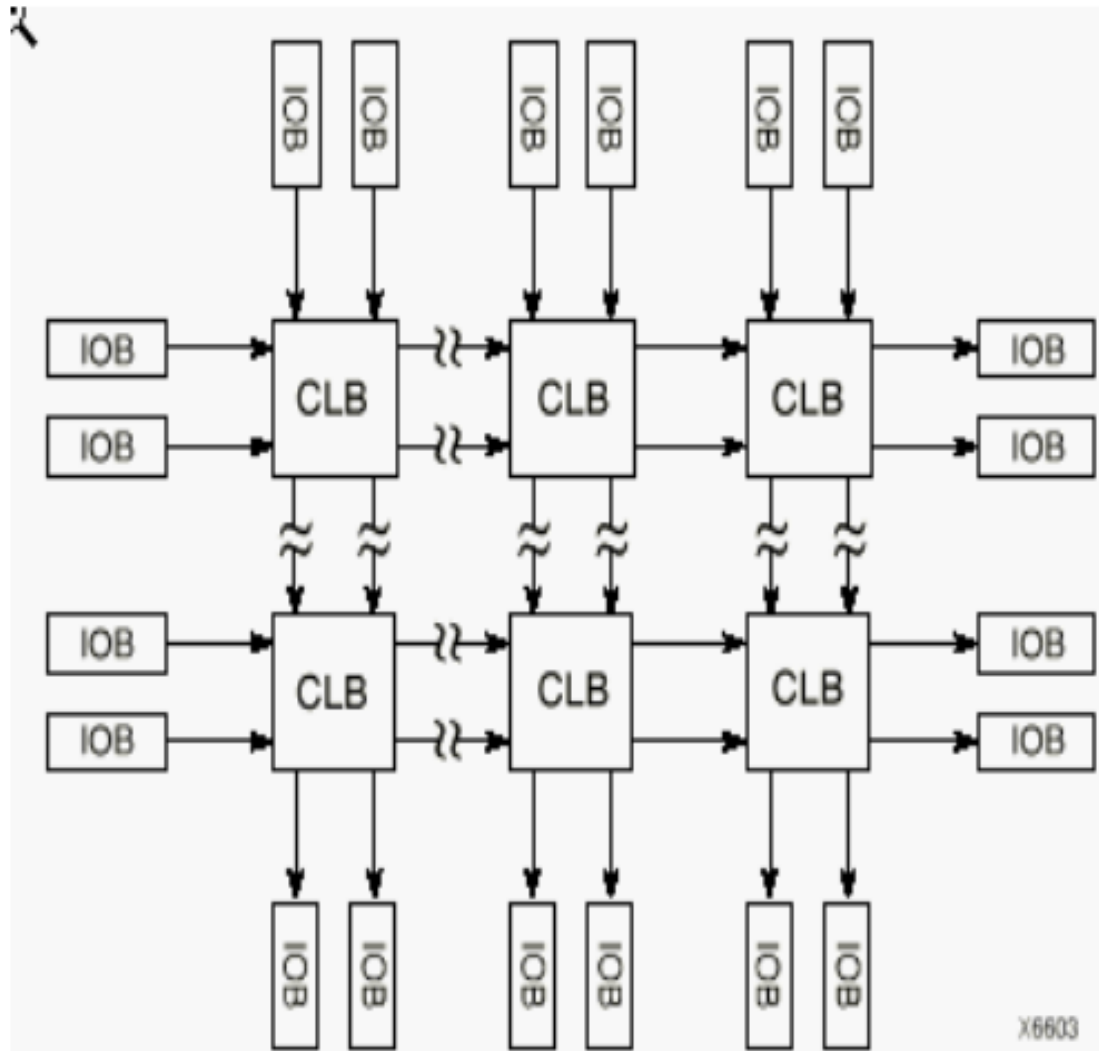
Simplified diagram

3 types:

* **Fast Direct Connections**

* **General Purpose Connections with Switching Matrix**

* **Horizontal/Vertical Long Lines**

Types of lines:

* **Single length (8)**
* **Double length (4)**
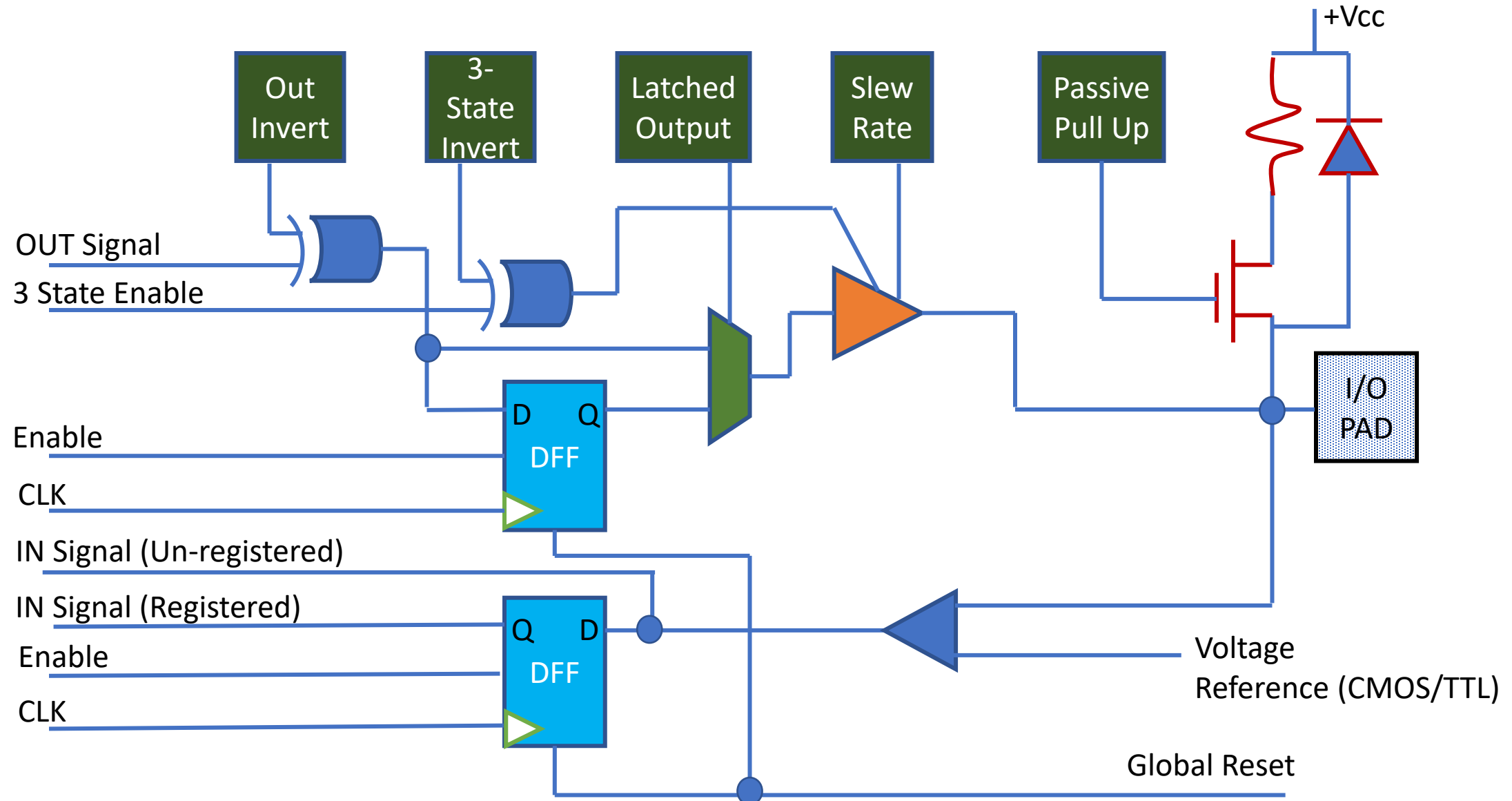* **Long lines (6)**
* **Global lines (4)**
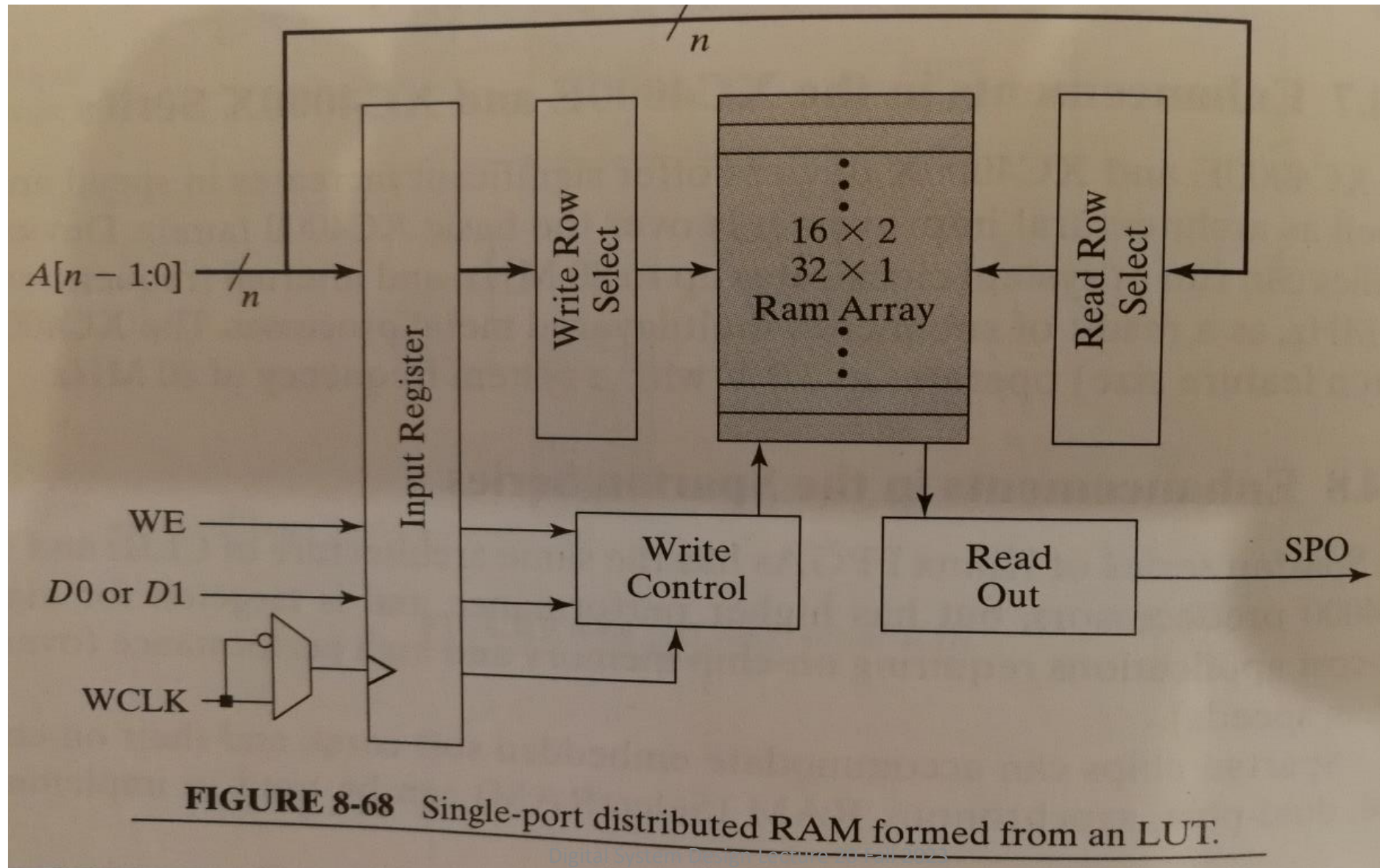
Direct Interconnect in Xilinx 4000

- Between neighboring blocks
- From CLB to CLB
- From CLB to IOB
- Fastest, short distance connections
- X: Hor. connection
- Y: Vert. connection
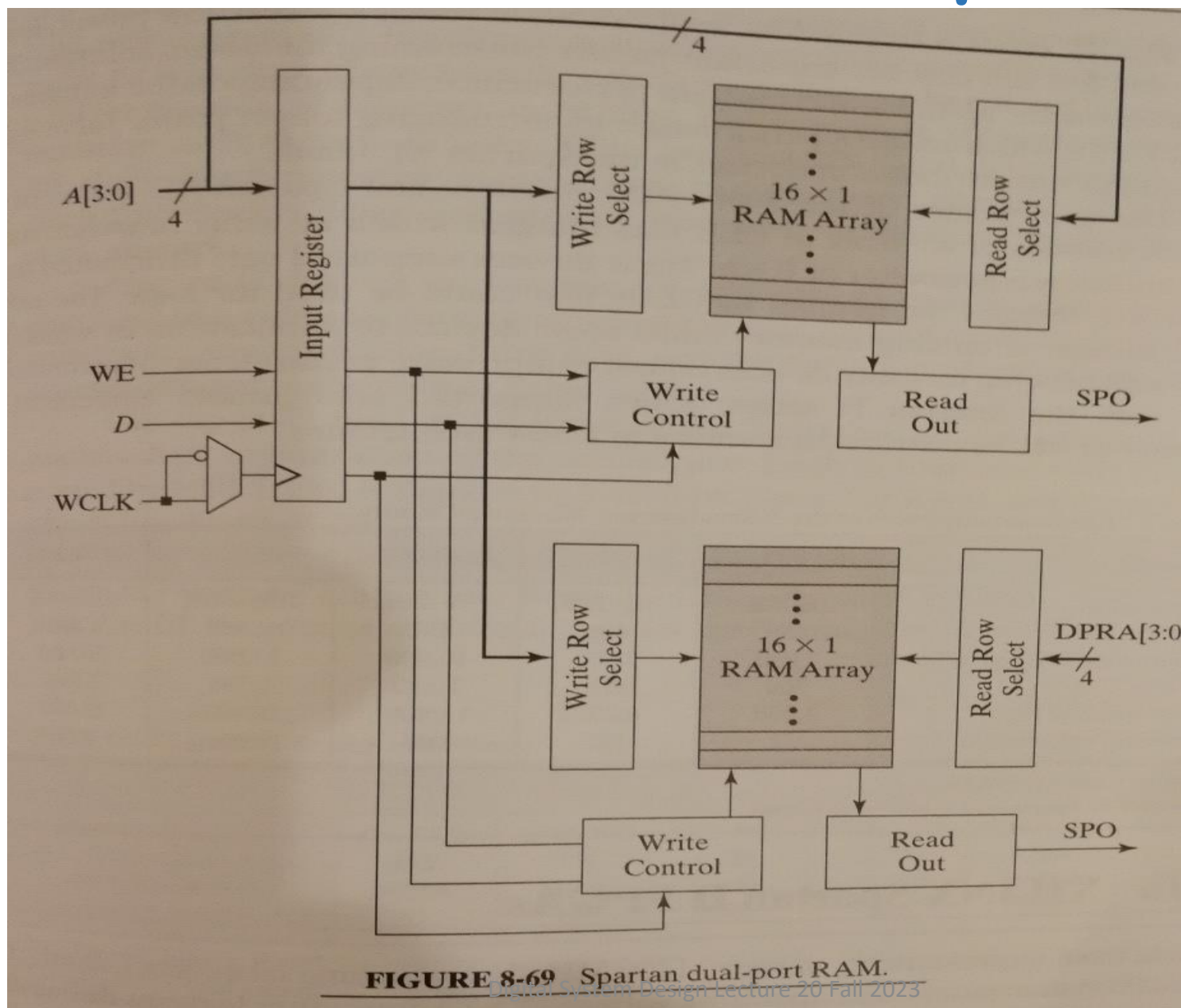
Programmable I/O Blocks in FPGA
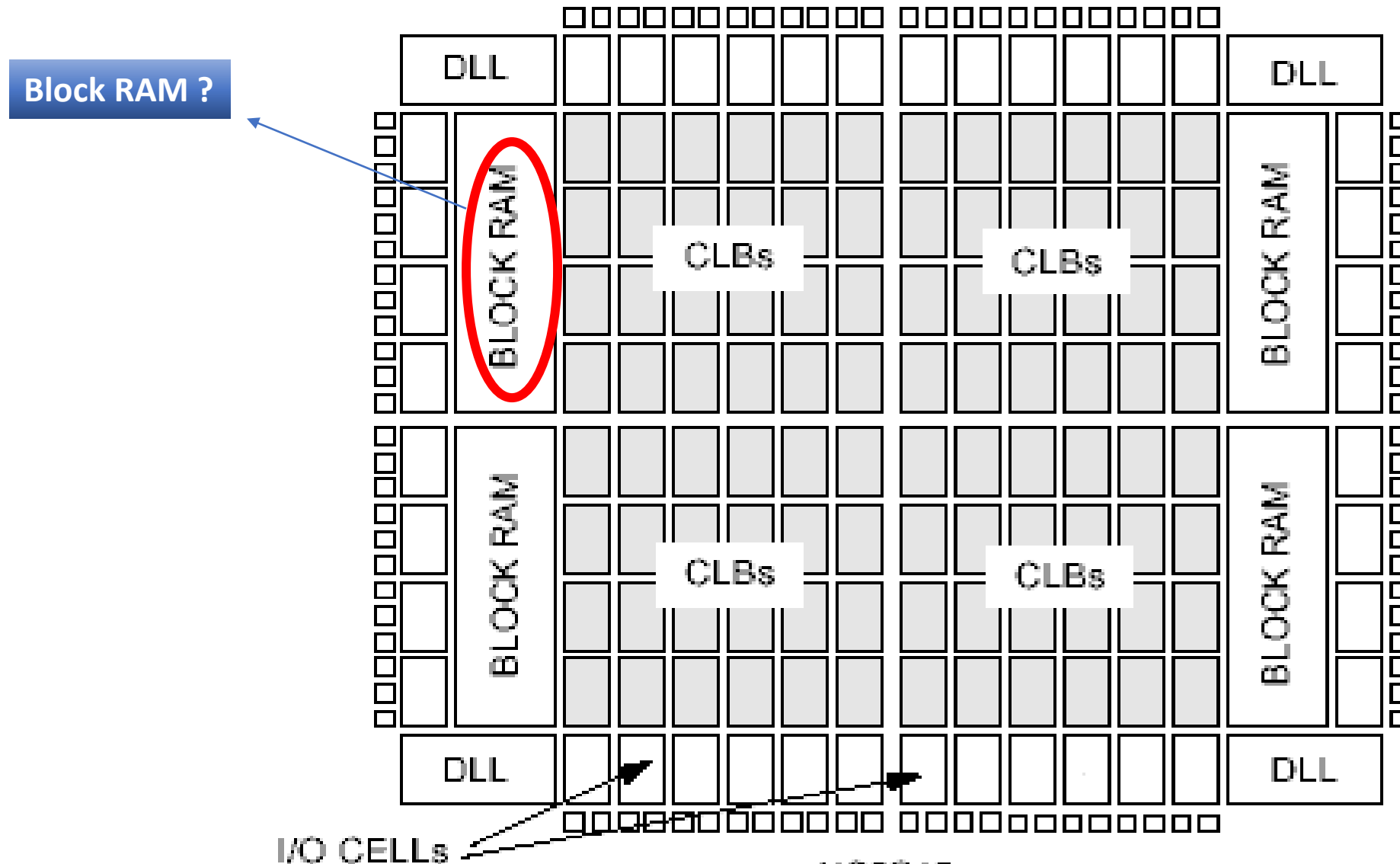
Memory Storage for Configuration

Single Port Distributed RAM from LUT based CLB

FIGURE 8-68 Single-port distributed RAM formed from an LUT.

Dual Port RAM in Xilinx Spartan FPGA

FIGURE 8-69 Spartan dual-port RAM.

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Xilinx Spartan Architecture

Block RAM ?

DLL = Delay Locked Loop For Clock Management

Digital Clock Module in Xilinx FPGA

Clock Management

- Digital Clock Managers (DCMs)
  - Clock de-skew
  - Phase shifting
  - Clock multiplication
  - Clock division
  - Frequency synthesis