Very Large Scale Integration (VLSI)

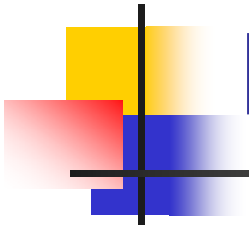
Lecture 9

Dr. Ahmed H. Madian

Ah_madian@hotmail.com

Content

- Packaging
- Input/Output pads
  - Overall organization
  - V_{DD} and V_{SS} pads
  - Output Pads
  - Input pads
  - Tristate and Bidirectional Pads

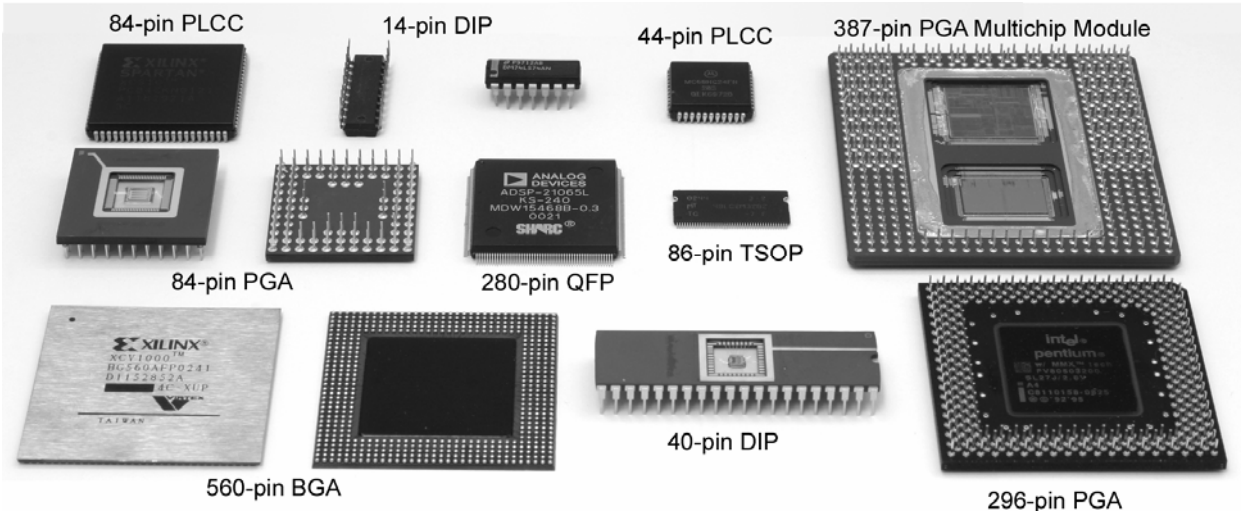


Packages

- Package functions
  - Electrical connection of signals and power from chip to board with little delay and distortion.
  - Mechanical connection of chip to board
  - Removes heat produced on chip
  - Protects chip from mechanical damage
  - Compatible with thermal expansion
  - Inexpensive to manufacture and test

Package Types

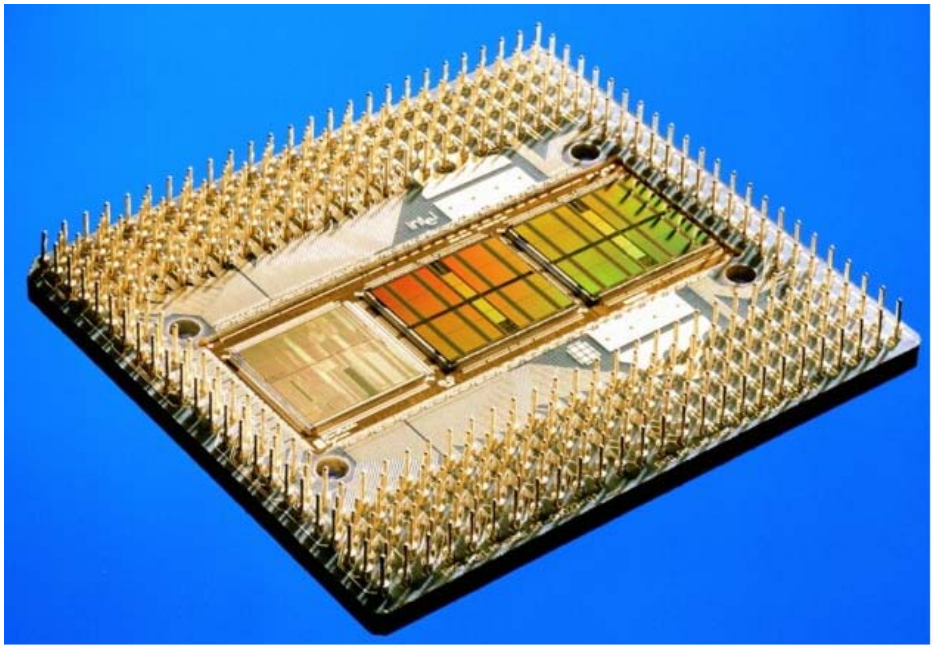
- Through-hole vs. surface mount



- Dual Inline Packages (DIP), Pin Grid Array (PGA), Plastic Leadless Chip Carrier (PLCC) are convenient for components that might be removed for reprogramming, While Ball Grid Array (BGA) provides large number of high-bandwidth signals in compact form

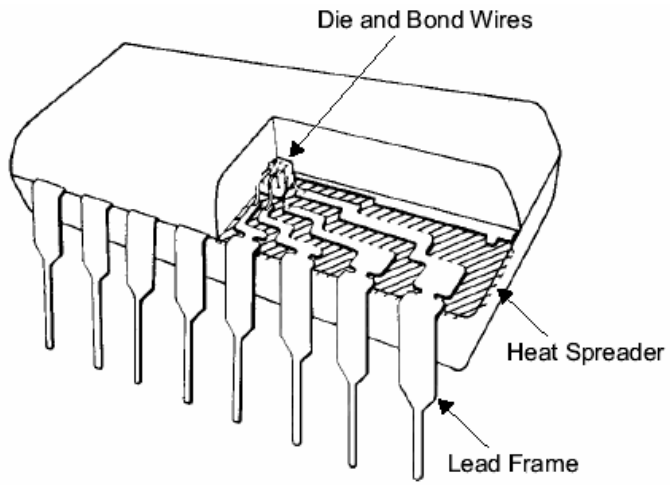
Multichip Modules (MCM)

- Pentium Pro MCM
  - Fast connection of CPU to cache, higher speed.
  - Expensive.



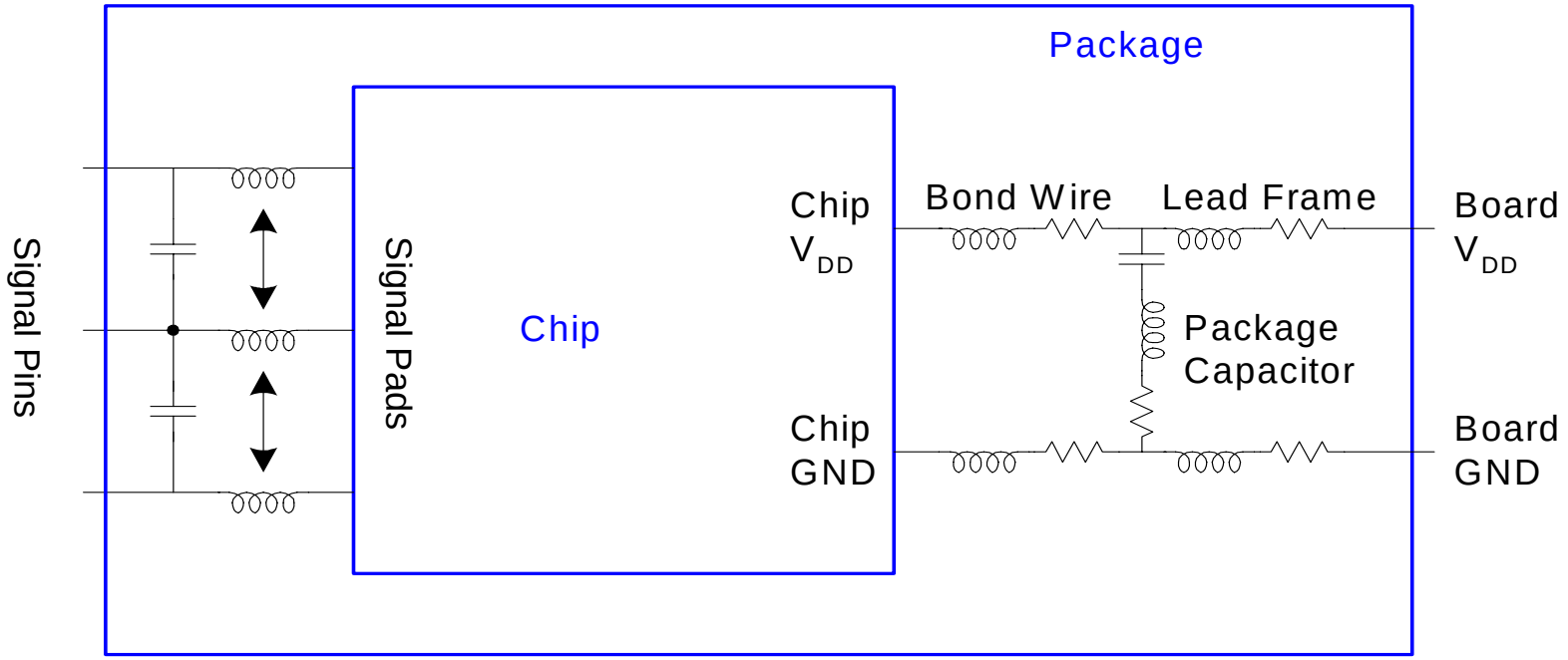
Chip-to-Package Bonding

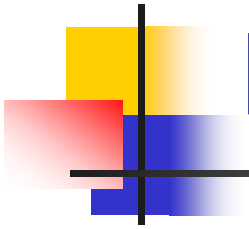
- Traditionally, chip is surrounded by *pad frame*
  - Metal pads on 100 – 200 μm pitch
  - Gold *bond wires* attach pads to package
  - *Lead frame* distributes signals in package
  - Metal *heat spreader* helps with cooling



Package Parasitics

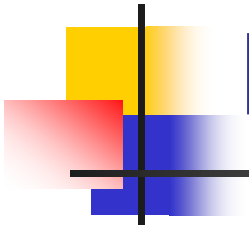
- Use many V_{DD}, GND in parallel
  - Inductance, I_{DD}





Heat Dissipation

- 60 W light bulb has surface area of 120 cm^2
- Itanium 2 die dissipates 130 W over 4 cm^2
  - Chips have enormous power densities
  - Cooling is a serious challenge
- Package spreads heat to larger surface area
  - Heat sinks may increase surface area further
  - Fans increase airflow rate over surface area
  - Liquid cooling used in extreme cases ($)

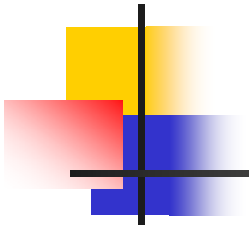


Power Distribution

- Power Distribution Network functions
  - Carry current from pads to transistors on chip
  - Maintain stable voltage with low noise
  - Provide average and peak power demands
  - Provide current return paths for signals
  - Avoid wear-out of electromigration & self-heating
  - Consume little chip area and wire
  - Easy to lay out

content

- Input/Output pads
  - Overall organization
  - V_{DD} and V_{SS} pads
  - Output Pads
  - Input pads
  - Tristate and Bidirectional Pads

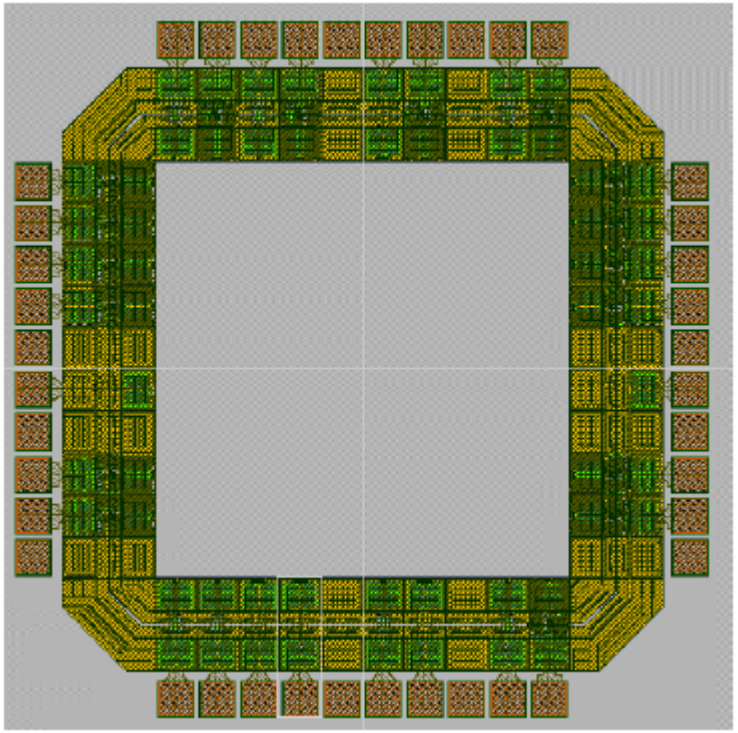


I/O pads

- The I/O system is responsible for communicating data between the chip and the external world.
- A good I/O system has the following properties
  - Drives large capacitances typical of off-chip signals
  - Operates at voltage levels compatible with other chips
  - Limits slew rates to control high-frequency noise
  - Protects chip against damage from electrostatic discharge (ESD)
  - Protect against over-voltage damage
  - Has a small number of pins (low-cost)

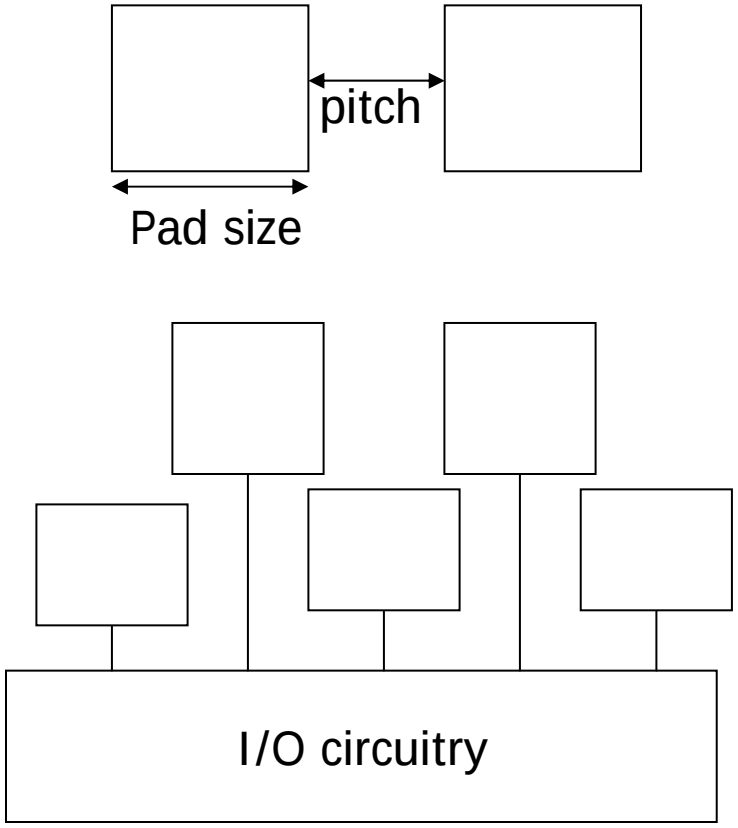
I/O pad organization

- Pad consists of a square of top-level metal of approximately 100µm on a side that is either soldered to bond wire connecting to a package or coated with lead solder ball.
- Pad refers to metal square only or to the complete I/O cell containing the metal, ESD protection circuit, and I/O transistors.
- Also sometimes it contains built in receiver and driver circuits to perform level conversion and amplification.



I/O pad organization (cont.)

- Pad size is defined usually by the minimum size to which a bond wire can be attached. This is usually of the border of 100-150μ square.
- The spacing of the pads is defined by the minimum pitch at which bonding machines can operate.
- Extremely high pad counts may be achieved by inter-digitating pads.

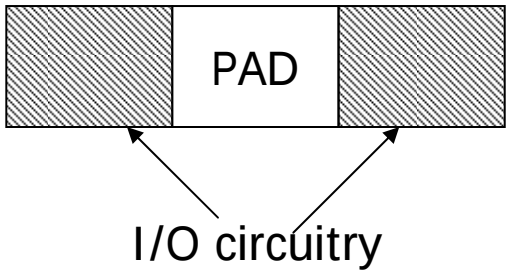


I/O pad organization (cont.)

- Pads could be designed according to following criteria:
  - Core-limited
  - Pad-limited

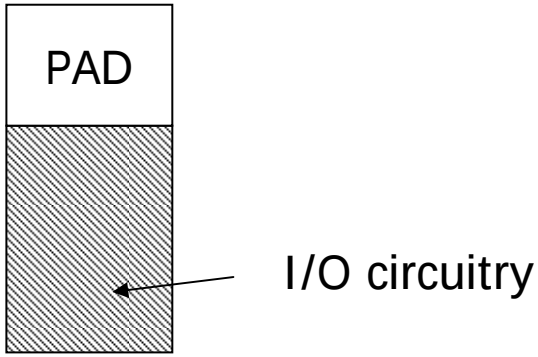
I/O pad organization (cont.)

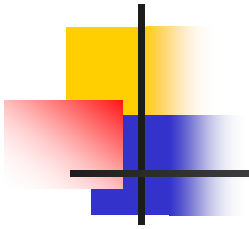
- Core limited
  - The internal core of the chip determines the size of the chip, so thin pads are required.
  - The input/output circuitry is placed on either side of the pad



I/O pad organization (cont.)

- PAD limited
  - The input/output circuitry is placed toward the center of the chip



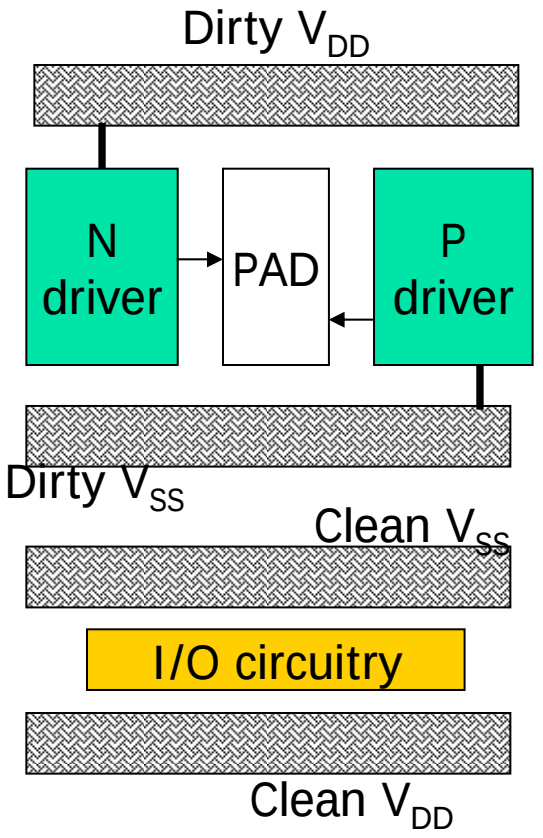


I/O pads

- V_{DD} and V_{SS} Pads
  - Power pads are simply squares of metal connected to the package and the on-chip power grid.
  - High performance chips devote about half of their pins to power. This large number is required to carry the high current and to provide low supply inductance.

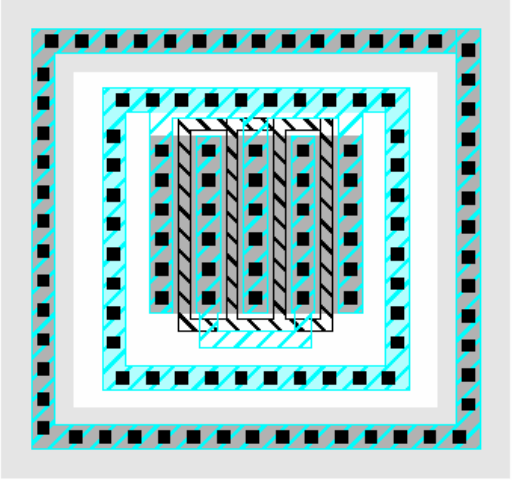
I/O pads (cont.)

- V_{DD} and V_{SS} Pads
  - One of the largest sources of noise in many chips is the ground bounce caused when output pads switch.
  - The pads must rapidly charge the large external capacitive loads, causing a big current spike and high L di/dt noise.
  - The problem is especially bad when many pins switch simultaneously, as could be the case of 64-bit off-chip data bus.
    - Solution is to interdigitated such buses with power and ground pins to supply the output current through a low-inductance path.
  - In many designs dirty supply lines are separated from the main power grid to reduce the noise.



Output Pads

- Drive large off-chip loads (2 – 50 pF)
  - With suitable rise/fall times
  - Requires chain of successively larger buffers
- Guard rings to protect against latchup
  - Large nMOS output transistor
  - p+ inner guard ring
  - n+ outer guard ring
    - In n-well

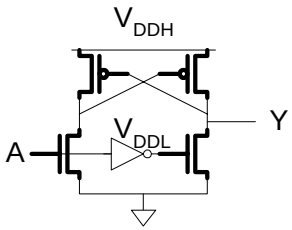


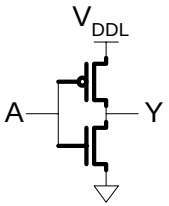
I/O pads

- Output Pads must have sufficient drive capability to deliver adequate rise and fall times into given capacitive load.
- If the pad drives resistive load it must also deliver enough current to meet the required DC transfer characteristics.
- Also, output pads generally contains adequate buffering to reduce the load seen by the on-chip circuitry driving the pad.

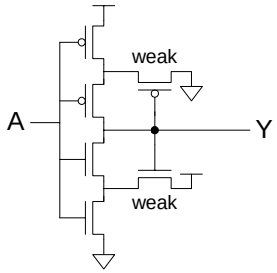
Input Pads

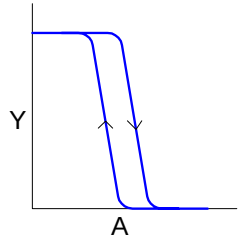
- Level conversion
  - Higher or lower off-chip V





- Noise filtering
  - Schmitt trigger
  - Hysteresis changes V_{IH}, V_{IL}

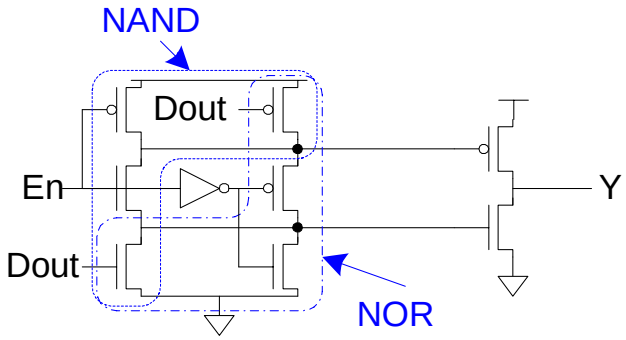


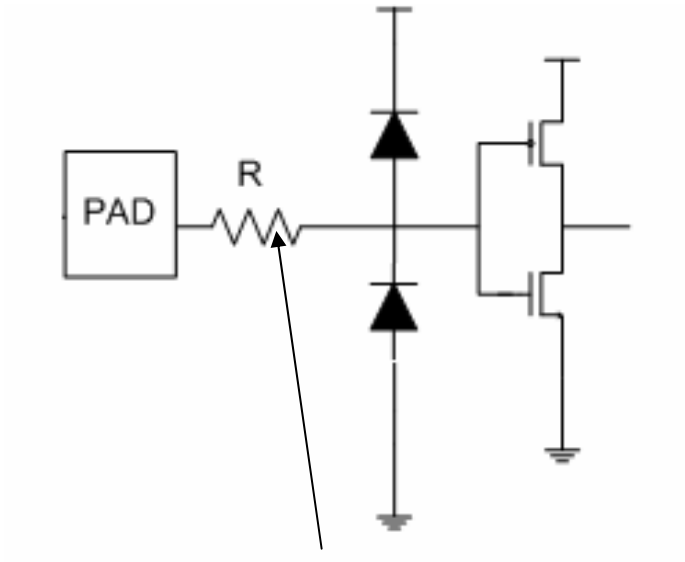


- Protection against electrostatic discharge

I/O pads

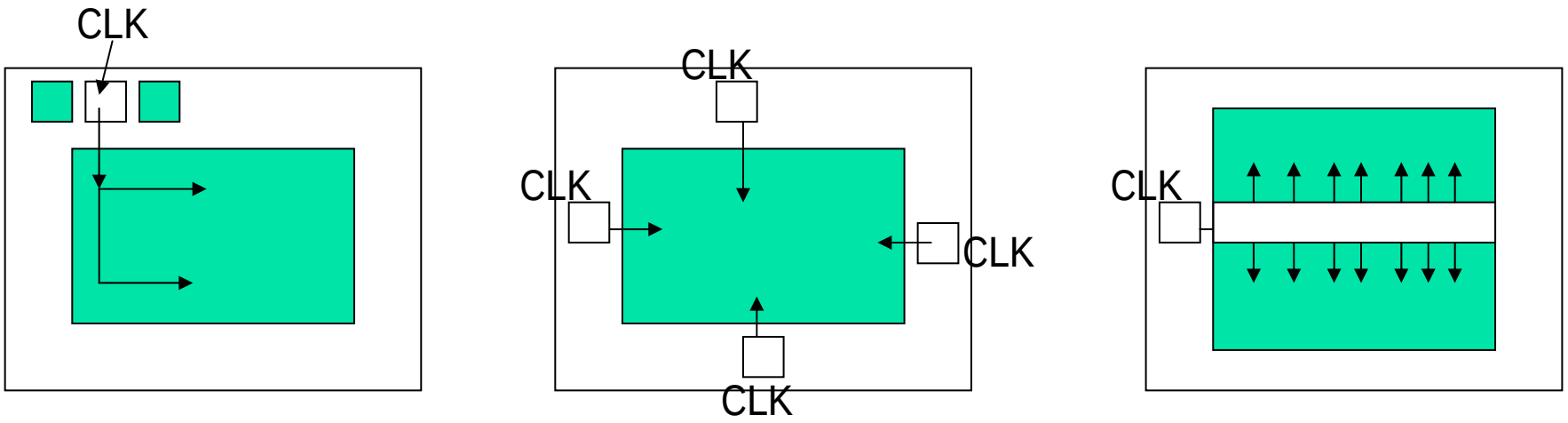
- Input pads ESD protection
  - Input pads have transistor gates connected directly to the external world. These gates are subject to damage from electrostatic discharge that can puncture and break down the oxide. (V_{BD} = 5V in modern processes)
  - A protection circuit from diodes and resistors is used to clamp the input signal





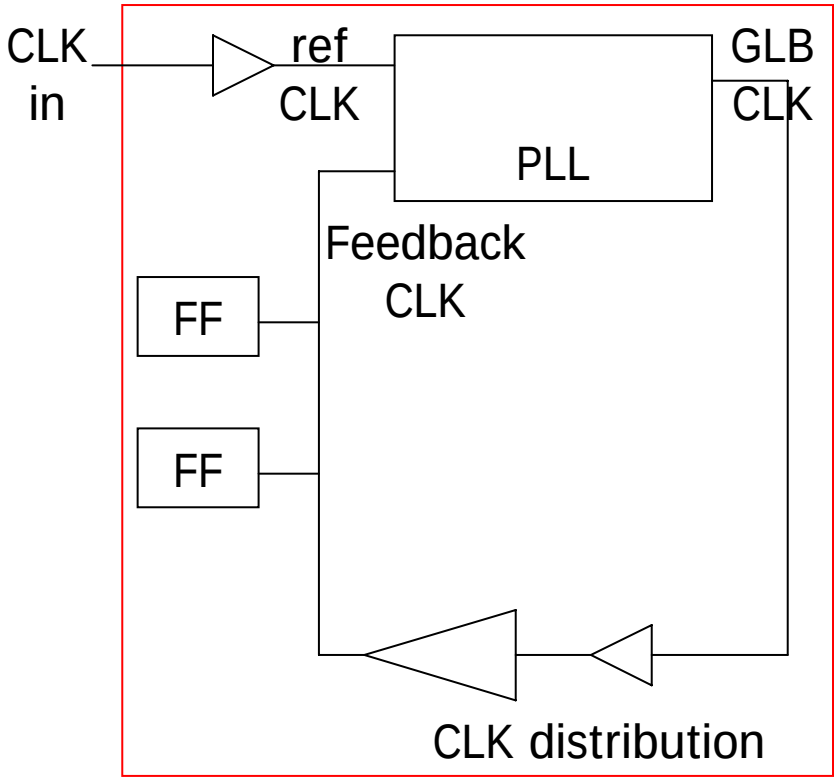
I/O pads (cont.)

- Clock pads
  - They usually have very high internal loading and have to provide extremely fast rise and fall times.
  - So we have three strategies for the clock buffer



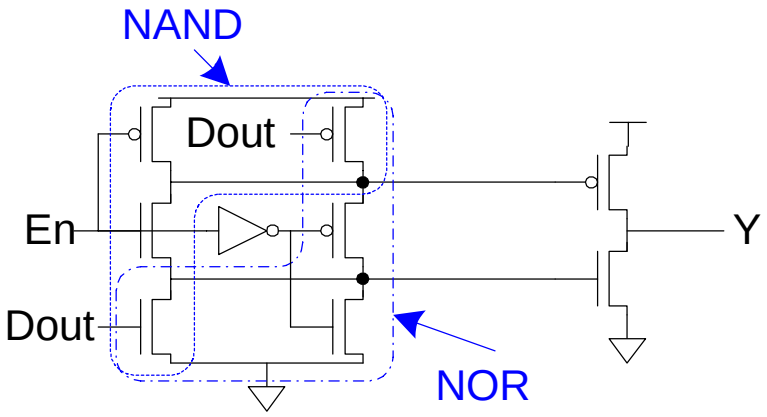
Phase Locked Loop Clock Technique

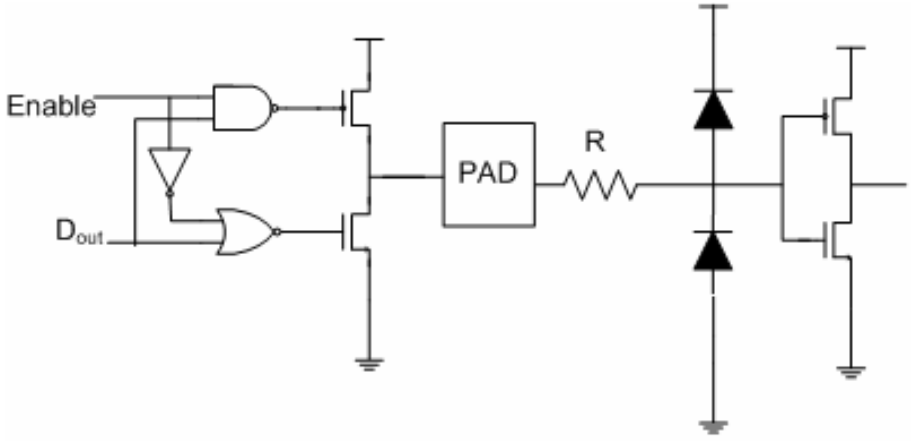
- Phase locked loops (PLL) are used to generate internal clocks on chips for two main reasons:
  - to synchronize the internal clock of a chip with an external clock
  - to operate the internal clock at a higher rate than the external clock input

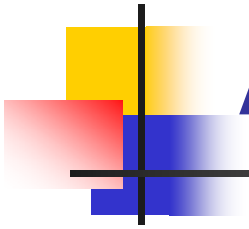


I/O pads (cont.)

- Bidirectional Pads
  - The output driver could be tri-stated according to the Enable signal

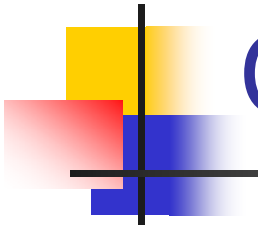






Analog Pads

- Pass analog voltages directly in or out of chip
  - No buffering
  - Protection circuits must not distort voltages



Quiz 2

- Next week check the web site for exact date