VLSI Design EE 523
Spring 2024

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Lecture 19

Topics for lecture 19

- Interconnect Modelling
- Cross Talk
- How to deal with Coupling effects?
- Some examples
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- Combinational Circuit Design Styles
  - Pseudo NMOS
  - Cascode / Differential Circuits

Quiz Next Tuesday

Lab coming Thursday

Interconnect E.g.

Example 6.5

Figure 6.15 models a gate driving wires to two destinations. The gate is represented as a voltage source with effective resistance R_1. The two receivers are located at nodes 3 and 4. The wire to node 3 is long enough that it is represented with a pair of π-segments, while the wire to node 4 is represented with a single segment. Find the Elmore delay from input x to each receiver.

SOLUTION: The Elmore delays are

$$T_{D_3} = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2 + R_3)C_3 + R_1C_4$$
$$T_{D_4} = R_1C_1 + R_1(C_2 + C_3) + (R_1 + R_4)C_4 \qquad (6.18)$$

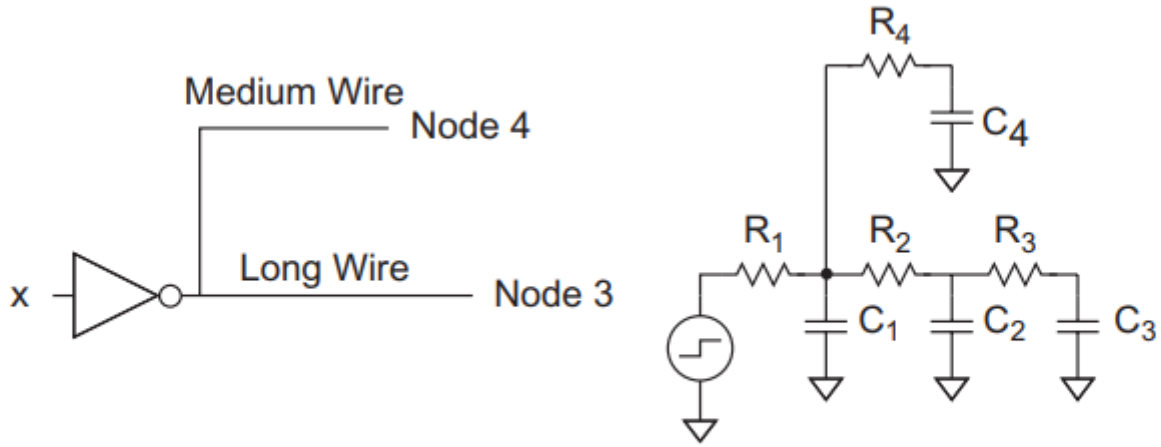

FIGURE 6.15 Interconnect modeling with RC tree

Interconnect Example 2

Example 6.8

Each wire in a pair of 1 mm lines has capacitance of 0.08 fF/μm to ground and 0.12 fF/μm to its neighbor. Each line is driven by an inverter with a 1 kΩ effective resistance. Estimate the contamination and propagation delays of the path. Neglect parasitic capacitance of the inverter and resistance of the wires.

SOLUTION: We find $C_{gnd} = (0.08\ \text{fF}/\mu\text{m})(1000\ \mu\text{m}) = 80\ \text{fF}$ and $C_{adj} = 120\ \text{fF}$. The delay is RC_{eff}. The contamination delay is the minimum possible delay, which occurs when both wires switch in the same direction. In that case, $C_{eff} = C_{gnd}$ and the delay is $t_{cd} = (1\ \text{k}\Omega)(0.08\ \text{pF}) = 80\ \text{ps}$. The propagation delay is the maximum possible delay, which occurs when both wires switch in opposite directions. In this case, $C_{eff} = C_{gnd} + 2C_{adj}$ and the delay is $t_{pd} = (1\ \text{k}\Omega)(0.32\ \text{pF}) = 320\ \text{ps}$. This is a factor of four difference between best and worst case.

Inductance Coupling in Wires

A bus made of closely spaced wires far above a ground plane is particularly susceptible to crosstalk. Figure 6.23 shows the worst case crosstalk scenario. The victim line is in the center. The two adjacent neighbors rise, capacitively coupling the victim upward. The other bus wires fall. Each one creates a loop of current flowing counterclockwise through the wire and back along the ground plane. These loops induce a magnetic field, which in turn induces a current flowing in the other direction in the victim line. This is called mutual inductive coupling and also makes the victim rise. The noise from each aggressor sums on to the victim in much the same way that multiple primary turns in a transformer couple onto a single secondary turn. Computing the inductive crosstalk requires extracting a mutual inductance matrix for the bus and simulating the system. As this is not yet practical for large chips, designers instead either follow design rules that keep the inductive effects small or ignore inductance and hope for the best. The design

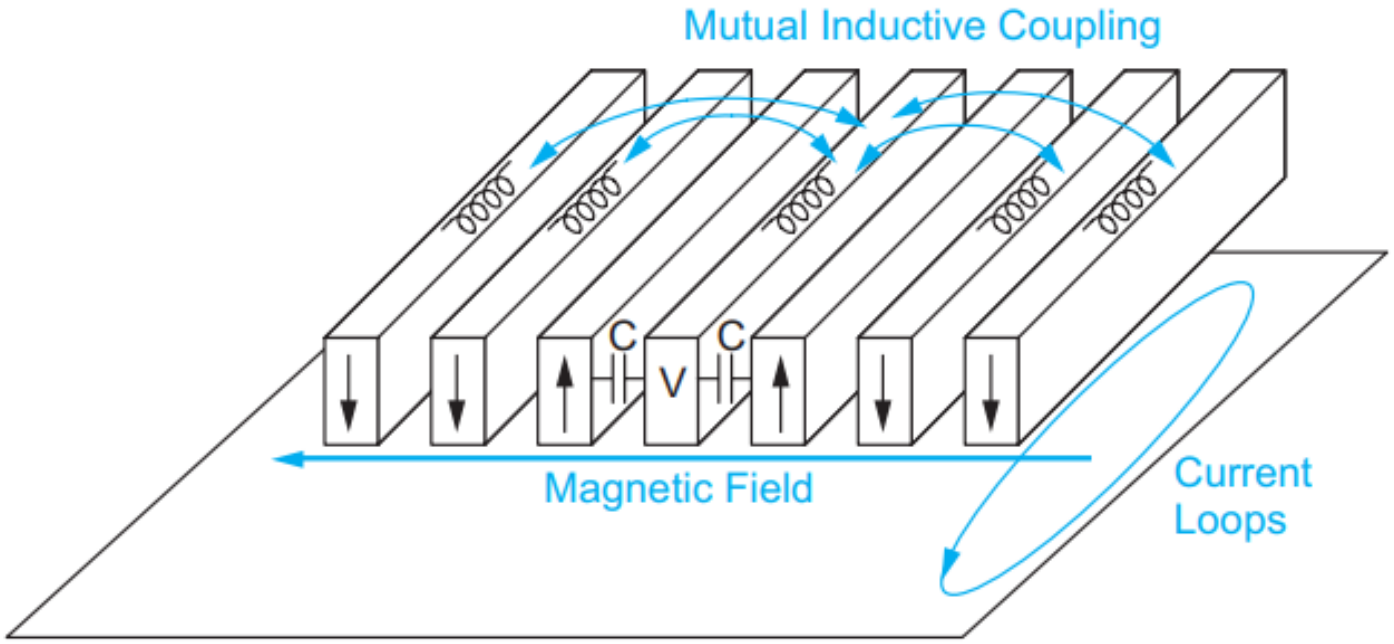

FIGURE 6.23 Inductive and capacitive crosstalk in a bus

Repeaters Example

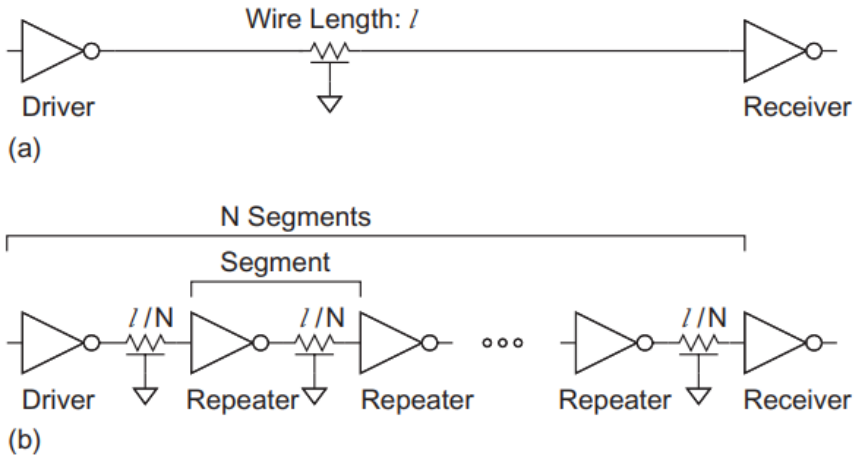

FIGURE 6.26 Wire with and without repeaters

The delay per unit length of a properly repeated wire is

$$\frac{t_{pd}}{l} = \left(2 + \sqrt{2\left(1 + p_{\text{inv}}\right)}\right)\sqrt{RCR_w C_w} \approx 1.67\sqrt{\text{FO4}\, R_w C_w}$$

To achieve this delay, the inverters should use an nMOS transistor width of

$$W = \sqrt{\frac{RC_w}{R_w C}} \qquad (6.30)$$

The energy per unit length to send a bit depends on the wire and repeater capacitances

$$\frac{E}{l} = C_w + NWC\left(1 + p_{\text{inv}}\right) = C_w\left(1 + \sqrt{\frac{1 + p_{\text{inv}}}{2}}\right)V_{DD}^2 \approx 1.87 C_w V_{DD}^2 \qquad (6.31)$$

Example 6.10

Compute the delay per mm of a repeated wire in a 65 nm process. Assume the wire is on a middle routing layer and has 2x width, spacing, and height, so its resistance is 200 Ω/mm and capacitance is 0.2 pF/mm. The FO4 inverter delay is 15 ps. Also find the repeater spacing and driver size to achieve this delay and the energy per bit.

SOLUTION: Using EQ (6.29), the delay is

$$t_{pd} = 1.67\sqrt{(15\text{ ps})(200\ \Omega/\text{mm})(0.2\text{ pF/mm})} = 41\text{ ps/mm} \qquad (6.32)$$

This delay is achieved using a spacing of 0.45 mm between repeaters and an nMOS driver width of 18 μm (180x unit size). The energy per bit is 0.4 pJ/mm.

Reducing Crosstalk

There are several approaches to controlling this crosstalk:

- Increase spacing to adjacent lines
- Shield wires
- Ensure neighbors switch at different times
- Crosstalk cancellation

Readings

- Interconnects are in Chapter 6 of textbook ‘CMOS VLSI Design’ by Weste and Harris
- Combinational Logic Styles are in Chapter 9 of text book