Lecture 20

EE 421 / CS 425

Digital System Design

Fall 2023

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Topics

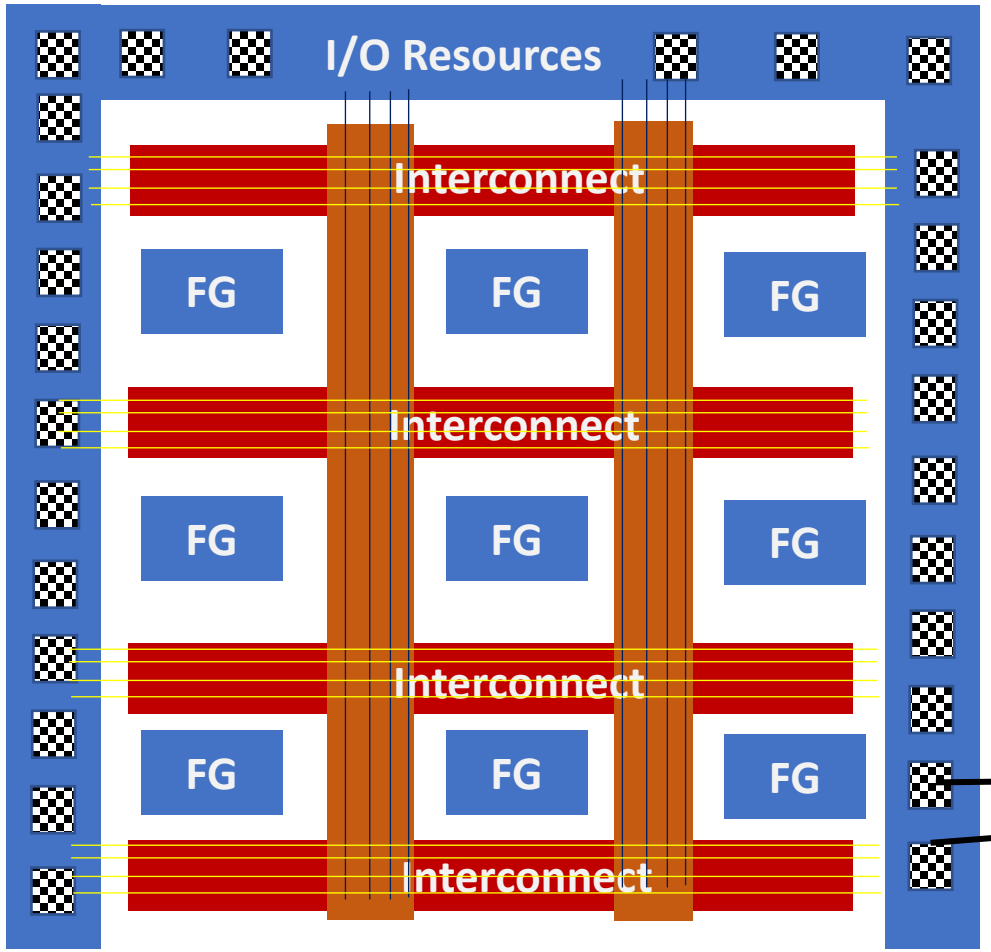
- FPGA Architectures
- Configurable Logic Block
- Configurable I/O Blocks
- Distributed RAM, Block RAM, Dual Port Memory
- Special Features and DSP Slice in FPGA

Quiz 4

Recap from last lecture

- PLA and PAL Devices – Limited Programmability
- CPLD from Xilinx and Altera
- Architecture Differences between CPLD Families
- Important Building Blocks of CPLD
- Limitations of CPLD
- Predictable Timing Performance of CPLD
- How can logic complexity of CPLD macrocell be enhanced?
  - Expanders, etc.

Field Programmable Gate Arrays Generic Architecture



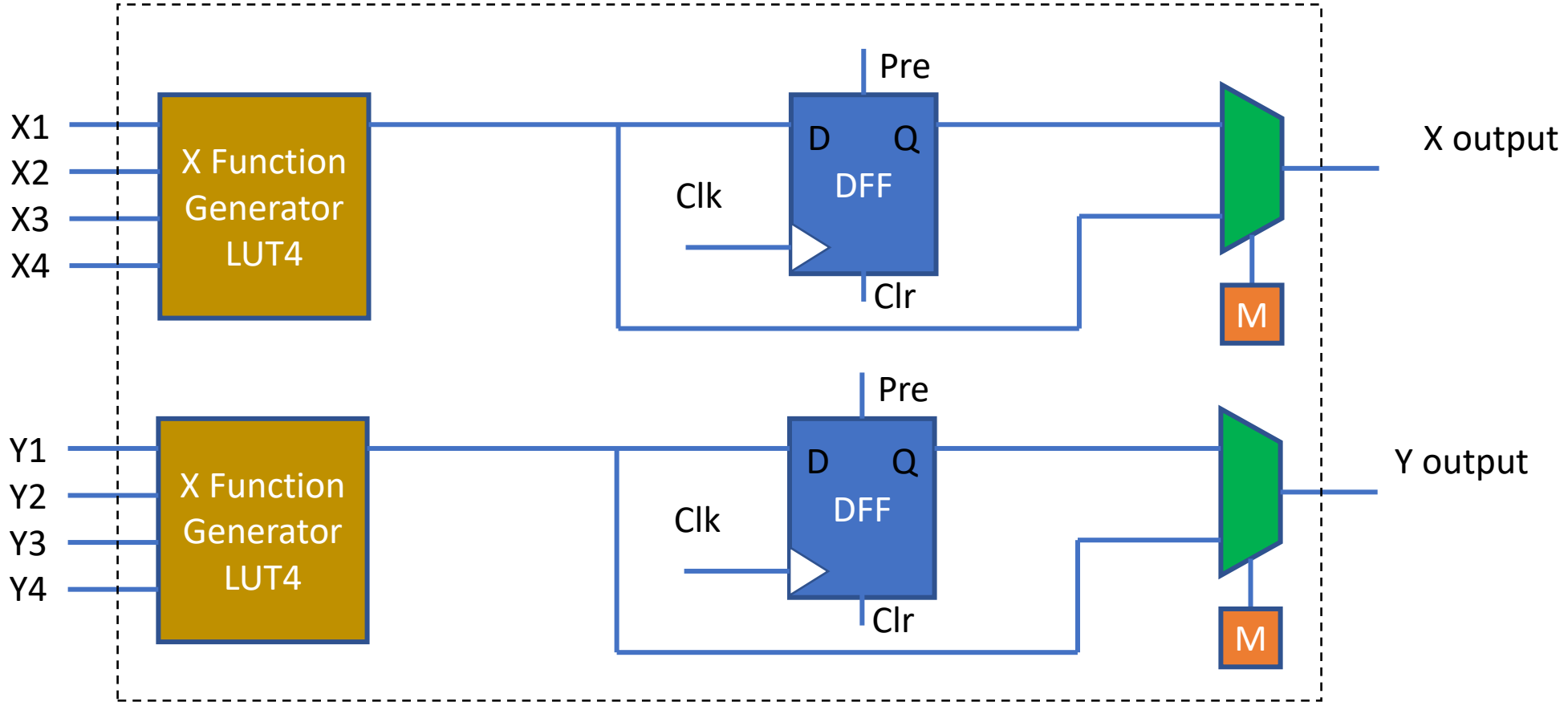
FG = function generator for Logic implementation

I/O Blocks

USB or JTAG Cable

SRAM Configuration Memory

Lookup Table (LUT) based Configurable Logic Blocks

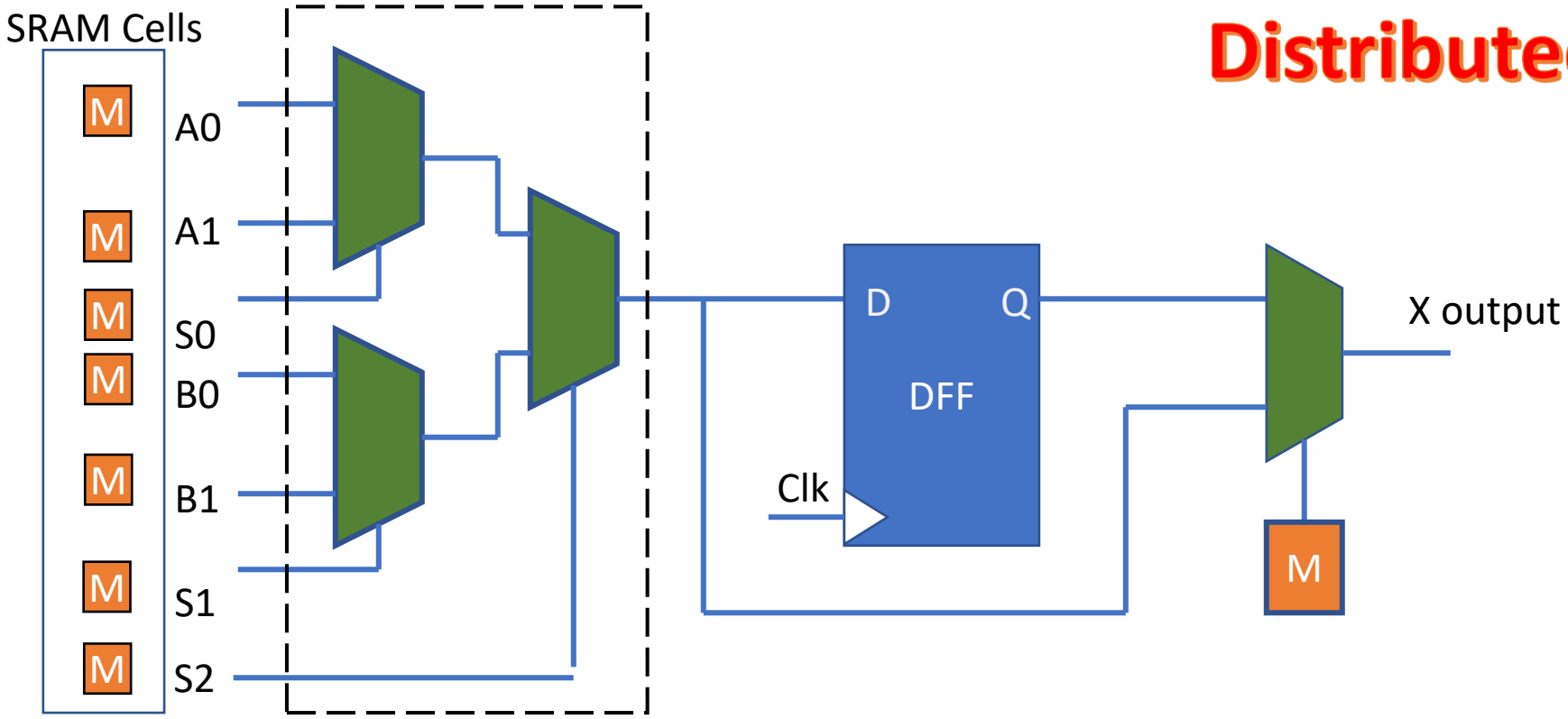


Details of LUT based CLB

- Uses a four-variable look-up table and a flipflop as the basic configurable hardware element. Several of these are combined in different families and types
- Any two functions X and Y of four variables each can be generated in the LUT
- Flipflops at the output can be used. DFF have external preset and clear as well as clock selection mechanism
- Output multiplexer selects from un-registered or registered output

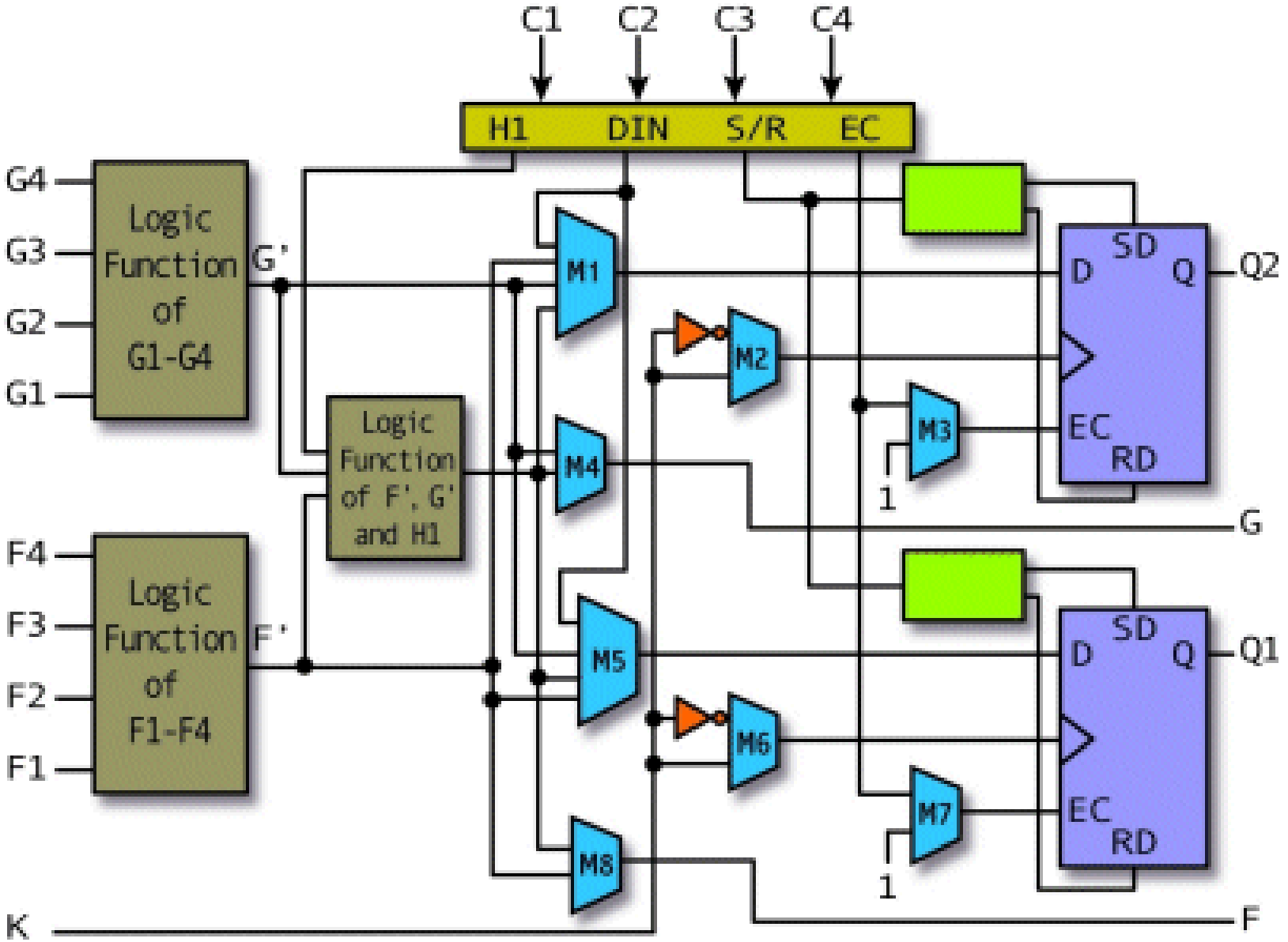
Configurable Logic Blocks based on Multiplexers

Where is Distributed Memory?



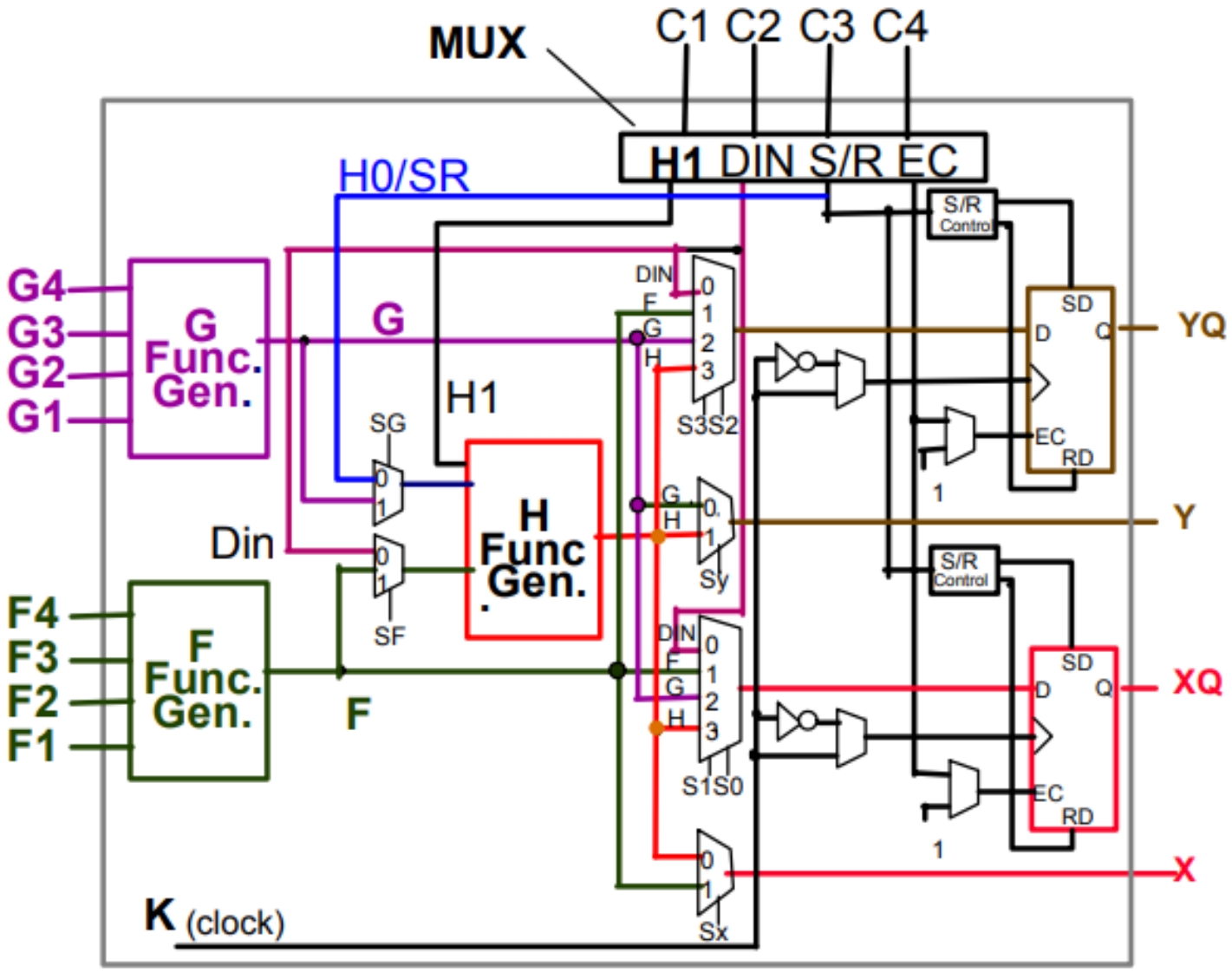
4:1 MUX to generate required SOP Expression

Xilinx 4000 CLB



LUT Configuration and Extension

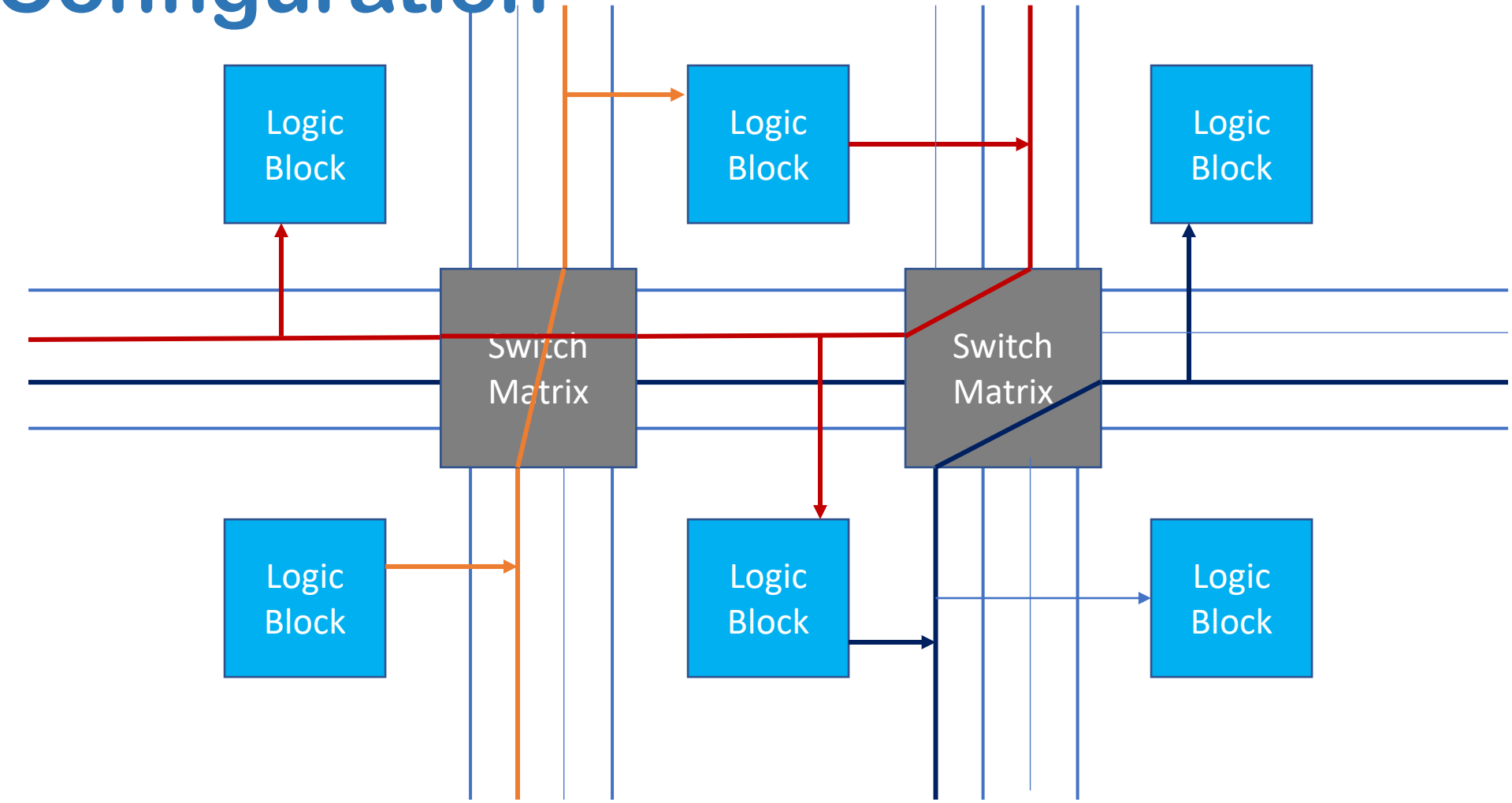
2 Four-input function generators (Look Up Tables)
1 Three-input function
2 Registers:
- Pos. or Neg. edge-trig. Synchronous and asynchr. Set/Reset
Possible functions:
- any fct of 5 var.
- two fcts of 4 var. + one fct of 3 var.
- some fct of 9 var.



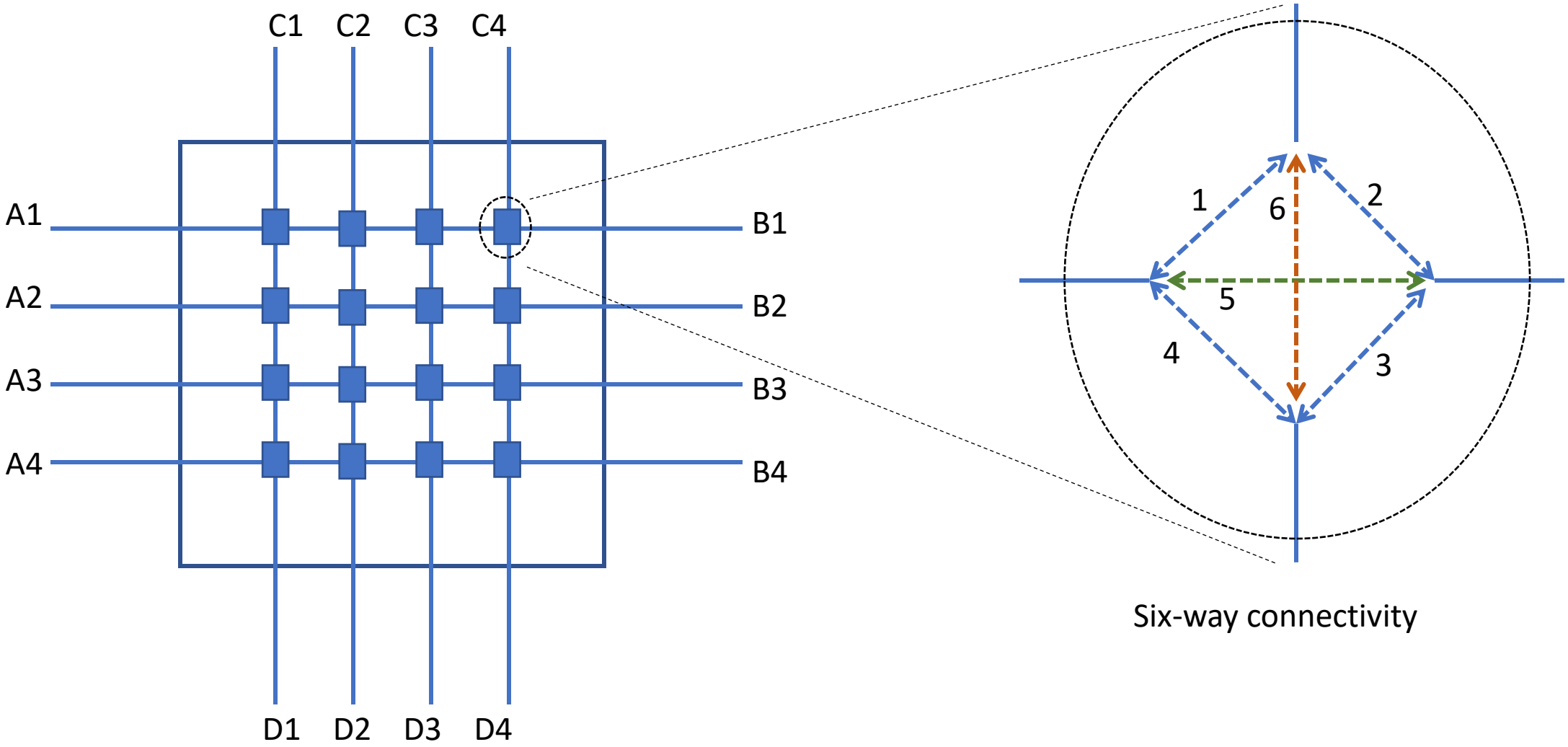
Interconnects

- FPGA in Symmetric Array Configuration (Eg Xilinx)
  - General Purpose Interconnect
  - Direct Interconnects
  - Global Lines
- FPGAs in hierarchical interconnect routing architecture (Eg Altera)
- FPGA in Row Based Configuration (Eg Actel)
- FPGAs in Sea of Gates Fine-Grained Configuration (Eg IBM)

Symmetric (Matrix) Based FPGA Configuration

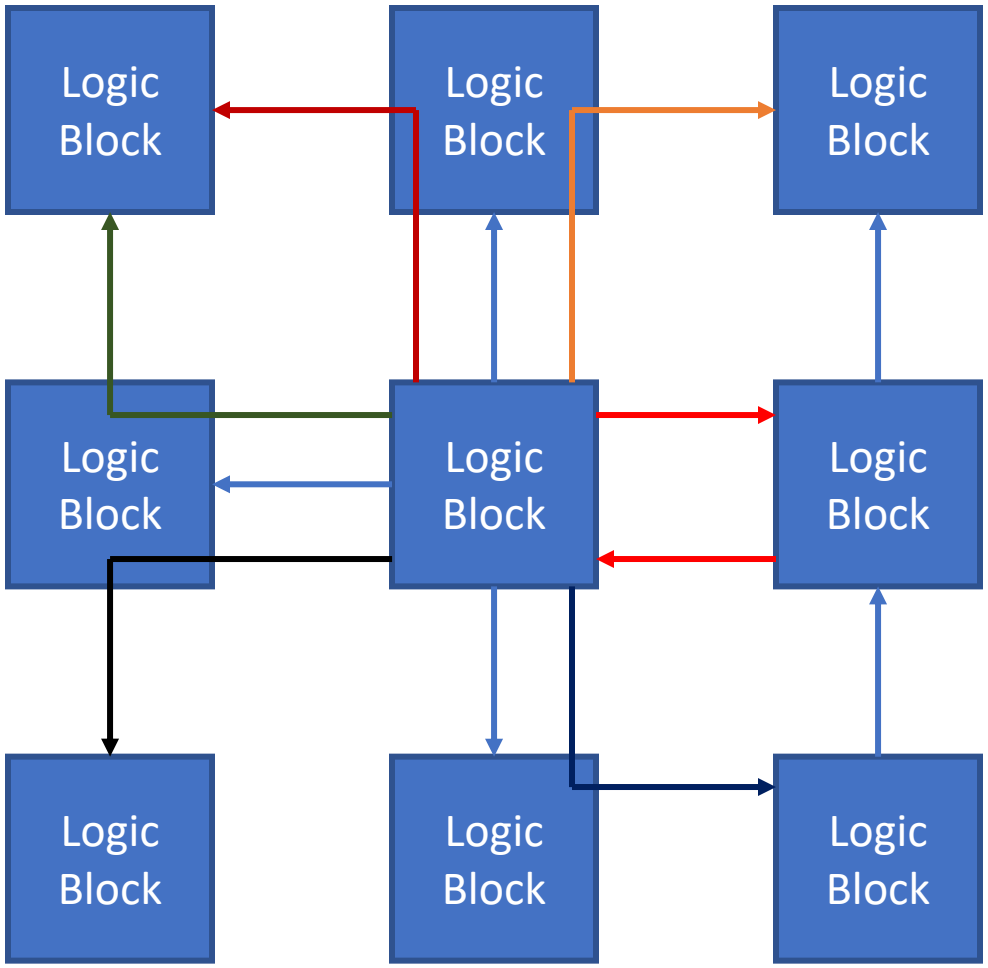


Routing Matrix for General Purpose Interconnection in FPGA

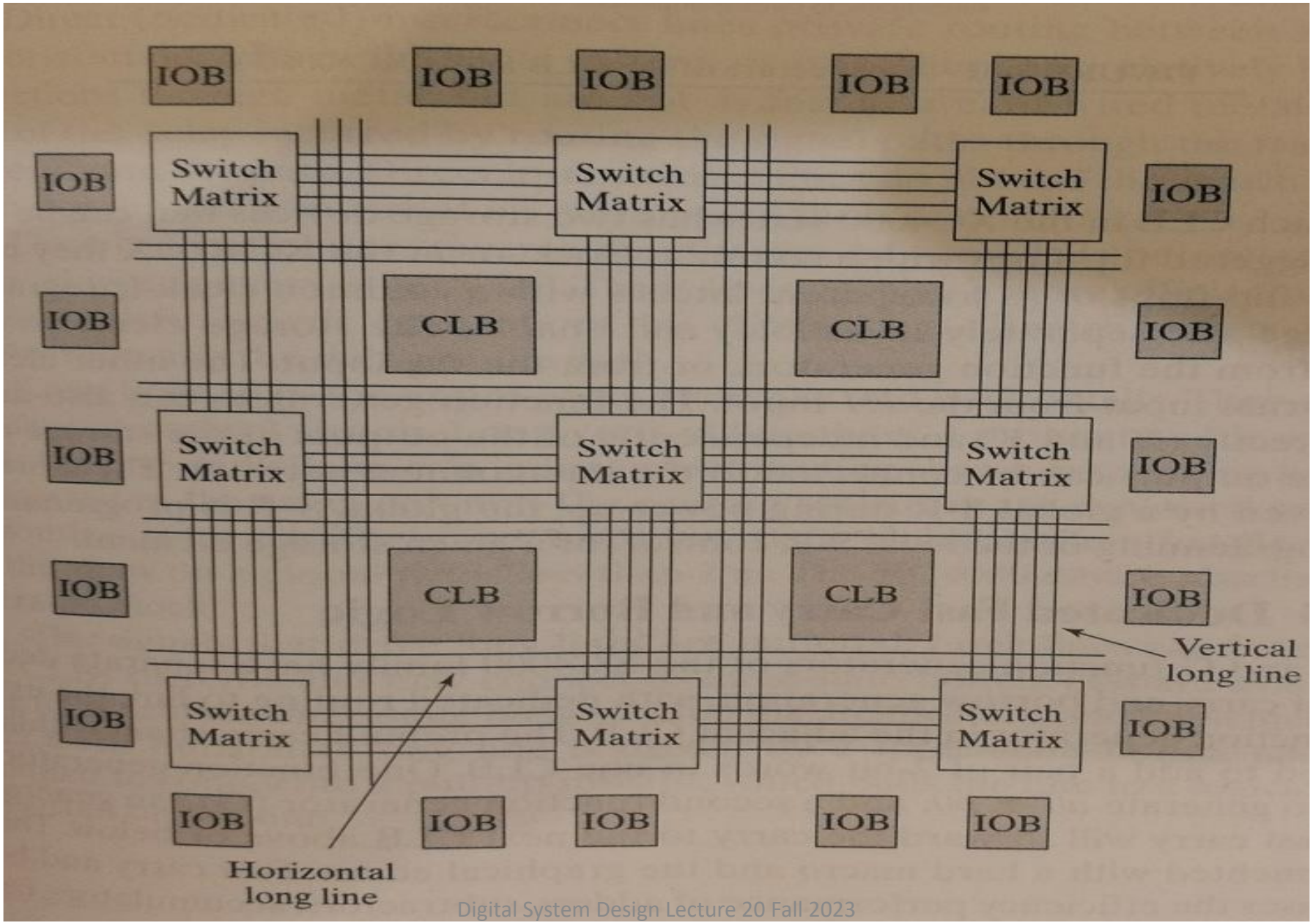


Six-way connectivity

Direct Interconnection to Neighboring Blocks



Xilinx 4000 FPGA Top Level Architecture



Xilinx 4000 Routing Resources with CLB

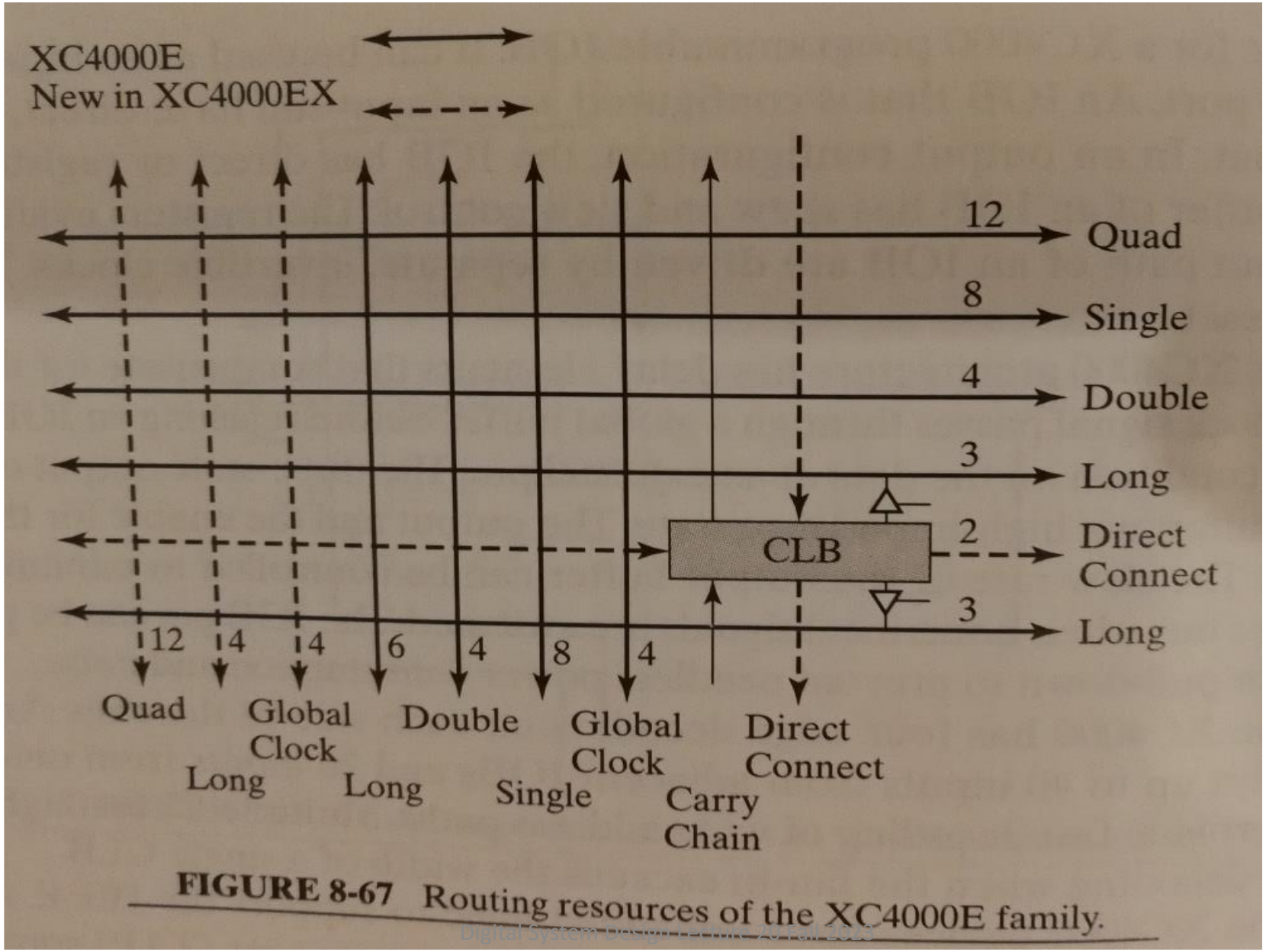
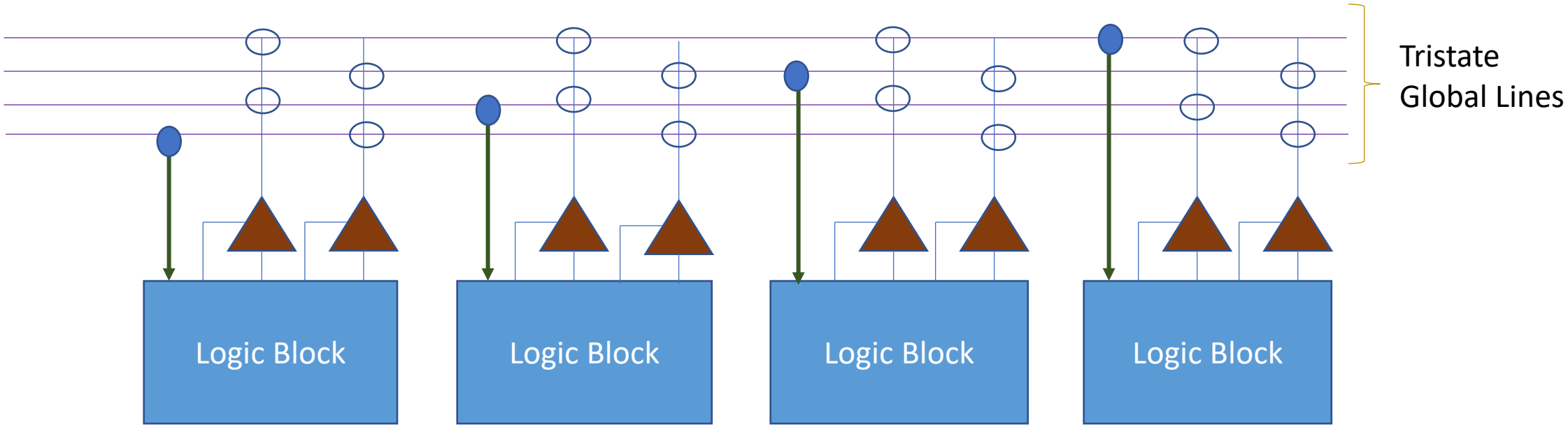


FIGURE 8-67 Routing resources of the XC4000E family.

Global Interconnection Lines



Xilinx 4000 Different types of Interconnects

Simplified diagram

3 types:

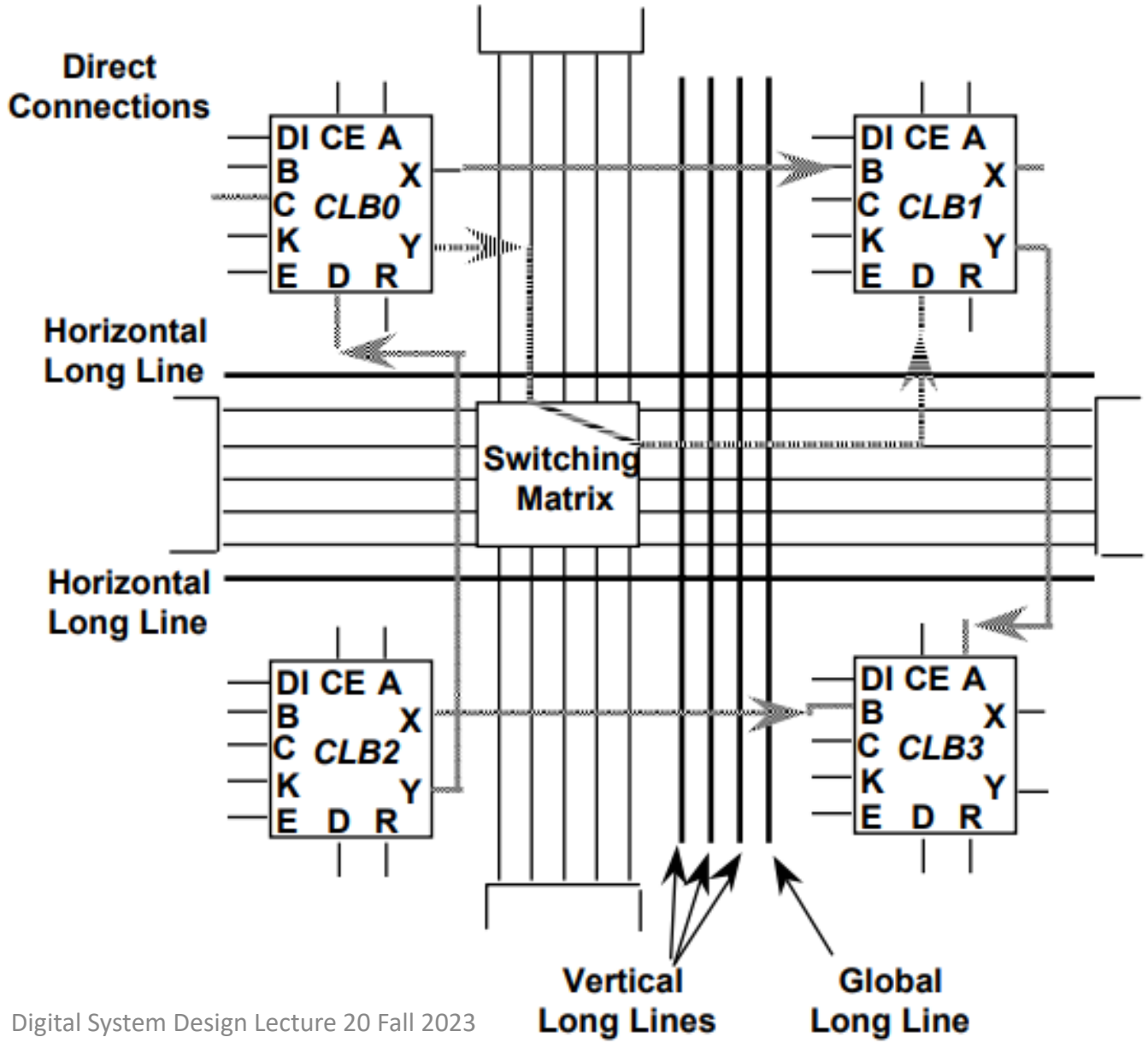
* Fast Direct Connections

* General Purpose Connections with Switching Matrix

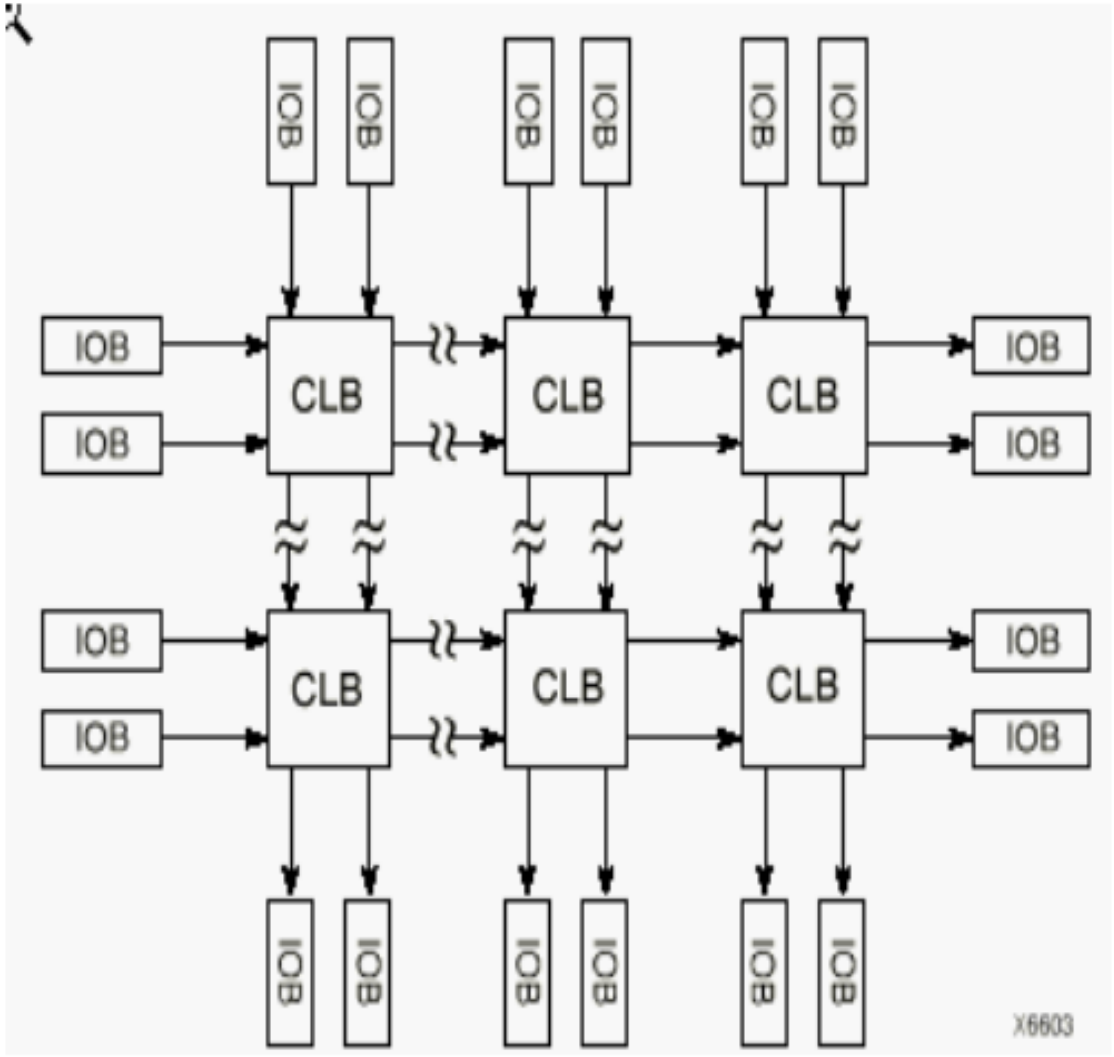
* Horizontal/Vertical Long Lines

Types of lines:

* Single length (8)
* Double length (4)
* Long lines (6)
* Global lines (4)

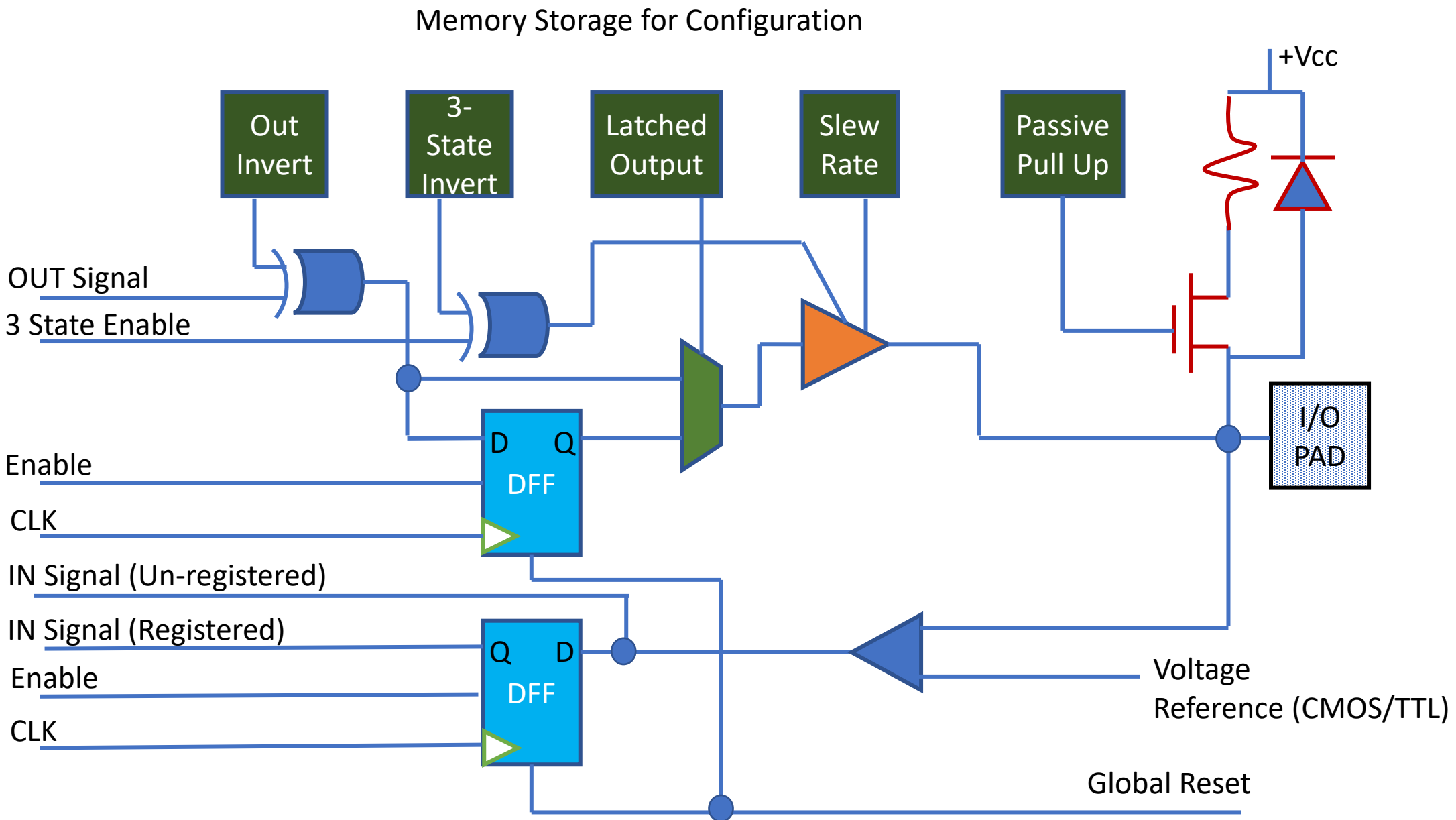


Direct Interconnect in Xilinx 4000



- Between neighboring blocks
- From CLB to CLB
- From CLB to IOB
- Fastest, short distance connections
- X: Hor. connection
- Y: Vert. connection

Programmable I/O Blocks in FPGA



Single Port Distributed RAM from LUT based CLB

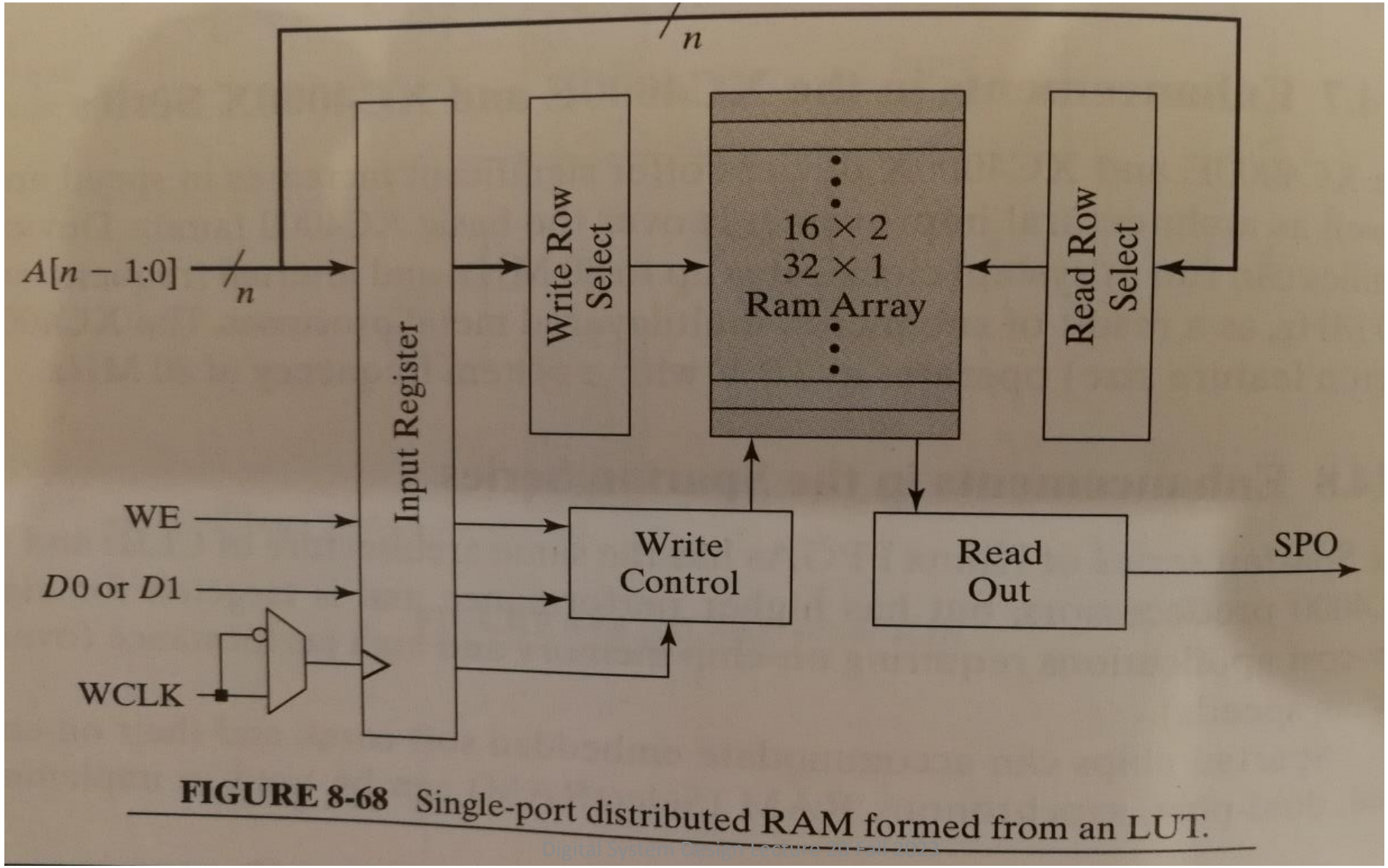


FIGURE 8-68 Single-port distributed RAM formed from an LUT.

Dual Port RAM in Xilinx Spartan FPGA

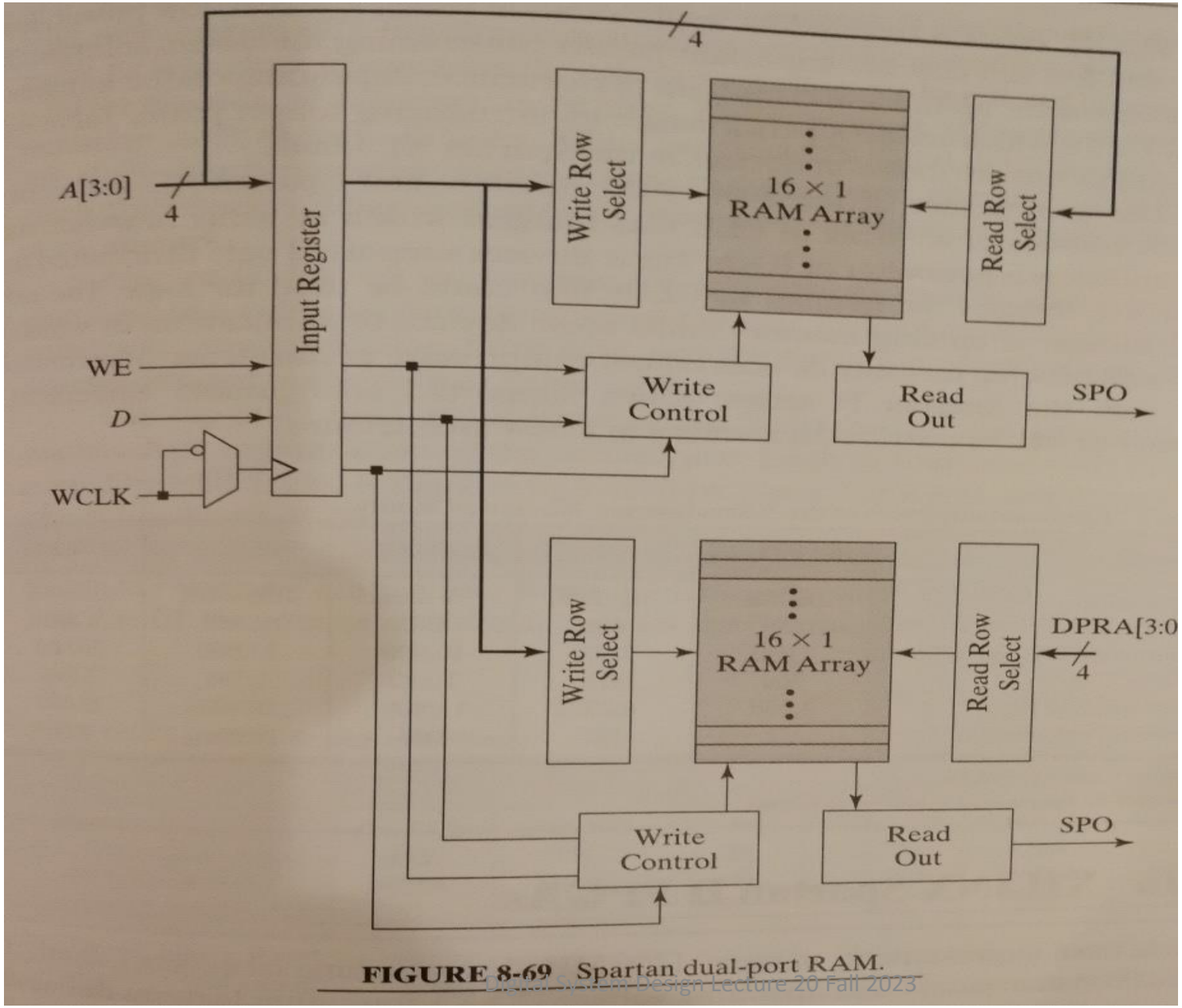
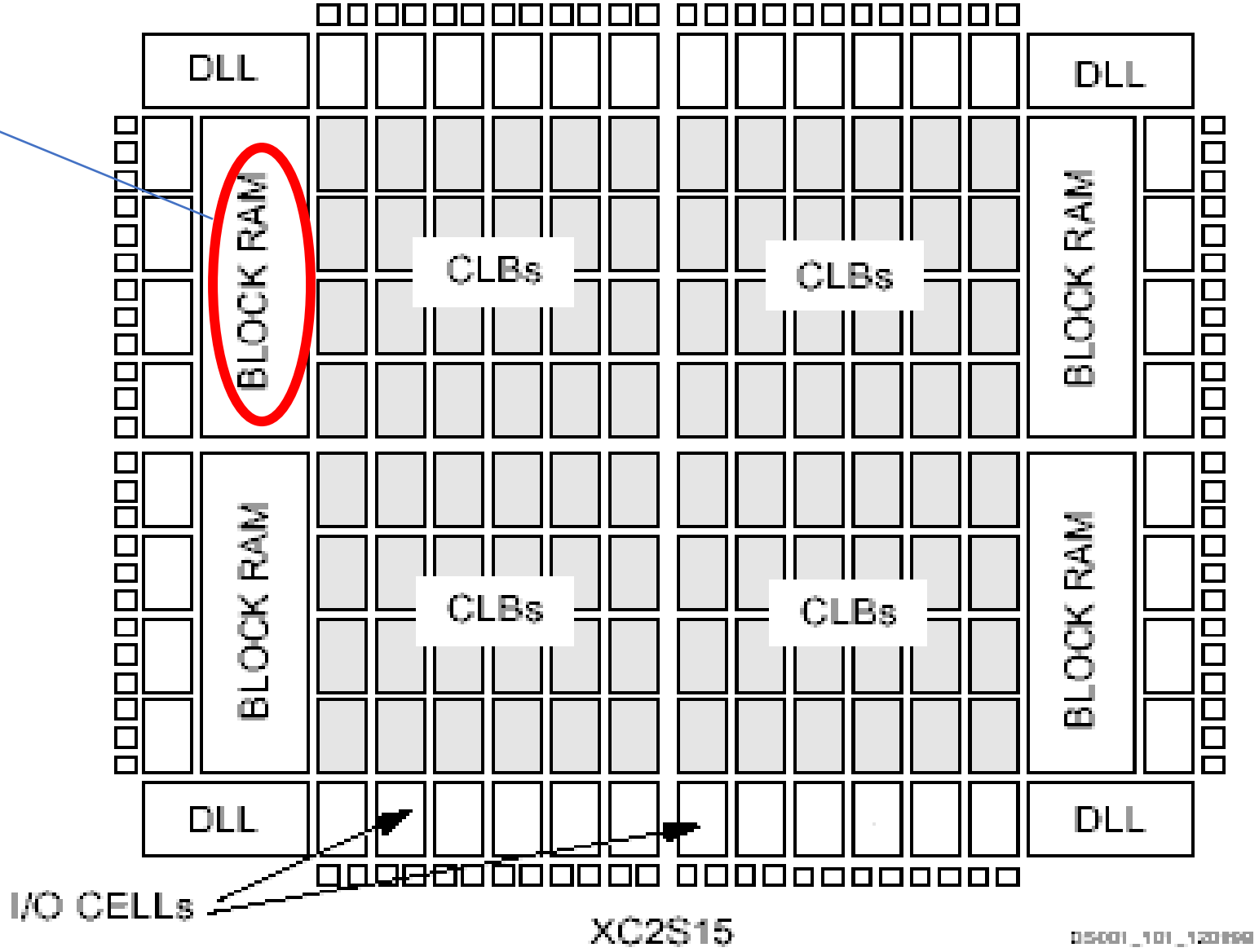


FIGURE 8-69 Spartan dual-port RAM.

Xilinx Spartan Architecture

Block RAM ?



DLL = Delay Locked Loop
For Clock Management

Digital Clock Module in Xilinx FPGA

Clock Management

- Digital Clock Managers (DCMs)
  - Clock de-skew
  - Phase shifting
  - Clock multiplication
  - Clock division
  - Frequency synthesis