G.Bhuvaneshwari.
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EXPERIENCE SUMMARY

- Having 12yrs Experience in "PCB DESIGN".
- Good Knowledge in library development and schematic entry, placement
- Worked extensively in board placement and routing and Gerber generation.
- Experience in routing and Gerber checking and Library.
- QA experience in checking library footprints in IPC 7351 standard and library development.
- Good communication and interpersonal skills.

Presently working as a Design Manager Past from july13 to till date

PROFESSIONAL EXPERIENCE.

- Worked as a pcb trainee in B.E.L bangalore in 1998-1999
- Worked as a pcb designer in Alpha Imager Pvt Ltd 1999-2000
- Worked with D'gipro Systems Pvt Ltd from Mar 2000 to Aug 2004 as a Member CAD.
- Worked as a Design Engineer in CG-COREEL PROGRAMMABLE SOLUTIONS PVT LTD from sep1-2005 to june30-2006.
- Working as a design manager for Sierra Electrotech past from july-13-2006 to July-2008.
- Presently working for pro-cad solutions worked onsite for asmaitha wireless technology

Worked for DARE,DRDO,LRDE,BEL CRL and ISRO Projects also

TECHNICAL SKILLSETS

DESIGN TOOLS:

Allegro from cadence-Version 13.6 & 14.1,15.2
Cad star from Zuken-Redac-Version 4.5
Orcad from ORCAD-ver 9.0 For Schematic capture
Gerbtool (for gerber checking)
AutoCad.
View mate.
Expedition cell Editor.
PADS PCB spac1 and spac2 version 2005 and 2004.
Protel.

Spec liased in Allegro 15.2 to 15.6,Cadence 16.3,Cadstar6,Pads spac2 software.
IPC7351 standards of library creation.
CAM checking and Design QC Routing, Schematic updating and placement.
SI Anlaysis Knowledge.

EDUCATIONAL DETAILS:

Degree: Diploma in electronics and communication. (SRI Jaya chamarajendra Polytechnic)
School: S.S.L.C (B.E.L SCHOOL)

Major assignment

PROJECT#1 : SP-REV1 TO SP-REV6
CLIENT : L R D E
TOOL : Cadstar VER: 4.5
No. of Layers : 16 layers

Project Description

- Symbol creation. & schematic capture
- Shape creation, Board creation, Placement, Routing, CAM and Output generation.
- Board Complexity-8 layers 5k pins, Frequency of 40 Mhz, high Component & pin density with 204 pin Z-pack connectors Both
- Normal standard of 8 mill track & mil clearence for digital & high Reliability standards {12 mil track. 12 mil spacing} for Analog Signals used.
  The routing of back-plane PCB was a challenge as it involved the Routing of very high voltage analog signals along with other Analog & digital signals.

Project#2 : FD-BRD
Client : L&T
Tool Used : CADSTAR4.5
No of layers: 8

- Symbol creation & Schematic capture
- Shape creation, Board creation, Database creation, Placement, Routing, Graphic editing CAM, & Output generation.
- Board Complexity-6 Layers, 3k pins, 120 MHz freq design, high component & pin density with 169 pin UBGA (0.5mm pitch), 169 pin PGA socket, standard line technology of 8-mile track & 8-mile spacings.
- Board Challenge was to fit all components and routing complexity into the firm board size and # of layers. This was a controlled impudence board & hence the board had lot of routing constraints.
- The routing was a challenge as both differential pair as well as analog & Digital signals had to be routed.

Project#3 : ETX MODULE
Client : PG AUSTRALIA.
No of layers : 16
Design thru : ALLEGRO VER: 16.3

- Symbol creation & Schematic capture.
- Shape creation, Board creation, Database creation, Placement, Routing, Graphic editing, CAM & output generation.
- Board complexity-10 layer, pins, SODIMM CONNECTOR,DDR RAM, High Component and pin density with 360 pins, BGA 2nos,456 pins BGA 2nos,146 pins PQFP, Buffers and SMD Discrete.
- Board Challenge was to fit all components and routing complexity into the firm board size and # of layer.

Project#4 : NEXTBIT CPU
Client : NEXTBIT COMPUTER
No of Layers : 20 Layers
Design thru : CADENSE 16.3

- Symbol Creation & Schematic Capture.
- Shape Creation, Board Creation, Placement, Routing, Graphic editing CAM and Output Generation.
- Board Complexity-16 layers,2805 PINS, 20mhz frequency, High component

  & pin density with CON208BA AND SMD discretes.

- Board Challenge was to fit all components and routing complexity into the firm board size and # of layers.
- Routing should be done without vias.

Project #5 : RF CARDS.
Client : BELCRL)
NO of layers : 2 Layers.
Design Thru : ALLEGRO VER14.1

- Symbol creation & Schematic capture
- Shape creation, Board creation, Database creation, Placement, Routing, Graphic editing, CAM, & Output Generation.
- Board Complexity-10 Layers. 25MHZ AND 50 MHZk pins, Board Challenge was to fit all components and routing complexity into the firm board size and # of layers.

Handle as a lead team and also manager and also work for the target to reach.
This Card will work under high density and this card will work impedance control,
This card is routed differential pairs and length matching.
Bga 526pin
This card all the tracks should be minimum length and circuit flow (Processor to SDram and SDram to connectors)

The challenging tasks in this job are this card was routed within 15days with full length match.

Worked as a manager in Sierra Electrotech Managing all type of high speed boards, library creation schematic capture.
IPC library creation and cam checking

Worked On CPCI,PCI,VME, PCC, PMC, ETX CARD ALL TYPE OF CARDS.

Presently I am woking as a contract job for Greenmill International.

Projects taken as a librarian and CG-COREEL systems

All types of component were created in IPC7351 standard.
The components created or more then 700 with different footprint.
My work is Strong in Library Development and full flow of PCB design.

PERSONAL DETAILS

Name	:	G.BHUVANESHWARI.
Husband Name	:	K.MANJUNATH.
Father's Name	:	RAMESHA.
DATE OF BIRTH	:	10-07-1976.
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