RESUME

CHANDRASHEKAR

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Objective: Seeking a successful and satisfying career in VLSI Design and Embedded system domain, which will require me to apply my experience and education to make an immediate contribution to the organization and assist in the accomplishment of its goal.

Academic Details:

Level	Stream	Institute	Board/University	Passing Year	Percentage
M.Tech	VLSI Design & Embedded System	Nitte Meenakshi Institute of Technology Bangalore	VTU Belagavi	2016	64.79%
B.E	Electronics & Communication	Rao Bahadur Y Mahabaleswarappa Engg. College Ballari	VTU Belagavi	2014	64.56%
PUC	Science	R V independent PU college Yadgir	Board of Pre University Karnataka	2010	70.88%
SSLC	General	Govt. Junior High School Yadgir	Karnataka Secondary Education	2008	82.56%

Professional Experience: Internship

Company: EKUBE Design Solution Bangalore

Designation: Analog Circuit Design and PCB Designer

Duration: July 2015 to December 2015 (6 month)

Key responsibilities:

- Software Circuit designing and testing using LTSpice tool
- Controller Programming
- Hardware testing
- PCB designing (2 layer) using Cadence (OrCAD capture CIS, PSpice, Layout Plus)
- Analog circuit simulation

Course Completion

Course name: PCB design and VLSI front end design

Duration: January 2016 to May 2016 (5 months)

Institution: LIVEWIRE Yalahanka Bangalore

Technical skills

Software:

Operating System: Linux platforms (kernel Programming) and Windows (XP, Vista, 7 and 8).

RTOS: Free-RTOS.

Languages: C, Data Structure, Assembly language, Verilog, VHDL

IDEs: KEIL, CCSv5, Atmel-Studio, Win-AVR, STM-Cube, MATLAB, Eclipse

Protocols: UART, SPI, I2C, CAN, USB, RS-232/ 485 Bluetooth, TCP/IP, UDP/IP.

Technology: Linux kernel, Linux Device Drivers, RTOS, IoT.

PCB Software: PCB Layout Plus, Eagle.

Hardware:

Micro Controllers: 8051, 8086, Atmel‟s-AVR, ARM7, ARM Cortex M Series (M0, M3, M4,M7).

Robotics Motors and its drivers, Encoders, Sensors and Actuators

Key Skills:

- Team work
- Problem Solving
- Communicative
- Design and innovation

Personal Skills and Achievements:

- Good team leader, Quick learner and smart worker
- Flexible and creative thinking
- Got first place in District level Science exhibition competition during high school
- Participated in State level Science Exhibition competition held in Chikkamagaluru
- Participated in Taluka level Bharatha Sevadala Program.

Paper publication

Journal: Global Journal of Advanced Engineering Technology

Title: ADPLL Xilinx design and implementation for High frequency Transceiver Applications

Academic Project Details:

B.E Project

Title: Automated Library management system with fingerprint security system

Domain: Embedded system

Guide: Mrs. Anitha A

Brief Explanation: Our proposed model is done with the automatic thumb impression based login process to reduce the work of librarians. RFID cards are sticking on each and every book, this card contains different and unique ID numbers, and all the card numbers name of book and name of the author are pre entered in a system. Student who is borrowing books can entered into the library with the thumb attendance and speak the author name or book name from your android speaker or mike in the library the speaking voice sends the information to the RFID tag, this tag will search all racks of row and column wise. If the book is found we get a voice message like the book is found in this rack of this row and this column. Along with the smoke sensor will alert from the fire. The proposed project will save the time consuming and strict security from the thief.

MTECH Project

Title: ADPLL Design and Implementation for S Band Transceiver System

Domain: VLSI Design

Guide: Mrs. Varsha Prasad

Brief Explanation: This project deals with the system level design of ADPLL for the S band standard (2 – 4GHz). The architecture of ADPLL is presented with the functional illustration for each and every building block like TDC (Time to Digital Converter) and DCO (Digital Controlled Oscillator). The ADPLL system is modelled and described in Cadence using verilog. The performance of the system is analysed in Z domain. Design of ADPLL is to make the higher bit rate of data transformation greater than GSM. Proposed ADPLL design and implementation is a frequency synthesizer and it will generate the high frequency with the fast locking technology for the high speed communication and another advantage is to consume the low power as much as possible. The future enhancement of the design and implementation of ADPLL is tested for the fast phase locking and high frequency synthesis is to be done up to 20MHz frequency range.

Mini Project

Title: MEMS Accelerometer sensor Design and Parameters analysis

Domain: Microelectronics and Nano materials (MEMS)

Guide: Prof. Veda S.N

Brief Explanation: An accelerometer is a sensor that measures the physical acceleration experienced by an object due to inertial forces or due to mechanical excitation. In aerospace applications accelerometers are used along with gyroscopes for navigation guidance and flight control. Conceptually, an accelerometer behaves as a damped mass on a spring. When the accelerometer experiences acceleration, the mass is displaced and the displacement is then measured to give the acceleration. They are unmatched in terms of their upper frequency range, low packaged weight and high temperature range. Capacitive accelerometers performance is superior in low frequency range and they can be operated in servo mode to achieve high stability and linearity.

Personal Details:

Fathers Name:	Jagadish
Mothers Name:	Ningamma
Nationality:	Indian
Marital Status:	Single
Date of Birth:	26th January 1993
Languages known:	Kannada, English, Hindi & Telugu
Address:	C/O Dist. Health & FW Office Kanaka Nagar Yadgiri Dist: Yadgiri Pin: 585201

Declaration:

I assure that the information furnished above is true and correct to the best of my knowledge.

Date: Yours Faithfully,

Place: Bangalore [*CHANDRASHEKAR*]