ROHITH BALAKRISHNAN

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Objective

To pursue a challenging and rewarding career in VLSI design where I can utilize my knowledge and skills for the success and growth of the organization.

Educational Qualification

Qualification	Institute	Board/university	CGPA/percentage	Year of passing
B.Tech (Electronics and communication)	MES College of Engineering, Kuttippuram	Calicut University	7.00	2014
AISSCE	Bharatiya Vidya Bhavan,Kannur	CBSE	90.8	2009
AISSE	Nithyananda Bhavan English Medium School,Kannur	CBSE	93.2	2007

Experience

VLSI Design Engineer at Silica Tech, Kochi (January 2015-Present)

As a VLSI Designer I was working mainly on RTL development and its verification using Verilog HDL and its FPGA implementation.

Technical Skills

- Digital Design
- FPGA based system design
- Verilog
- System Verilog
- Universal Verification Methodology (UVM)
- EDA tools Xilinx ISE and Questasim

Additional Qualification

1. **Advanced VLSI Design and Verification** training from **Maven Silicon**, Bangalore
2. Sound knowledge of FPGA design and implementation.
3. Experience in writing RTL models in Verilog HDL and Test benches in System Verilog and UVM (Universal Verification Methodology).
4. Good knowledge of ASIC/FPGA front-end Design and Verification, RTL Coding, FSM based design, Simulation and Synthesis.

Projects Undertaken

VLSI Design Projects:

- **Physical Coding Sublayer (Gigabit Ethernet)**

  The PCS is the Gigabit Media Independent Interface (GMII) that provides a uniform interface to the Reconcillation Sublayer. Designed the Physical coding Sublayer (Gigabit Ethernet) and verified the same by creating a test bench using Verilog HDL and synthesized the design. Xilinx ISE was used.
- **Tiny Encryption Algorithm (TEA)**

  It is a cryptographic algorithm based on Fiestel Iteration which uses large number of rounds to get security with simplicity.It can be translated into different languages and assembly languages easily and is safe due to length of key and number of rounds in the encoding. It was designed in Verilog and implemented in Spartan-6 FPGA.
- **JPEG image compression using 2D-DCT,quantization and zigzag process using Verilog HDL**

  This paper presents the Verilog design of a Two Dimensional Discrete Cosine Transform (2D-DCT) with quantization and zigzag arrangement. This design is used as the core and path in JPEG image compression hardware. Implemented in Spartan-6 FPGA.
- **Improved matrix multiplier design for high speed digital signal processing applications**

  An improved matrix multiplication method for high speed digital signal processing applications based on matrix element transformation and multiplication. The code was designed in Verilog and implemented in Spartan 6 FPGA.
- **Elliptic curve cryptography**

  This is a very efficient cryptographic algorithm that reduces memory so much suitable in wireless devices where size is always a constraint. This algorithm provides the same security like other algorithms but with reduced key size. This was implemented in Verilog HDL.
- **Router 1x3 –RTL design and Verification**

  The router accepts data packets on a single 8-bit port and routes them to one of the three output channels, channel0, channel1 and channel2. Implemented RTL using Verilog HDL. Architected the class based verification environment using UVM. Generated code coverage for the RTL verification and synthesized the design. Questasim and ISE were the EDA tools used.

VLSI Verification Projects:

- **GPIO IP Core Verification**

  The GPIO IP Core is a user programmable general purpose I/O controller, which is used to implement functions that are not implemented with dedicated controllers in the system. It was verified by creating a class based verification model using UVM. Generated functional coverage for the RTL verification.

Achievements

- School topper of Nithyananda Bhavan English Medium School in AISSE 2007.
- Chemistry topper of Bharatiya Vidya Bhavan, Kannur in AISSCE 2009.
- Represented MES College of Engineering, Kuttippuram in All Kerala Inter collegiate energy quiz conducted by Bharat Petroleum in January 2014.

Personal Information

Age and date of birth	: 23, 26 November 1991
Gender	: Male
Languages Known	: English, Malayalam and Hindi