**CURRICULUM VITAE**

**R. SIVAKUMAR,**

27, S4, II-Floor, 7 th cross St, 1 st main Road, Maruthi Nagar,

BTM Layout 1 st stage, **Madiwala, Bangalore** - 560068.

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**OBJECTIVE**

To obtain a position in your organization, where all my skills and knowledge can be utilized to the organization growth and also myself.

**EXPERIENCE**

**5 years** in **VLSI** Cutting edge technologies - **Digital chip design and verification**, **9 months** in **International Customer Support** (E-Mail support agent), **3+ years** in **HTML/CSS** as **UI/Frontend/Web developer.**

**EDUCATIONAL BACKGROUND**

|  |  |  |  |
| --- | --- | --- | --- |
| **CLASS** | **INSTITUTION** | **YEAR** | **SCORE** |
| B.E.,(ECE) | PSR Engg College, Sivakasi (Anna University, Chennai) | 2006 | 85.0% |
| HSC | 36 GST Hr Sec School, SNKL | 2002 | 93.5% |
| SSLC | 36 GST Hr Sec School, SNKL | 2000 | 87.6% |

**CAREER SYNOPSIS**

|  |  |  |
| --- | --- | --- |
| **Company** | **Period** | **Designation** |
| Freelancer Projects, Bangalore | Apr’2013 - Till now | UI/FrontEnd Developer |
| Sutherland Global Services, Chennai | Jun’2012 – Feb’2013 | Associate |
| Wipro Technologies Pvt Ltd, Cochin | Dec’2010 - Feb’2012 | Senior Project Engineer |
| Arasan Technologies, Tuticorin | Sep’2006 – Jun’2010 | Associate |

**SKILLSET**

1. Language : **HTML, CSS, JQUERY, JAVASCRIPT, ObjectiveC, VERILOG**, **VHDL**
2. Tools : **XCODE, MODELSIM**, **CADENCE, PSPICE, MULTISIM**

3 Protocols : **SD**, **eMMC**, **MIPI - CSI**, **DSI** & **AMBA - AHB**

**PROJECTS, ROLES AND RESPONSIBILITIES IN THE COMPANIES SERVED**

**1.** **Through Freelancer Projects, Bangalore**

Duration : **Apr’2013-Present** Team size : **3**

Projects : **faithcallcenter.com, okapia-mobile.com, ypaycash.com, gocarwash.in, zomint.com, trifectaprojects.com, directadmissioninallianceuniversity.com,..**

**Description** : **UI/FrontEnd/Web** Development using HTML/CSS/ Wordpress/JS for the sites using Photoshop file with responsive/I phone application.

**Responsibility** :

* Developed the front-end web page by using HTML5, CSS3, and JavaScript.
* Estimated time to develop for all approved prototypes and the implementation of those prototypes using jQuery and CSS as well as showing to project leads and receiving and implementing any changes or implementation updates
* Working with browsers compatibility issues,
* Responsible for creating the JavaScript code, for different modules.
* From the designed file, implemented and maintained web content portals for the company’s web pages/systems
* Helped establish templates for coding design comps mockups and wireframes, Instrumental in the design of the company’s QA process and quality standards

**2.** **in Sutherland Global Services, Chennai**

Client: **Amazon.com**

Duration: **9 Months (June’2012 – February’2013)**

Position: **Customer Support** **Executive (E-Mail)**

**Responsibility** :E-Mail support for the US customers of Amazon.com regarding their delivery issues (not received at all, received in the time not assured), Product condition issues (received defect, damage products). Should take necessary action like replacing the order placed or refund the money of the order as they asked or per situation.

**3. in Wipro Technologies Pvt Ltd, Cochin**

**a.** Name : **DM385** Duration : **6 Months (January 2011 – May 2011)**

Team size : **6** Position : **Team Member (Verification Engineer)**

**Description :** DM385 is a Multimedia Application Processor Platform based on Centaurus IP.

**Environment :** Sun Solaris, Cadence VCS.

**Responsibility :** Test case verification in system C.

**b.** Name : **DDR PHY Interface Design**

Duration : **6 Months (June 2011 – December 2011)** Team size : **6,**

**Description :** The DDR PHY Interface (DFI) is an interface protocol that defines the connectivity between a DDR memory controller (MC) and a DDR physical interface (PHY).

**Environment :** Sun Solaris, Cadence VCS.

**Responsibility :** Developed Memory controller model in VERILOG.

**4. in Arasan Technologies Pvt Ltd, Tuticorin**

**a.** Name: **MIPI Alliance standard for Camera & Display Serial Interfaces (CSI & DSI)**

Duration : **12 Months (Sept 2007 – August 2008)** Clients : **Intel & Quick Logic** Team size : **6, P**osition : **Team Member (Verification Engineer)**

**Description :** The MIPI (Mobile Industry Processor Interface) alliance standard for Camera & Display Serial Interfaces (CSI & DSI) provides a standard, robust, scalable, low-power, high-speed, cost-effective serial interface between the peripheral devices (Camera & Display) and a host processor.

**Environment :** Windows XP, Modelsim

**Responsibility :** Developed test cases in VERILOG and verified RTL.

**b.** Name : **UART with Local & Asynchronous Bus Interface**

Duration : **2 Months (Sept’2008 – October 2008)** Client : **Internal**

Team size : **2,** Position : **Team Member (Verification Engineer)**

**Description :** TheUART (Universal Asynchronous Receiver/Transmitter) with local & asynchronous bus interface provides a standard interface between the local & asynchronous bus processor and a peripheral device or MODEM.

**Environment :** Windows XP, Modelsim

**Responsibility :** Written Local/asynchronous bus model blocks in VERILOG and verified RTL.

**c.** Name : **SMIA CCP2 Transmitter and Receiver**

Duration : **6 Months (Nov’ 2008 - May 2009)** Client : **NEC**

Team size : **10,** Position : **Team Member (Verification Engineer)**

**Description :** TheSMIA CCP2 (Standard Mobile Imaging Architecture - Compact Camera Port) provides a universal standard interface between a digital camera module and a mobile phone engine. It is a development version of current camera interface (CCP).

**Environment :** Windows XP, Modelsim

**Responsibility :** Written Microcontroller model in VERILOG.

**d.** Name : **Arasan’s SD/eMMC Device with AHB**

Duration : **12 Months (Jun 2009 – May 2010)** Clients : **SD, Densbits**

Team size : **10,** Position : **Team Member (Verification Engineer)**

**Description :** The core is fully tested to meet the requirements of the Multimedia Card (MMC) system specification version 4.4 and the SD physical layer specification 1.01 & 2.0.

**Environment :** Windows XP, Modelsim

**Responsibility :** AHB Master and Target models in VERILOG.

**PERSONAL INFORMATION**

Father’s Name : **P. Ramasubbu (Late)**

Age and Date of Birth : **31 (April - 17, 1985)**

Marital status : **Single**

Languages known : **Tamil & English**

Pass Port : **F9729523**

PAN Card : **BNEPS0393E**

**Present Address** : 27, S4, II-Floor, 7 th cross St, 1 st main Road, Maruthi Nagar,

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Tirunelveli District, Tamilnadu, India.

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**DECLARATION**

Given information’s are true to the best of my knowledge & belief.

Yours faithfully,

sign

**(R.SIVAKUMAR)**