



East West University
Department of Computer Science and Engineering

Course: CSE345 Digital Logic Design

Expt No.: 2

Title: Design and Implementation of a Combinational Circuit

Objectives:

1. To design a combinational circuit from descriptive problem specification.
2. To implement a combinational circuit using AND-OR and OR-AND logic.

Theory:

The design procedure of a combinational circuit is discussed in Section 6.2 of Textbook 1. Students are advised to go through the above section of the Textbook 1 before preparing the pre-lab report.

Pre-Lab Report Questions:

Problem specification: In a combinational logic circuit, four input lines A , B , C , and D are being used to represent a 4-bit binary number with A as the MSB and D as the LSB. The circuit produces a high (logic 1) output only when the binary number is greater than 0101_2 .

1. Prepare a truth table for the given combinational circuit. Represent the truth table in a 4-variable K-map.
2. Write simplified sum of products function from the K-map. Draw the AND-OR logic diagram for the simplified sum of products function.
3. Write simplified product of sums function from the K-map. Draw OR-AND logic diagram for the simplified product of sums function.

ICs Required:

7408 Quadruple 2-input AND gates

7432 Quadruple 2-input OR gates

Pin Diagram of the Required ICs:

1	1A	V_{CC}	14	1	1A	V_{CC}	14
2	1B	4B	13	2	1B	4B	13
3	1Y	4A	12	3	1Y	4A	12
4	2A	4Y	11	4	2A	4Y	11
5	2B	3B	10	5	2B	3B	10
6	2Y	3A	9	6	2Y	3A	9
7	GND	3Y	8	7	GND	3Y	8
7408 (4 2-In AND)				7432 (4 2-In OR)			

Lab Procedure:

1. Construct two logic diagrams from your pre-lab report on a digital logic trainer individually. For each logic circuit, connect four inputs to four data switches and the output to a LED indicator. Construct truth table for each logic circuit.

Post-Lab Report Questions:

1. Verify that two truth tables obtained in your lab work agree with the truth table prepared in your pre-lab report.
2. Write structural Verilog code for two logic circuits from your pre-lab report and simulate them using Quartus II software.