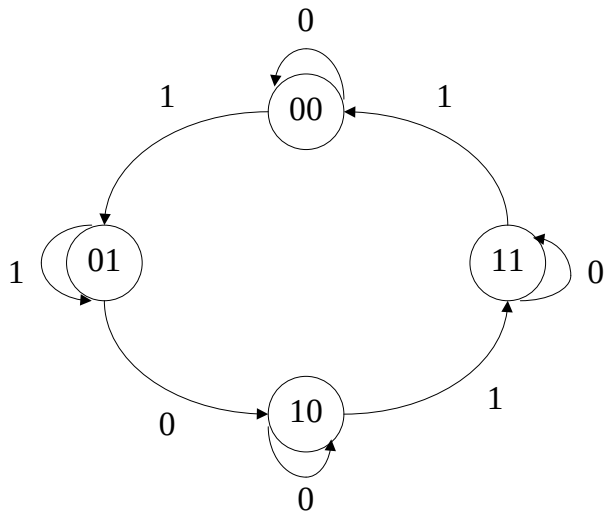
Chapter 10
Sequential Logic Design

Design



Design the sequential circuit using J-K Flip-Flop

Q_nQ_{n+1}	J_nK_n
0 0	0 X
0 1	1 X
1 0	X 1
1 1	X 0

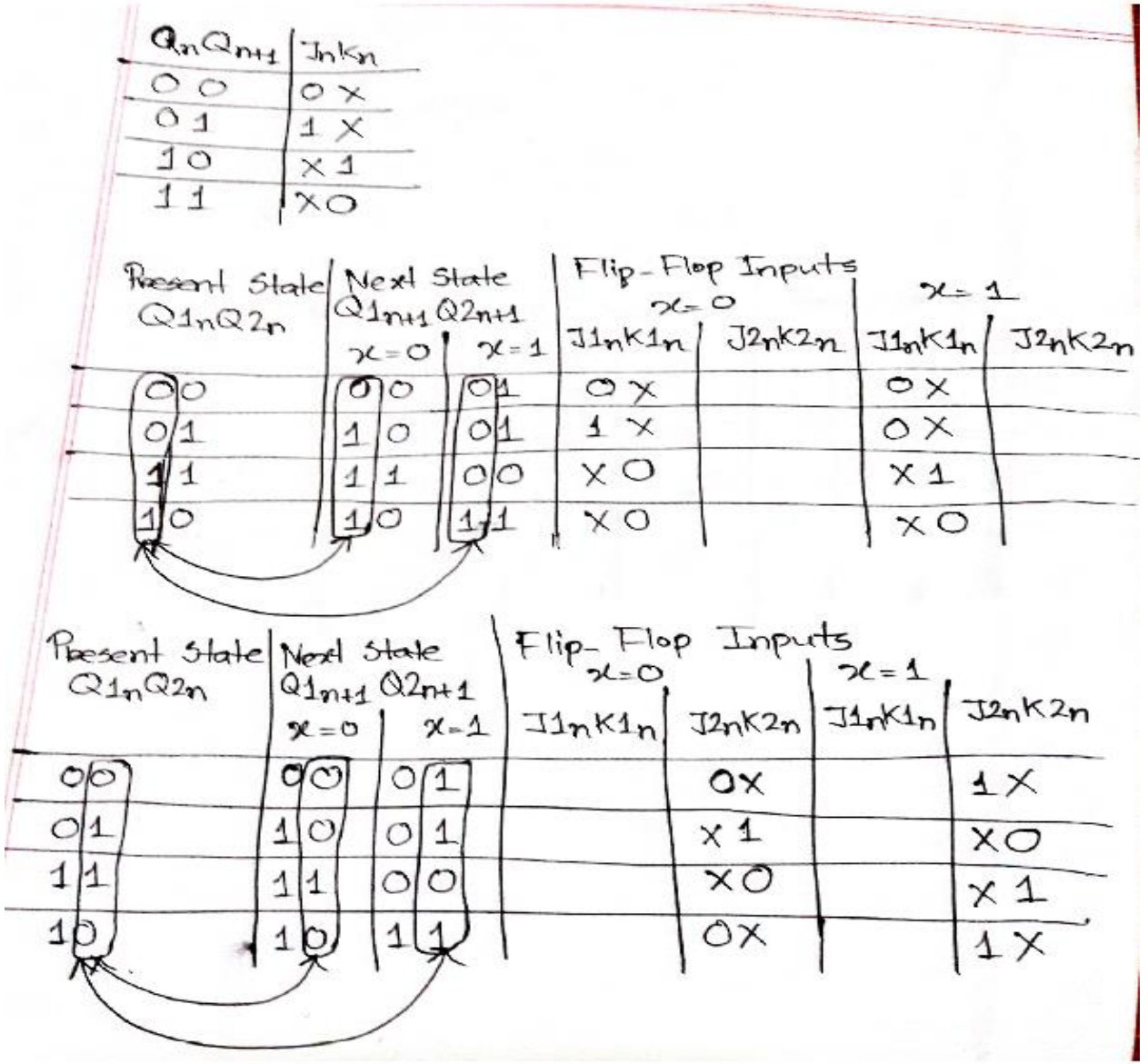
Present State	Next State		Flip-Flop Inputs			
			$x=0$		$x=1$	
$Q1_nQ2_n$	$Q1_{n+1}$ $x=0$	$Q2_{n+1}$ $x=1$	$J1_nK1_n$	$J2_nK2_n$	$J1_nK1_n$	$J2_nK2_n$
0 0	0 0	0 1	0 X			
0 1	1 0	0 1	1 X			
1 1	1 1	0 0	X 0			
1 0	1 0	1 1	X 0			

Design (Contd.)

Q_nQ_{n+1}	J_nK_n
0 0	0 x
0 1	1 x
1 0	x 1
1 1	x 0

Present State	Next State		Flip-Flop Inputs			
			$x=0$		$x=1$	
$Q1_nQ2_n$	$Q1_{n+1}$ $x=0$	$Q2_{n+1}$ $x=1$	$J1_nK1_n$	$J2_nK2_n$	$J1_nK1_n$	$J2_nK2_n$
0 0	0 0	0 1	0 x		0 x	
0 1	1 0	0 1	1 x		0 x	
1 1	1 1	0 0	x 0		x 1	
1 0	1 0	1 1	x 0		x 0	

Design (Contd.)



Q_nQ_{n+1}	J_nK_n
0 0	0 X
0 1	1 X
1 0	X 1
1 1	X 0

Present State Q_1nQ_2n	Next State $Q_{1n+1}Q_{2n+1}$ x=0	Next State $Q_{1n+1}Q_{2n+1}$ x=1	Flip-Flop Inputs x=0 J_1nK_1n	Flip-Flop Inputs x=0 J_2nK_2n	Flip-Flop Inputs x=1 J_1nK_1n	Flip-Flop Inputs x=1 J_2nK_2n
0 0	0 0	0 1	0 X		0 X	
0 1	1 0	0 1	1 X		0 X	
1 1	1 1	0 0	X 0		X 1	
1 0	1 0	1 1	X 0		X 0	

Present State Q_1nQ_2n	Next State $Q_{1n+1}Q_{2n+1}$ x=0	Next State $Q_{1n+1}Q_{2n+1}$ x=1	Flip-Flop Inputs x=0 J_1nK_1n	Flip-Flop Inputs x=0 J_2nK_2n	Flip-Flop Inputs x=1 J_1nK_1n	Flip-Flop Inputs x=1 J_2nK_2n
0 0	0 0	0 1		0X		1X
0 1	1 0	0 1		X 1		X0
1 1	1 1	0 0		X0		X 1
1 0	1 0	1 1		0X		1X

Present State $Q1_nQ2_n$	Next State $Q1_{n+1}Q2_{n+1}$		Flip-Flop Inputs			
			$x=0$		$x=1$	
	$x=0$	$x=1$	$J1_nK1_n$	$J2_nK2_n$	$J1_nK1_n$	$J2_nK2_n$
00	00	01	0X	0X	0X	1X
01	10	01	1X	X1	0X	X0
11	11	00	X0	X0	X1	X1
10	10	11	X0	0X	X0	1X

$J1_n$:

$Q1_nQ2_n$ \ x	0	1
00	0	0
01	1	0
11	X	X
10	X	X

$J1_n = Q2_nx'$

$K1_n$:

$Q1_nQ2_n$ \ x	0	1
00	X	X
01	X	X
11	0	1
10	0	0

$K1_n = Q2_nx$

$J2_n$:

$Q1_nQ2_n$ \ x	0	1
00	0	1
01	X	X
11	X	X
10	0	1

$J2_n = x$

$K2_n$:

$Q1_nQ2_n$ \ x	0	1
00	X	X
01	1	0
11	0	1
10	X	X

$K2_n = Q1_n'x' + Q1_nx$

$Q1_n$ \ $Q2_nx$	00	01	11	10
0				1
1	x	x	x	x

$J1_n = Q2_nx'$

$Q1_n$ \ $Q2_nx$	00	01	11	10
0	x	x	x	x
1			1	

$K1_n = Q2_nx$

$Q1_n$ \ $Q2_nx$	00	01	11	10
0		1	x	x
1		1	x	x

$J2_n = x$

$Q1_n$ \ $Q2_nx$	00	01	11	10
0	x	x		1
1	x	x	1	

$K2_n = Q1_n'x' + Q1_nx$

Design (Contd.)

$Q1_n$ \ $Q2_n x$	00	01	11	10
0				1
1	x	x	x	x

$J1_n = Q2_n x'$

$Q1_n$ \ $Q2_n x$	00	01	11	10
0	x	x	x	x
1			1	

$K1_n = Q2_n x$

$Q1_n$ \ $Q2_n x$	00	01	11	10
0		1	x	x
1		1	x	x

$J2_n = x$

$Q1_n$ \ $Q2_n x$	00	01	11	10
0	x	x		1
1	x	x	1	

$K2_n = Q1'_n x' + Q1_n x$

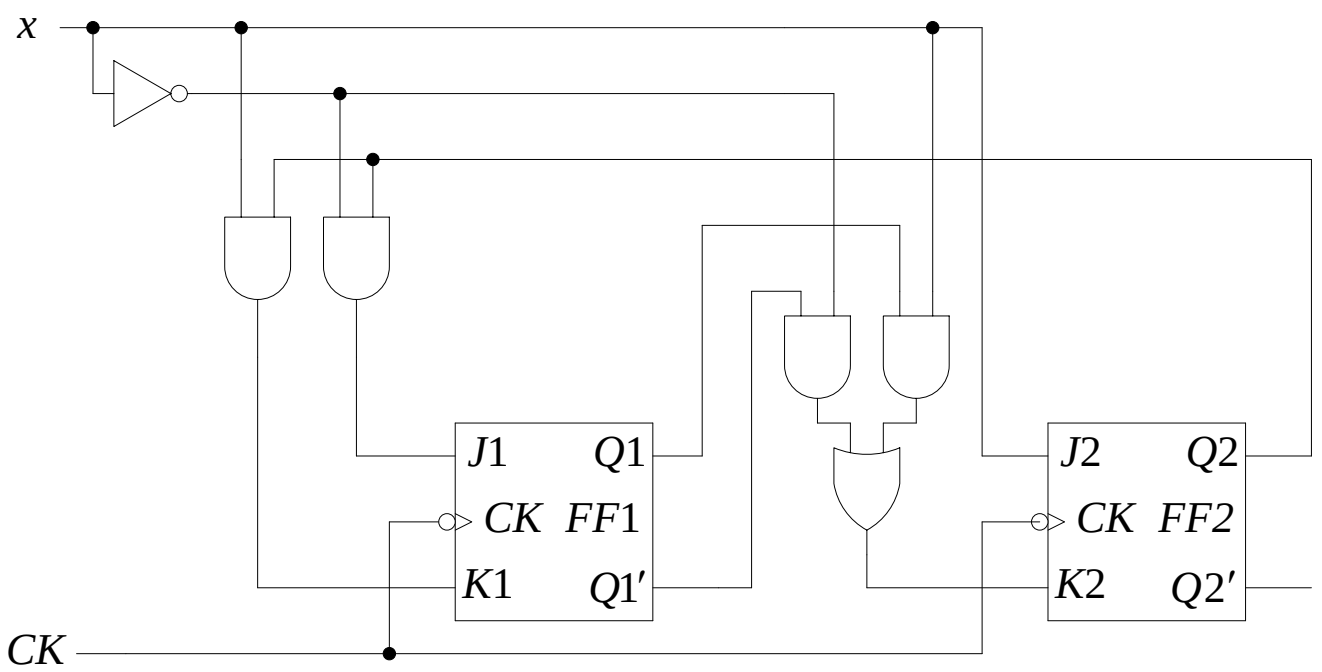
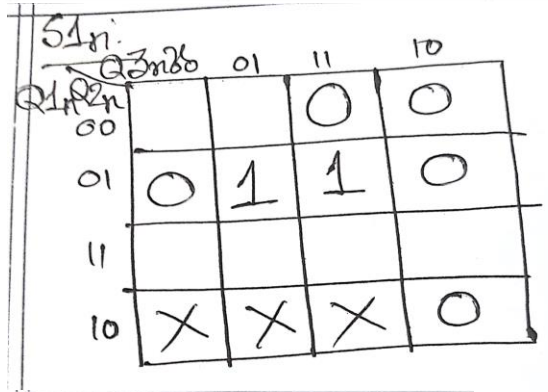
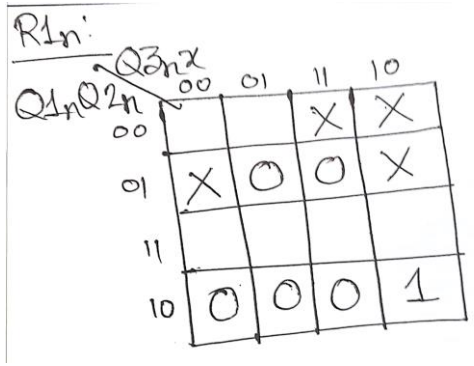
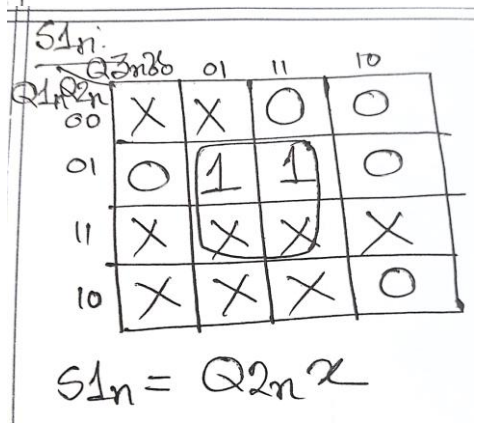


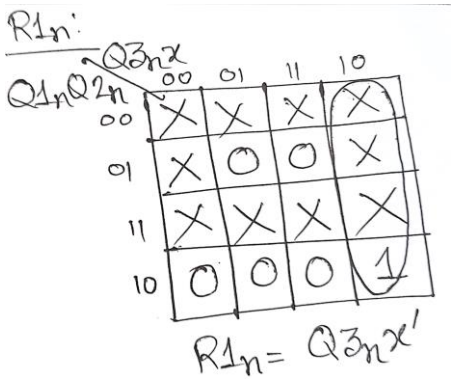
Table 10.13 Excitation for the sequential circuit specified by the state table of Table 10.4.

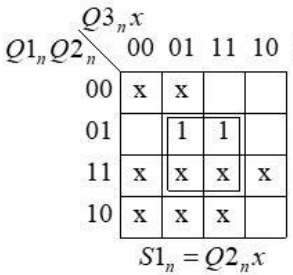
Present state $Q1_nQ2_nQ3_n$	Next state $Q1_{n+1}Q2_{n+1}Q3_{n+1}$		Flip-flop inputs						Output z	
			$x=0$			$x=1$			Input x	
	$x=0$	$x=1$	$S1_nR1_n$	$S2_nR2_n$	$S3_nR3_n$	$S1_nR1_n$	$S2_nR2_n$	$S3_nR3_n$	0	1
001	001	010	0x	0x	x0	0x	10	01	0	0
010	011	100	0x	x0	10	10	01	0x	0	0
011	001	100	0x	01	x0	10	01	01	0	0
100	101	100	x0	0x	10	x0	0x	0x	0	1
101	001	100	01	0x	x0	x0	0x	01	0	1

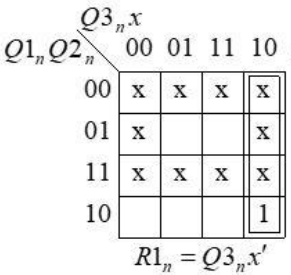


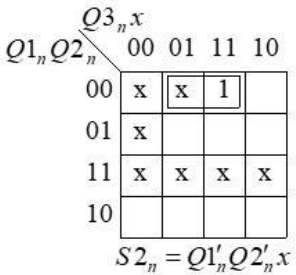


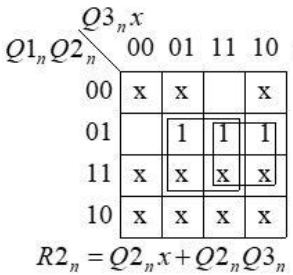


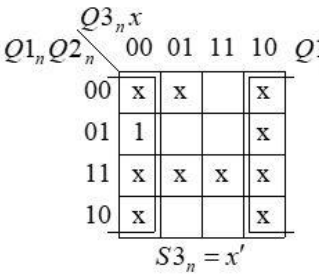


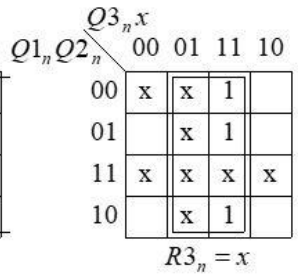


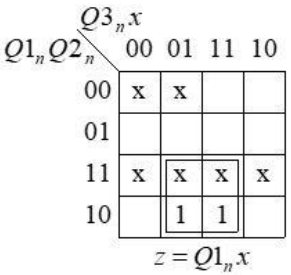












$$S1_n = Q2_n x$$
$$R1_n = Q3_n x'$$
$$S2_n = Q1'_n Q2'_n x$$
$$R2_n = Q2_n x + Q2_n Q3_n$$
$$S3_n = x'$$
$$R3_n = x$$
$$z = Q1_n x$$

Step 7. The logic diagram is shown in Figure 10.10.