EAST WEST UNIVERSITY

Department of Computer Science and Engineering
Fall 2021 Semester
CSE345 Digital Logic Design, Section-3
Lab Exam
Marks:7
Time: 25 minutes (Including Submission)

Submit Verilog code and Simulation Waveform.

Last Digit 0/5:

Write a Procedural Verilog description using case statement for the following Boolean function

$$F(A,B,C,D) = (A + B')(C + D')A'$$

Last Digit 1/6:

Write a Procedural Verilog description using case statement for the following Boolean function

$$F(A,B,C,D) = \sum(1,5,7,8,13,14) + \sum_{d.c.}(0,4,9,15)$$

Last Digit 2/7:

Write a Procedural Verilog description using case statement for the following Boolean function

$$F(A,B,C,D) = \prod(2,3,7,10,13,15) \cdot \prod_{d.c.}(1,6,9,12)$$

Last Digit 3/8:

Write a Procedural Verilog description using if statement for implementing a 2×4 Decoder with active-LOW Enable input and active-HIGH outputs.

Last Digit 4/9:

Write a Procedural Verilog description using if statement for implementing a 2×4 Decoder with active-HIGH Enable input and active-LOW outputs.