12 December, 2021

EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Mid Term II Examination, Fall 2021 Semester

Course:	**CSE 345 Digital Logic Design, Section-3**
Instructor:	**Musharrat Khan, Senior Lecturer, CSE Department**
Full Marks:	**40 (20 will be counted for final grading)**
Time:	**1 Hour and 25 Minutes (Including Submission)**

Note: There are SIX questions, answer ALL of them. Course Outcome (CO), Cognitive Level and Mark of each question are mentioned at the right margin.

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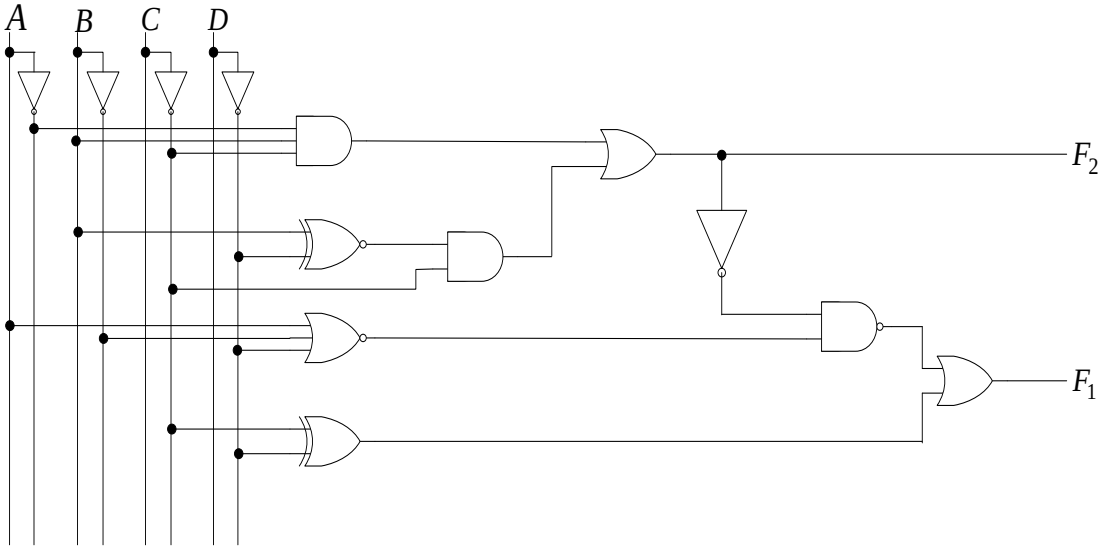
1. Consider that $ABCD$ is a 4-bit input and F is a 1-bit output of a combinational circuit. The output is $F = 1$ for both case 1 and case 2:
Case 1: When only A and C are 1
Case 2: When only B and D are 1
Design the combinational circuit. [CO3,C3, EP1,EP2, Mark: 6]

2. **Analyze** the following circuit by constructing truth table of the outputs. [CO2,C4, EP1, Mark: 8]



3. **Design** a full-adder using only AND, and OR gates. [Draw block diagram, construct truth table, determine Boolean equations of outputs, and draw logic diagram] [CO3,C3, Mark: 6]

4. **Design** a 10×4 Encoder for active-LOW inputs. [Draw block diagram, construct truth table, determine Boolean equations of outputs, and draw logic diagram] [CO3,C6, Mark: 6]

5. Given that only 8×1 MUXs are available. Design a 24×1 MUX using necessary number of 8×1 MUXs. [Properly label all inputs and outputs] [CO3,C6, EP1,EP2, Mark: 6]

6. **Write** a Procedural Verilog description using case statement for implementing a 4×1 MUX with active-LOW Enable input. [CO3,C6, EP1,EP2, Mark: 8]