



EAST WEST UNIVERSITY

Department of Computer Science and Engineering

B.Sc. in Computer Science and Engineering Program

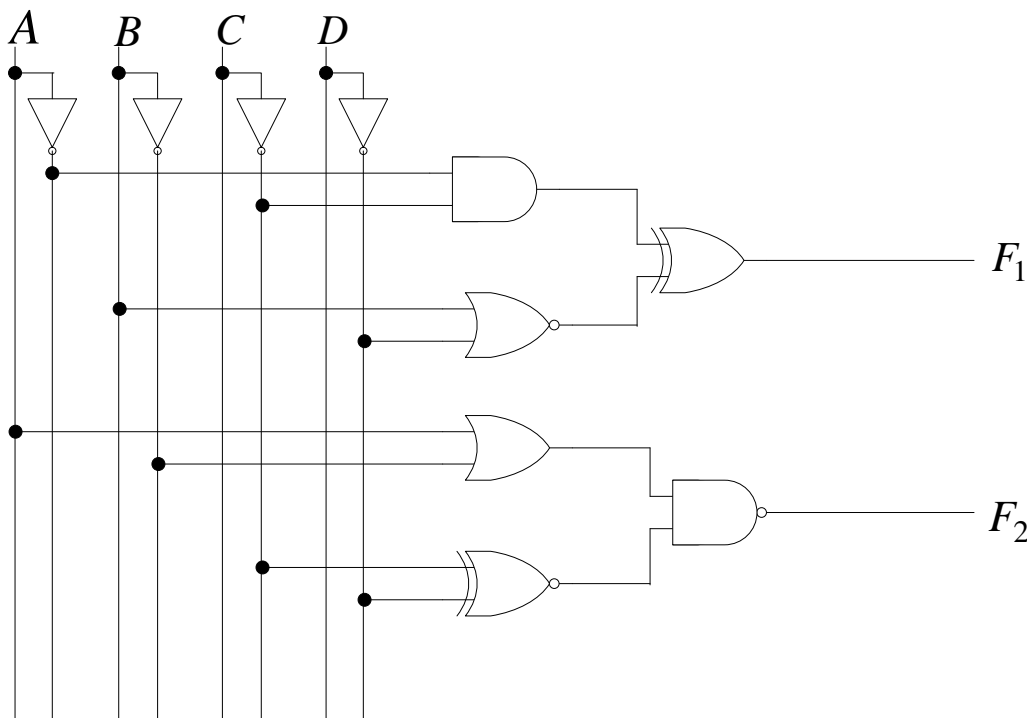
Mid Term II Examination, Summer 2021 Semester

Course: CSE 345 Digital Logic Design, Section-2
Instructor: Musharrat Khan, Senior Lecturer, CSE Department
Full Marks: 40 (20 will be counted for final grading)
Time: 1 Hour and 30 Minutes (Including Submission)

Note: There are SIX questions, answer ALL of them. Course Outcome (CO), Cognitive Level and Mark of each question are mentioned at the right margin.

1. Consider that $ABCD$ are 4-bit inputs and X is 1-bit output of a combinational circuit. The output is $X = 1$ if at least two of BCD are 0; otherwise $X = 0$. **Design** the combinational circuit. [CO3,C3, Mark: 6]

2. **Analyze** the following circuit by constructing truth table of the outputs. [CO2,C4, Mark: 8]



3. **Design** a full-adder using only AND, EXOR, and OR gates. [Draw block diagram, construct truth table, determine Boolean equations of outputs, and draw logic diagram] [CO3,C3, Mark: 6]
4. **Design** a 10×4 Encoder for active-HIGH input. [Draw block diagram, construct truth table, determine Boolean equations of outputs, and draw logic diagram] [CO3,C6, Mark: 6]

5. **Construct** a combinational circuit using an 8×1 MUX for implementing the following Boolean function. [Properly label all the inputs and outputs] [CO3,C6, Mark: 6]

$$F(A, B, C, D) = \prod (2, 5, 7, 9, 10, 12, 15)$$

6. **Write** a behavioral Verilog code to design the following Boolean function using Procedural technique using case statement. [CO3,C6, Mark: 8]

$$F(A, B, C, D) = BD' + B' + AC'$$