Reg Write Read ALUMUX Write ALUOP Reg MUX Broanch

O 0 1 (Linn) 1 ADD X

ALUMUX is the control signal that controls mux at the ALV input, O (Reg) selects the autput of the register bile, and 1 (Imm) select the immediate brom the instruction word as the second input to the ALV.

RegMux is the contral signal that controls the Mux at the Data input to the register bile. O (ALV) At selects the ordered of the ALV. and I (mem) relects the output of memory.

the new Pe, and MUX to select that value This instruction uses instruction memory both register read ports, the ALV to add Rd and Rs together, data memory and write port in Registers.

None, This instruction can be implemented using the existing blocks. latencies:

2905 + 2906 + 2906 + 29005 + 2005

The latency of this path is 400 ps + 200 ps + 200 ps +120 PS + 850 PS + 30 PS

= 1130 PS

1430 ps (1130ps + 300 ps, IALUsippon the critical puth).

lime is 1430! instead of 1130.

ALVATIVE in the control of the cutput of the register of the register of the resident of the register of the resident of the resident of the means actually have could show down. The instruction word as the record input to the ALV.

Regmux is the control signal that controls the muse

4.4 The critical path for this instruction is through the instruction memory, Sign - extend and shift left-2. to get the obt set, Add unit to compute

the new PC. and MUX to select that value

This instruction uses journal we will be and be together duta

The ad equation to add Rd and Re together duta

The ad equation of the point in Registers.

The path through Pesna is longer bore these latencies:

200 Pg + 90 PS + 20 PS + 90 PS + 20 PS

The lutency of this path is 400ps + 2087 693 70ps + 120 ps + 30ps

= 1130 PS

The data memory is used by Lw and Sw instructions so the answer is: (25% + 10%)

The pign - extend circovit is actually computing a result in every cycle, but its output is ignored bor ADD and NOT instructions. So the answer is:

All as south stand hours and many or stand in the destroyers the destroyers the formation the destroyers and instruction the less to form this boult size need can instruction who se instruction the land instruction the land instruction the Reg Dest signal is "don't care" because it doesn't write to any registers, so the implementation while to any registers, so the implementation and so or may not allow must be retired to o and so set born the down to be instruction.

ALU OP [1-0]	Instruction [5-6]	memera	deta	The
00	010100	2100 (VUD)	Ahe	ر و

MEM/ Wo Reg Mux ALU MUX ALU MUX Branch MUX Jump MUX 2010 (Reg Ost) 20 chep pre pro ontere is iduated for you

and NOT instructions so the answere is:

We already computed clock cycle times bore pipelined single cycle organizations. and the multi-cycle organization has the same clock rate time as the pipelined organization. We will compute execution time relative to the pipe lined organization.

In single - eyele every instruction take one (long)

Clock eyele.

white to any neglishers, so the implementation

of Multi-cycle execution walls single eyele execution time is x times pipelined execution time, where time is x times pipe - lined execution thime, when 0.20×5 + 0.80× 4 = 4.20

1250 63 / 350 65 = 3 87

200 PS (IF)

4.5				911
Instruction sec	juence		Dependences	
I1: OR RI, RR,	R3 (RAW OR	RI brom II	to I2
IS: OK KS KI	JARAM R	RAW on	Ra brom 1214	DISI
23: OR RI, RI.	R2 1 V		RR brom I1 to	
ID Ex MEM WE	** * \		R1 brom I'e.	l
F ID 4 F & MEM			R1 bnom 11 A	
			(120) 0 (12	
			RI, O(RI)	
.9.2			4007 'ND 18	D-10
OR R1, R2, R3				-
NOP	Delay	I2 to	avoid RAW has	zavid
NOP 1	1 or	n RI B	nom 11	21
NOP ANTRONS NOP OR RI, RI, dRe of OR RI, RI, dRe	inem in	te I sh	dences to t	negen
stall is algore	Delay	puls xpc	avoid RAW h	azand
bad NOP dead- of	on	R2 bro	m 12	- 20 00
OR RI, RI, RE		1	3.3 3.7	<u></u> 2
nce to the end	ependen	0 . 4013	ext instruc	n puz
one stall eyele.	in c	beorle	instruction	next
10				We !
			cycle with	
Instruction executed (Zycle with	5 stages	4 stages	speedup
5	4+5=	9	3+5=8	9/8=1.13
' एउ छोट्टे '।	10756		149	
	5 46°%	8.1=12	0.35×2 +0.15	
Cycle time	Cye	ele time	3	
with 5 stages	with	a stage	9p	eedup
			100	2//0 × 2/2

210 PS (MEM +20PS)

(0x200)/(8x210)

= 1.07

Dependences	motivetica actionical
LW DRIJ O (RI) 18 -10 WB	II OR RIRGIRE
LW RISION(RI) 29 110 6×19	
BER RITRONLOOP no IDIW	* * * GX MEM WB
LW of RICORDA no IFW.	* ** ID EX MEM WB
WAR ON RISAWISI (1 & DIA	IF ID ** * EX MEM
LW RI, O(R)	
LW RI, O(RI)	
BLA RI, RO, LOOP	

Delay . Is to avoid RAW hazard

OR RI, RZ, R3

Dependences to the 1st next instruction result in 2 stall eycles and the stall is also 2 cycles it the dependence is to sooth 1st and 2nd next instruction. Dependences to the 2nd

next instruction result in one stall eyele.

We have:

agele with historion executed eyel with 5 stages 4 istages Spredup Stall Cycles 19/8=1-13 3+5=8

(38.1/28.0) % 34 (38.1=1x81.0+ cx86.0+1 Cycle Lime

Speedup

with a stages

with 5 stages

210 PS (MEIN +20PS) (0x200)/ (8x210)

200 PS (IF)

TO:1 =