East West University
Department of Computer Science and Engineering
CSE 251 –Electronic Circuits, Section: 05
Semester: Fall 2020

Quiz 1

Duration: 30 minutes	Total Mark: 10	Date: 4.11.2020	Marks obtained:

Question:

1. A silicon diode (in Figure 01) is operating at room temperature with an internal resistance, $r_D = 20\,\Omega$ .Find the voltage drop, V_d across the diode and the current, I_d flowing through the diode. [Use the piecewise linear model of the diode for analysis]

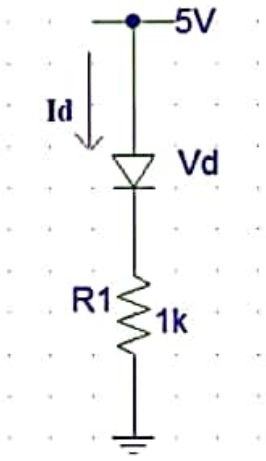


Figure 01

2. Find the voltage drop across a silicon diode with saturation current, I_S = 0.1 fA operating at room temperature at a current of 300 μA.

EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Mid Term I Assessment, Fall 2020

Course:	**CSE 251 – Electronic Circuits, Section-5**
Instructor:	**M. Saddam Hossain Khan, Senior Lecturer, CSE Department**
Full Marks:	**15**
Time:	**1 Hour and 30 Minutes (including attachment time)**

Note: There are FOUR questions, answer ALL of them. Course outcomes (CO) and marks of each question are mentioned at the right margin.

1. The circuit in Figure 01, contains a silicon diode which is operating at a temperature of 50°C. (hints: $V_T = kT/q$, (k=1.38 × 10^{-23} J/K, q=1.6× 10^{-19} C) [CO1, Mark: 3]

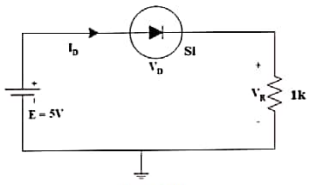


Figure 01

a) **Calculate** the diode current, I_D.
b) Also, calculate the diode saturation current, I_S .

2. Assuming that the diodes in the circuit given in Figure 02 are ideal, **determine** the values of the labeled voltage and current. [CO1, Mark: 3]

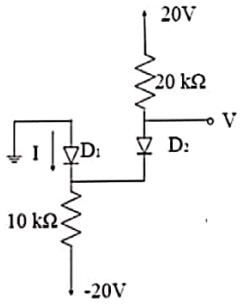


Figure 02

3. Consider a bridge rectifier circuit which is fed by a sinusoid input, V_S with 1.5kΩ load, whose input and output wave is given in Figure 03. The semiconductor material used to build the diodes of the rectifier is germanium. [CO2, C3, Mark: 4]

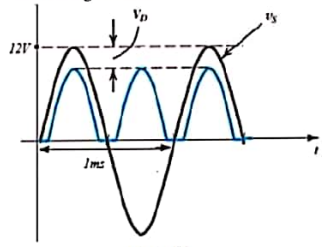


Figure 03

(a) **Calculate** the output peak, V_{OP} .
(b) **Calculate** the fraction of the cycle during which the diodes conduct.
(c) **Calculate** the average output, Vo_{avg} across the load.

4. a) For the network given in Figure 04, the input signal v_i is given as a square wave with 40V peak to peak. **Analyze** the circuit and **sketch** the waveform of output v_0 with proper labeling. Also, mention which type of circuit the given networ depicts. [CO2, Mark: 5]

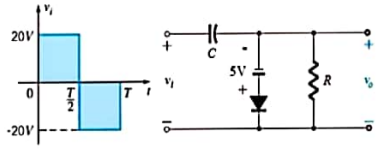
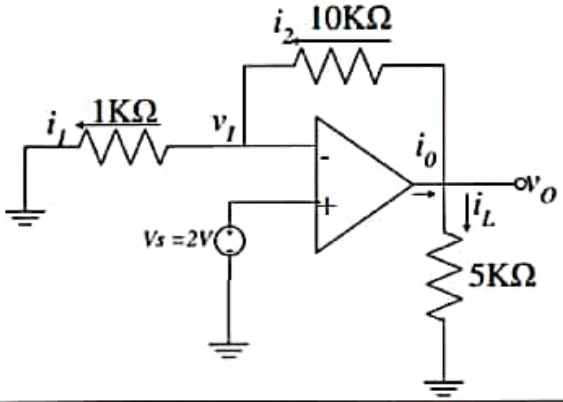
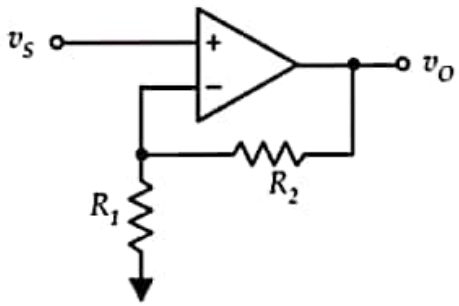


Figure 04

b) Half wave rectifier circuit is a clipper or a clamper? Justify your answer with proper explanation.

East West University
Department of Computer Science and Engineering
CSE 251 –Electronic Circuits, Section: 05
Semester: Fall 2020
Quiz 2

Name:			Id:
Duration: 30 mins	Total Mark: 15	Date: 22.11.2020	Marks obtained:

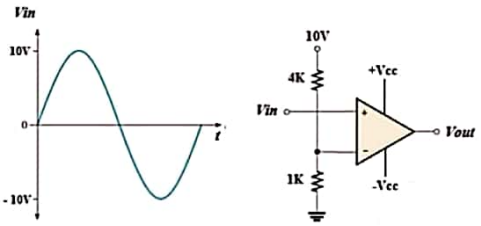
1.	Determine all the labeled voltage and currents for the circuit given below. 	[6]
2.	In the circuit given below, $R_2 = 115k\Omega$. Assume that, the op-amp is ideal. Determine the value of R_1 so that the gain, $A_v = \frac{v_o}{v_s} = 24$. 	[4]

EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Mid Term II Assessment, Fall 2020

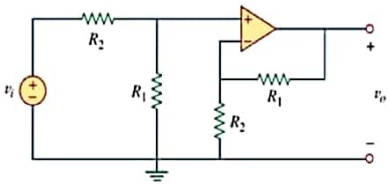
Course:	**CSE 251 – Electronic Circuits, Section-5**
Instructor:	**M. Saddam Hossain Khan, Senior Lecturer, CSE Department**
Full Marks:	**20**
Time:	**1 Hour 20 minutes [Including attachment time]**

Note: There are FOUR questions, answer ALL of them. Course outcomes (CO), cognitive levels and marks of each question are mentioned at the right margin.

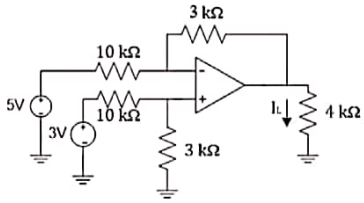
1. a) **Estimate** and **sketch** the output signal, V_{out} showing its proper relationship to the input signal, V_{in} for the circuit given below. [*Note that, the maximum output levels of the op amp circuit are ± 15 V*] [CO2, Mark: 3.5]



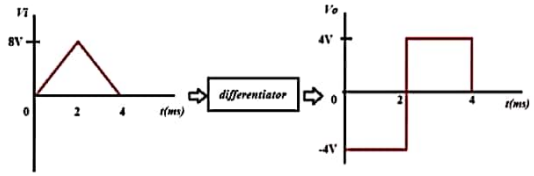
b) Design the amplifier circuit given below (i.e. **determine** the values of the resistors) to get the desired output of $V_O = 3V_i$. [CO2, Mark: 3.5]



2. **Determine** I_L for the circuit given below. [CO2, Mark: 4]



3. A differentiator circuit has the following input V_i and output V_o waveforms. Now, design the circuit i.e. **determine** the value of the input capacitor, C if the value of the feedback resistor, R is given as $1K$. [CO2, Mark: 4]



4. **Design** a circuit using two op amps, to perform the following operation: [CO2, Mark: 5]

$$v_O = v_1 + v_2 - 3v_3$$

Now, **choose** the values of the feedback resistors and the input resistors such that for a maximum output of "X" V the current in the feedback resistor is $0.5mA$.
[*Note that,* $X =$ *summation of last* 3 *digits of your ID*]

CSE 251Electronic Circuits
(Course Project)

Project-1: Design of a Triangular wave generator using Operational Amplifier for a specified input.

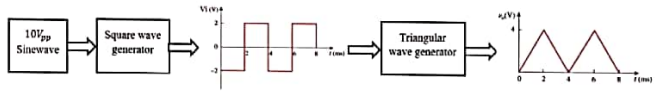


Fig. 1

Fig.1 shows a design process of a Triangular wave generator circuit. The design process includes two design segments (a square wave generator & a triangular wave generator) to get the final output v_o(V). Use a $10V_{pp}$ sinusoid as input and operational amplifiers to design. Design the circuit components and finally simulate to test the circuit.[Note that, for design purpose, the values of the resistors should not exceed more than 10kΩ.]

Project-2: Design a 5V DC Power Supply using Diode for a specified input.

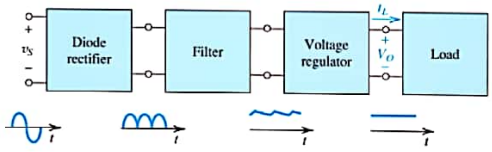


Fig. 2

Fig.2 shows the block diagram of a dc power supply design process. The design process includes three design segments: a diode rectifier, a filter and a voltage regulator to get the final output v_o. The diode rectifier converts the input sinusoid v_S to a unipolar output, which can have the pulsating waveform indicated in Fig. 3. The variations in the magnitude of the rectifier output are considerably reduced by the filter block. The output of the rectifier filtercontains a time-dependent component, known as ripple. To reduce the ripple and to stabilize the magnitude of the dc output voltage against variations caused by changes in load current, a zener shunt voltage regulator can be implemented. Design the circuit components, and finally simulate to test the circuit. Use sine wave (*24Vp-p*) as input signal, and capacitor, resistors and zener diode of suitable value for the design. Note that, for design purpose, the values of the resistors should not exceed more than 10kΩ.

Marks Distribution

Assessment Area	Mark
C3: Cognitive: Applying	4
P2: Psychomotor: Manipulation	2
P3: Psychomotor: Precision	2
A2: Affective: Responding	2
Total	10

Project Report should contain:

1. Problem Statement
2. Design Details (Identify the circuit structures of the internal blocks and theoretically design the values of unknown parameters)
3. Circuit Diagram (Draw using **VISIO**)
4. Simulation Results (Using the designed & given values of the parameters); you have to take the screenshots of your simulation results.

[Note that, report should contain maximum 5 pages. Also, follow the provided report template].

Project Presentation slide should contain:

1. Problem Statement
2. Design Details
3. Circuit Diagram
4. Simulation Results
5. Comparison of theoretically calculated and simulated values

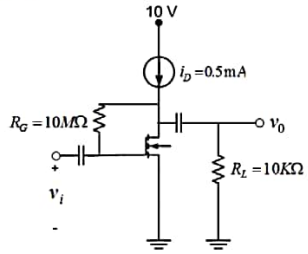
[Note that, each group will get overall 10 minutes for the presentation. You'll get 6 minutes to present and remaining 4 minutes are for Question-answering session].

EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Final Examination, Fall 2020

Course: **CSE 251 – Electronic Circuits, Section-5**
Instructor: **M. Saddam Hossain Khan, Senior Lecturer, CSE Department**
Full Marks: **20**
Time: **1 Hour and 15 Minutes [Attachment & submission time included]**
Note: There are FOUR questions, answer ALL of them. Course outcomes (CO), cognitive levels and marks of each question are mentioned at the right margin.

---

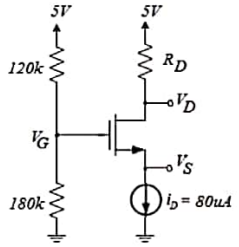
1. Figure below represents a MOS amplifier using a feedback biasing arrangement. The transistor has threshold voltage $V_t = 0.9\,\text{V}$, early voltage $V_A = 20\,\text{V}$ and operates with $V_D = 2\,\text{V}$. Assume the coupling capacitors to be sufficiently large so as to acts as short circuits at the signal frequencies. [CO2, Mark: 7]



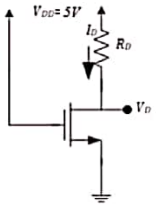
a. **Calculate** the transconductance, gm.
b. **Determine** the small signal gain of the amplifier.
c. **What** is the minimum V_{DS} required to ensure linear amplification?

2. The circuit given below has classical biasing arrangement to establish a dc drain current I_D= 80uA. Biasing has performed by fixing the gate voltage. The transistor is operating at $V_{GS} = 2V$ and $V_{DS} = 0.3V$. [CO2, Mark: 5]

a) **Estimate** all the node voltages.
b) **Find** the value of R_D .

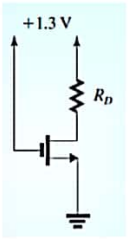


3. An N-MOSFET circuit in figure below has drain voltage, $V_D = (0.1 * x)\,V$, threshold voltage, V_t = 1V, and $K_n'(W/L)$ = 1mA/V². **Design** the circuit. Also **determine** the effective resistance between drain and source at the operating point. [x = *summation of the last three digits of your id*] [CO1, Mark: 4]



4. a) The transistor in circuit below has $k_n' = 0.4\,mA/V^2$ and $V_t = 0.4\,V$. **Show** that operation at the edge of saturation is obtained when the following condition is satisfied: [CO1, Mark: 4]

$$\left(\frac{W}{L}\right) R_D \cong 2.5\,K\Omega$$



b) In practical case, for an N-channel mosfet, why the drain current, I_D is not constant with respect to V_{DS} ? Justify your answer with a **very short** explanation.