

EAST WEST UNIVERSITY

Department of Computer Science and Engineering B.Sc. in Computer Science and Engineering Program Mid Term II Examination, Summer 2020 Semester

Course: CSE 345 Digital Logic Design, Section-3

Instructor: Musharrat Khan, Senior Lecturer, CSE Department

Full Marks: 30 (15 will be counted for final grading)

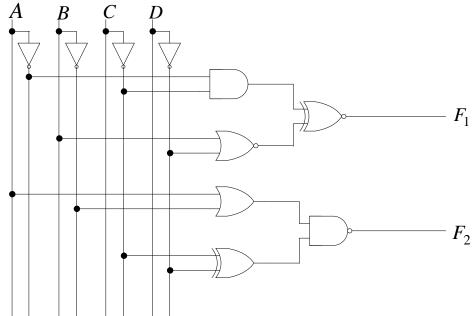
Time: 1 Hour and 20 Minutes (Including submission)

Note: There are FIVE questions, answer ALL of them. Course Outcome (CO), Cognitive Level and Mark of each question are mentioned at the right margin.

1. A combinational circuit has four inputs *A*, *B*, *C*, and *D*. The output *F* is 1 for two cases: [CO3,C3, Mark: 6]

Case 1: When only *A* and *C* are 1. Case 2: When only *B* and *D* are 1. **Design** the combinational circuit.

2. Analyze the following circuit by constructing truth table of the outputs. [CO2,C4, Mark: 6]



Design a full-adder using only AND, EXOR, and OR gates. [Draw block diagram, construct truth table, determine Boolean equations of outputs, and draw logic diagram]

[CO3,C3, Mark: 6]

- 4. Construct a combinational circuit using an 8×1 MUX for implementing the following Boolean function. [Properly label all the inputs and outputs]

 [CO3,C6, Mark: 6]
 - $F(A, B, C, D) = \prod (1,5,6,8,10,12)$
- **5. Write** a behavioral Verilog code to design a 4×1 MUX with active-LOW [CO3,C6, enable input using Procedural technique using case statement. Mark: 6]