

EAST WEST UNIVERSITY Department of Computer Science and Engineering Fall 2021 Semester

CSE345 Digital Logic Design, Section-2, Class Test-3

Marks:10

Time: 25 minutes

1. Design a sequential circuit represented by the following transition table using T Flip-Flop.

Present State	Next State		Output, z_1z_2	
$Q1_nQ2_n$	$Q1_{n+1}Q2_{n+1}$			
	x = 0	x = 1	x = 0	x = 1
00	00	10	11	01
01	11	01	00	11
11	11	10	01	10
10	01	11	10	01