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Assignment-3

a) My PC:

i) System Description:

- AMD Ryzen 5 1600
- Number of Cores : 6
- Number of Threads : 12
- Base Clock Speed : 3.2 GHz
- PSU : 550 W

ii) Main Memory Specification:

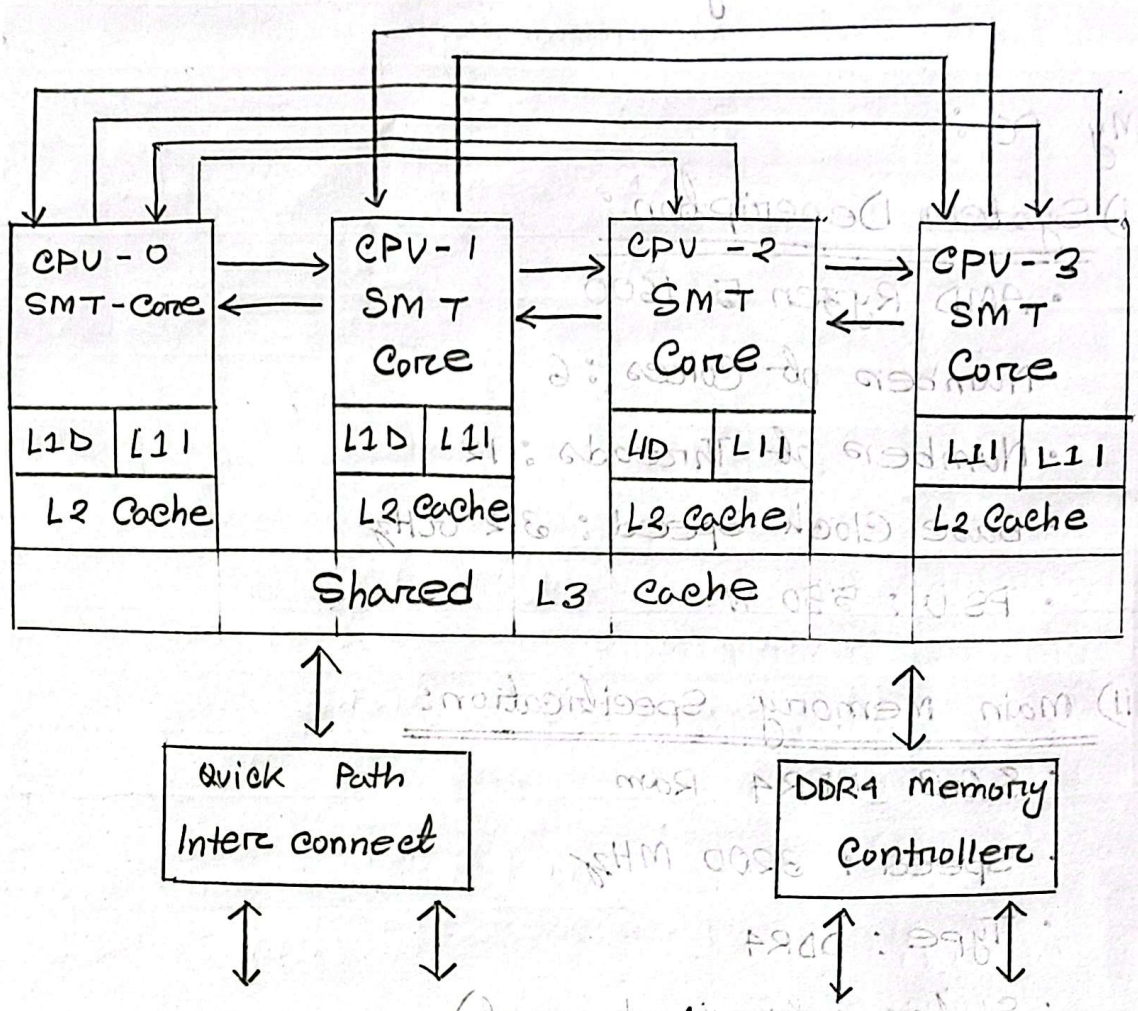
- 8 GB DDR4 Ram
- Speed : 3200 MHz
- Type : DDR4
- Slots: 2 (Dual-channel)

iii) Storage details:

- 512 GB NVMe SSD
- 1 TB HDD
- SSD:
  Read speed : up to 3200 MB/S
  Write speed : up to 2700 MB/S

ii) Process Details:

1) Block Diagram:



Ref: wikichipbase.com

2. Instruction Set Related Specification:

- ISA: x86-64 (also known as x64)
- Supports SIMD Extensions: SSE4, AVX, AVX2
- Instruction Fetch, Decode, Execute Memory Access, white black stages

3. Specification:

- Pipeline Details: 14 stage pipline boos throughput.
- Multiple Issue Details: Supports Hyper Threading Technology (SMT)
- Cache Memory Details:
  - → L1 cache - 32KB Per core
  - → L2 cache - 256 KB per core

→ L3 cache: 12 MB Shared

- Bus: Direct Media Interface (DMI) 3.0
- Interrupt: Advanced Programmable Interrupt Controller
- I/O: PCI 3.0, USB 3.1
- DMA: Integrated Directed Memory Access controller

b) My Mobile Phone: (OPPO)

i) System Discription:

- Processor: Media Tek Dimensity 8100 - Max
- Number of cores: 8
- Config: Octa-core (4x Cortex-A78 at 2.85 GHz + 4x Cortex-A55 at 2.0 GHz)
- Manufacturing Process: 5nm

2. Main memory specification:

- 8 GB LPDDR5 RAM
- Speed: 2750 MHz
- Type: LPDDR5

3. Storage Details:

- 256 GB UFS 3.0
- Read Speed: Up to 2100 MB/S
- Write Speed: Up to 1200 MB/S

ii) Processor Details:

1) Block Diagram:

<table>
<tr><td colspan="3">Snapdragon 865</td></tr>
<tr><td>Prime Core (Cortex - A77) @ 2.84 GHz</td><td>Performance Cores (x3) (Cortex - A77) 2.42 GHz</td><td>Efficiency Cores (Cortex - A55) 1.8 GHz</td></tr>
<tr><td colspan="3">L3 Cache (4MB shared)</td></tr>
<tr><td colspan="3">Adreno 650 GPU (Graphics Processor Unit)</td></tr>
<tr><td colspan="3">Hexagon 698 DSP</td></tr>
<tr><td colspan="3">Spectra 480 ISP</td></tr>
<tr><td colspan="3">Memory Controller (LPDDR5)</td></tr>
<tr><td colspan="3">AI Engine</td></tr>
<tr><td colspan="3">Modem (x55 5G Modem)</td></tr>
<tr><td colspan="3">Connectivity (Wifi, Bluetooth)</td></tr>
<tr><td colspan="3">I/O Interfaces (USB 3.1)</td></tr>
</table>

Ref: Bonearea.com

2. Instruction related Info:

- ISA ARM v8-A
- Supports SIMD Extensions: NEON
- Instruction Fetch, Decode, Execute, Memory Access and write back stages.

3. Specifications:

- Pipelining Details: Out of order execution with a 10 stage pipeline.
- Multiple Issue Details: Supports big Little architecture for power efficiency
- Cache memory Details:
  - → L1 Cache: 64 kB (I) + 64 kB (D) Per core
  - → L2 cache: 1 MB (A77) + 512 kB (A55)
  - → L3 cache: 4 MB shared

- Bus : AXJ , AHB
- Interrupt : Generic Interrupt Controller
- I/O : USB 3.1 , PCIe 3.0
- DMA : Integrated DMA controller

c) Recent & Popular Embedded Micro Controller:

STM32F407VGTG

i) System Description :

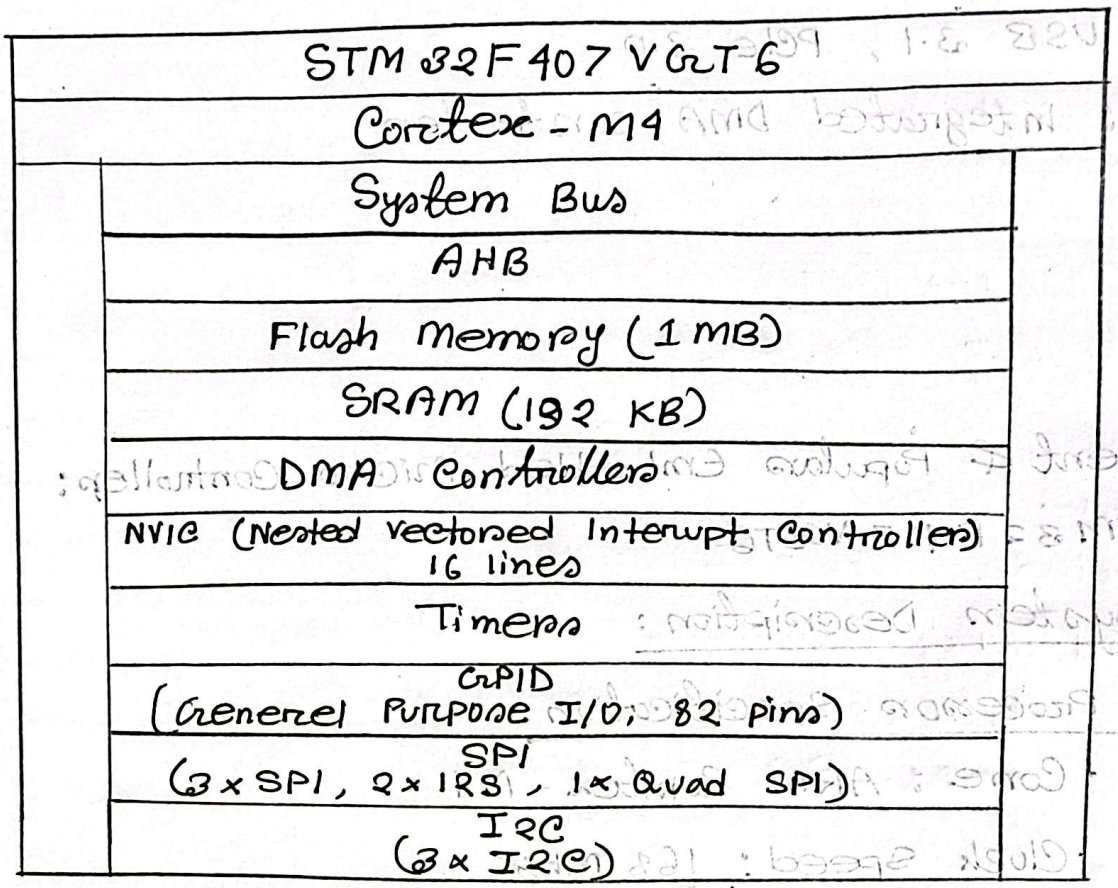
1. Processor Specification :
   - Core : ARM Cortex-M4
   - Clock Speed : 168 MHz
   - Flash memory : 1 MB
   - SRAM : 192 KB

2. Main memory Specification :
   - Internal SRAM : 192 KB
   - External memory Interface : FSMC for external SRAM, PSRAM, NOR, NAND memory

3. Storage Details :
   - Embedded Flash : 1 MB
   - External storage : Support for external NAND/NOR flash via FSMC

ii) Processor Details:

1. Block Diagram:



Ref: researchgate.com

2. Instruction Set Related Info:

- ISA : ARMv7-M (Thumb-2)
- Supports SIMD extensions : ARM DSP extensions.
- Instruction fetch, Decode, Execute memory Access and write back stages.

3. Specifications:

- Pipelining Details : 3 stage (fetch, decode, execute)
- Multiple Issue details : Single issue.
- Cache Memory details -
  - → Instruction Cache : 4kB
  - → Data Cache : 4kB
- I/O : GPIO, UART, SPI, I2C, CAN, USB
- DMA : 16-stream DMA controllers.

(iii) Application and Programming:

Application:

→ Industrial Control system
→ Medical device
→ Consumer electronics

Setup i→ Install STM32 CubeIDE
→ Connect STM 32407VGT6 to the PC via ST-link

Example Code:

```
#include "stm32f4xx.h"
void delay (uint32_t count){
    while (count--){
        __NOP();
    }
}
int main (void){
    RCC->AHB1ENR |= RCC_AHB1NR_GPIOGEN;
    GPIOG->MODER |= GPIO_MODER_13_0;
    while (1){
        GPIOG->ODR = GPIO_ODR_ODR_13;
        delay (5000000);
    }
}
```