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Course : CSE345

Section : 03

Ans To The Ques No-01

$$J_{1n} = x' \oplus Q_{2n}'$$
$$= x Q_{2n}' + x' Q_{2n}$$

$$K_{1n} = x$$

$$J_{2n} = (Q_{1n} \cdot x)'$$
$$= Q_{1n}' + x'$$

$$K_{2n} = Q_{1n}'$$

$$Z = Q_{2n} x (x + Q_{1n})$$
$$= Q_{2n} x + Q_{1n} Q_{2n} x$$

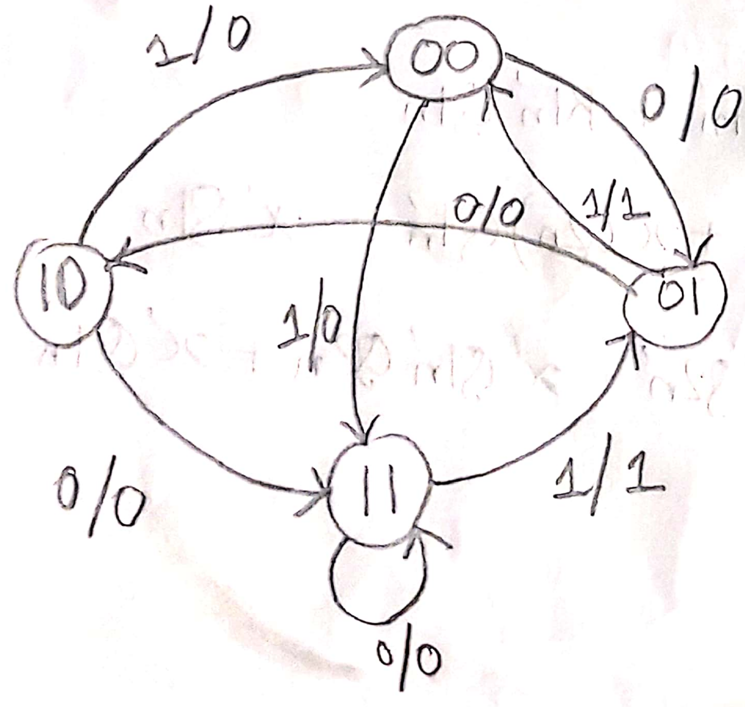
$$Q_{1n+1} = J_{1n} Q_{1n}' + K_{1n}' Q_{1n}$$
$$= (x Q_{2n}' + x' Q_{2n}) Q_{1n}' + x' Q_{1n}$$
$$= x Q_{1n}' Q_{2n}' + x' Q_{1n}' Q_{2n} + x' Q_{1n}$$

$$Q_{2n+1} = J_{2n} Q_{2n}' + K_{2n}' Q_{2n}$$

$$= (Q_{1n}' + x') Q_{2n}' + Q_{1n} Q_{2n}$$

$$= Q_{1n}' Q_{2n}' + x' Q_{2n}' + Q_{1n} Q_{2n}$$

Present State Q_{1n} Q_{2n}	Next State Q_{1n+1} Q_{2n+1} (input x)		output Z (Input x)	
	0	1	0	1
00	01	11	0	0
01	10	00	0	1
11	11	01	0	1
10	11	00	0	0



Ans To The Ques No-2

Present State $Q_{1n}Q_{2n}$	Next State $Q_{1n+1}Q_{2n+1}$ $x=0$	$x=1$	Flip Flop Inputs $x=0$ $S_{1n}R_{1n}$	$S_{2n}R_{2n}$	$x=1$ $S_{1n}R_{1n}$	$S_{2n}R_{2n}$	Output Z_1Z_2 $x=0$	$x=1$
00	11	01	10	10	0X	10	11	00
01	11	11	10	X0	10	X0	00	11
11	00	10	01	01	X0	01	10	10
10	10	00	X0	0X	01	0X	01	10

S_{1n}:

$Q_{1n}Q_{2n}$ \ x	0	1
00	1	0
01	1	1
11	0	X
10	X	0

$$S_{1n} = Q_{1n}'x' + Q_{1n}'Q_{2n}$$

R_{1n}:

$Q_{1n}Q_{2n}$ \ x	0	1
00	0	X
01	0	0
11	1	0
10	0	1

$$R_{1n} = Q_{1n}Q_2x' + Q_{2n}'x$$

$S2n$:

$Q1nQ2n$ \ x	0	1
00	1	1
01	X	X
11	0	0
10	0	0

$S2n = Q1n'$

$R2n$:

$Q1nQ2n$ \ x	0	1
00	0	0
01	0	0
11	1	1
10	X	X

$R2n = Q1n$

$Z1$:

$Q1nQ2n$ \ x	0	1
00	1	0
01	0	1
11	1	1
10	0	1

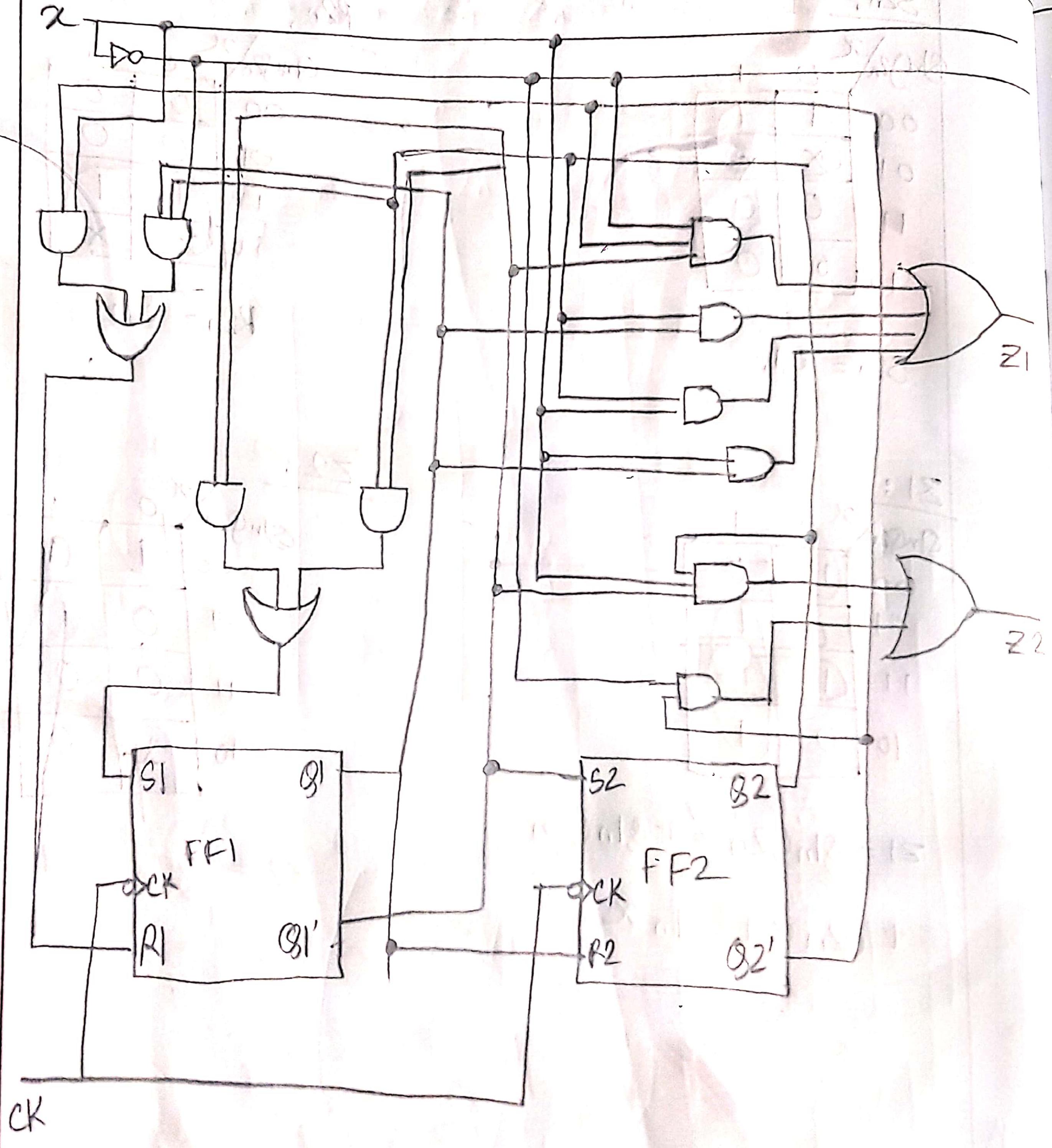
$Z1 = Q1n'Q2n'x' + Q1nQ2n$

$+ Q2nx + Q1nx$

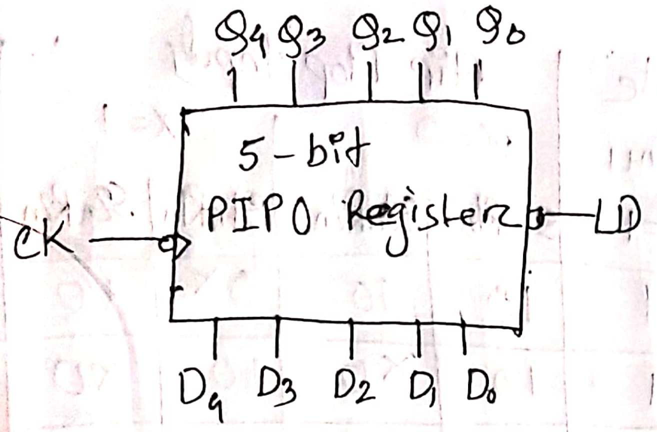
$Z2$:

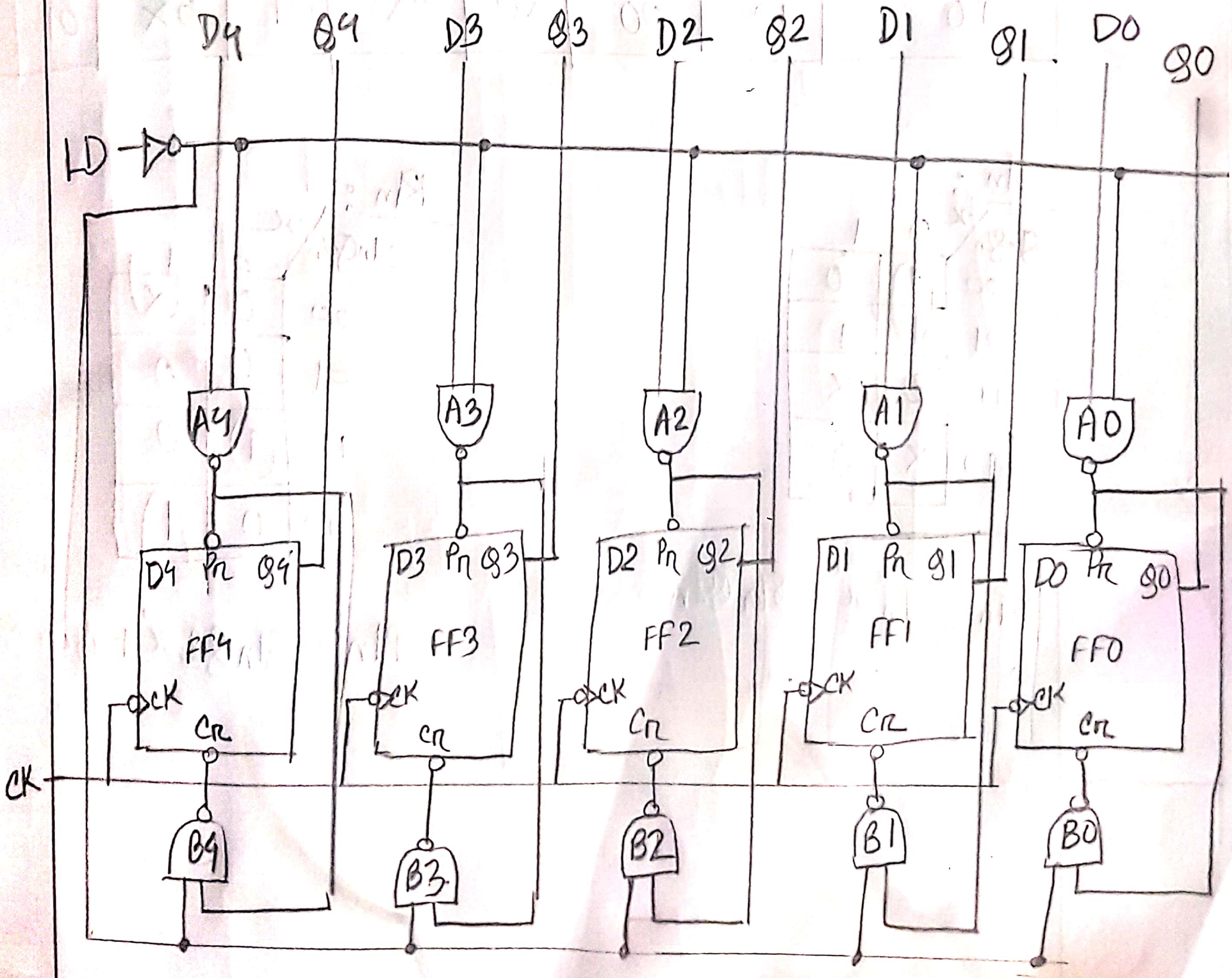
$Q1nQ2n$ \ x	0	1
00	1	0
01	0	1
11	0	0
10	X	0

$Z2 = Q2n'x' + Q1n'Q2nx$

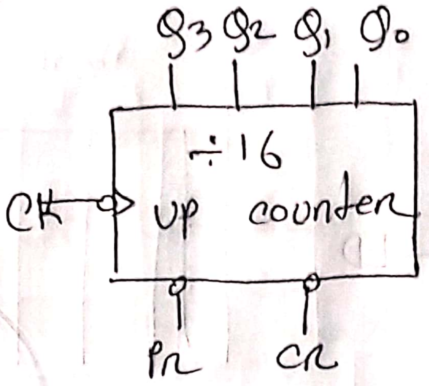

x
S1
Q1
FF1
CK
R1
Q1'
S2
Q2
FF2
CK
R2
Q2'
Z1
Z2
CK

Ans. To The Ques No-03

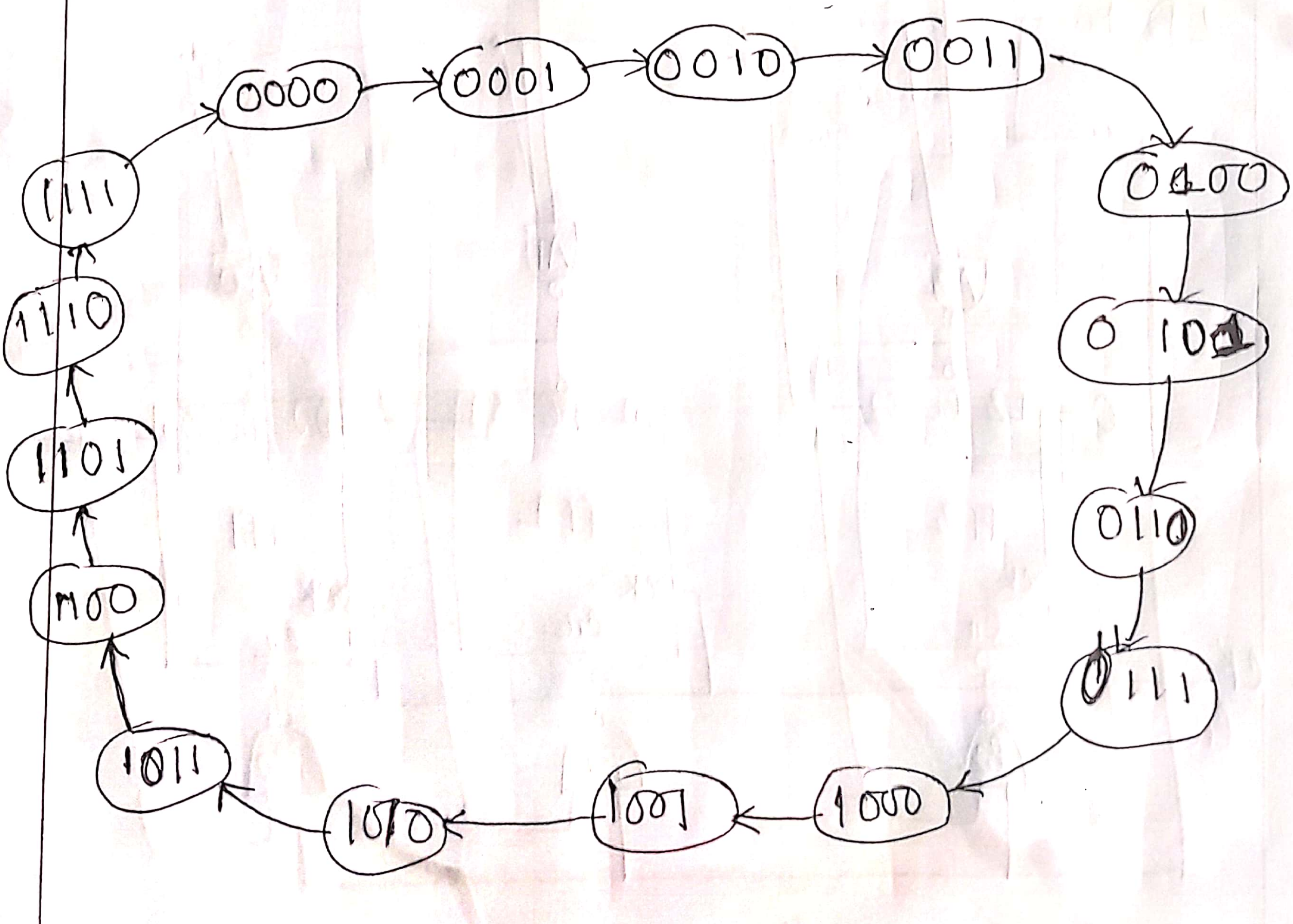




Ans. To The Ques No-4



(a) Block Diagram



(b) Transition Diagram

Present State				Next State				Flip Flop Inputs			
$Q3_n$	$Q2_n$	$Q1_n$	$Q0_n$	$Q3_{n+1}$	$Q2_{n+1}$	$Q1_{n+1}$	$Q0_{n+1}$	T3	T2	T1	T0
0	0	0	0	0	0	0	1	0	0	0	1
0	0	0	1	0	0	1	0	0	0	1	1
0	0	1	0	0	0	1	1	0	0	0	1
0	0	1	1	0	1	0	0	0	1	1	1
0	1	0	0	0	1	0	1	0	0	0	1
0	1	0	1	0	1	1	0	0	0	1	1
0	1	1	0	0	1	1	1	0	0	0	1
0	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	0	0	1	0	0	0	1
1	0	0	1	1	0	1	0	0	0	1	1
1	0	1	0	1	0	1	1	0	0	0	1
1	0	1	1	1	1	0	0	0	1	1	1
1	1	0	0	1	1	0	1	0	0	0	1
1	1	0	1	1	1	1	0	0	0	1	1
1	1	1	0	1	1	1	1	0	0	0	1
1	1	1	1	0	0	0	0	1	1	1	1

T_3:

$Q_{3n}Q_{2n} \backslash Q_{1n}Q_{0n}$	00	01	11	10
00				
01			1	
11			1	
10				

$$T_3 = Q_{2n} Q_{1n} Q_{0n}$$

T_2:

$Q_{3n}Q_{2n} \backslash Q_{1n}Q_{0n}$	00	01	11	10
00			1	
01			1	
11			1	
10			1	

$$T_2 = Q_{1n} Q_{0n}$$

T_1:

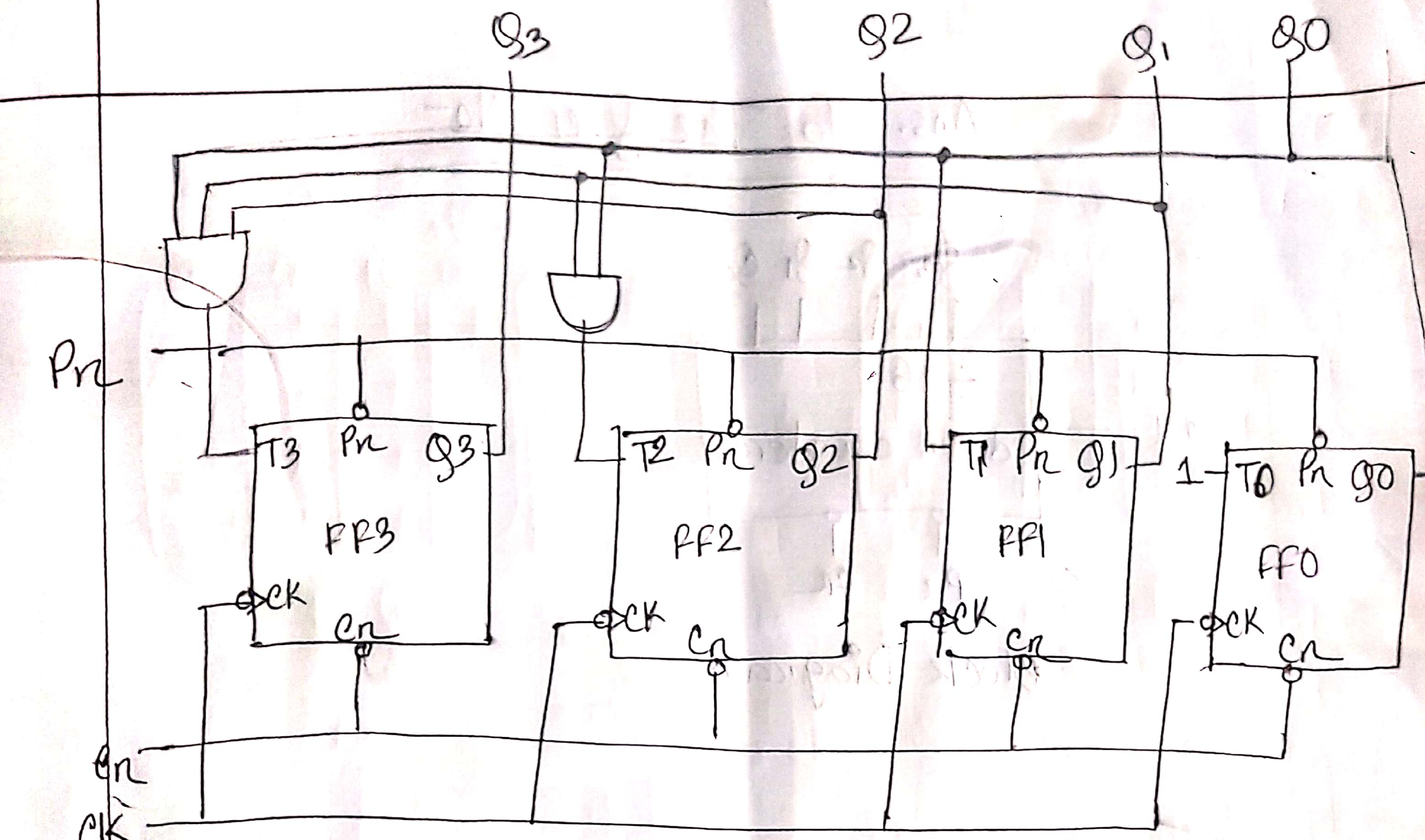
$Q_{3n}Q_{2n} \backslash Q_{1n}Q_{0n}$	00	01	11	10
00		1	1	
01		1	1	
11		1	1	
10		1	1	

$$T_1 = Q_{0n}$$

T_0:

$Q_{3n}Q_{2n} \backslash Q_{1n}Q_{0n}$	00	01	11	10
00	1	1	1	1
01	1	1	1	1
11	1	1	1	1
10	1	1	1	1

$$T_0 = 1$$



Logic diagram of ÷16 synchronous up counter

Ans To The Ques No-5

```
module   fsm (input i, clock, reset, ~~output reg[1:0] out~~
              output reg [1:0] out);

   reg [2:0]   currentState, nextState;

 localparam [2:0]   A = 3'b 0 0 0,
                    B = 3'b 0 0 1,
                    C = 3'b 0 1 0,
                    D = 3'b 0 1 1,
                    E = 3'b 1 0 0;

always @ (*)
case (currentState)

 A :   begin
          nextState = (i==0) ? C : D ;
          out = (i==0) ? 3'b10 : 3'b10 ;

       end

 B :  begin
          nextState = (i==0)? A : C ;
          out = (i==0) ? 3'b01 : 3'b11 ;

       end
```

```
C : begin
        nextstate = (i==0) ? D : A ;
          out = (i==0) ? 3'b10 : 3'b11 ;

    end
D : begin
        nextState = (i==0) ? E : A ;
         out = (i==0) ? 3'b10 : 3'b01 ;

    end

E : begin
        nextState = (i==0) ? E : E ;
          out = (i==0) ? 3'b10 : 3'b00 ;

    end

defoult : begin
          nextState = A ;
            out = 3'b xxx ;

    end

endcase
```

```
always@ (posedge clock, negedge reset)
    if (~reset)
            currentState <= A;
    else
         currentState <= nextState;
  end-module
```