

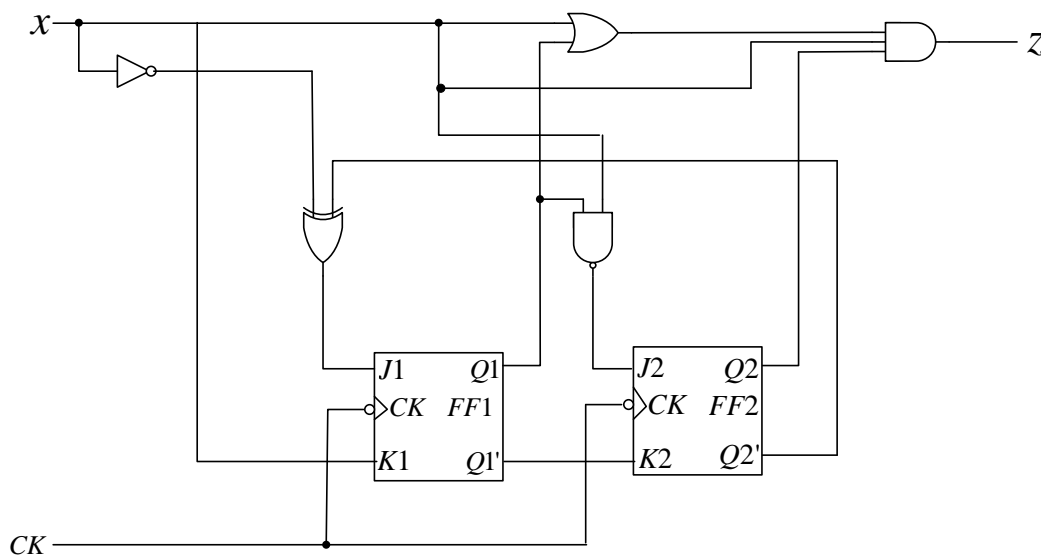


**EAST WEST UNIVERSITY**  
**Department of Computer Science and Engineering**  
**B.Sc. in Computer Science and Engineering Program**  
**Final Examination, Fall 2021 Semester**

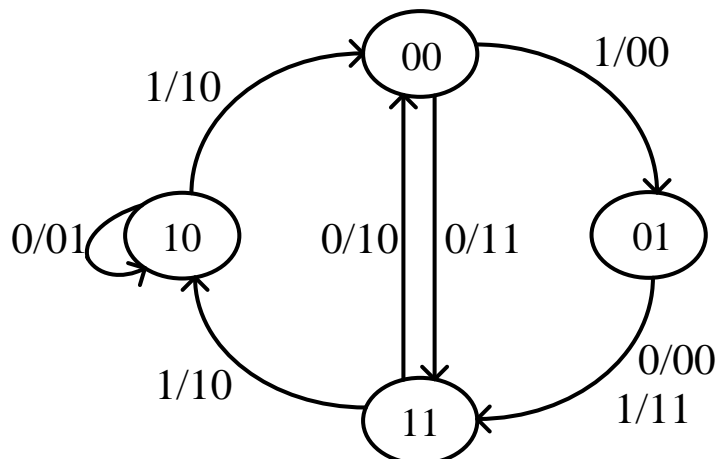
**Course:** CSE 345 Digital Logic Design, Section-3  
**Instructor:** Musharrat Khan, Senior Lecturer, CSE Department  
**Full Marks:** 40 (20 will be counted for final grading)  
**Time:** 1 Hour and 25 Minutes (Including submission)

**Note:** There are FIVE questions, answer ALL of them. Course Outcome (CO), Cognitive Level and Mark of each question are mentioned at the right margin.

1. **Write down** next state and output equations for the following sequential circuit. From these equations **analyze** the sequential circuit and draw the transition diagram. [CO2,C4, EP1, Mark: 8]



2. **Design** a sequential circuit represented by the following state diagram using S-R flip-flop. [CO3,C3, EP1,EP2, Mark: 8]



3. **Design** a 5-bit parallel-in parallel-out register using D flip-flops. [Draw its block diagram, and logic diagram] [CO3,C6, Mark: 8]
4. **Design** a  $\div 16$  synchronous up counter using T flip-flops. [Draw its block diagram, transition diagram, excitation table, equation, and logic diagram] [CO3,C6, Mark: 8]
5. **Design** a synchronous sequential circuit represented by the following state diagram using explicit style Verilog code. Assume a positive-edge clock. Also assume that reset will be done when the reset signal will go from 1 to 0. [CO3,C6, EP1,EP2, Mark: 8]

