

Answer to the Question No:03

3 bit serial in-parallel out Bidirectional shift register.

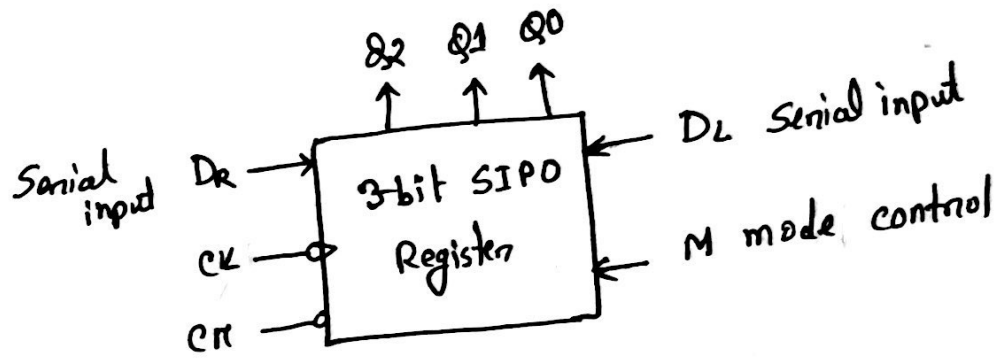


Fig: Block diagram.

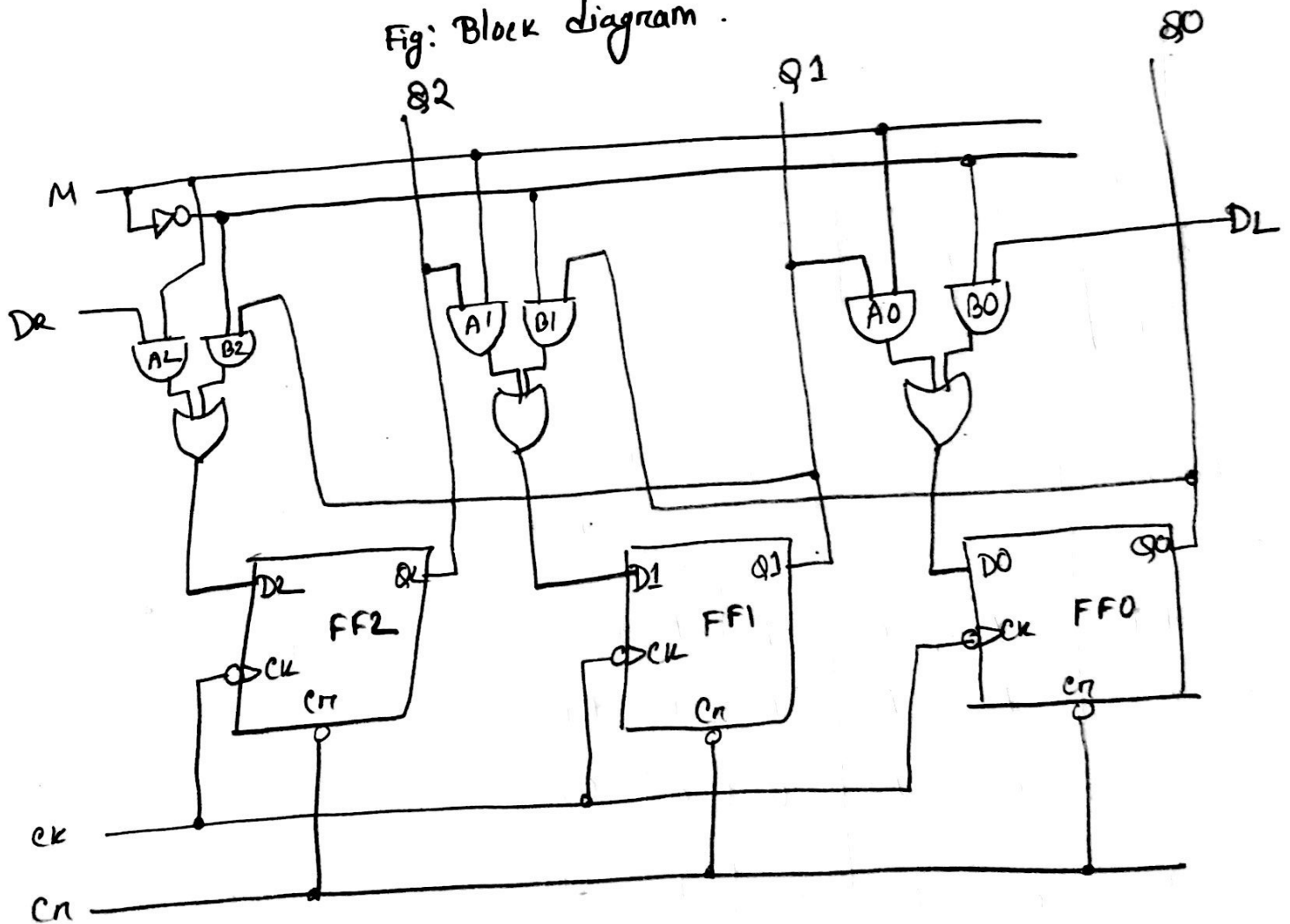


Fig: Logic Diagram.

Answer to the Question No:05

```
module fsm (input i, clock, reset, output reg [1:0] out);  
    reg [1:0] currentstate, nextstate;  
    localparam [1:0] A = 2'b00,  
                     B = 2'b01,  
                     C = 2'b10,  
                     D = 2'b11;
```

always @(*)

case (currentstate)

```
    A: begin  
        nextstate = (i==0) ? C : D;  
        out = 2'b10;  
    end
```

```
    B: begin  
        nextstate = (i==0) ? A : C;  
        out = (i==0) ? 2'b01 : 2'b11;  
    end
```

```
    C: begin  
        nextstate = (i==0) ? D : A;  
        out = (i==0) ? 2'b10 : 2'b11;  
    end
```

```
    D: begin  
        nextstate = (i==0) ? C : A;  
        out = (i==0) ? 2'b01 2'b10 : 2'b01;  
    end
```

endcase

PTU

always @ (negedge clock, posedge reset)

if (reset)

current state <= A;

else

current state <= next state;

end module.

Answer to the Question No: 02

D-Flip Flop

Q_n	Q_{n+1}	D_n
0	0	0
0	1	1
1	0	0
1	1	1

Present state Q_1, Q_2	Next state, Q_{1n+1}, Q_{2n+1}		Flip-flop input				Output Z_1, Z_2	
	$x=0$	$x=1$	$x=0$		$x=1$		$x=0$	$x=1$
00	11	00	1	1	0	1	11	00
01	11	11	1	1	1	1	00	11
11	00	10	0	0	1	0	10	10
10	10	00	1	0	0	0	01	10

D1

$Q_1 Q_2 \backslash x$	0	1
00	1	0
01	1	1
11	0	1
10	1	0

$$D1 = Q1'n x' + Q2n x + Q2'n x'$$

D2

$Q_1 Q_2 \backslash x$	0	1
00	1	1
01	1	1
11	0	0
10	0	0

$$D2 = Q1'n$$

Z1

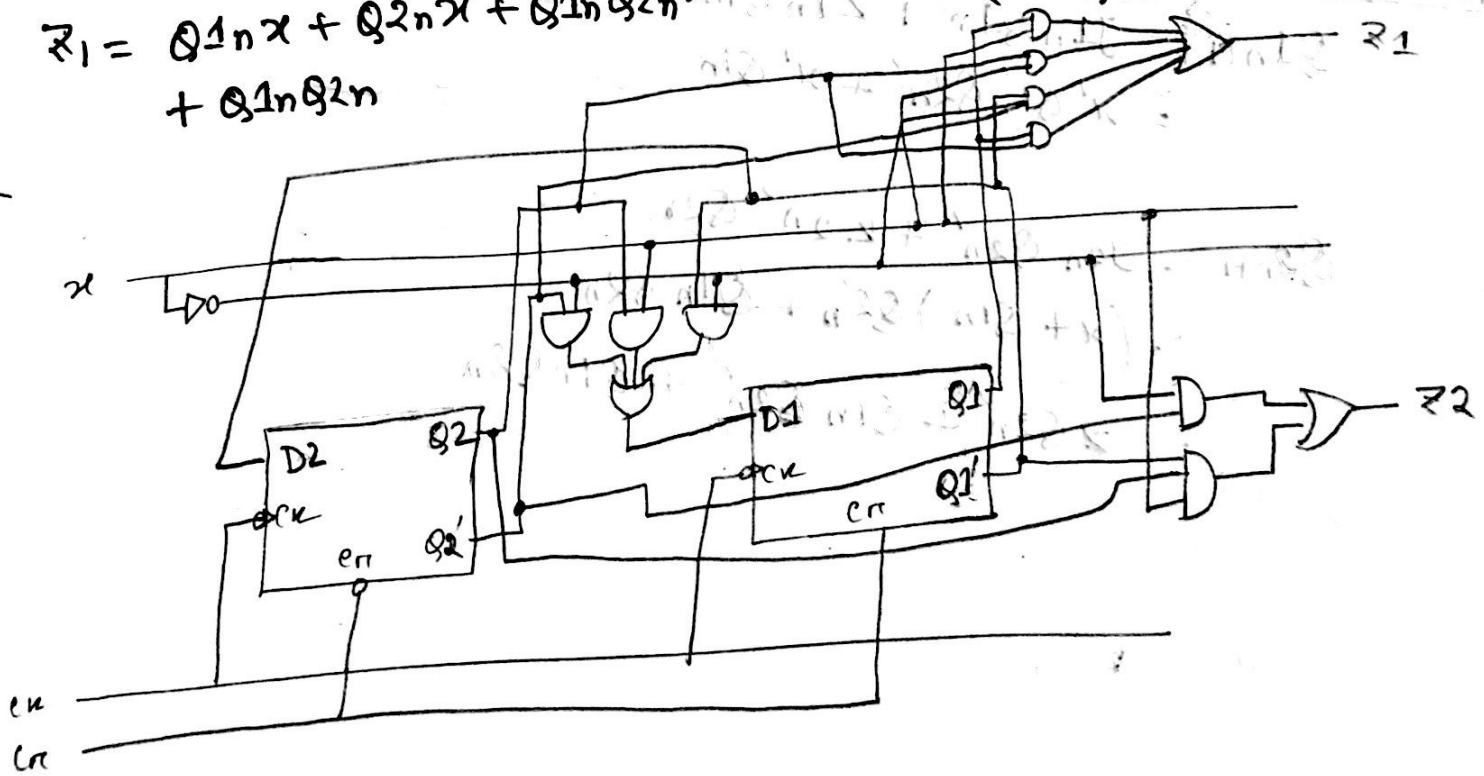
$Q_1 Q_2 \backslash x$	0	1
00	1	0
01	0	1
11	1	1
10	0	1

$$Z1 = Q1n x + Q2n x + Q1'n Q2'n x' + Q1n Q2n$$

Z2

$Q_1 Q_2 \backslash x$	0	1
00	1	0
01	0	1
11	0	0
10	1	0

$$Z2 = Q2'n x' + Q1'n Q2n x$$



Answer to the Question No: 01

Output equation:

$$\begin{aligned} Z &= Q_{2n} (x_1 Q_{1n} + x_1 Q_{1n}') \\ &= x_1' Q_{1n} Q_{2n} + x_1 Q_{1n}' Q_{2n} \end{aligned}$$

Excitation equation:

$$J_{1n} = x_1' Q_{2n}'$$

$$J_{2n} = x_1 + Q_{1n}$$

$$K_{1n} = x_1$$

$$K_{2n} = Q_{1n}'$$

Next state equation:

$$\begin{aligned} Q_{1n+1} &= J_{1n} Q_{1n}' + K_{1n}' Q_{1n} \\ &= x_1' Q_{1n}' Q_{2n}' + x_1' Q_{1n} \end{aligned}$$

$$\begin{aligned} Q_{2n+1} &= J_{2n} Q_{2n}' + K_{2n}' Q_{2n} \\ &= (x_1 + Q_{1n}) Q_{2n}' + Q_{1n}' Q_{2n} \\ &= x_1 Q_{2n}' + Q_{1n} Q_{2n}' + Q_{1n}' Q_{2n} \end{aligned}$$

Present state $Q_{2n} Q_{2n}$	Next state $Q_{2n+1} Q_{2n+1}$		Output Z Input x	
	$x=0$	$x=1$	0	1
00	1 0	0 1	0	0
01	0 0	0 0	0	1
11	1 1	0 1	1	0
10	1 1	0 1	0	0

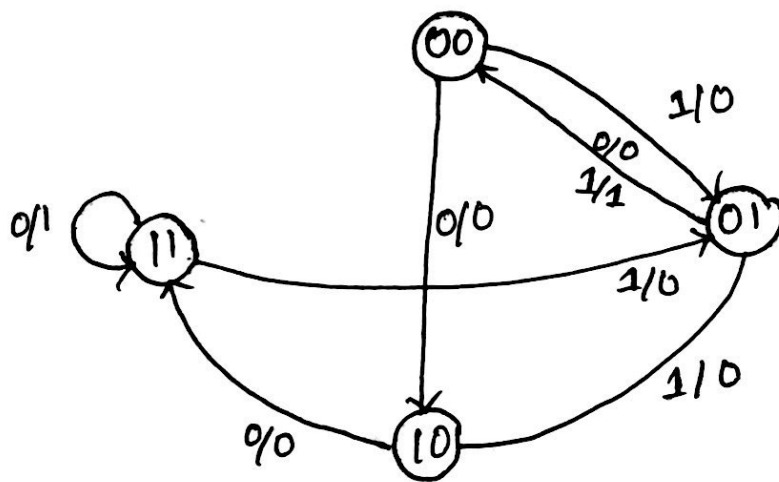


Fig: Transition diagram.

Answer to the Question No: 04

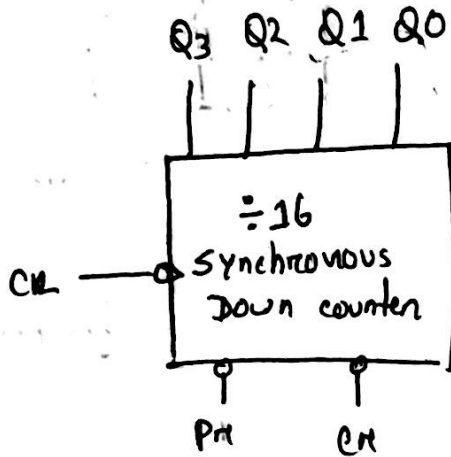


Fig: block - diagram.

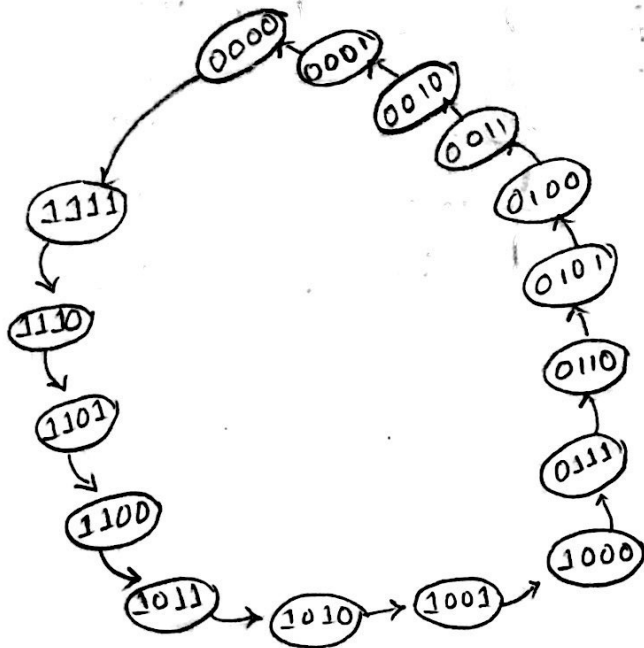


Fig: Transition diagram.

Count Sequence

Q3	Q2	Q1	Q0
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0
1	1	1	1

Excitation table :

Present state $Q_3n \ Q_2n \ Q_1n \ Q_0n$				Next state $Q_3n+1 \ Q_2n+1 \ Q_1n+1 \ Q_0n+1$				FlipFlop input $T_3 \ T_2 \ T_1 \ T_0$			
0	0	0	0	1	1	1	1	1	1	1	1
0	0	0	1	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	1	0	0	1	1
0	0	1	1	0	0	1	0	0	0	0	1
0	1	0	0	0	0	1	1	0	1	1	1
0	1	0	1	0	1	0	0	0	0	0	1
0	1	1	0	0	1	0	1	0	0	1	1
0	1	1	1	0	1	1	0	0	0	0	1
1	0	0	0	0	1	1	1	1	1	1	1
1	0	0	1	1	0	0	0	0	0	0	1
1	0	1	0	1	0	0	1	0	0	1	1
1	0	1	1	1	0	1	0	0	0	0	1
1	1	0	0	1	0	1	1	0	1	1	1
1	1	0	1	1	1	0	0	0	0	0	1
1	1	1	0	1	1	0	1	0	0	1	1
1	1	1	1	1	1	1	0	0	0	0	1

③

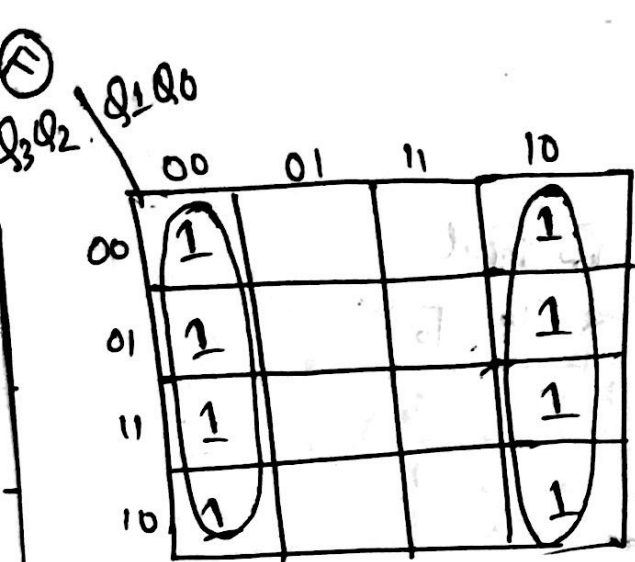
$Q_2n \ Q_1n$	00	01	11	10
00	1	1		
01				
11				
10	1			

$$T_3 = Q_2' Q_1' Q_0'$$

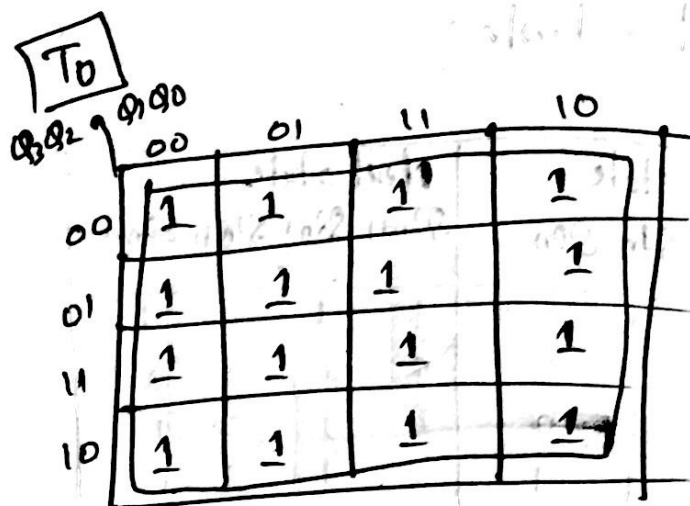
②

$Q_3n \ Q_2n$	00	01	11	10
00	1			
01	1			
11	1			
10	1			

$$T_2 = Q_1' Q_2'$$



$$T_1 = Q_0'$$



$$T_0 = 1$$

Here,

$$T_3 = Q_2' Q_1' Q_0'$$

$$T_2 = Q_1' Q_2'$$

$$T_1 = Q_0'$$

$$T_0 = 1$$

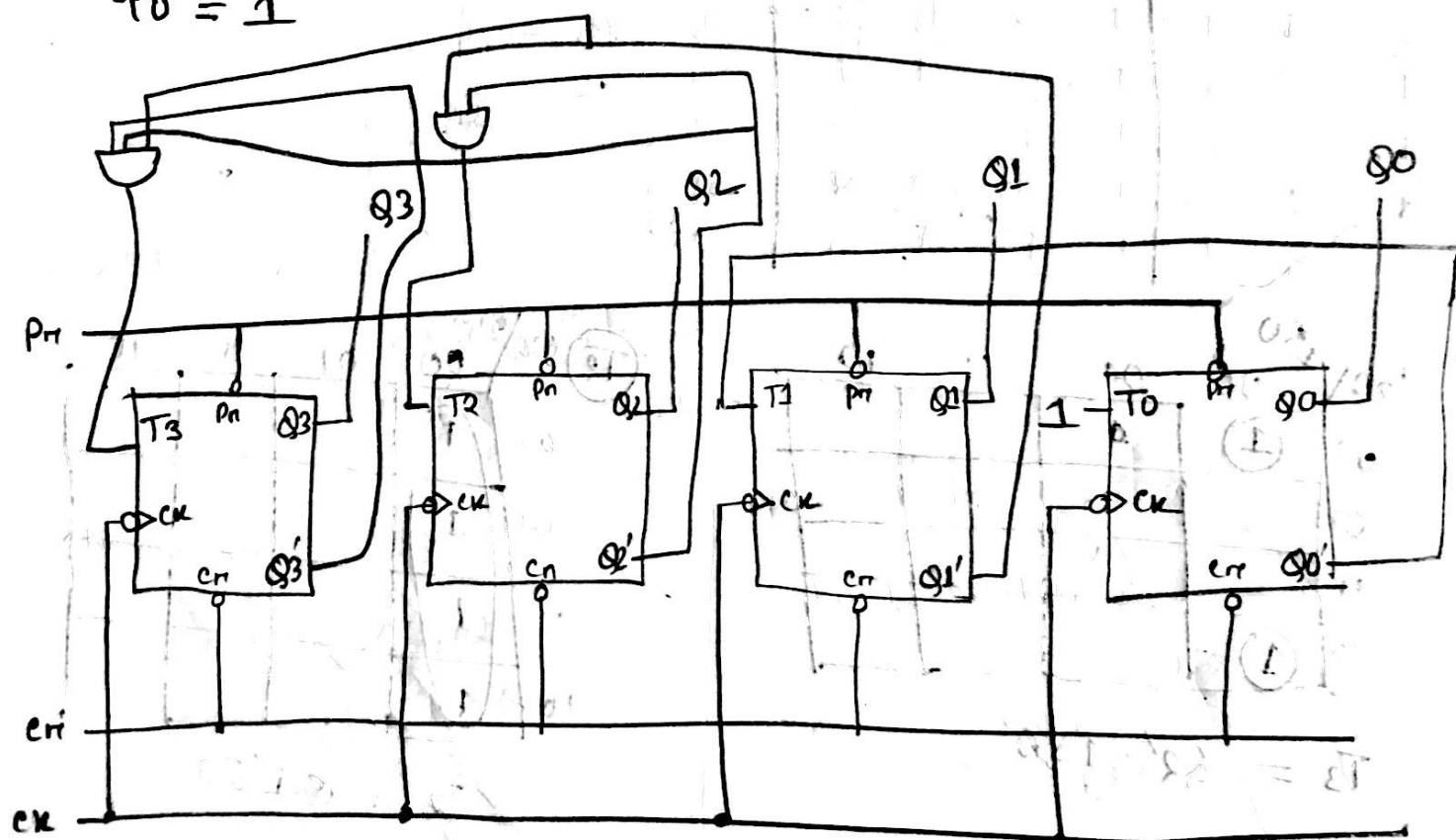


Fig: Logic diagram.