Block Diograms

Assignment-3

DMy PC:

i) System Description:

- · AMD Ryzen 5 1600
- · Number of Corces: 6
- · Number of Threads: 12
- · Base Clock Speed: 3.2 GLHz
- . PSU: 550 W

ii) Main Memory Specification:

- · 8 GLB DDR4 Rom
- · Speed: 3200 MHZ
- · Type: DDR4
- · Slots: 2 (Dual-channel)

2. Instruction Set Related Spilos to and suntani.

· 518 (GB NVME SSDEN Ocho) 42-385 : A21.

Supports SIMD Extensions: 8984, ATSE, AVXX

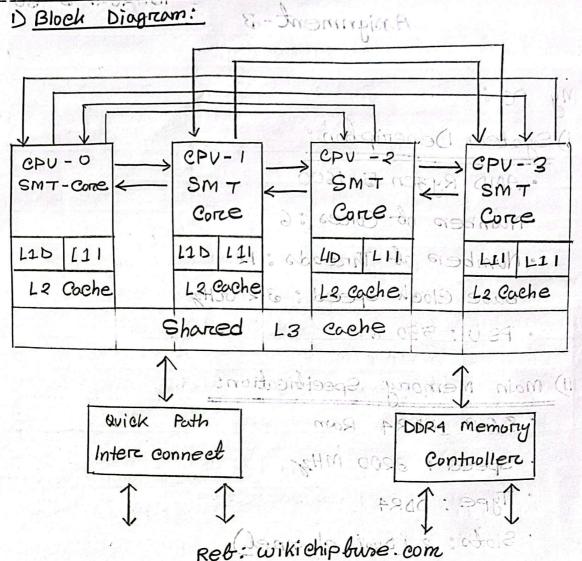
Write speed: Up to 2700 mB/s

3. Specification:

· Pipeline Details: 14 stage poline boto throughput.
· Muthiple house Details Supported Hyper Thresaling
Technology (SMT)

. Owle Memory Details:
-> 11 enche - 32 KB Fer Cone.
-> 12 cache - 256 KB Fer Cone.

D Block Diagram:



2. Instruction Set Related Specification:

- · 15A: 286-64 (also known as 264)
- · Supports SIMD Extensions : 35E4, AVX, AVX2
- · Instruction Fetch, Decode Execute Memory Access, white whack stages: 69990 staring

3. Specification:

- · Pipeline Details: 14 stage Apline boss throughput.
- Details: Supports Hyper Threading · Multiple Imue Technology (SMT)
- . Cache Memory Details:
 - → L1 cache 32KB Per Cone
 - -> L2 cache 256 kB per core

· Bus: Direct Media Interbace (DMI) 3.0 · Interrupt: Advanced Programmable Interrupt controller · I/O : PC 3.0 JUSB 3.1 · DMA: integrated Directed Memory Access controller A77) E3 Quehe (4nr shorred) Adreno (50 out Conophies Procession Unit) Hexagen 600 DSP Specifica 489 1517 Memory Controller (LPDDRS) - E LEE b) my mobile Phone: (OPRO) = IA i) System Discription: 32 82x) maboun · Processors: Media Tek Dimensity 8100 - Masc · Number of cones: 8 · Conbig: Octo - core (4 x Contex - A78 at 285 orth + 4x Cortex - ASS at 2.0 GHz) · manu bacturing Procession minis advingare. · Instruction Fetch, Decode, Gue oute, memory Access 2. Main mamory specification ind stinos bus · 8 GB LPDDR5 RAM · Speed: 2750 MHz : GNOWDID 19 1992 . E. · Pipelining Detwins Out of Page 14 & 20 Third with a 10 stage pipeline. in storage Details: sighisted such sighten. 1911916 93.256 CCB UES 13:0 -· Read speed: (Up to 2100 MB/S write speed: (Up to 1200 MB/S) > LQ COCKE: I MB (A77) + SIR WB (A55) -> 13 eache: 4 mB shaned

-> L3 cache: 12 MB Sharred

allocation probable

ii) Processon Details?

· Block Diagram: Direct media Infortace (DM : margard Asoll (

Prime Core (Contex - A77) \$2.84 GHz L3 Cache (4MB shared) Adreno 650 GPU (Graphics Processor Unitex agon 698 DSP Spectra 480 19P Memory Controller (LPDDR5)								
(Contex - A77) \$2.84 Gilly Corres (x3) Contex - A77) 2.42 Gilly L3 Cache (4MB shared) Adreno 650 GPU (Graphics Processors Unitex agon 698 DSP Spectra 480 ISP Memory Controller (LPDDR5)	instal Shi	ennope	tennuple	tal Sna	pdragon	865	egrov bf	ाः चेत्राम
(Contex - A77) \$2.84 GHz L3 Cache (4MB shared) Adreno 650 GPU (Grophics Processors Unitex agon 698 DSP Spectra 480 19P Memory Controller (LPDDR5)	one Pe	me Cone	ne Core	Pe	re bor ma	nce 6	Bicien	ey cores
S2.84 GHZ L3 Cache (1MB shared) Adreno 650 GPU (Grophics Processors Uni- Hexagon 698 DSP Spectra 480 19P Memory Controller (LPDDR5)	A77) C	tex - A77	ex - A77)) Co	nes (x3) / (a	Contex -	A55)
Adreno 650 GPU (Grophics Processors Uni- Hexagon 698 DSP Spectra 480 19P Memory Controller (LPDDR5)	Citize (Co	2. 84 Gulla	· 84 Octizy	y (Con	1ex - A77 42 GH3	20110	1.8 G	HZ
Hexagon 698 DSP Spectra 480 ISP Memory Controller (LPDDR5)	L3 @			L3 Ca	che (1n	18 sha	red)	
Spectra 480 19P Memory Controller (LPDDR5)	650 GPU	Ireno C	reno 69	550 GPU	Corrophi	es Pro	eemon	Unit)
memory Controller (LPDDR5)	Hexago			Hexagor	7 698	DSP		
	Spectn			Spectru	x 480 19	3P		44 - JA
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Modem (255 5G modem) mesons	lodem (25	Mode	Mode	em (25	5 5G n	nodem	Did ms	mens (1
Connectivity (with Bluetooth)						The second secon	The state of the s	109.
I/O Intentuces (USB 3.1)	I/O Inter	I/0	I/0	Inten	buees (USB 3	3.1)	1.40

+1.3 coche: 12 MB Shoned

Ret: bone area. Com

2. Instruction related in bo: 000 - atoo : Bidnos.

- ·ISA ARM V8-A XXXXIII OF T
- · Supports SIMD Extensions! NEON -
- and write back otages of Francis nich s

3. Specifications:

- · Pipelining Details: Out of orders execution with a 10 stage Pipeline.
- · Multiple Losue Details: Supports big Little architecture bor powers efficiency

Speed: 2750-MHz

- · Cache memory Details:
 - → LI cache: 64 KB (1) + 69 KB (D) Per cone
 - -> Le cache: 1 MB (A77) + 512 NB (ASS)
 - -> 13 eache: 4 MB shared

- · Bus : AXJ , AHB
- · Interrupt: Generie Interrupt Controller
- · I/O : USB 3.1, PCle 3.0 5047 55 MTS
- · DMA: Integrated DMA controller

System Bus

1) Rucessor pelly

SHB

Flush Mermores (I MB)

SRAM (192 KB)

C) Recent & Popular Embedded micro (Controllep: STM 32 F1902 (VGTG quotal begades) ketan) EIVA

i) System Description:

- 1. Processon Specification sacquis (samenes)
 - · Cone: ARM Contex-MAIX (198x8)
 - · Clock speed: 168 mHz x 8)
 - Flash memory 1 MB 1 Relocted lives ? Trashrotton Set Relocted lives !
 - · SRAM: 192 KB January M TV MAR: AST .
- . and involve 921 MSIA: and involve of MIZ attropped.
 - Internal SRAM: 192 KB . 194.90 not surtent.
 - external SRAM, PSRAM, NOR NAND memory
 - Pipplining Details: 3 stage (betch, decode, exceeds). 3. Storage Details: Single: Willey a sporate. 8.
 - · Embedded Flash: 1 MB = yourself show.
 - · External storage: Support bor external NAND/NOR blash via FSMC

· I/o: GRP10, UART, SPI, 120, CAN, USB.

ii) Processor Details?

1. Block Diagram:

STM 32F 407 VOT69 1.8 820 : 013
Coretex = M4 Amd betwigst M Amc
System Bus
AHB
Flash Memory (1 MB)
SRAM (192 KB)
Recent & Pepular Entrollering and Among Theorem
NVIC (Nested vectored Interupt (Controller) = 81 17 2
Timepo: mois-jimocad matique (i
(General Purpose I/0; 82 pins) 9000000 .1
(3xSPI, QxIRS), IX Quad SPI)A STO
[3x I2(C)) 231 : 63972 15019;

SHA : EXA : OND.

Intercrupt: branspic Interrupt

Ret: researchgate.com

2. Instruction Set Related Inbo:

- · ISA: ARM V 7 M (Thumb-2) > Sel: MA93.
- · Supports SIMD Extensions: ARM DSP extensions.
- Access and write back stages.

b 3. Specibications: MASS Junios 30

· Pipelining Debits: 3 stage (betch, decode. execute)

· Embedded Floah

- · Multiple Issue details: Single issue!
- Cache Memory details -
- Instruction cache: 4KBorota Jones
 - -> Data cache : AKBFION JOHAN
 - · I/O: GP10, UART, SPI, IRC, CAN, USB
 - · DMA: 16 otream DMA controllers.

```
(iii) Application and Programming?
  Application:
     -> Industrial Control system
     -> medical device
     -> Consumer electronies
    Setup in Install STMBQ Cube IDE
    -> Connect STM 32407 Vate to the Pe via ST-link
  Example Code:
   # include "stm32f-4xex.h"
     void delay (vint 32 t court) {
      Cown - NOP C);
         while (count - -) {
   int main (void) f
```

```
nt main (void) {

RCC -> AHBIENR! = RCC _ AHBINR - GPIOGEN;

GPIOG > MODER! = GPIO_MODER_13_0;

while (1) {

CRPIOG -> ODR = GPIO_DDR_ODR_13;

delay (5000000);

}
```