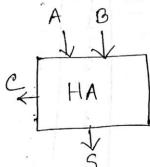
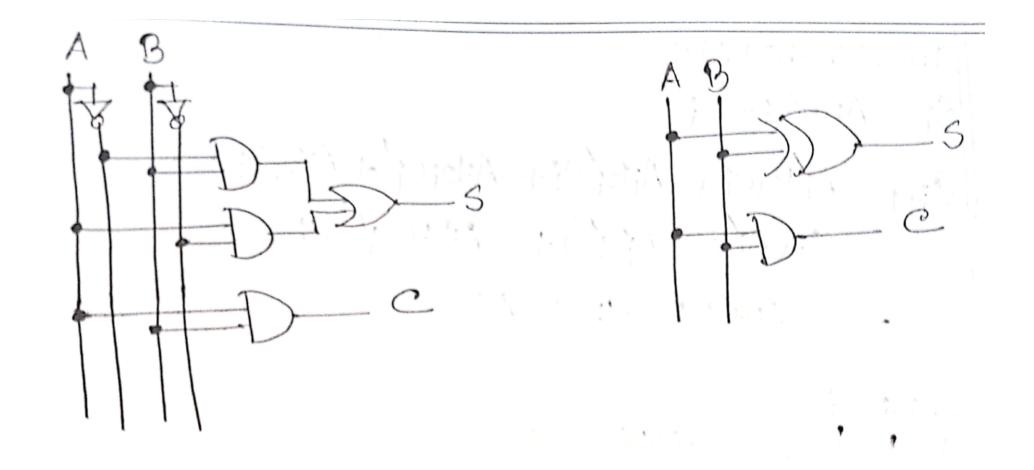
Chapter 7 Arithmetic and Comparator Circuits

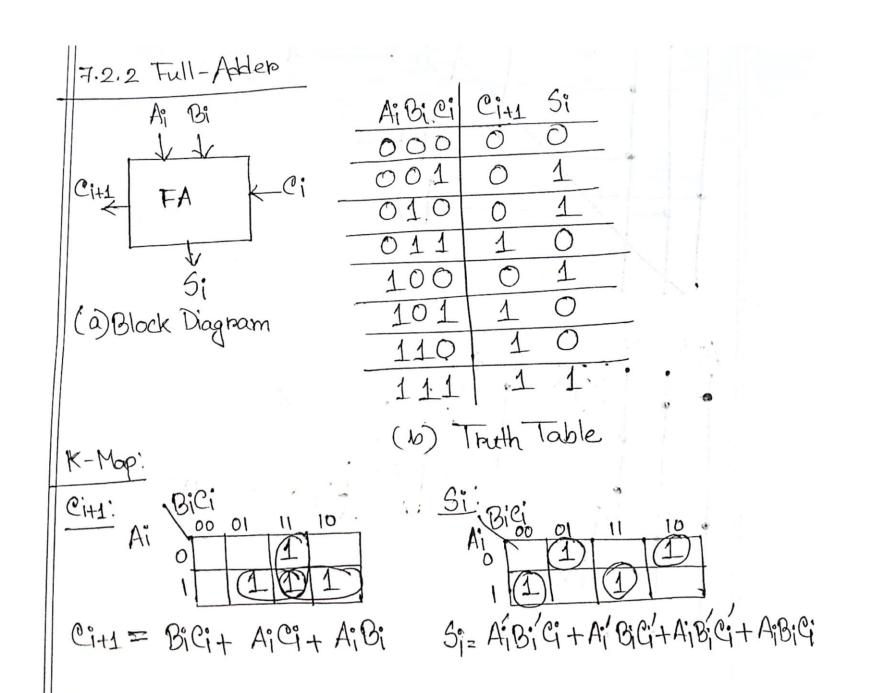
1) Half - Adder (HA) 11) Full - Adder (FA) 7.2.1 Half Adder (HA)

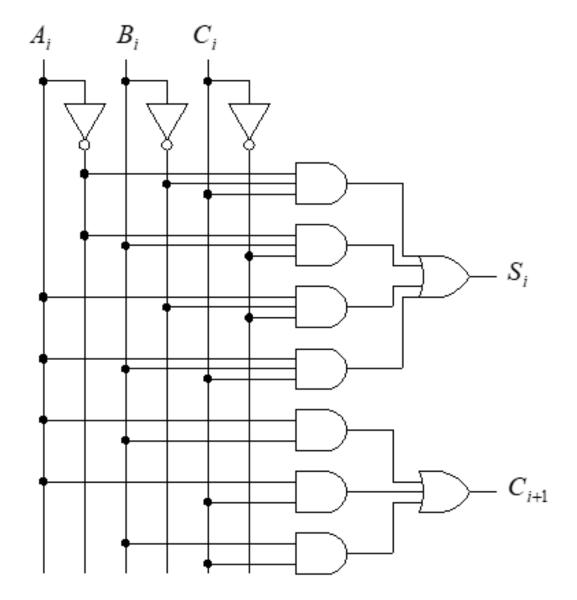


(a) Block diagram

$$C = AB$$



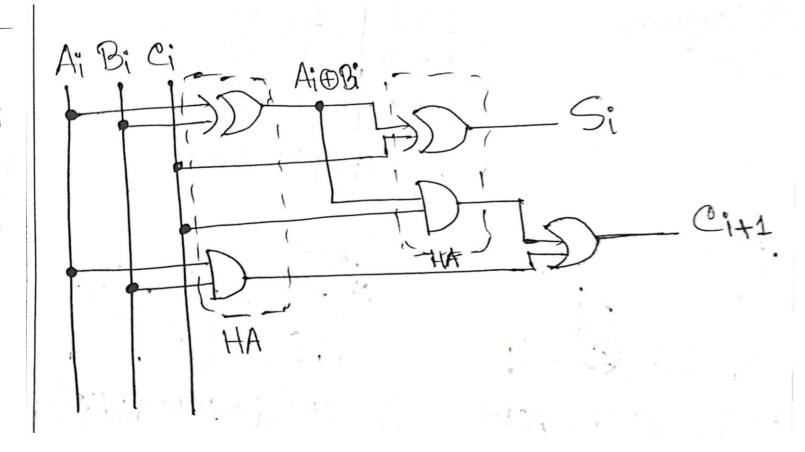


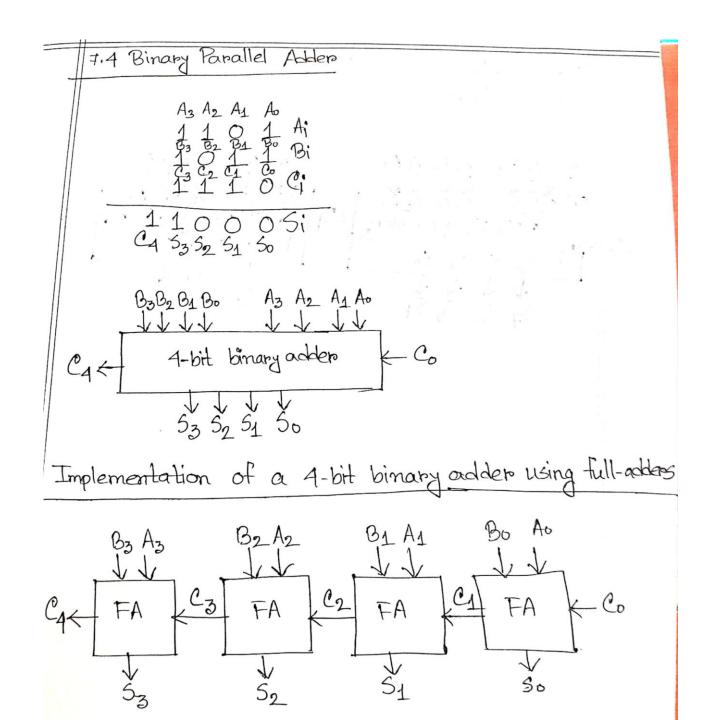


Ai Bi Ci	Ci+1	51	45
000	0	\mathcal{O}	
001	0	1_	
010	0	1	
011	1	0	1
100	0	1	-
101	1	0	
110	1	0	\$ 10°.
111	-1	1	
(b)	Truth	Table	ý

From Truth Table:
Si = Ai & Bi & Ci
Ci+1 = AiBiCi + AiBiCi + AiBiCi + AiBiCi
= C; (A; B; +A; B;) + A; B; (C; +C;)
= (Ai DBi) Ci + AiBi

From Truth Table: Si = Ai \Bi \Bi \Ci Ci+1 = Ai Bi Ci + Ai Bi Ci + Ai Bi Ci = Ci (Ai Bi + Ai Bi) + Ai Bi (Ci + Ci) = (Ai \Bi) Ci + Ai Bi





Implementation of a 8-bit binary adder using 4-bit AT AG AS AT

