

Chapter 11

Registers and Counters

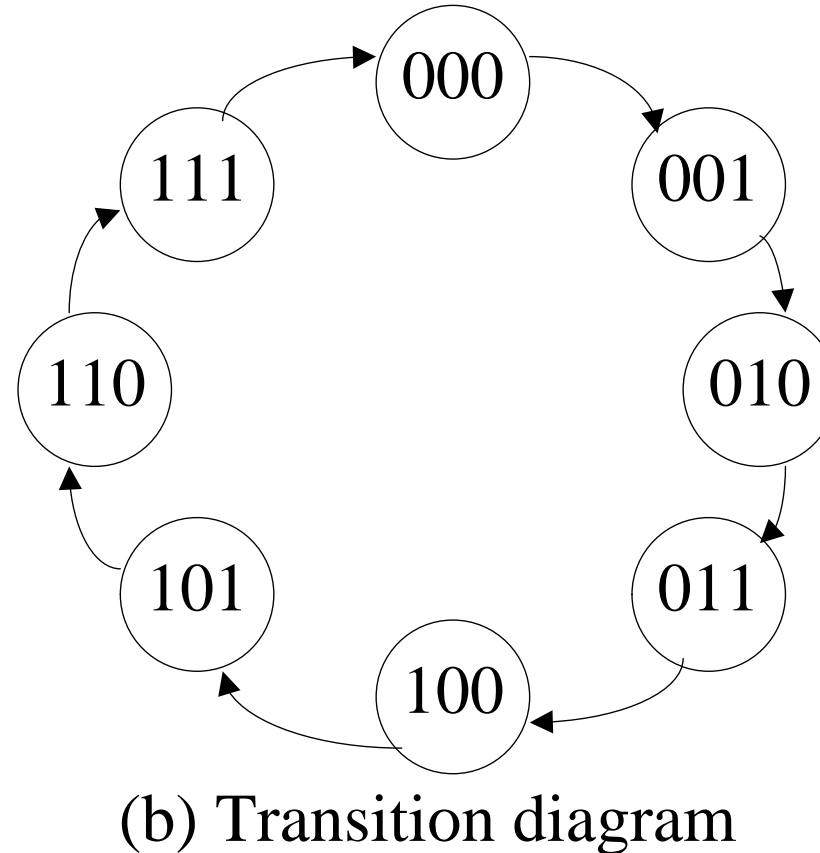
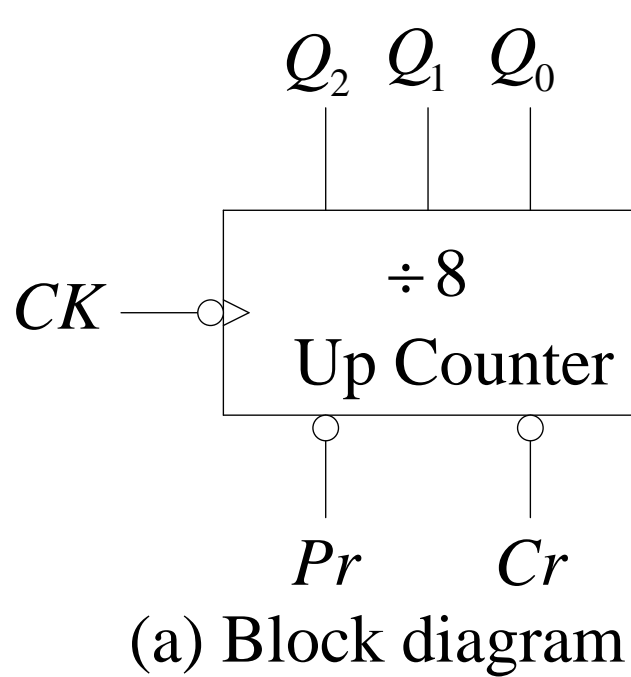
Counters

Counters and Their Classification

- Based on Count Order
 - Up Counter
 - Down Counter
- Based on Operating Mode
 - Asynchronous Counter (All FFs are not controlled by the same clock)
 - Synchronous Counter (All FFs are controlled by the same clock)

Binary Asynchronous Counters

Binary Asynchronous $\div 8$ Up Counter



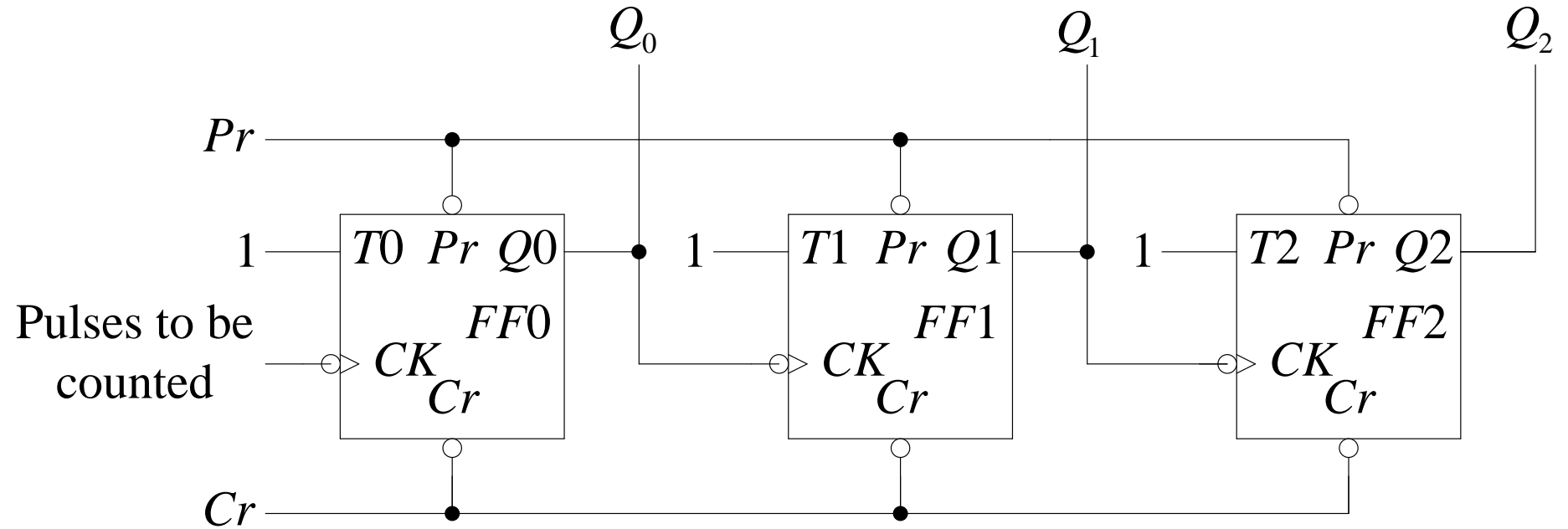
Count Sequence

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0

Binary Asynchronous Counters (Contd.)

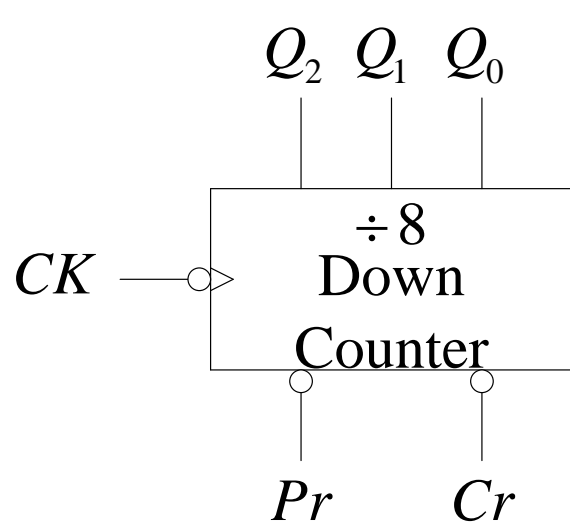
Count Sequence

Q_2	Q_1	Q_0
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1
0	0	0

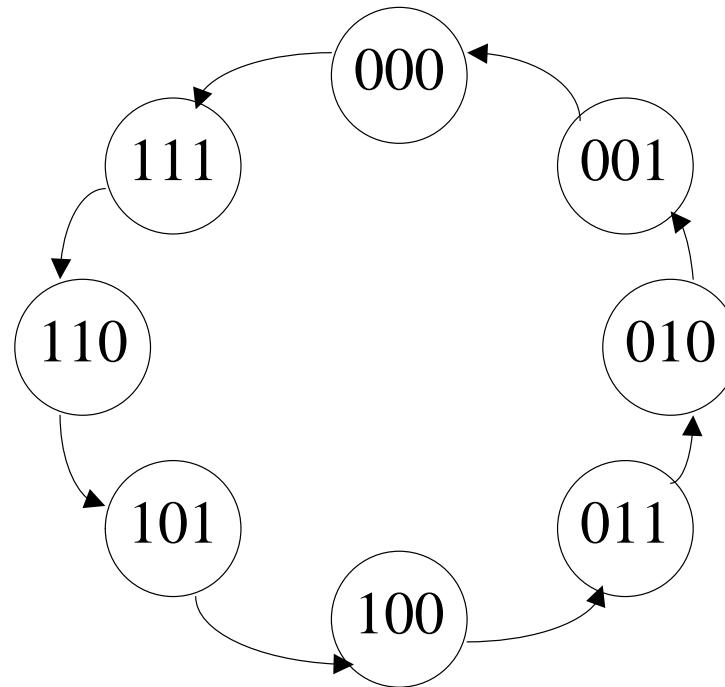


Binary Asynchronous Counters (Contd.)

Binary Asynchronous $\div 8$ Down Counter



(a) Block diagram



(b) Transition diagram

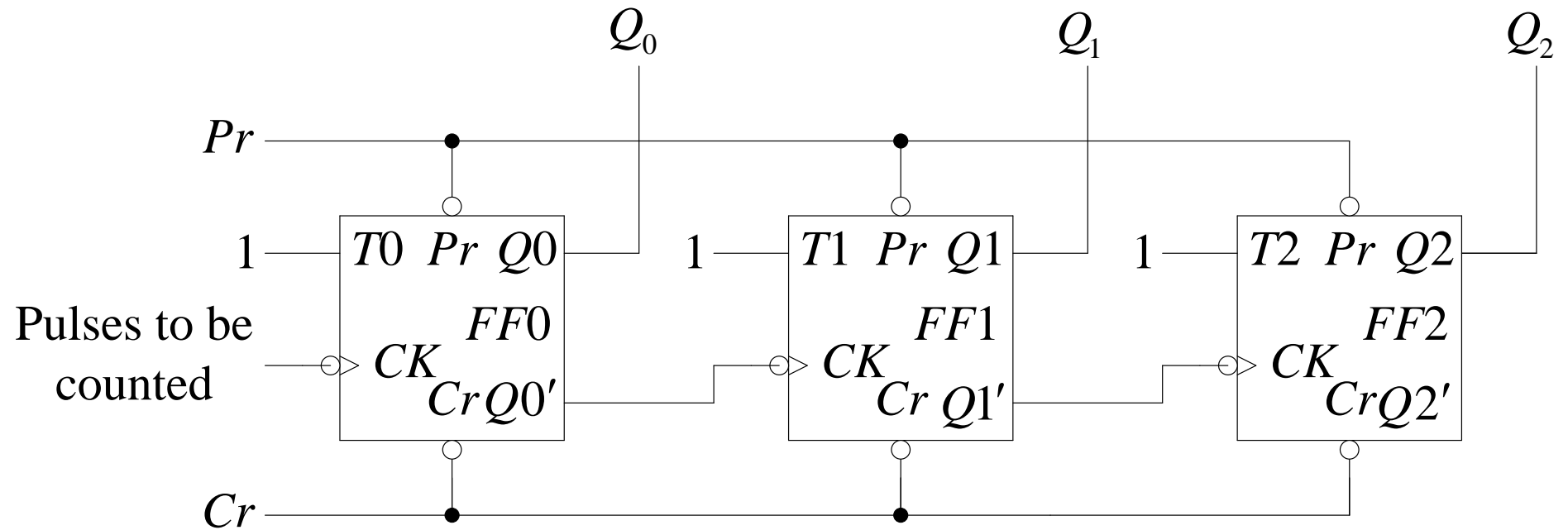
Count Sequence

Q_2	Q_1	Q_0
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0
1	1	1

Binary Asynchronous Counters (Contd.)

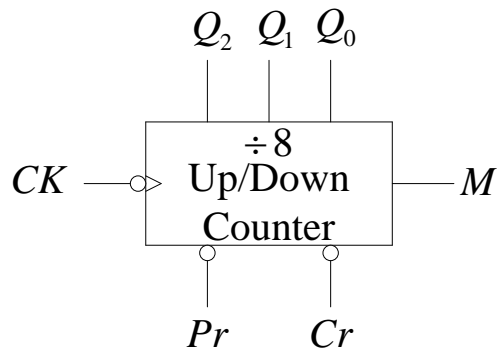
Count Sequence

Q_2	Q_1	Q_0
1	1	1
1	1	0
1	0	1
1	0	0
0	1	1
0	1	0
0	0	1
0	0	0
1	1	1

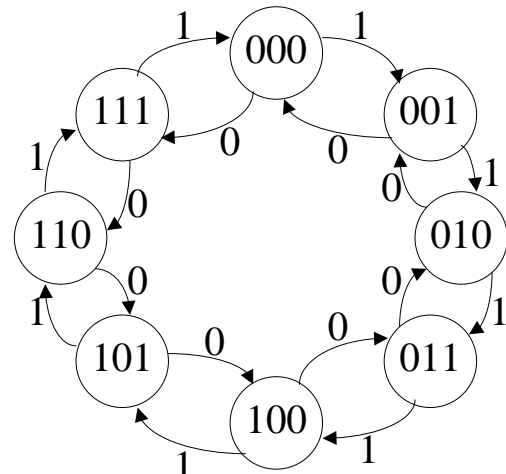


Binary Asynchronous Counters (Contd.)

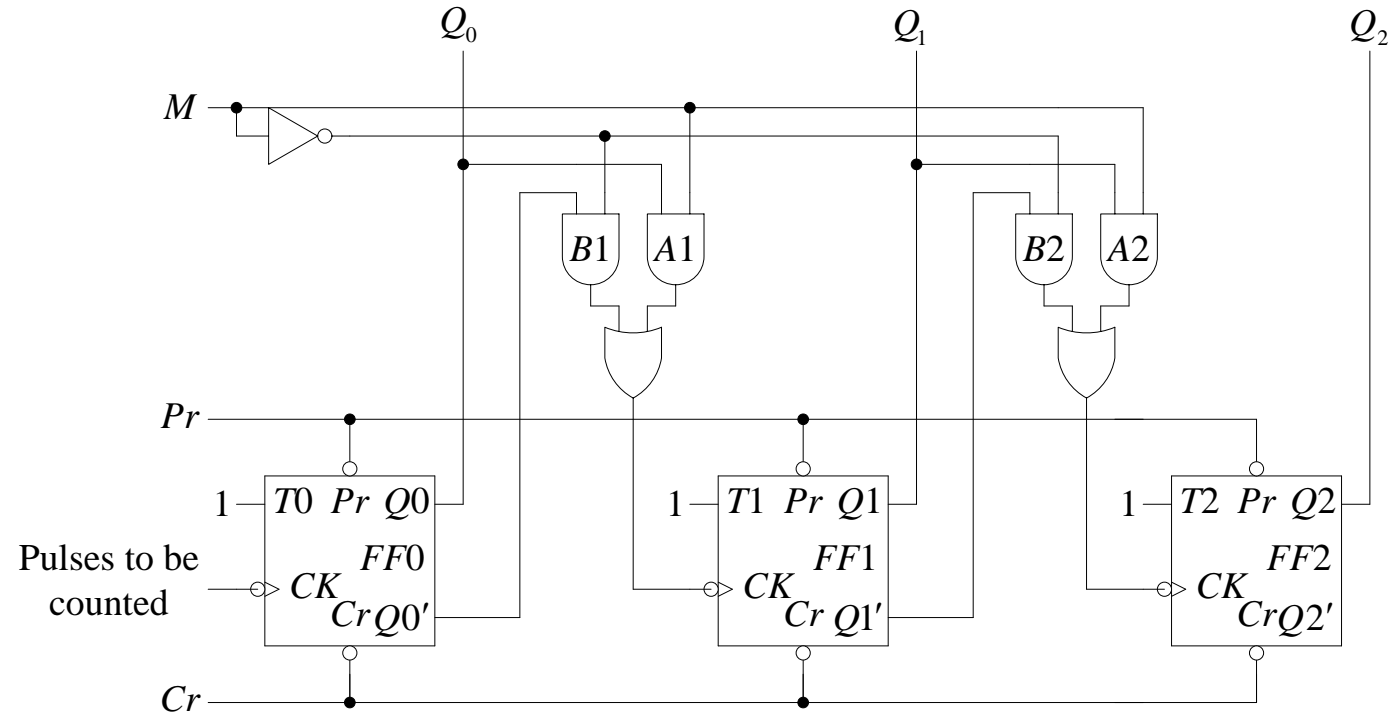
Binary Asynchronous $\div 8$ Up/Down Counter



(a) Block diagram



(b) Transition diagram



Binary Synchronous Counters

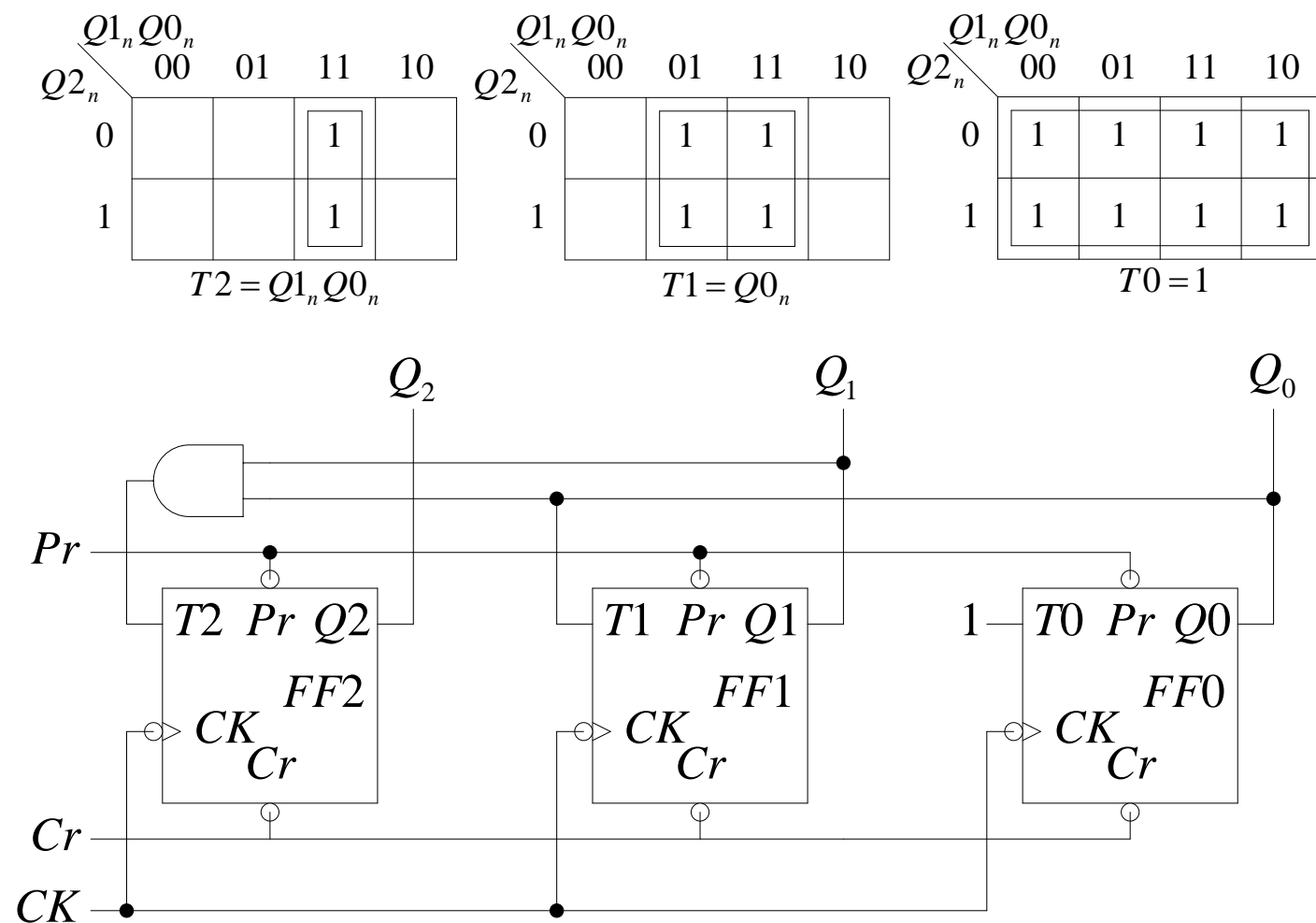
Binary Synchronous Up Counter

Excitation Table:

Present State $Q_{2n} Q_{1n} Q_{0n}$			Next State $Q_{2n+1} Q_{1n+1} Q_{0n+1}$			Flip-Flop Inputs $T_2 T_1 T_0$		
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1

Binary Synchronous Counters (Contd.)

Present State $Q2_n Q1_n Q0_n$	Next State $Q2_{n+1} Q1_{n+1} Q0_{n+1}$	Flip-Flop Inputs $T2 T1 T0$
000	001	001
001	010	011
010	011	001
011	100	111
100	101	001
101	110	011
110	111	001
111	000	111



Binary Synchronous Counters (Contd.)

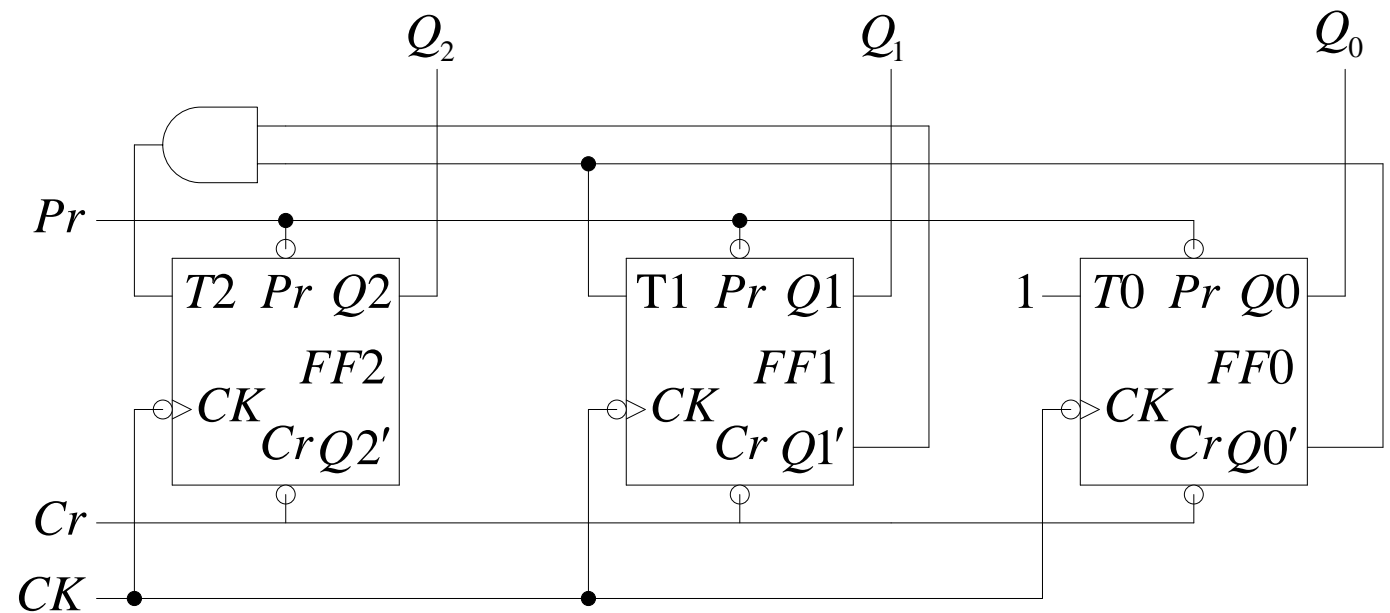
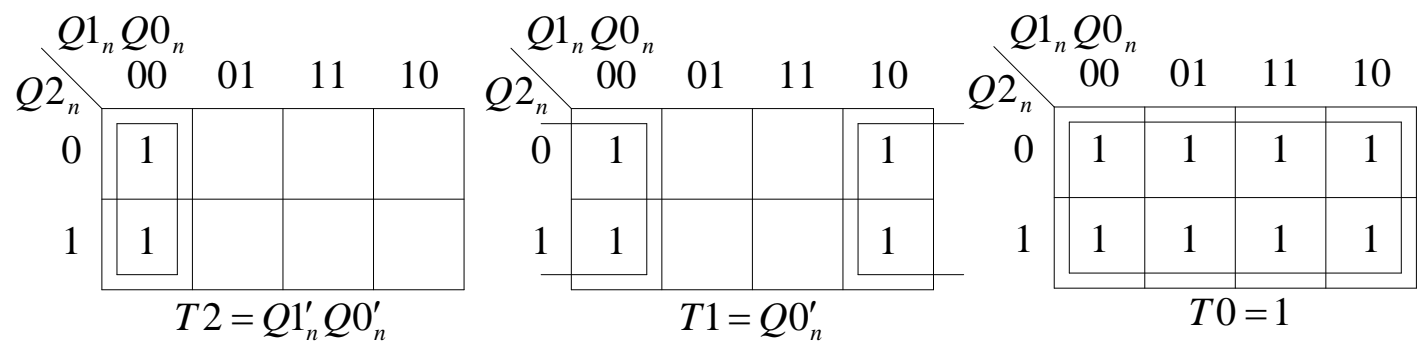
Binary Synchronous Down Counter

Excitation Table:

Present State $Q_{2n} Q_{1n} Q_{0n}$			Next State $Q_{2n+1} Q_{1n+1} Q_{0n+1}$			Flip-Flop Inputs $T_2 T_1 T_0$		
0	0	0	1	1	1	1	1	1
0	0	1	0	0	0	0	0	1
0	1	0	0	0	1	0	1	1
0	1	1	0	1	0	0	0	1
1	0	0	0	1	1	1	1	1
1	0	1	1	0	0	0	0	1
1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	0	0	1

Binary Synchronous Counters (Contd.)

Present State $Q2_n Q1_n Q0_n$	Next State $Q2_{n+1} Q1_{n+1} Q0_{n+1}$	Flip-Flop Inputs $T2 T1 T0$
000	111	111
001	000	001
010	001	011
011	010	001
100	011	111
101	100	001
110	101	011
111	110	001



Binary Synchronous Counters (Contd.)

Binary Synchronous Up/Down Counter

Excitation Table of a ÷8 Up/Down Synchronous Counter

Present State $Q_{2n}Q_{1n}Q_{0n}$	Next State $Q_{2n+1}Q_{1n+1}Q_{0n+1}$		Flip-Flop Inputs T2T1T0	
	$M=0$	$M=1$	$M=0$	$M=1$
0 0 0	1 1 1	0 0 1	1 1 1	0 0 1
0 0 1	0 0 0	0 1 0	0 0 1	0 1 1
0 1 0	0 0 1	0 1 1	0 1 1	0 0 1
0 1 1	0 1 0	1 0 0	0 0 1	1 1 1
1 0 0	0 1 1	1 0 1	1 1 1	0 0 1
1 0 1	1 0 0	1 1 0	0 0 1	0 1 1
1 1 0	1 0 1	1 1 1	0 1 1	0 0 1
1 1 1	1 1 0	0 0 0	0 0 1	1 1 1

		Q_0M			
		00	01	11	10
Q_2Q_1	00	1			
	01			1	
	11			1	
	10	1			

$$T2 = Q_1'Q_0'M' + Q_1Q_0M$$

		Q_0M			
		00	01	11	10
Q_2Q_1	00	1		1	
	01	1		1	
	11	1		1	
	10	1		1	

$$T2 = Q_0'M' + Q_0M$$

		Q_0M			
		00	01	11	10
Q_2Q_1	00	1	1	1	1
	01	1	1	1	1
	11	1	1	1	1
	10	1	1	1	1

$$T0 = 1$$

Binary Synchronous Counters (Contd.)

		$Q_0 M$			
		00	01	11	10
Q_2	Q_1	1			
	00				
Q_2	01			1	
	11			1	
Q_2	10	1			
	00				

$T2 = Q_1' Q_0' M' + Q_1 Q_0 M$

		$Q_0 M$			
		00	01	11	10
Q_2	Q_1	1		1	
	00				
Q_2	01	1		1	
	11	1		1	
Q_2	10	1		1	
	00				

$T2 = Q_0' M' + Q_0 M$

		$Q_0 M$			
		00	01	11	10
Q_2	Q_1	1	1	1	1
	00				
Q_2	01	1	1	1	1
	11	1	1	1	1
Q_2	10	1	1	1	1
	00				

$T0 = 1$

