East West University
Department of Computer Science and Engineering

Course: CSE345 Digital Logic Design
Expt No.: 6
Title: Multiplexer and Its Use in Combinational Logic Implementation

Objectives:

1. To implement and test a 4-to-1-line multiplexer with active-LOW enable input using random gates.
2. To implement and test combinational logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input).

Theory:

Design of multiplexers using random gates is discussed in Section 8.7 of textbook 1. The IC 74151 (8-to-1-line multiplexer with active-LOW enable input) is introduced in Section 8.7 of textbook 1. Combinational logic implementation using multiplexers is also discussed in Section 8.7 of textbook 1.

Pre-Lab Report Questions:

Implementing and testing a 4-to-1-line multiplexer with active-LOW enable input using random gates:

1. Write the truth table of a 4-to-1-line multiplexer with active-LOW enable input.
2. Draw the logic diagram of a 4-to-1-line multiplexer with active-LOW enable input using random gates.

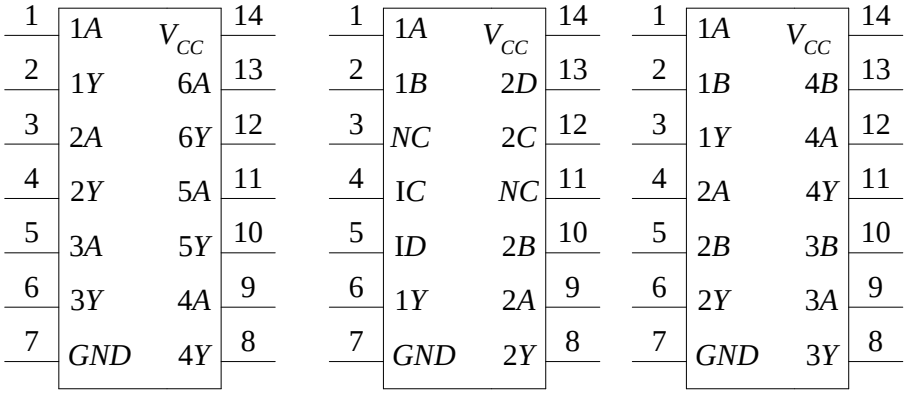
Implementing and testing combinational logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input):

3. Prepare the implementation table for implementing the combinational logic function $F(A,B,C,D) = \sum(0,3,4,6,8,11,13,15)$ using an 8-to-1-line multiplexer.
4. Draw the logic diagram for implementing the above logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input).

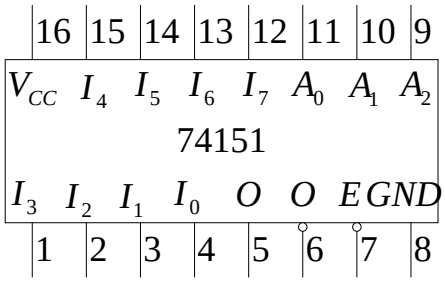
ICs Required:

7404 Hex Inverters (NOT gates)
7421 Double 4-input AND gates
7432 Quadruple 2-input OR gates
74151 8-to-1-line multiplexer with active-LOW enable input

Pin Diagram of the Required ICs:



7404 (6 NOT) **7421** (2 4-In AND) **7432** (4 2-In OR)



Lab Procedure:

Implementing and testing a 4-to-1-line multiplexer with active-LOW enable input using random gates:

1. Construct the logic diagram for a 4-to-1-line multiplexer with active-LOW enable input from your pre-lab report using random gates. Connect the four data inputs I_0 through I_3 to an arbitrary 4-bit binary number. Connect A_1, A_0, and E to three switches and the output O to an LED indicator.
2. Apply binary 00 to 11 to address lines A_1A_0 and observe the outputs by changing E input. Check that, when the circuit is enabled, the output is equal to the selected data input. Prepare the observed truth table indicating the inputs applied.

Implementing and testing combinational logic function using IC 74151 (8-to-1-line multiplexer with active-LOW enable input):

3. Construct the logic diagram for implementing the logic function $F(A,B,C,D) = \sum(0,3,4,6,8,11,13,15)$ from your pre-lab report using IC 74151 (8-to-1-line multiplexer with active-LOW enable input).
4. Prepare the truth table of the circuit and verify that it implements the given combinational logic function.

Post-Lab Report Questions:

1. Verify that all experimental outputs agree with your pre-lab report.
2. Write structural Verilog code for the logic diagram for a 4-to-1-line multiplexer with active-LOW enable input from your pre-lab report and simulate it using Quartus II software.
3. Write behavioral Verilog code for a 4-to-1-line multiplexer with active-LOW enable input and simulate it using Quartus II software.