27 May, 2021

EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Final Examination, Spring 2021 Semester

Course:	**CSE 345 Digital Logic Design, Section-2**
Instructor:	**Musharrat Khan, Senior Lecturer, CSE Department**
Full Marks:	**48 (24 will be counted for final grading)**
Time:	**1 Hour and 35 Minutes (Including submission)**

Note: There are SIX questions, answer ALL of them. Course Outcome (CO), Cognitive Level and Mark of each question are mentioned at the right margin.

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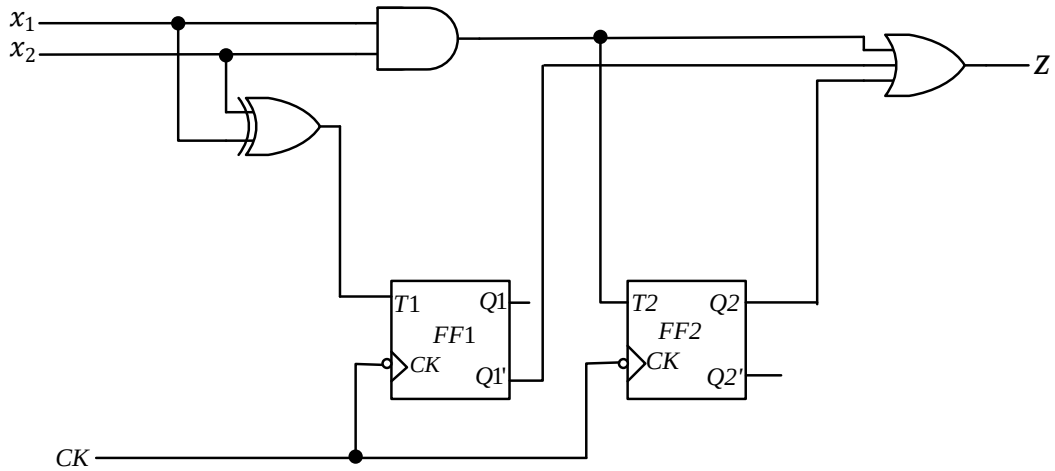
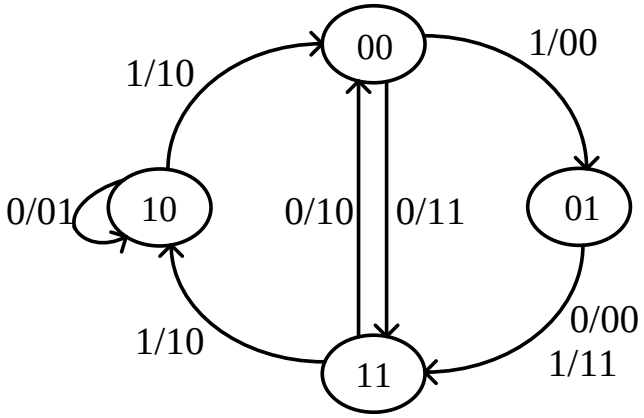
1. **Write down** next state and output equations for the following sequential circuit. From these equations **analyze** the sequential circuit and draw the transition diagram. [CO2,C4, Mark: 8]



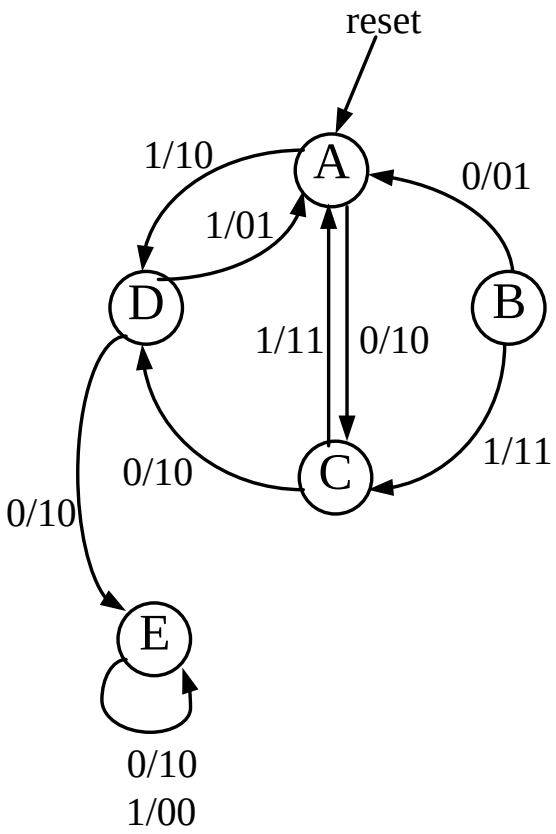
2. **Design** a sequential circuit represented by the following state diagram using J-K flip-flop. [CO3,C3, Mark: 8]



3. **Design** a 3-bit parallel-in parallel-out register using D flip-flops. [Draw its block diagram, and logic diagram] [CO3,C6, Mark: 8]

4. **Design** a ÷16 synchronous up counter using T flip-flops. [Draw its block diagram, transition diagram, excitation table, equation, and logic diagram] [CO3,C6, Mark: 8]

5. **Design** a synchronous sequential circuit represented by the following state diagram using explicit style Verilog code. Assume a positive-edge clock. Also assume that reset will be done when the reset signal will go from 1 to 0. [CO3,C6, Mark: 8]



6. **Write** a behavioral Verilog code to design a 4×1 MUX with active-LOW enable input using Procedural technique using case statement. [CO3,C6, Mark: 8]