EAST WEST UNIVERSITY

Department of Computer Science and Engineering

Course Code: CSE360

Course Title: Computer Architecture

Section: 03

Semester: Spring 2024

Assignment 01

Submitted to:

Md. Ezharul Islam, Phd

Professor

Department of Computer Science and Engineering

Submitted by:

Name: B M Shahria Alam

ID: 2021-3-60-016

Date of submission: 10th March, 2024

Chapter-1

1.1 Personal computer (includes laptop): Personal computers normally delivery good performance to single user at low cost.

Server: Computer used to run large problems and usually accessed via a network.

Personal mobile device (including tablets): These devices are battery operated with wireless connectivity to the internet and typically cost a little bit and as a PC it has software which is known as 'Apps'.

Super computer: Computer composed of hundreds to thousands of processors and terabytes of memory.

1.2
a) Performance via Pipelining
b) Dependability via Redundancy
c) Performance via Prediction
d) Make the common Case Fast
e) Hierarchy of memories
f) Performance via Parallelism.
g) Design for Moore's Law
h) Use Abstraction to Simplify Design.

1.3 The program is compiled into an assembly language program, which is then asembled into a machine language program.

1.5

a) Performance of $(P_1) = \frac{\text{Clock Rate}}{\text{CPI}} = \frac{3\times10^9}{1.5} = 2\times10^9$

Performance of $(P_2) = \frac{\text{Clock Rate}}{\text{CPI}} = \frac{2.5\times10^9}{1} = 2.5\times10^9$

Performance of $(P_3) = \frac{\text{Clock Rate}}{\text{CPI}} = \frac{4\times10^9}{2.2} = 1.8\times10^9$

$\therefore$ The processor (P_3) result in the highest performance expressed in instruction per second.

b) Number of cycles $(P_1) = (\text{Time} \times \text{Clock rate})$

$$= 10 \times 3\times10^9$$
$$= 30\times10^9 s$$

$\therefore$ Number of instructions $(P_1) = \frac{\text{Number of cycle}}{\text{CPI}}$

$$= \frac{30\times10^9}{1.5}$$
$$= 20\times10^9$$

Number of cycles $(P_2) = (\text{Time} \times \text{clock rate}) = 10 \times 2.5\times10^9 = 25\times10^9 s$

$\therefore$ Number of instructions $(P_2) = \frac{\text{Number of cycle}}{\text{CPI}} = \frac{25\times10^9}{1} = 25\times10^9$

Number of cycles $(P_3) = (\text{Time} \times \text{clock rate}) = 10 \times 4\times10^9 = 40\times10^9 s$

$\therefore$ Number of instructions $(P_3) = \frac{\text{Number of cycle}}{\text{CPI}} = \frac{40\times10^9}{2.2} = 18.18\times10^9$

c) Consider the old cpu time is 10 second, time is decreased by 30%. 20% CPI increasing means 1.2x of the old CPI

$\therefore CPI_{new}(P_1) = (1.2 \times CPI_{old}) = (1.2\times1.5) = 1.8$

$CPI_{new}(P_2) = (1.2\times1) = 1.2$

$CPI_{new}(P_3) = (1.2\times2.2) = 2.6$

we know,

$$\text{clock rate} = \left(\frac{\text{Number of instruction} \times CPI}{\text{time}}\right)$$

$\therefore$ Clock rate $(P_1) = \left(\frac{20\times10^9 \times 1.8}{7}\right) = 5.14$ GHz

$\therefore$ Clock rate $(P_2) = \left(\frac{25\times10^9 \times 1.2}{7}\right) = 4.28$ GHz

$\therefore$ Clock rate $(P_3) = \left(\frac{18.18\times10^9 \times 2.6}{7}\right) = 6.75$ GHz

1.6

a) Class A : 10^5 instr
Class B : 2×10^5 instr
Class C : 5×10^5 instr
Class D : 2×10^5 instr

Time = (No. instr $\times$ CPI) / clock rate

$\therefore$ Total time $P_1 = (10^5 + 2\times10^5\times2 + 5\times10^5\times3 + 2\times10^5\times3)/(2.5\times10^9)$
$= 10.4\times10^{-4}$ s

$\therefore$ Total time $P_2 = (10^5\times2 + 2\times10^5\times2 + 5\times10^5\times2 + 2\times10^5\times2)/(3\times10^9)$
$= 6.66\times10^{-4}$ s

CPI of P1 $= (10.4\times10^{-4}\times2.5\times10^9)/10^6$
$= 2.6$

CPI of P2 $= (6.66\times10^{-4}\times3\times10^9)/10^6$
$= 2.0$

b) Clock cycle (P1) $= 10^5\times1 + 2\times10^5\times2 + 5\times10^5\times3 + 2\times10^5\times3$
$= 26\times10^5$

Clock cycle (P2) $= 10^5\times2 + 2\times10^5\times2 + 5\times10^5\times2 + 2\times10^5\times2$
$= 20\times10^5$

1.7

a) Execution time of A compiler 1.1 s
Execution time of B compiler 1.5s
we know,

$$CPI = (T_{exe} \times f) / No.instr$$

$\therefore$ Compiler A CPI = 1.1
$\therefore$ Compiler B CPI = 1.25

b) $f_B / f_A = (No.instr(B) \times CPI(B)) / (No.instr(A) \times CPI(A))$

$= (1.2 \times 1.25) / (1 \times 1.1)$

$= 1.37$

c) $T_A / T_{new} = 1.67$

$T_B / T_{new} = 2.27$

So the speedup will be in the processor A by the new T_{new}.

1.8.1

we know,

Capacitive load Processor, $C = \frac{2 \times \text{dynamic Power}}{(\text{voltage}^2 \times \text{frequency})}$

1st,

$\therefore C\ (\text{Pentium } 4) = \frac{2 \times 90}{(1.25)^2 \times 3.6 \times 10^6}$

$= 3.2 \times 10^{-3}\ F$

2nd,

$\therefore C\ (\text{Core } i5) = \frac{2 \times 40}{(0.9)^2 \times 3.4 \times 10^6}$

$= 2.9 \times 10^{-8}\ F$

1.8.2

Pentium 4 $= 10/100$

$= 10\%$

Core i5 $= 30/70$

$= 42.9\ \%$

1.10.1

1st step:

$$\text{Wafer area} = \pi \times (r^2)$$
$$= 3.14 \times \left(\frac{15}{2}\right)^2$$
$$= 176.7 \text{ cm}^2$$

$$\text{Die area} = \frac{\text{Wafer area}}{\text{dies per wafer}}$$
$$= \frac{176.7}{84}$$
$$= 2.10 \text{ cm}^2$$

~~yei~~ $$\text{yield}_{(15\text{cm})} = \frac{1}{\{1 + (\text{Defects per area} \times \text{pie area}/2)\}^2}$$

$$= \frac{1}{\{1 + (0.020 \times 2.10/2)\}^2}$$

$$= 0.959$$

2nd step

$$\text{wafer area} = \pi r^2$$
$$= 3.14 \times \left(\frac{20}{2}\right)^2$$
$$= 314 \text{ cm}^2$$

$$\text{Die area} = \frac{\text{wafer area}}{\text{dies per wafer}}$$
$$= \frac{314}{100}$$
$$= 3.14 \text{ cm}^2$$

$$\text{yield}_{(20\text{cm})} = \frac{1}{\{1 + (\text{Defects per area} \times \text{pie area}/2\}^2}$$

$$= \frac{1}{\{1 + (0.031 \times 3.14/2\}^2}$$

$$= 0.910$$

1.10.2

$$\text{Cost per die}_{(15cm)} = 12/(84 \times 0.9593)$$
$$= 0.1489$$

$$\text{Cost per die}_{(20\,cm)} = 15/(100 \times 0.9093)$$
$$= 0.1650$$

1.10.3

$$\text{die area}_{(15\,cm)} = \text{wafer area/dies per wafer}$$
$$= \{3.1416 \times (7.5)^2\}/(84 \times 1.1)$$
$$= 1.91\ cm^2$$

$$\text{yield}_{(15\,cm)} = 1/(1+(0.020 \times 1.15 \times 1.91/2))^2$$
$$= 0.9575$$

$$\text{die area}_{(20\,cm)} = \text{wafer area/dies per wafer}$$
$$= 3.1416 \times 10^2/(100 \times 1.1)$$
$$= 2.86\,cm^2$$

$$\text{yield}_{(20\,cm)} = 1/(1+(0.03 \times 1.15 \times 2.86/2))^2$$
$$= 0.9082$$

1.11

We know,

$$\text{Clock rate} = 1 / \text{cycle time}$$

$$\therefore \text{Clock rate} = \frac{1}{0.333\,ns}$$

$$= 3GHz$$

$$\therefore CPI = \frac{3\times10^9 \times 750}{2.389\times10^{12}}$$

$$= 0.94$$

1.12

$$\text{CPU time} = \frac{CPI \times \text{Instruction Count}}{\text{Clock rate}}$$

$$\therefore P_1(CPU) = \frac{0.9\times5\times10^9}{4\times10^9}$$

$$= 1.125\,sec$$

$$\therefore P2\,(CPU) = \frac{0.75\times1\times10^9}{3\times10^9}$$

$$= 0.25\,sec$$

Here CPU time of P_1 (CPU) = 1.125 sec greater than the CPU time of P2(CPU) = 0.25 sec the processor P2 perform better than the processor P1.

Therefore even the clock rate of the processor P1 is greater than the clock rate of P2, P2 perform better than P1 which shows that statement the computer with largest clock rate have the largest performance is false.