31 August, 2021

EAST WEST UNIVERSITY
Department of Computer Science and Engineering
Summer 2021 Semester
CSE345 Digital Logic Design, Section-3, Class Test-3
Marks:10
Time: 25 minutes

1. Design a sequential circuit represented by the following transition table using S-R Flip-Flop.

Present State $Q1_nQ2_n$	Next State $Q1_{n+1}Q2_{n+1}$		Output, z_1z_2	
	$x=0$	$x=1$	$x=0$	$x=1$
00	01	10	11	01
01	11	00	00	11
11	01	10	01	10
10	01	10	10	01