

East West University Department of Computer Science and Engineering

Course: CSE345 Digital Logic Design

Expt No.: 3

Title: Behavioral Verilog Simulation of a Combinational Logic Circuit

Objectives:

- 1. To learn behavioral Verilog coding of a combinational logic circuits using procedural model.
- 2. To learn behavioral Verilog coding of a combinational logic circuits using continuous assign statement.

Introduction:

The Boolean expression of the combinational logic circuit of Figure 1 is S = A'B + AB'. The behavioral Verilog code for the combinational logic circuit of Figure 1 using the procedural model is as follows:

```
module expt3_1 (input A, B, output reg S); always @(A, B) begin S=0; if(\simA & B) S=1; if(A & \simB) S=1; end endmodule
```

The behavioral Verilog code for the combinational logic circuit of Figure 1 using continuous assign statement is as follows:

```
\label{eq:special_continuity} \begin{split} \text{module expt3\_2 (input A, B,} \\ \text{output S);} \\ \text{assign S} = (\sim &A \& B) \mid (A \& \sim &B); \\ \text{endmodule} \end{split}
```

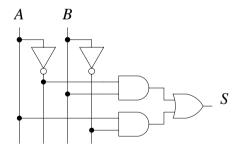


Figure 1: Example of a combination logic circuit.

See Section 14.3 of Textbook 1 for more details.

Pre-Lab Report Question:

- 1. Write behavioral Verilog code for the combinational logic circuit of Figure 2 using procedural model.
- 2. Write behavioral Verilog code for the combinational logic circuit of Figure 2 using continuous assign statement.

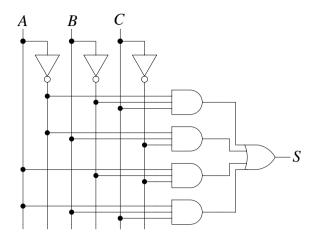


Figure 2: Combinational circuit for lab practice.

Lab Procedure:

1. Simulate both the Verilog codes from your pre-lab report using Quartus II software. Get printouts of Verilog codes and simulation outputs of both the cases in a single page and have it signed by your instructor.

Post-Lab Report Question:

- 1. Prepare the truth table of the combinational circuit of Figure 2.
- 2. Compare whether the simulation results agree with the truth table prepared in step 1.