

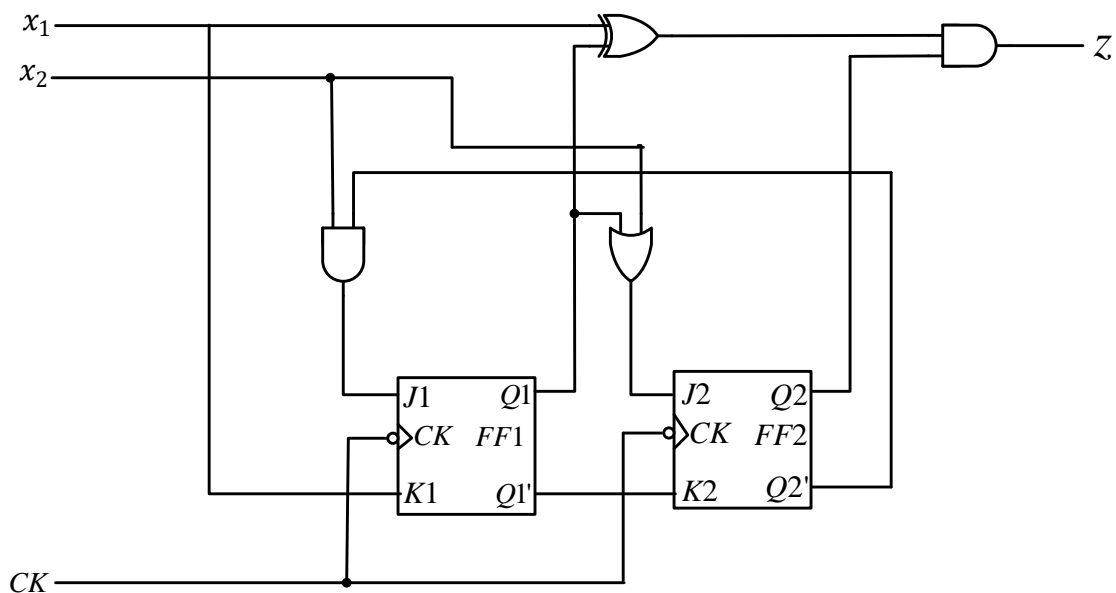


EAST WEST UNIVERSITY
Department of Computer Science and Engineering
B.Sc. in Computer Science and Engineering Program
Final Examination, Spring 2021 Semester

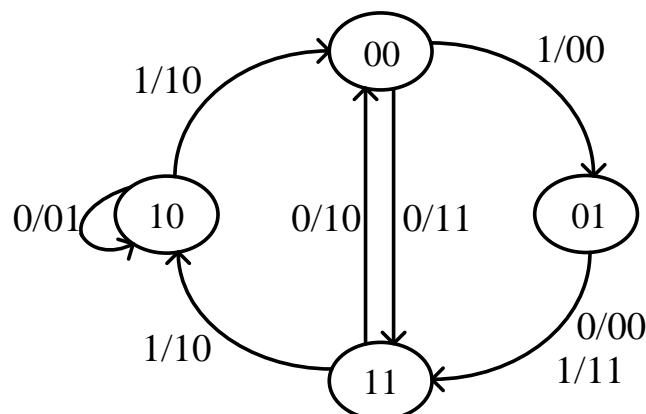
Course: CSE 345 Digital Logic Design, Section-3
Instructor: Musharraf Khan, Senior Lecturer, CSE Department
Full Marks: 48 (24 will be counted for final grading)
Time: 1 Hour and 35 Minutes (Including submission)

Note: There are SIX questions, answer ALL of them. Course Outcome (CO), Cognitive Level and Mark of each question are mentioned at the right margin.

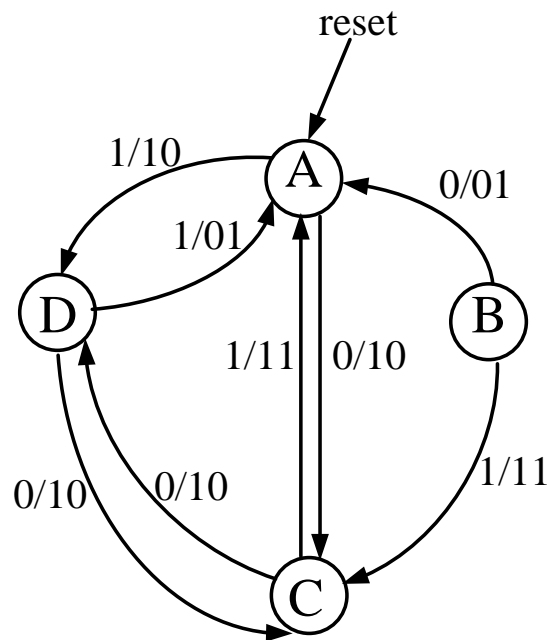
1. **Write down** next state and output equations for the following sequential circuit. From these equations **analyze** the sequential circuit and draw the transition diagram. [CO2,C4, Mark: 8]



2. **Design** a sequential circuit represented by the following state diagram using D flip-flop. [CO3,C3, Mark: 8]



3. **Design** a 3-bit serial-in parallel-out bi-directional shift register using D flip-flops. [Draw its block diagram, and logic diagram] [CO3,C6, Mark: 8]
4. **Design** a $\div 16$ synchronous down counter using T flip-flops. [Draw its block diagram, transition diagram, excitation table, equation, and logic diagram] [CO3,C6, Mark: 8]
5. **Design** a synchronous sequential circuit represented by the following state diagram using explicit style Verilog code. Assume a negative-edge clock. Also assume that reset will be done when the reset signal will go from 0 to 1. [CO3,C6, Mark: 8]



6. **Write** a behavioral Verilog code to design the following Boolean function using Procedural technique using case statement. [CO3,C6, Mark: 8]
- $$F(A, B, C, D) = A'D' + C' + B'C$$