Chapter 10
Sequential Logic Design

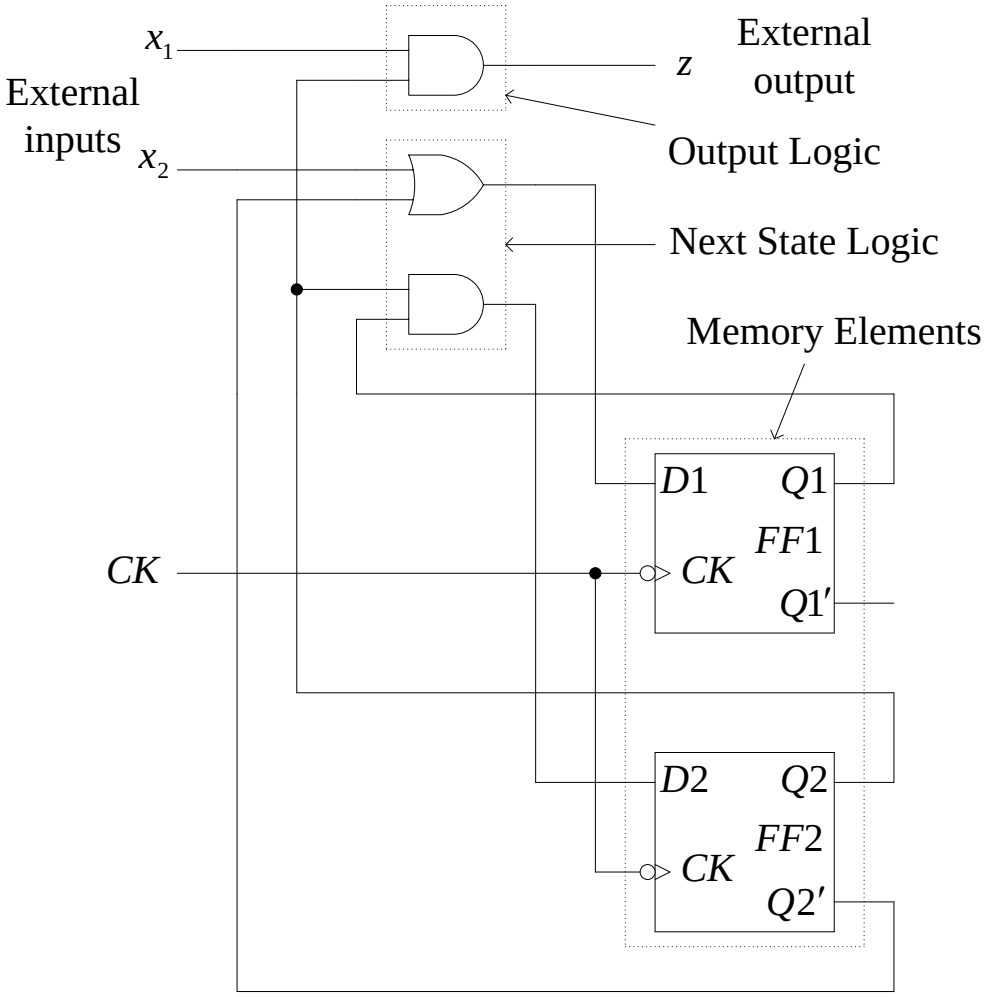
Analysis

Representation of Sequential Circuits

There are three main methods to represent the analytical properties of a sequential circuit:

- State equations and output equations.
- Transition table and state table.
- Transition diagram and State diagram.

Analysis (Contd.)



Output Equation:

$z = x_1 Q2_n$

Excitation Equations:

$D1_n = x_2 + Q2'_n$

$D2_n = Q1_n Q2_n$

Next State Equations:

$Q1_{n+1} = D1_n = x_2 + Q2'_n$

$Q2_{n+1} = D2_n = Q1_n Q2_n$

Analysis (Contd.)

Transition Table:

$Q1_{n+1} = D1_n = x_2 + Q2'_n$ (1, 0′=1)

$Q2_{n+1} = D2_n = Q1_n Q2_n$

$Z = x_1 Q2_n$ (1, 1)

Present State $Q1_nQ2_n$	Next State, $Q1_{n+1}Q2_{n+1}$ Input x_1x_2				Output Z Input x_1x_2			
	00	01	11	10	00	01	11	10
00		1	1					
01		1	1				1	1
11		1	1				1	1
10		1	1					

Analysis (Contd.)

$Q1_{n+1} = D1_n = x_2 + Q2'_n$ (1, 0′=1)

$Q2_{n+1} = D2_n = Q1_n Q2_n$

$Z = x_1 Q2_n$ (1, 1)

Present State $Q1_nQ2_n$	Next State, $Q1_{n+1}Q2_{n+1}$ Input x_1x_2 00	01	11	10	Output Z Input x_1x_2 00	01	11	10
00	1	1	1	1				
01		1	1				1	1
11		1	1				1	1
10	1	1	1	1				

Analysis (Contd.)

$Q1_{n+1} = D1_n = x_2 + Q2'_n$ (1, 0′=1)

$Q2_{n+1} = D2_n = Q1_n Q2_n$

$Z = x_1 Q2_n$ (1, 1)

Present State $Q1_nQ2_n$	Next State, $Q1_{n+1}Q2_{n+1}$ Input x_1x_2				~~Output~~ Z Input x_1x_2			
	00	01	11	10	00	01	11	10
00	1	1	1	1	0	0	0	0
01	0	1	1	0	0	0	1	1
11	0	1	1	0	0	0	1	1
10	1	1	1	1				

Analysis (Contd.)

$Q1_{n+1} = D1_n = x_2 + Q2'_n$ (1, 0′=1)

$Q2_{n+1} = D2_n = Q1_n Q2_n$ (1, 1)

$Z = x_1 Q2_n$ (1, 1)

Present State $Q1_nQ2_n$	Next State, $Q1_{n+1}Q2_{n+1}$ Input x_1x_2				Output Z Input x_1x_2			
	00	01	11	10	00	01	11	10
00	1	1	1	1	0	0	0	0
01	0	1	1	0	0	0	1	1
11	01	11	11	01	0	0	1	1
10	1	1	1	1				

Analysis (Contd.)

$Q1_{n+1} = D1_n = x_2 + Q2'_n$

$Q2_{n+1} = D2_n = Q1_n Q2_n$

$Z = x_1 Q2_n$

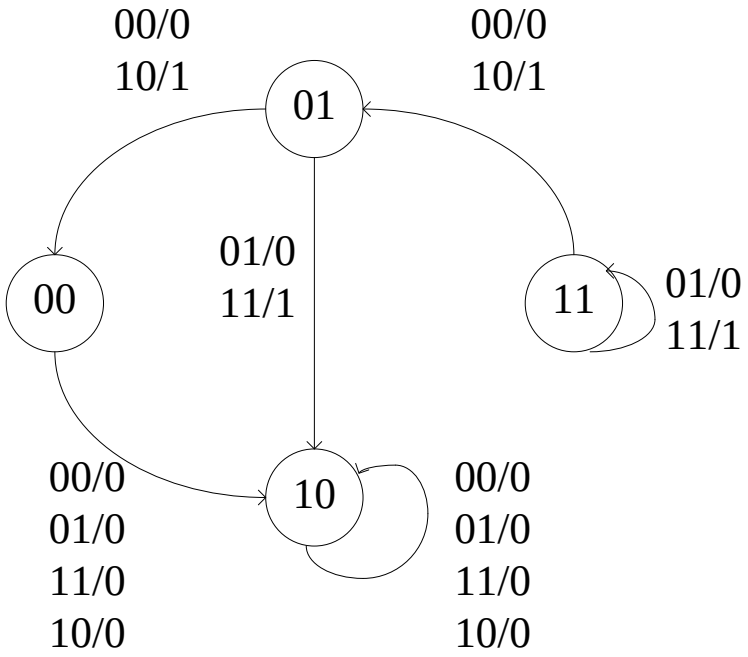
Present State $Q1_nQ2_n$	Next State, $Q1_{n+1}Q2_{n+1}$ Input x_1x_2				Output Z Input x_1x_2			
	00	01	11	10	00	01	11	10
00	10	10	10	10	0	0	0	0
01	00	10	10	00	0	0	1	1
11	01	11	11	01	0	0	1	1
10	10	10	10	10	0	0	0	0

Analysis (Contd.)

Table 10.1 Transition table for the sequential circuit of Figure 10.1.

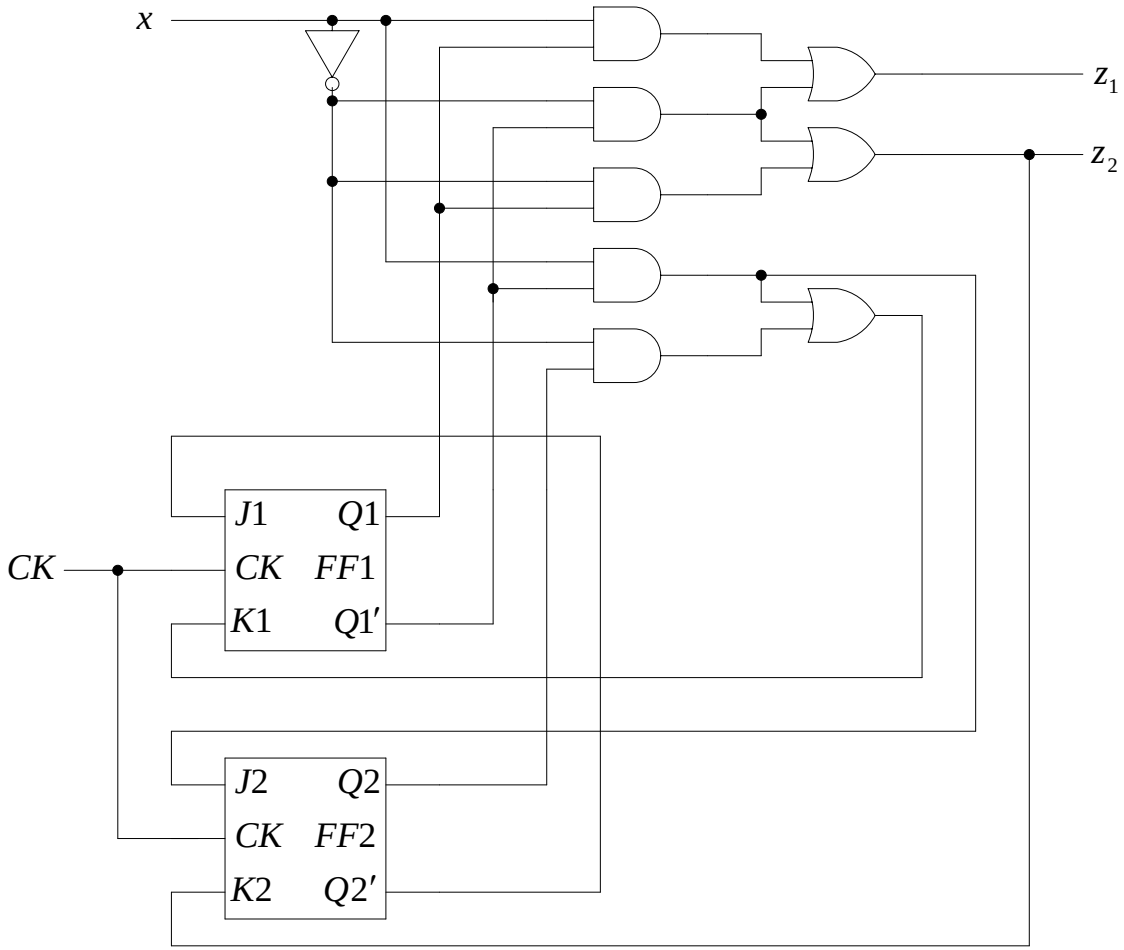
Present state $Q1_n Q2_n$	Next state $Q1_{n+1}Q2_{n+1}$ Input x_1x_2 00 01 11 10	Output z Input x_1x_2 00 01 11 10
00	10 10 10 10	0 0 0 0
01	00 10 10 00	0 0 1 1
11	01 11 11 01	0 0 1 1
10	10 10 10 10	0 0 0 0

Transition Diagram:



Analysis (Contd.)

Analyze this sequential circuit:



Step 1. The excitation equations of the flip-flops are written from the combinational circuit as:

$$J1_n = Q2'_n$$
$$K1_n = xQ1'_n + x'Q2_n$$
$$J2_n = xQ1'_n$$
$$K2_n = x'Q1'_n + x'Q1_n = x'$$

The output equations are written from the combinational logic circuits as:

$$z_1 = xQ1_n + x'Q1'_n$$
$$z_2 = x'Q1'_n + x'Q1_n = x'$$

Step 2. The next state equations of the J-K flip-flops are written from the excitation equations in conjunction with characteristic equation of J-K flip-flops as:

$$\begin{aligned} Q1_{n+1} &= J1_n Q1'_n + K1'_n Q1_n \\ &= Q2'_n Q1'_n + (xQ1'_n + x'Q2_n)'Q1_n \\ &= Q1'_n Q2'_n + (x' + Q1_n)(x + Q2'_n)Q1_n \\ &= Q1'_n Q2'_n + x'Q1_n Q2'_n + xQ1_n + Q1_n Q2'_n \\ &= Q1'_n Q2'_n + Q1_n Q2'_n (x' + 1) + xQ1_n \\ &= Q2'_n (Q1'_n + Q1_n) + xQ1_n \\ &= Q2'_n + xQ1_n \end{aligned}$$

$$\begin{aligned} Q2_{n+1} &= J2_n Q2'_n + K2'_n Q2_n \\ &= xQ1'_n Q2'_n + xQ2_n \end{aligned}$$

Step 3. The transition table for the circuit is prepared from the next state equations and output equations and shown in Table 10.3.

Table 10.3 Transition table for the sequential circuit of Figure 10.4.

Present state $Q1_n Q2_n$	Next state $Q1_{n+1} Q2_{n+1}$ Input x		Outputs $z_1 z_2$ Input x	
	0	1	0	1
00	10	11	11	00
01	00	01	11	00
11	00	11	01	10
10	10	10	01	10

Analysis (Contd.)

Step 4. The transition diagram for the circuit is prepared from the transition table of Table 10.3 and is shown in Figure 10.5.

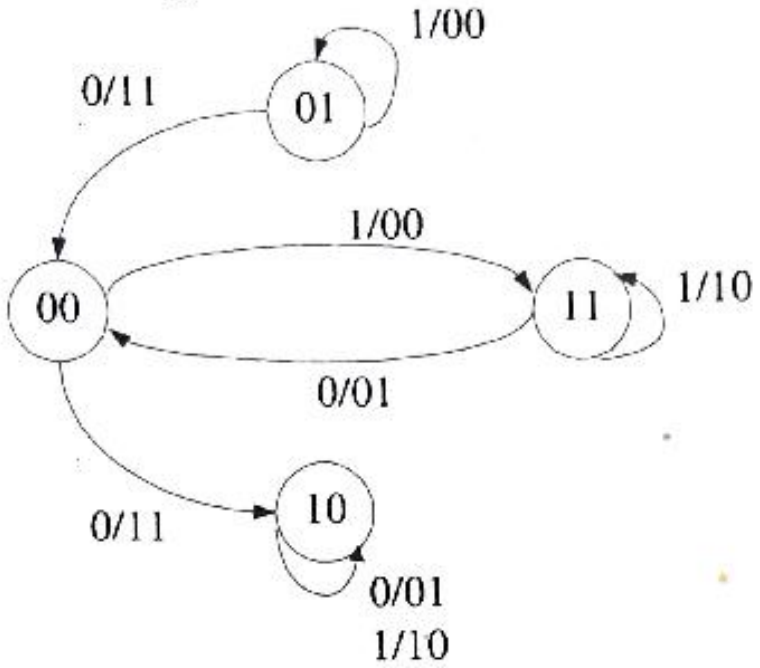


Figure 10.5 Transition diagram for the sequential circuit of Figure 10.4.