

Time: 25 minutes

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- The logic diagram shows a sequential circuit with two flip-flops, FF1 and FF2, and an output Z . The inputs are x and CK .
- Flip-flop FF1:** Labeled with $T1$, $Q1$, $Q1'$, and $FF1$. Its clock input CK is connected to the CK input. Its $T1$ input is connected to the output of an OR gate. The OR gate has inputs x and the output of an inverter connected to x . The $Q1$ output is connected to the $T2$ input of FF2. The $Q1'$ output is connected to the input of an AND gate.
 - Flip-flop FF2:** Labeled with $T2$, $Q2$, $Q2'$, and $FF2$. Its clock input CK is connected to the CK input. Its $T2$ input is connected to the output of an AND gate. The AND gate has inputs x and the output of FF1 ($Q1$). The $Q2$ output is connected to the output of an AND gate that produces Z . The $Q2'$ output is connected to the input of an OR gate.
 - Output Z :** Produced by an AND gate with inputs $Q2$ and $Q1$.