1905105

Experiment No. 7

Topic: Flip-Flops and Registers

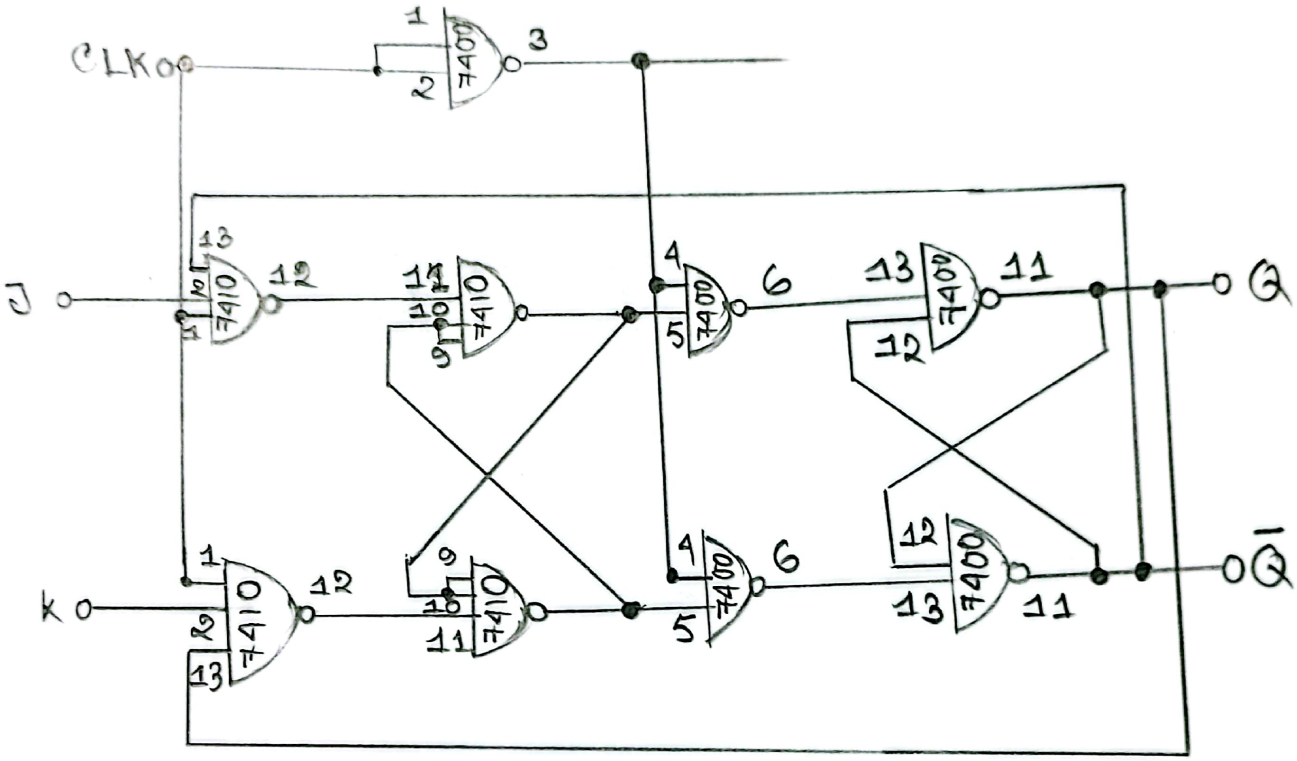
Problem-1: Design and implement a master-slave JK flip flop using only NAND gates.

Report:

CLK	J	K	Qn	Qn+1	Mode
0	X	X	0	0	No change (Qn)
0	X	X	1	1	
1	0	0	0	0	No change (Qn)
1	0	0	1	1	
1	0	1	0	0	Reset (0)
1	0	1	1	0	
1	1	0	0	1	Set (1)
1	1	0	1	1	
1	1	1	0	1	Toggle (Qn')
1	1	1	1	0	

1. Excitation Table

2. Circuit Diagram:



1905105

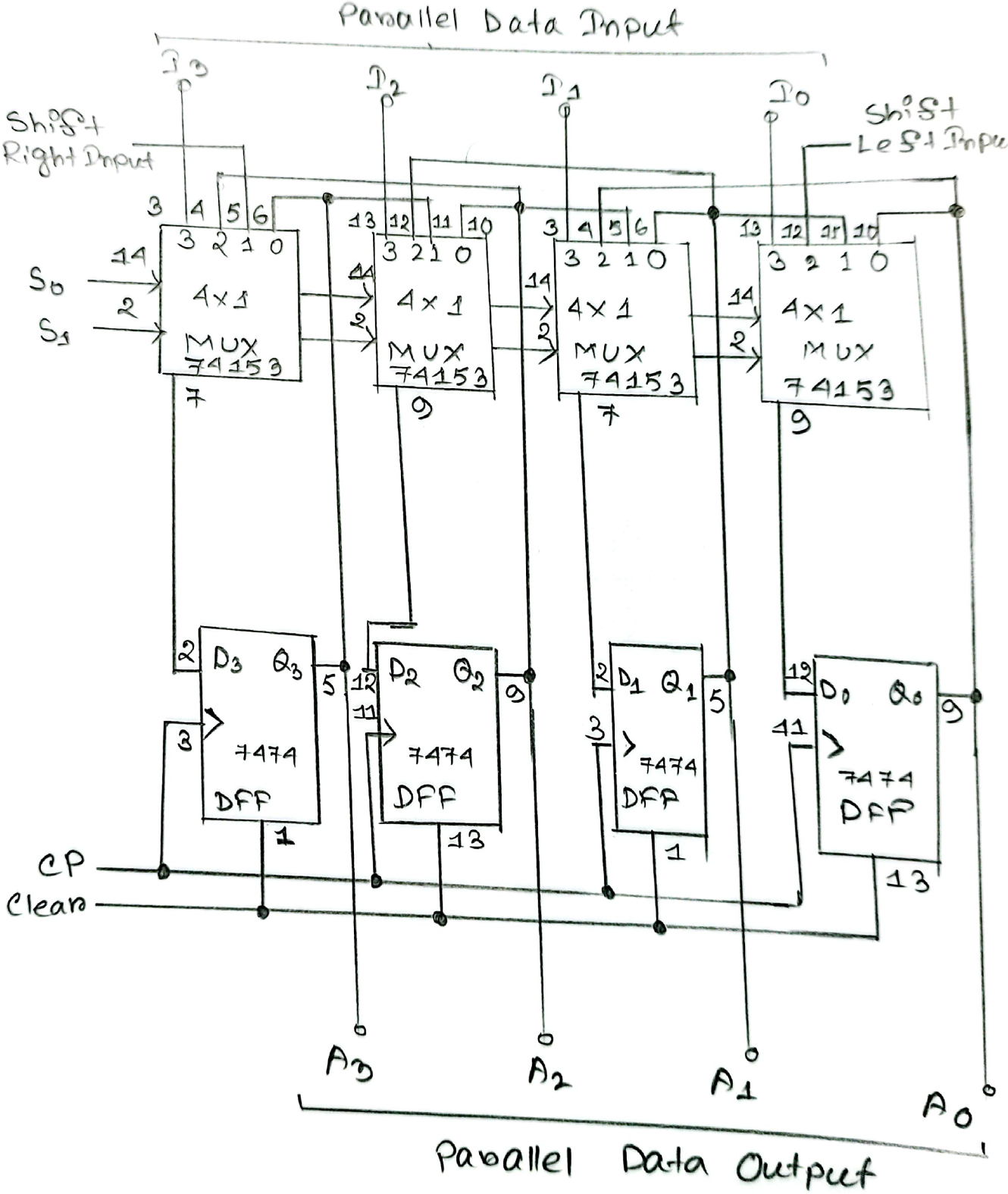
Problem - 2: Design and implement a 4-bit universal shift register.

Report:

Input					Output				
clear	clock	S_1	S_0	Internal signal D_i $(i=0,1,2,3)$	A_3	A_2	A_1	A_0	Mode
1	x	x	x	x	0	0	0	0	Asynchronous
0	x	0	0	x	A_3	A_2	A_1	A_0	Data hold
0	↑	0	1	A_{i-1}	I_R	A_3	A_2	A_1	Shift Right
0	↑	1	0	A_{i+1}	A_2	A_1	A_0	I_L	Shift Left
0	↑	1	1	A_i	I_3	I_2	I_1	I_0	Parallel load

1. Excitation Table

2. Circuit Diagram:



*. Circuit Diagram with IC Chips are designed and implemented with Logisim. (Universal-Shift-Register.circ)