Computer Architecture & Organization

CS520: Homework - 1

2/25/2021

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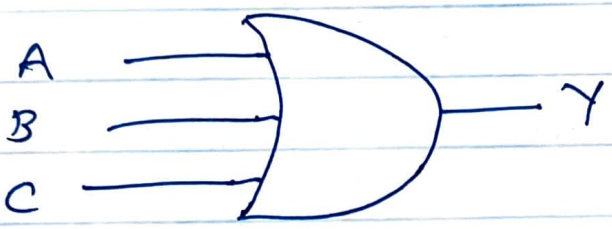
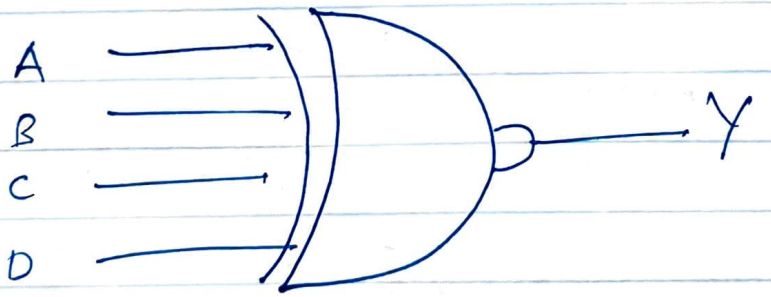
Que 1 Logic Gates

a) three-input OR gate



A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

b) four-input XNOR gate



$$Y = \overline{A \oplus B \oplus C \oplus D}$$

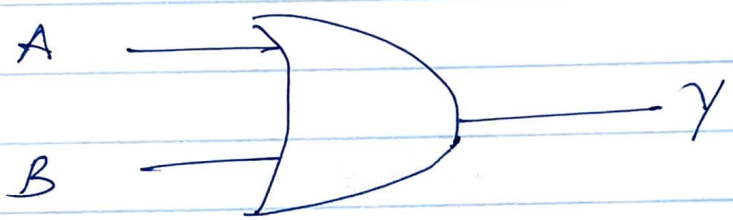
A	B	C	D	Y
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

que 4

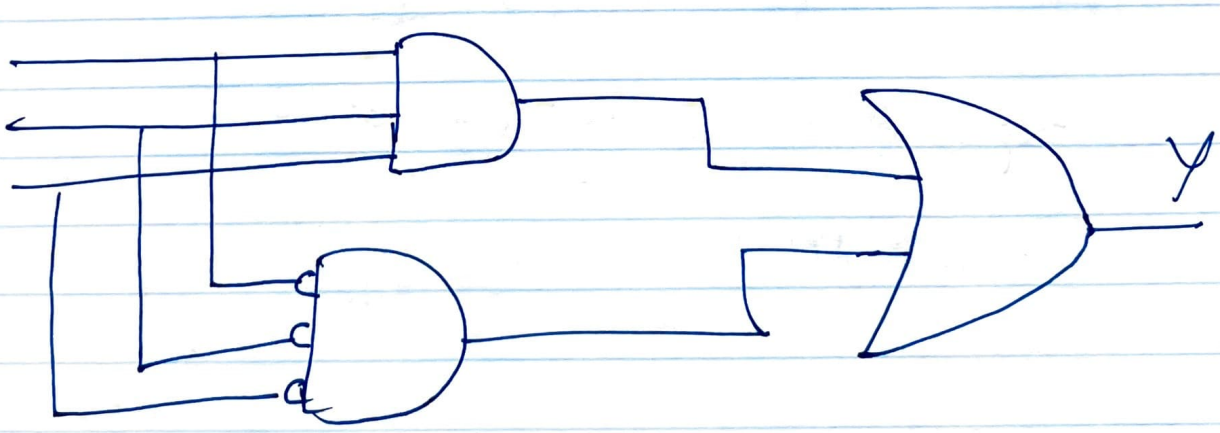
a)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

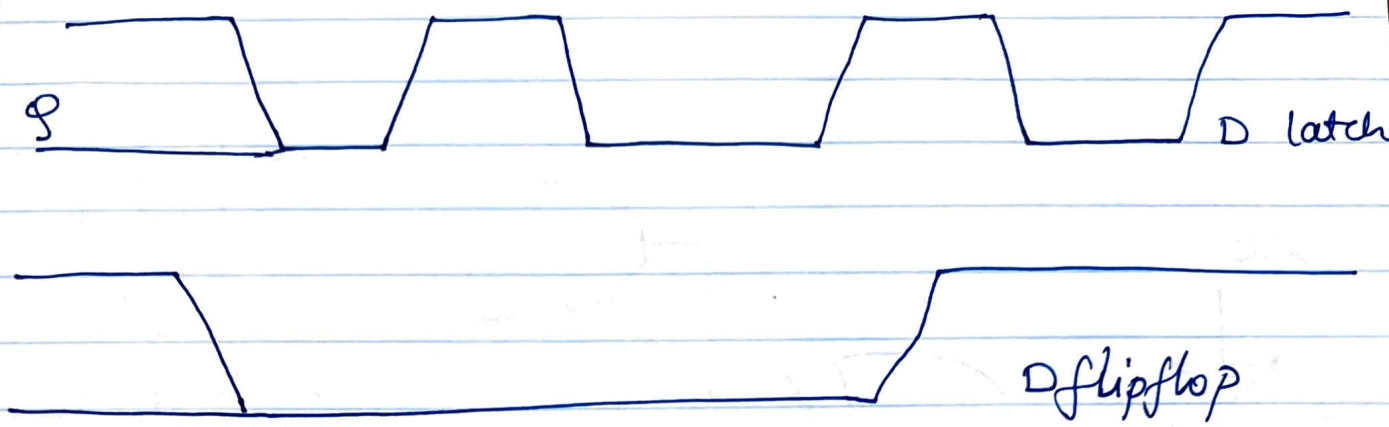
Ans:- $\bar{A}B + A\bar{B} + AB = Y$



b) $Y = \bar{A}\bar{B}\bar{C} + ABC$



Que 6



Que 7

a) $t = 3t - XOR$

$= 3 \times 80\ ps$

$= 240 ps$

Cycle time :-

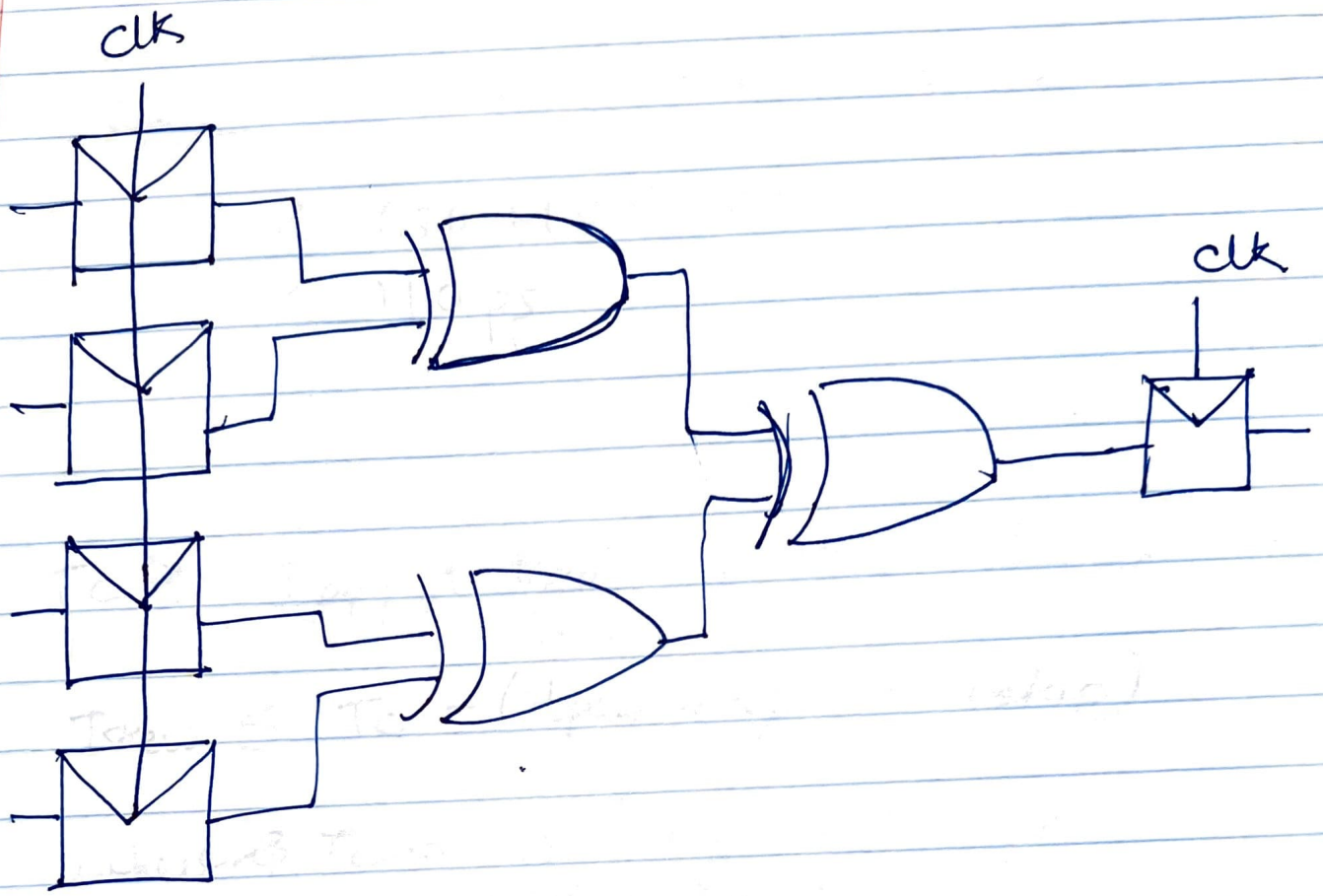
$Tc \geq t_{pcq} + t_{pd} + t_{setup}$

$\geq [60 + 240 + 40]\ ps$

$f = 1/340\ ps = 2.94\ GHz$

Que 8

a)



b) $t_{pd} = 2t_{pd} - XOR$

$= 2 \times 80$

$= 160\ ps$

$t_{cd} = 2t_{cd} - XOR$

$= 2 \times 50$

$= 100\ ps$

Cycle time ;- $T_c \geq T_{pcq} + t_{pd} + t_{setup}$

$\geq [60 + 160 + 40]\ ps$

$= 260\ ps$

$f = 1/260\ ps$

$= 3.84\ GHz$

que8

c) $t_{skew} < (t_{pcq} + t_{cd}) - t_{hold}$

$< (30 + 100) - 20$

$< 110\ ps$

que7

b) $T_c \geq T_{pcq} + t_{pd} + t_{setup} + t_{skew}$

$T_{skew} \leq T_c - (t_{pcq} + t_{pd} + t_{setup})$

where $T_c = 1/2\ GH_2 = 500\ ps$

$\leq [500 - 340]\ ps$

$= 160\ ps$

c) combination delay through combination log

$t_{cd} = t_{cd} - XOR$

$= 50\ ps$

$t_{ccq} + t_{cd} > t_{hold} + t_{skew}$

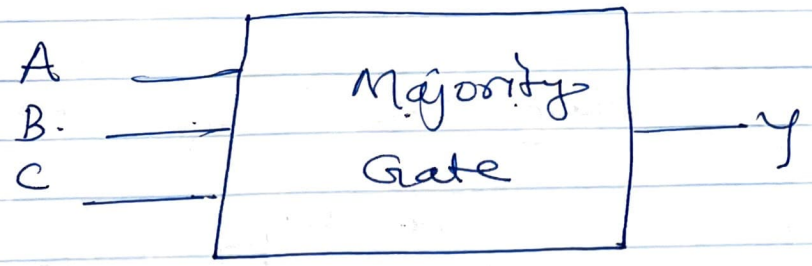
Thus,

$t_{skew} < (t_{ccq} + t_{cd}) - t_{hold}$

$< (30 + 50) - 20$

$< \underline{60\ ps}$

Que 2

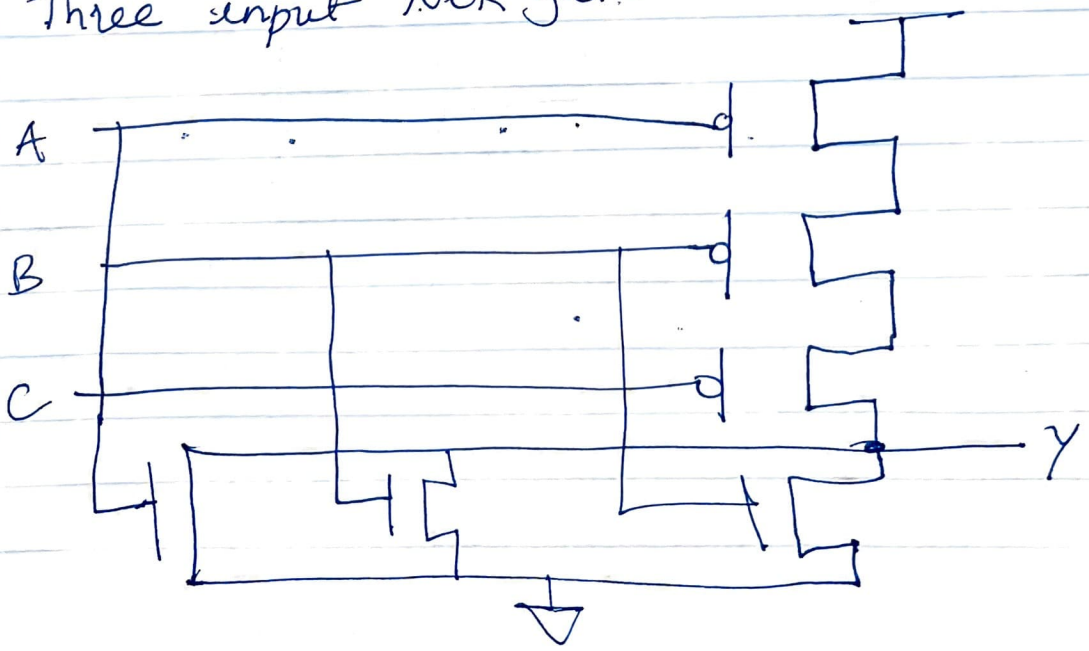


Truth table :-

A	B	C	y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

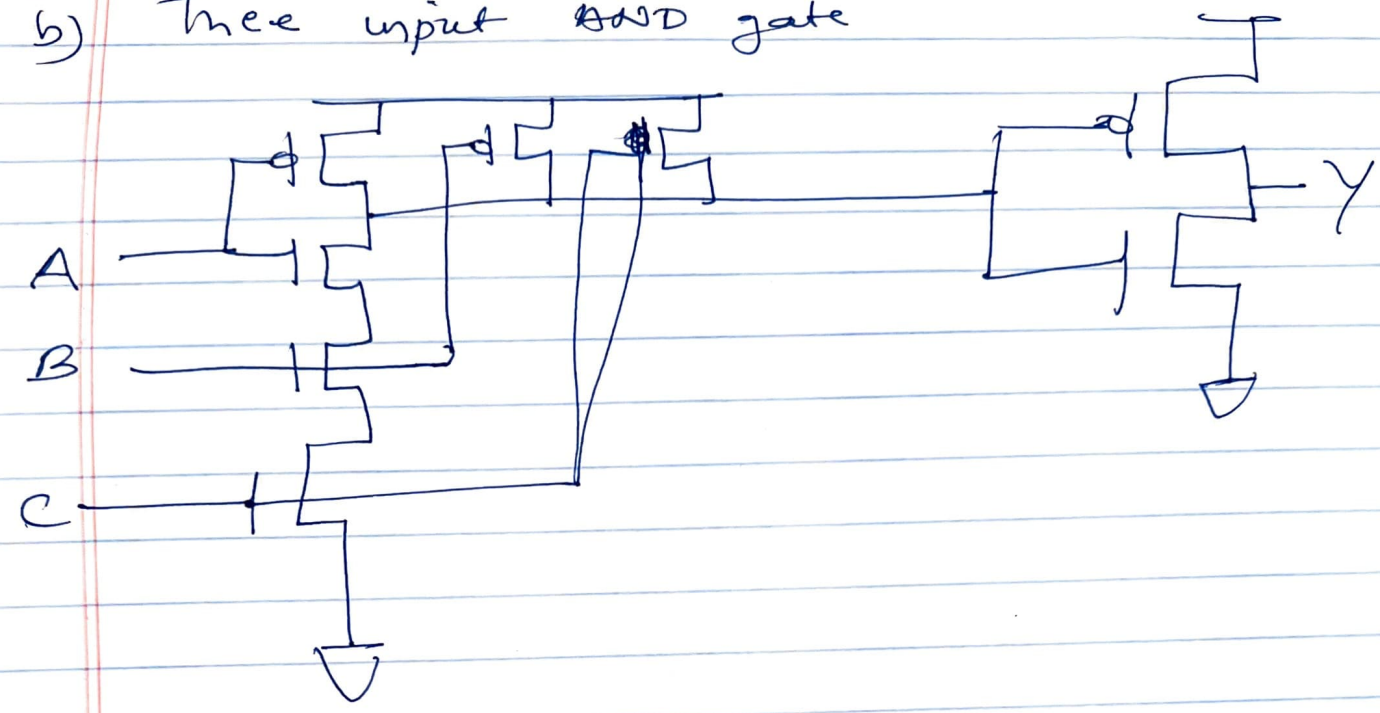
$$Y = BC + AC + AB$$

Que 3 a) Three input NOR gate



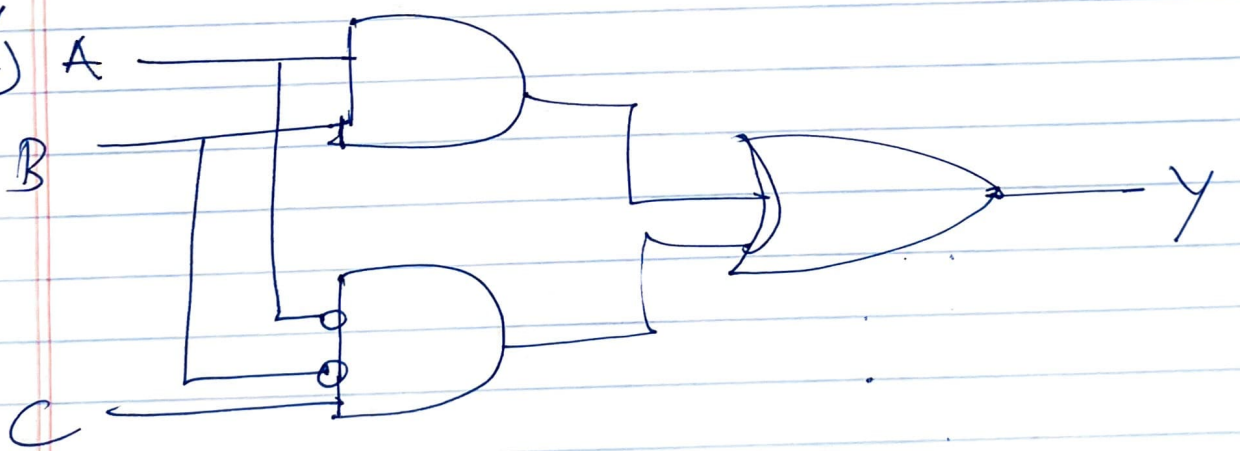
Que 3

b) Three input AND gate



Que 4

c)



$$Y = \bar{A}B\bar{C} + AB\bar{C} + ABC$$

$$= \bar{A}B\bar{C} + AB.$$