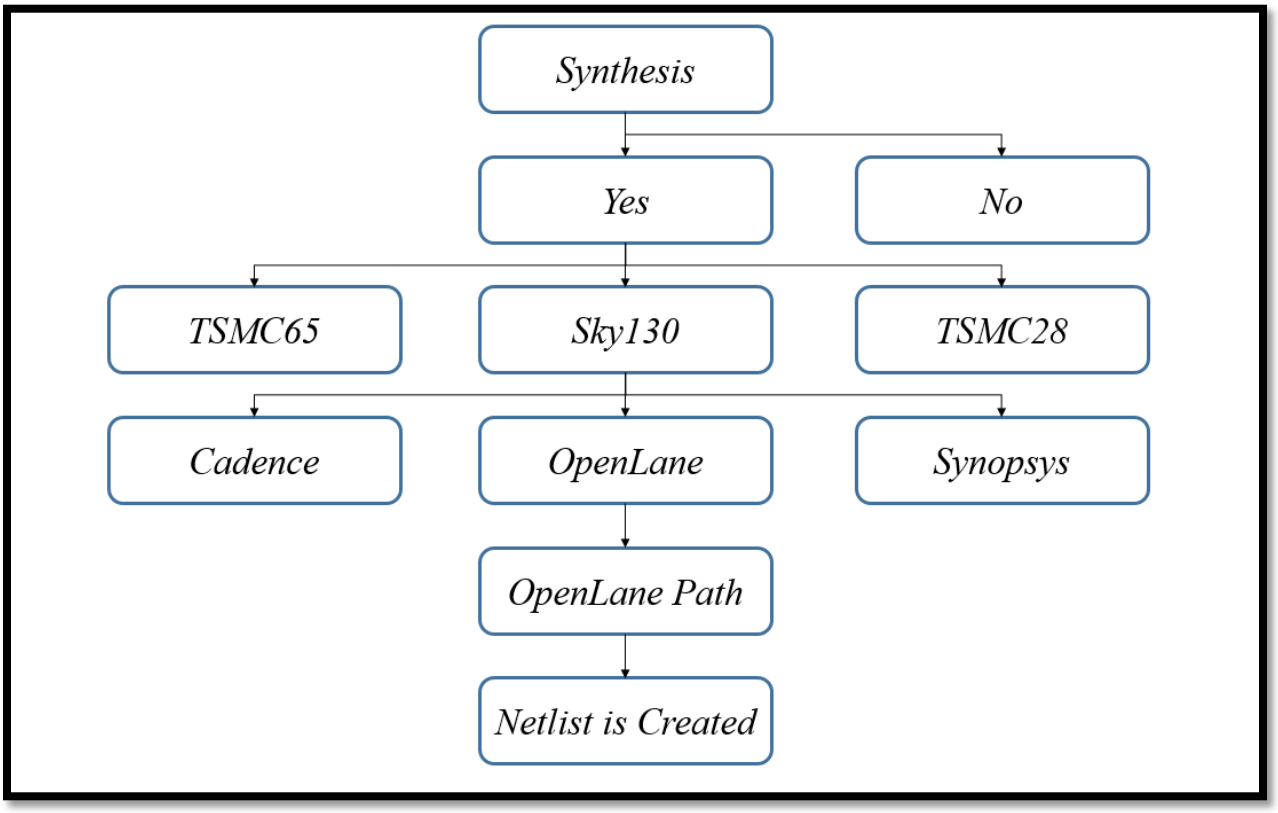
ADDING SYNTHESIS SCRIPT IN BRAM

GUI changes

The BRAM would have the following options for synthesis



The user would have the following options

1. Do the synthesis?
    a. Yes
    b. No
2. If yes, then select the technology from the three options
    a. Sky130
    b. TSMC65
    c. TSMC28
3. Currently we are working on Sky130, so after the technology the user is asked about the tool:
    a. OpenLane
    b. Cadence
    c. Synthesis

4. Currently we are adding the OpenLane Flow
5. After OpenLane, the user is asked about the path where the OpenLane is installed
6. Finally the result is given in the form of netlist

Back-End Script

The following steps would be executed to run synthesis

1. Make a folder:
    a. Mkdir /$OPENLANE_PATH/openlane/<bram_generated_verilog_top_module_name>
    b. Mkdir /$OPENLANE_PATH/openlane/<bram_generated_verilog_top_module_name>/src
2. Copy the Verilog files in src folder
3. Run the following command at /$OPENLANE_PATH
    a. Make mount
    b. ./flow.tcl –interactive –file file1.tcl
    c. ./flow.tcl –interactive –file file2.tcl

File.tcl

Before executing the above commands, make a file with the name **file1.tcl** and **file2.tcl** and place them at $OPENLANE_PATH

File1.tcl

Package require openlane

Prep –design < bram_generated_verilog_top_module_name > -init_design_config

File2.tcl

Package require openlane

Prep –design ./openlane/< bram_generated_verilog_top_module_name > -tag bram_netlist –overwrite

Run_synthesis

Netlist

The netlist is generated at

/$OPENLANE_PATH/openlane/<bram_generated_verilog_top_module_name>/runs/bram_netlist/results/synthesis/*.v