SoC-Now: An Open-Source Web based RISC-V SoC Generator

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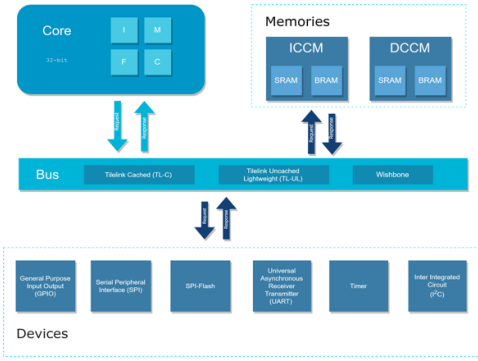
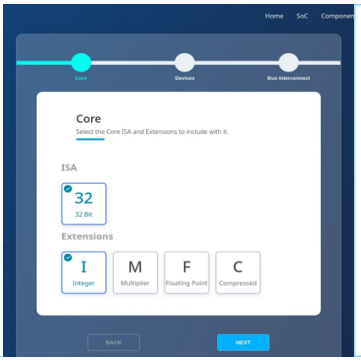
In the rapidly changing technological world of today, smart phones and other gadgets have taken over our daily lives. Every aspect of life is reliant on technology, or "smart devices." And these devices are called “smart” because they contain a computing system inside called as processor or system on chip (SoC). Development of SoC is a quite long process. It can take months to build and develop a SoC from scratch. Following the design stage, testing, and verification of it adds another layer of stress. Designers like to reuse a verified component in their design to save time. However, this doesn't save time because without adequate documentation, which is lacking in many contributions to open-source projects, it can be extremely challenging to grasp the functionality and usability of a component. The open-source semiconductor industry is therefore in need of software that can quickly produce or design a SoC rather than taking the designer years to complete the build or design. Alternately, any designer can also generate a component with sufficient documentation and plug and play support. SoC-Now is an open-source web-based RISC-V ISA [1][2][3] standardised SoC design solution in terms of generator that enables anyone to create a SoC as shown in Fig.1 with their own customized specifications as shown in Fig.2 and then further process that SoC to the Field Programmable Gate Array (FPGA) Emulation. Additionally, it provides the capability to produce any standalone, verified, and reusable SoC component (Core, Device, Bus) by means of generic interfaces as shown in Fig.3. A completely automated Verification system is also included.





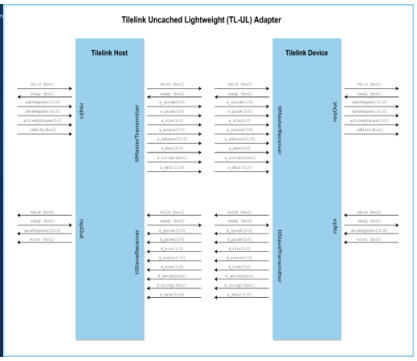


Fig.1 – System level Block Diagram of SoC-Now.	**Fig.2** – SoC configuration in SoC-Now.	**Fig.3** – Tilelink (TL-UL) Adapter implemented in Generic Interface (caravan)

References

[1] R.-V. Foundation. "The RISC-V Instruction Set Manual, Volume II: Privileged Architecture, version 1.10." https://content.riscv.org/wp-content/ uploads/2017/05/riscv-privileged-v1.10.pdf (accessed.

[2] R.-V. Foundation. "The RISC-V Instruction Set Manual, Volume I: User-Level ISA, document version 20191213. ." https://riscv.org/specifications/ (accessed.

[3] Waterman, A.S., 2016. Design of the RISC-V instruction set architecture. University of California, Berkeley.