




Bitstream Chef

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Electronic Design Automation[1] (EDA) technologies have become increasingly important in their fields of application with the open-source revolution in the silicon industry. These tools cover a wide range of automatic operations that save a significant amount of time. Bitstream Chef generates the bitstream of a design as shown in Fig.1 by taking an RTL design, allowing the user to map I/Os onto an FPGA using a GUI, and thus generating the bitstream through automated processes by use of an open-source tool F4PGA[2]. Additionally, it uploads the Bitstream onto the connected FPGA board while also letting the user know whether any boards are currently connected. It will also allow user to either have pre-defined program embedded in the bitstream or upload the program separately through UART. For further moving the design toward GDS generation, it has the Open Lane[3] toolchain integrated as well. Bitstream Chef is designed to be the go-to tool for every developer who frequently must upload or burn designs into FPGA, has a computer with less computing power.

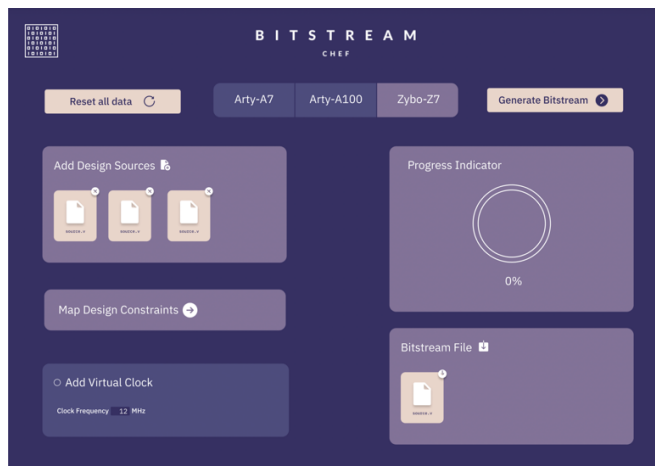


Fig.1 – Initial Mock-up of Bitstream Chef EDA Tool Graphical User Interface (GUI).

References

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