SHAHZAIB KASHIF

Software Engineer

To,
Recruitment Officer
Barcelona SuperComputing Center

Dear Sir/Ma'am,

I am writing to express my interest in the Job Vacancy in Barcelona SuperComputing Center (BCS) for the opening of "RTL Engineer for an Out of Order Processor". I found out about this opening from the BSC Website. I have been following BSC and its job opening for around 2 months. I am looking forward to exploring new boundaries of RISC-V and working on interesting new projects.

Currently finished exams of Final Year BSc Software Engineering, also learning and working on RISC-V. I have more than 2 years of experience in working with RISC-V ISA. I have hands-on experience in RISC-V Assembly as well. I have developed my own RISC-V Cores by using CHISEL (Constructing Hardware in Scala Embedded Language) Hardware Construction Language.

My Final Year Project (FYP) is a CHISEL based RISC-V System on Chip (SoC) Generator that takes in the user configuration for RISC-V Core Extensions (i,m,f,c), Device(s) (gpio, spi, spi-flash, uart, timer, i2c), Bus Interconnect (wishbone, tilelink uncached lightweight and tilelink cached) and generates the Complete SoC. The SoC RTL is provided to the user and further on the user can process the SoC to generate its Bitstream for FPGA Emulation.

I have hands-on experience with designing a RISC-V based Core from scratch and adding on extensions in it as well. I have expertise in CHISEL HDL and Scala but my verilog is quite weak. I can understand the RTL written in verilog but cannot write it on my own efficiently. I have also explored Rocket Chip Generator and its modification, Berkeley Out of Order Machine (BOOM).

Thank you for your consideration.

Yours Sincerely,
Shahzaib Kashif