




Burq Suite: An Automated RISC-V Core Verification Suite

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With the open source silicon revolution took place by the introduction of RISC-V[1] Instruction Set Architecture (ISA), a large number of designers and open source enthusiasts are participating in chip designing. Anyone can now design their own core (processor) easily by just only following the architecture that is defined and open sourced by RISC-V. Chip design is a time-consuming procedure, testing and verifying it as well as making sure the developed chip precisely follows the architecture are additional difficult tasks for developers. A tool that designers may use to quickly validate and verify their cores in line with the RISC-V ISA Standards is required to address this straightforward yet complex challenge. Burq-Suite is a RISC-V based Core Verification Suite that enables Chip designers to verify their core by running tests as shown in Fig.1 on their core and verifying the results of those tests in comparison with the RISC-V defined golden model Instruction Set Simulator (ISS) that is Spike[2], Whisper[3] and OVPSim. Burq-Suite will provide a report as shown in Fig.2 that will show the outcomes of testcases, whether they passed or failed meeting the golden model criteria, in the event of a failure, it will also provide the log for the designer to take reference on what went wrong and what should have been done instead.

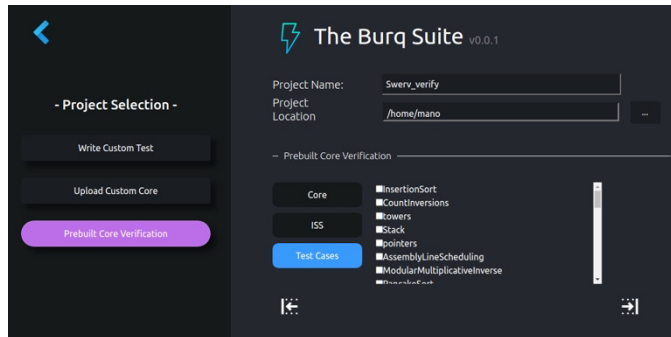


Fig.1 – Test Cases Selection option in Burq-Suite

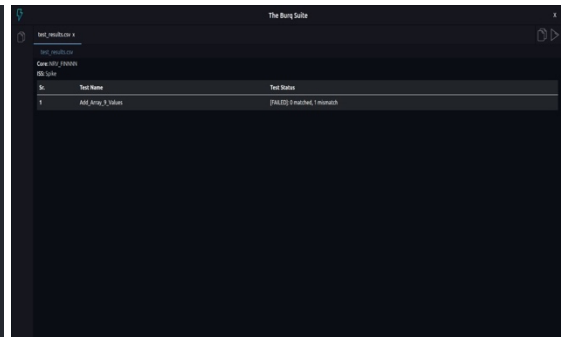


Fig.2 – Test Status Report in Burq-Suite

References

- [1] Waterman, A.S., 2016. Design of the RISC-V instruction set architecture. University of California, Berkeley.
- [2] Duran, C., Morales, H., Rojas, C., Ruospo, A., Sanchez, E. and Roa, E., 2020, October. Simulation and Formal: The Best of Both Domains for Instruction Set Verification of RISC-V Based Processors. In 2020 IEEE International Symposium on Circuits and Systems (ISCAS) (pp. 1-4). IEEE.
- [3] Kabylikas, N., Thorn, T., Srinath, S., Xekalakis, P. and Renau, J., 2021, October. Effective Processor Verification with Logic Fuzzer Enhanced Co-simulation. In MICRO-54: 54th Annual IEEE/ACM International Symposium on Microarchitecture (pp. 667-678).