Shahzaib Kashif

Software Engineer

+923171150567
shazaibceo@gmail.com

EXPERIENCE

Microelectronics Research Lab (MERL), — *Research Intern*

September 2019 - PRESENT (2 years, 11 months +)

Microelectronics Research Lab (MERL), — *Webmaster*

February 2022 - PRESENT (6 months +)

Techvolte — *Full Stack Developer*

May 2021 - September 2021 (5 months)

EDUCATION

Usman Institute of Technology — *BSc*

2018 - 2022

Bachelor of Science (BSc), Software Engineering.

PROJECTS

Ababeel Core — *A Risc-V RV32i Single Cycle Core*

A Single Cycle Processor Core based on RISC-V ISA, supporting Integer (i) extension, implemented on CHISEL Hardware Construction Language (HCL).

Ababeel Pipelined — *A Risc-V RV32i 5 Stage Pipelined Core*

A Five Stage Pipelined Processor Core based on RISC-V ISA, supporting Integer (i) extension, implemented on CHISEL HCL.

Reverse Engineering of Rocket Chip — *To Reverse Engineer the Rocket Chip SoC Generator*

Reverse Engineering of the Rocket Chip SoC Generator's Core source code by means of Software Methodologies i.e (Class Diagrams, Flow Charts).

SoC-Now — *A Mini SoC Generator based on Scala and CHISEL. (Final Year Project)*

Developed a Web based SoC Generator which will generate a customized

SKILLS

Python Programming Language

RISC-V

Scala

Constructing Hardware in Scala Embedded Language (CHISEL) HDL

C language

Bash Scripting

Makefiles

Object Oriented Software Engineering

Embedded Software Programming

Web Development

HTML, CSS

JavaScript

REACT JS

Desktop Application Development

Mobile Application Development

LANGUAGES

English

Urdu

Chinese (basic)

SoC, generate any custom component and verify core and/or SoC. The Generator is completely developed on CHISEL HDL along with the Functional Programming Paradigm of Scala to achieve high level reusability.

Google MPW6 — *Participated in MPW6*

Generated a SoC from our SoC-Now SoC Generator and submitted in Google's MPW6 Shuttle Programme for tapeout.

LFX Mentorship— *Porting AOSP 12 Emulator to RISC-V RV64GC*

Selected and Completed in LFX Mentorship programme in a project to port Android 12 Emulator to RISC-V RV64GC Architecture.

MERL Website— *Developed and Managing MERL's Website*

Developed MERL's Website from scratch, hosted it and now managing it. https://merledupk.org/

The NOVA Project— *Software Team for Cloud FPGA Emulation and Support*

Emulated multiple RTL Designs on AWS-FPGA Cloud FPGA Platform by writing runtime drivers. Configured Zephyr RTOS for the designed RISC-V based SoC and wrote Linux Kernel Device Drivers to boot OS by writing data into DDR.