SoC-Now: A Web based RISC-V SoC Generator

## Abstract:

SoC-Now is designed for those who want to quickly and simply build a SoC based on RISC-V. It allows the user to specify their requirements and have a SoC built, which they can then use for bitstream emulation by use of open-source F4PGA toolchain. SoC generation is made possible by some open source CHISEL frameworks such as Caravan for using buses by use of generic interfaces, Jigsaw for connecting memories and devices by use of caravan, and NucleusRV which is an open-source parametrized RV32-IMC Core. ~~SoC generation is made possible by generic bus interfaces which is basically a generalized wrapper upon ports of bus protocols in terms of “Request” and “Response”.~~ Additionally, it enables users to simply create any SoC component standalone for use in their design by implementing these generalized ports in their design. By using RISC-V compliance tests on their created designs, users can perform automated verification using the Verification component. Users can also perform manual verification by creating custom testcases and downloading VCDs. It is also being extended to integrate the GDS Backend workflow as well by use of OpenLane toolchain.