SHAHZAIB KASHIF

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Education

BSc in Software Engineering **Oct. 2018 – Aug 2022**
NED University of Engineering and Technology (UIT), Karachi *CGPA: 3.205*

Experience

CPU Design Engineer **Oct 2022 – Present**
Intensivate *Berkeley, California (Remote)*

- Worked in team connecting PCI express IP with the design in CHISEL.
- Assisted in writing bare-metal testing firmwares.
- assisted in verification and running RTL and Gate level Simulations.
- Attached RV compatible Debug Module with the design and made it work with on chip debuggers and gdb in simulation.

Research Assistant **Nov 2022 – Present**
Micro Electronics Research Lab (MERL) *Karachi, PK*

- Designed a full fledged System on Chip (SoC) Generator in CHISEL HDL.
- Worked on in-house simulation and verification tools.
- Lead Student Teams working on RV Vector Coprocessor, GeMM Accelerator, Neuromorphic Core.
- Taped out a generated SoC in Google MPW6 Shuttle using Skywater PDK.

Projects

SoC-Now | *CHISEL, System-on-Chip, FPGA* **https://github.com/merledu/SoC-Now-Generator**

- Designed generic plug and play compatible SoC Components like Buses (Wishbone, Tilelink), Devices (GPIO, UART, SPI, I2C, Timer) and the Core (RV32-imfc)
- Made every configuration inside SoC Generator parametrised using CHISEL.
- Integrated a Web Interface on top of Generator to automate the SoC generation process.
- Automated FPGA Mapping and Bitstream Generation process.

NOVA | *Cloud FPGA, Runtime Drivers* **https://github.com/The-Nova-Project/Runtime-Drivers**

- Emulated multiple RTL Designs on AWS-FPGA Cloud FPGA Platform by writing runtime drivers that used to communicate with the F1 Instance using the PCIe slot.
- Tweaked the FPGA toggling the buttons, switches and reading the status of LEDs to and from the cloud.
- Configured Zephyr Real Time Operating System (RTOS) for the designed RISC-V based SoC and wrote Linux Kernel Device Drivers to boot OS by writing data into DDR.

MAGMA-Si | *CHISEL, Accelerator, FPGA* **https://github.com/merledu/magmasi**

- Hardware accelerator developed in CHISEL HDL specifically for accelerating Generic Metric Multiply (GeMM) operations and is based on a Network on Chip architecture with generic interfaces.
- It contains several Dot Product Hardware Engines to compute the matrix multiplication and is 5.7x times faster than traditional systolic array based GeMM Accelerators.
- Leading a student team in designing, verifying and running real time applications on it.

Mentorships

Linux Foundation Mentorship: Porting AOSP 12 Emulator to RISC-V RV64GC
Google Summer of Code: Enhancing and Validating Power Modelling flow of LiveHD
Linux Foundation Mentorship (Mentor): Implementing TL-UH protocol in Caravan, Adding RISC-V F extension in NucleusRV Core

Poster Publications

RISC-V Summit Europe 2023: ChipShop: A Cloud-Based GUI for Accelerating SoC Design
First FireSim and Chipyard Workshop at ASPLOS 2023: ChipShop: A Cloud-Based GUI for Accelerating SoC Design
Workshop on Open Source EDA Technology (WOSET) 2023: SoC-Now: An Open-Source Web based RISC-V SoC Generator, Bitstream Chef

Technical Skills

Hardware Descriptive Languages: CHISEL, Verilog
ASIC/FPGA Design Tools: OpenLane, Vivado, Symbiflow/F4PGA
Concepts: RISC-V ISA, RV Debug, RV Vector, Spiking Neural Networks (SNN), STA
Others: Python, Git, Linux, RV GCC Compiler and Debugger