

21101098

CSE350

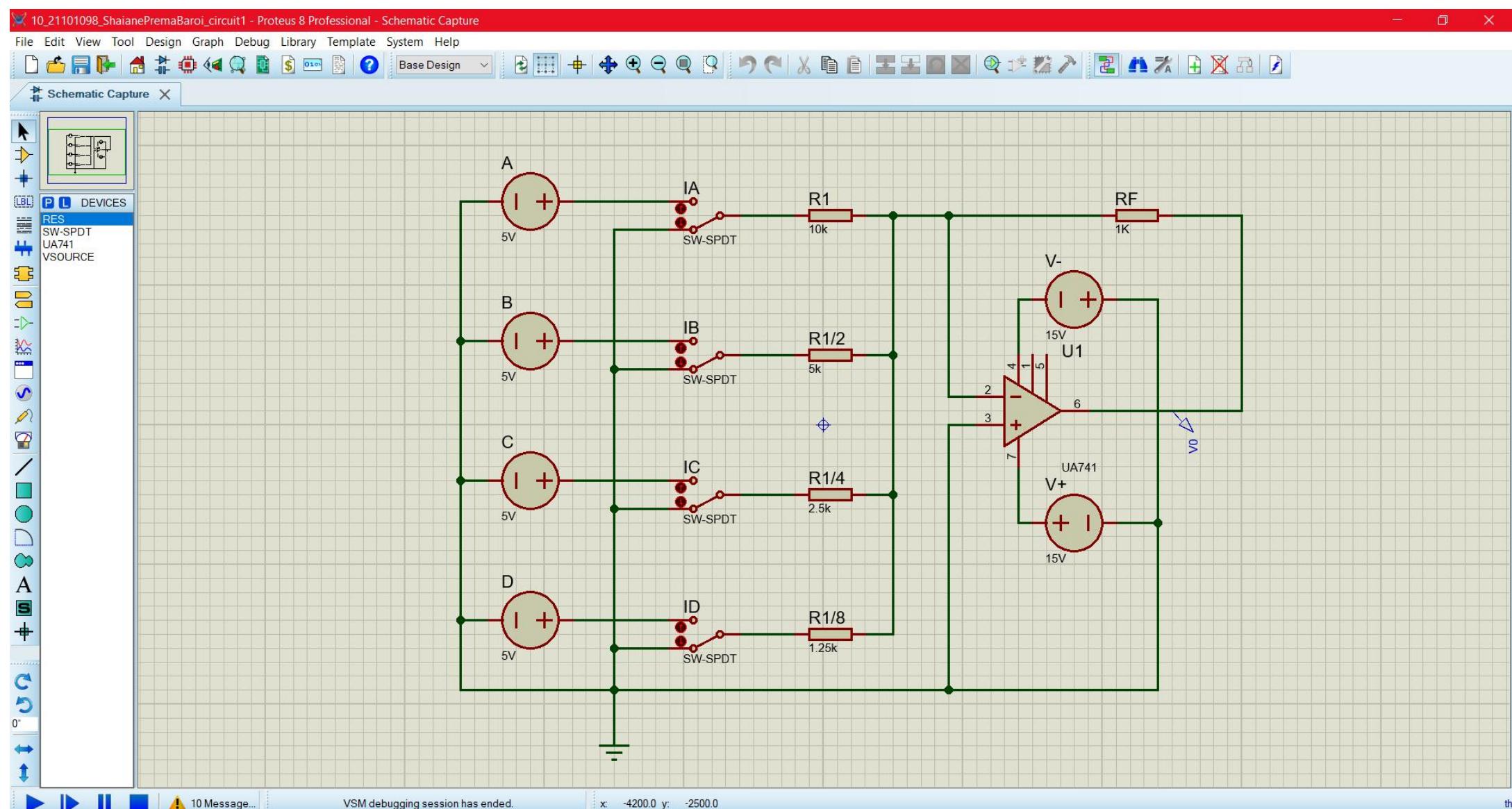
DIGITAL ELECTRONICS AND PULSE TECHNIQUES

LAB ASSIGNMENT 04

SHAIANE PREMA BAROI

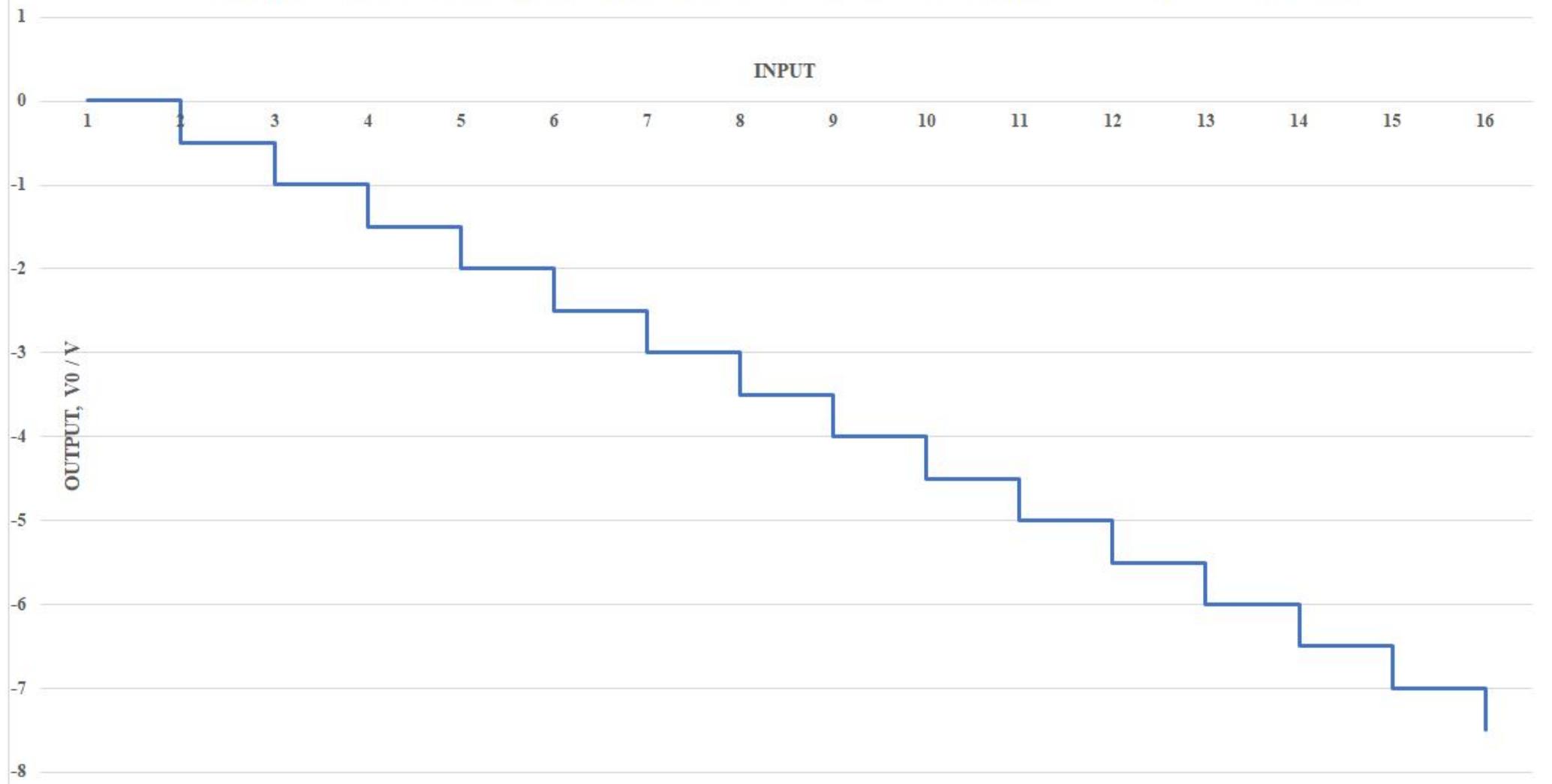
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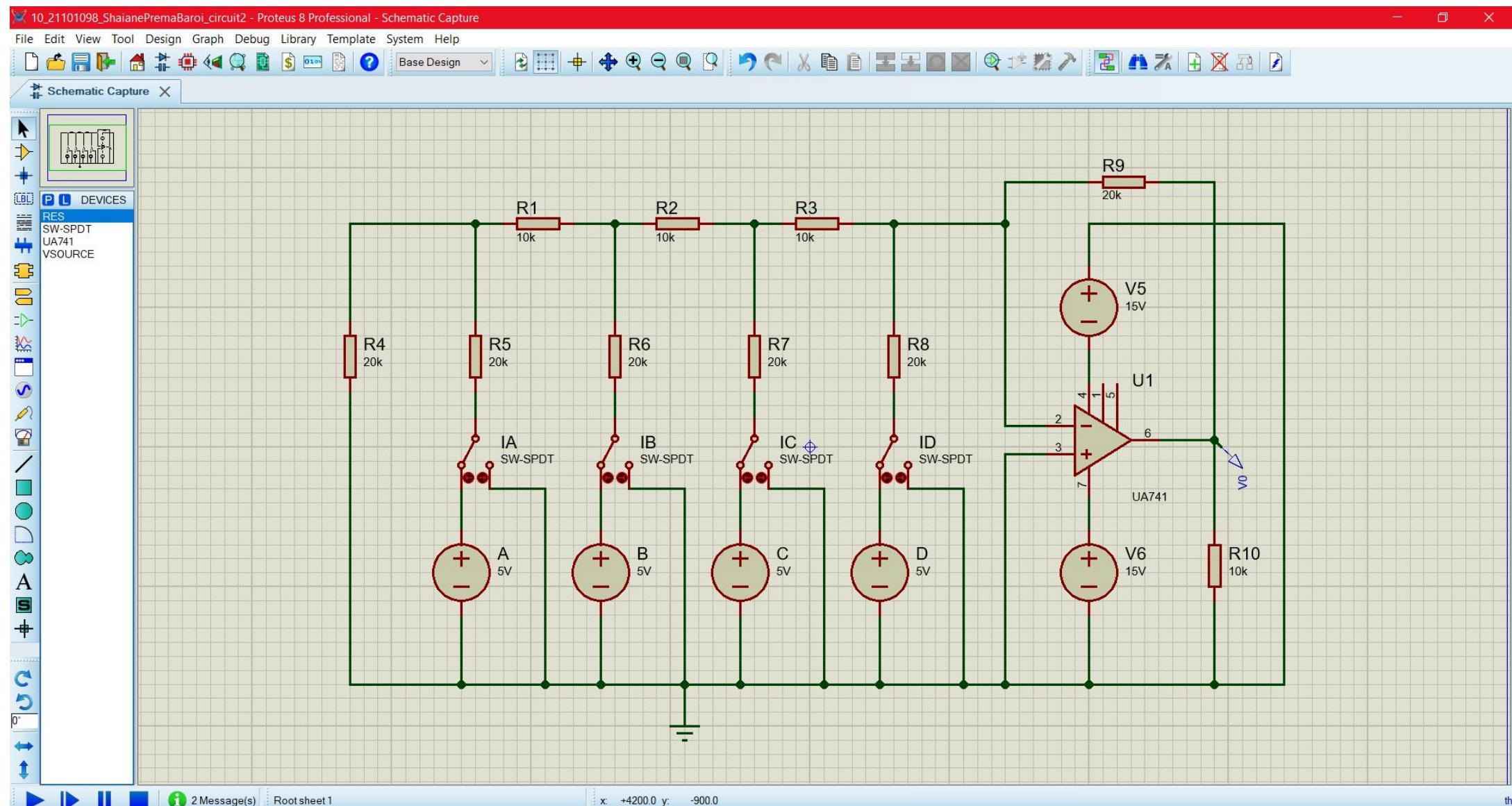
SECTION: 10



Datasheet for circuit 1

input configuration	D (V)	C (V)	B (V)	A (V)	output voltage, V _o (V)	
P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15 P16	0	0	0	0	0.00272281	
0 2 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	0	0	0.5	-0.497259	
1 3 6 4 0 1 0 0 5 0 0 0 0 0 0 0	0	0	5	0.0	-0.99723	
P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15 P16	0	0	5	0.5	-1.49721	
0 5 0 0 0 0 0 0 0 0 0 0 0 0 0 0	0	5	0	0.0	-1.99714	
6 8 9 11 0 0 0 0 0 0 0 0 0 0 0 0	0	5	0	0.5	-2.49712	
0 7 4 4 5 5 0 0 0 0 0 0 0 0 0 0	0	5	5	0.0	-2.9971	
8 P10 P11 P12 P13 P14 P15 P16	0	5	5	5	0.0	-3.49708
P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15 P16	5	0	0	0	0.0	-3.99685
0 10 11 0 0 0 0 0 0 0 0 0 0 0 0 0	5	0	0	0.5	0.0	-4.49683
11 P12 P13 P14 P15 P16	5	0	5	0	0.0	-4.9968
12 P13 P14 P15 P16	5	0	5	5	0.0	-5.49678
13 P14 P15 P16	5	5	0	0	0.0	-5.99672
14 P15 P16	5	5	0	5	0.0	-6.4967
15 P16	5	5	5	0	0.0	-6.99667
16 P16	5	5	5	5	0.0	-7.49665

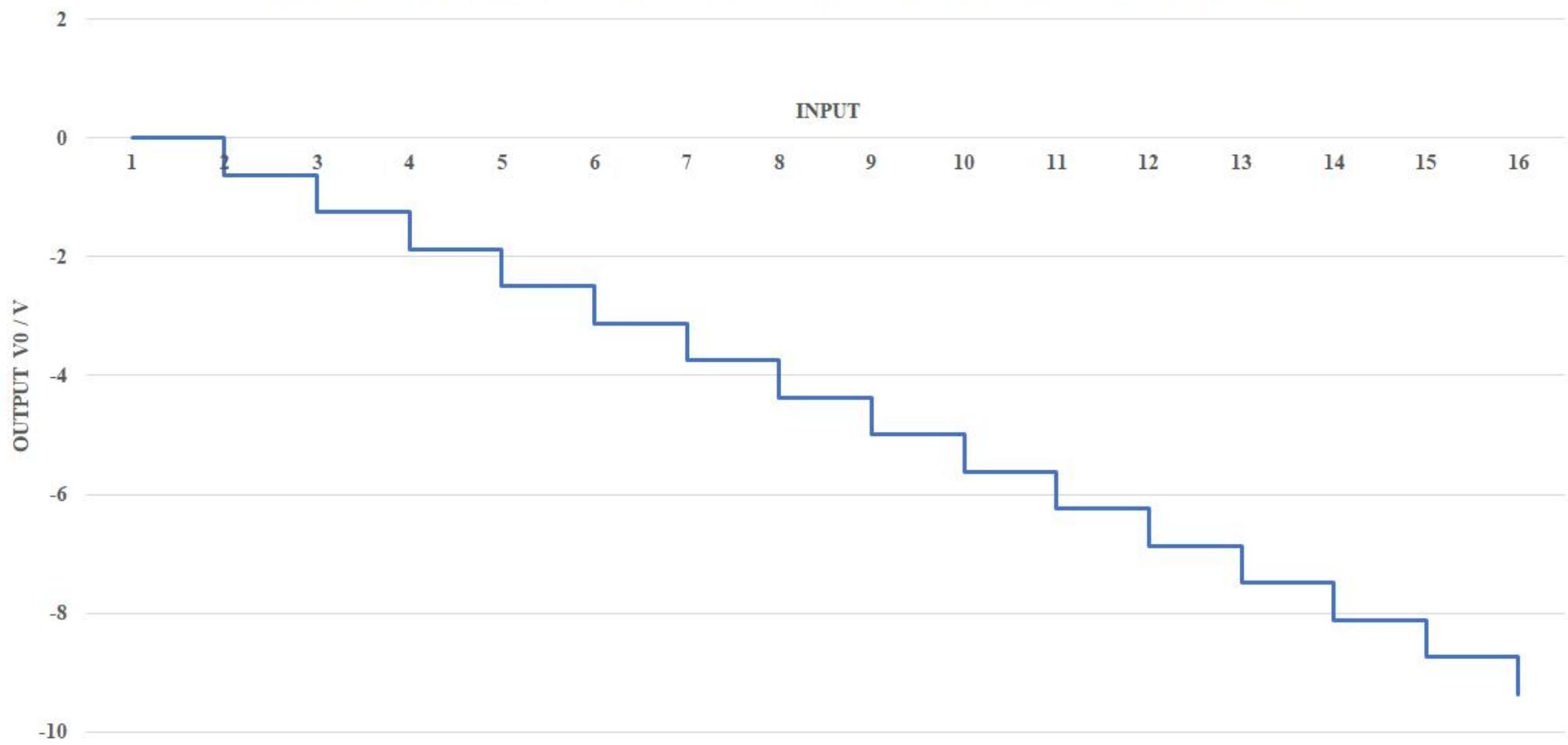
INPUT-OUTPUT GRAPH FOR DIGITAL TO ANALOG CONVERTER USING BINARY-WEIGHTED RESISTORS



Datasheet for circuit 2

1. timing and load test

<u>v_{in}</u> input voltage configuration	<u>D</u>	<u>A</u>	<u>B</u>	<u>A</u>	<u>output voltage, v_o</u>
(v)	(v)	(v)	(v)	(v)	(v)
18.8541000.0	0	00	0	0	0.00495409
8.827240.0	0	10	0	5	-0.620026
8.825380.0	0	00	5	0	-1.24501
1.867400.0	0	10	5	5	-1.86999
HP500P.0	0	05	0	0	-2.49496
01F6H.0	0	15	0	5	-3.11994
LF7P.0	0	5	5	0	-3.74492
20E8H.0	0	15	5	5	-4.3699
32.99P.0	5	0	0	0	-4.99487
8.8210P.0	5	0	0	5	-5.61985
8.8211P.0	5	0	5	0	-6.24483
8F.012H.0	5	0	5	5	-6.86981
FF.013H.0	5	5	0	0	-7.49478
8F.014H.0	5	5	0	5	-8.11976
F.015H.0	5	5	5	0	-8.74474
8.016H.0	5	5	5	5	-9.36972

INPUT-OUTPUT GRAPH FOR DIGITAL TO ANALOG CONVERTER WITH R AND 2R RESISTORS

Report

A 11 A 21 A

- 1> No, we cannot get an output higher than $\pm 15V$ in D2A converters. This is because $\pm 15V$ and $\pm 15V$ are the bias voltage and hence output has to be between $-15V$ to $+15V$. ~~as input = magnitude of output~~
~~as input = output (in magnitude)~~
 - 2> input, $n = 4$
- \therefore full step output = $2^n - 1$
 $= 2^4 - 1$
 $V_O = \pm 15$ steps V (for both D2A converters)

Binary Weighted Resistor D2A

$$\text{step size} = -0.49994 \text{ V}$$

$$\text{full scale output} = -7.49665 \text{ V}$$

$$\therefore \text{resolution} = \frac{\text{step size}}{\text{full scale output}} = \frac{-0.49994}{-7.49665} = 0.0667$$

R/2R D/A

tac909

step size = -0.62498 V two most significant bitsfull scale output = -9.36972 V first four bits of ADC

assumed word length of 8 bits and bias voltage and gain

$$\text{resolution} = \frac{\text{step size}}{\text{full scale output}} = \frac{-0.62498}{-9.36972} = 0.0667$$

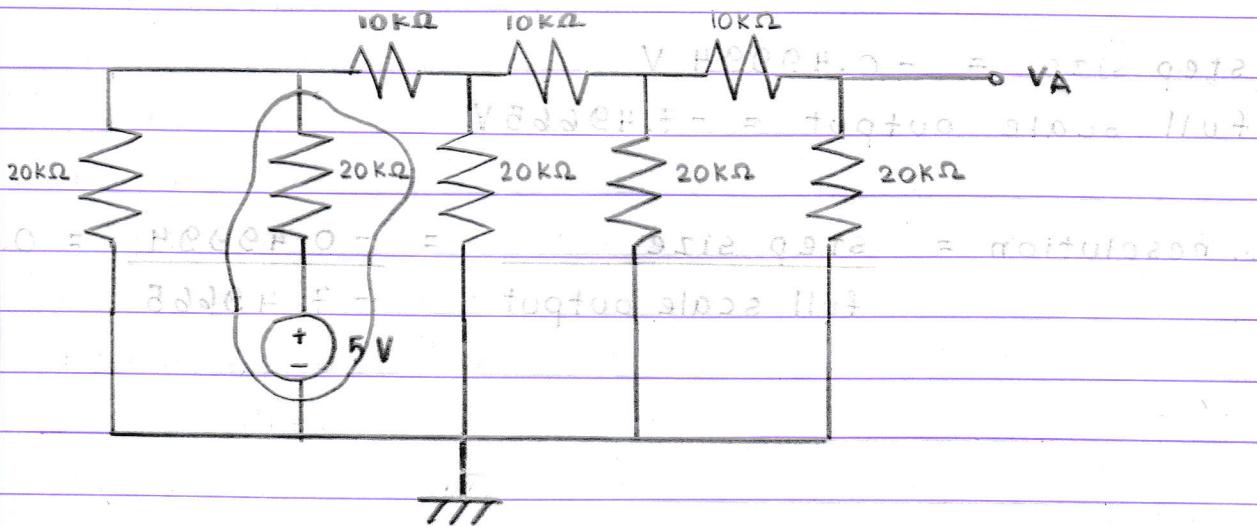
3) assuming,

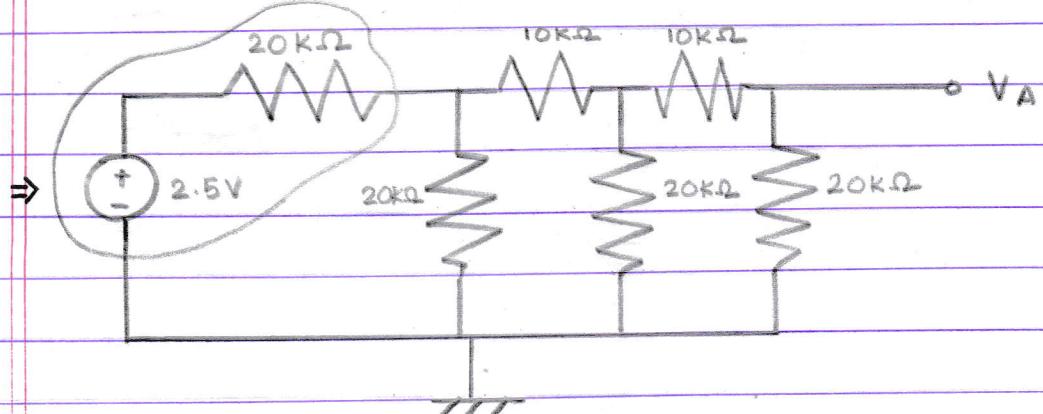
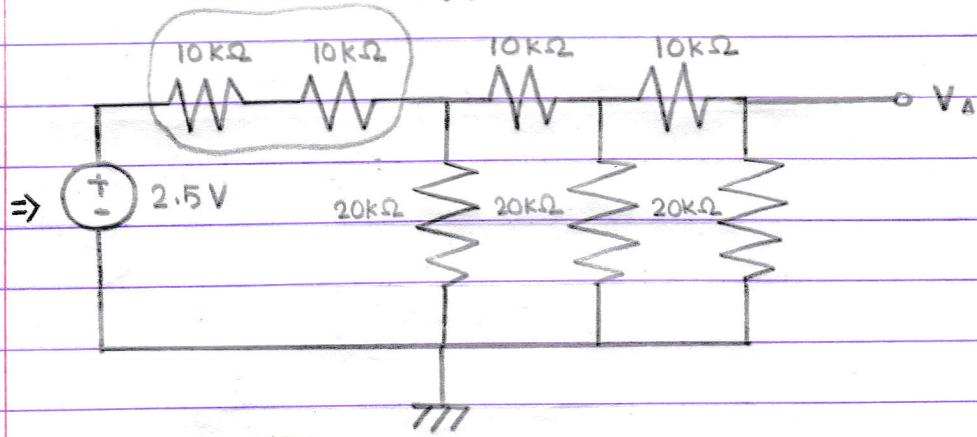
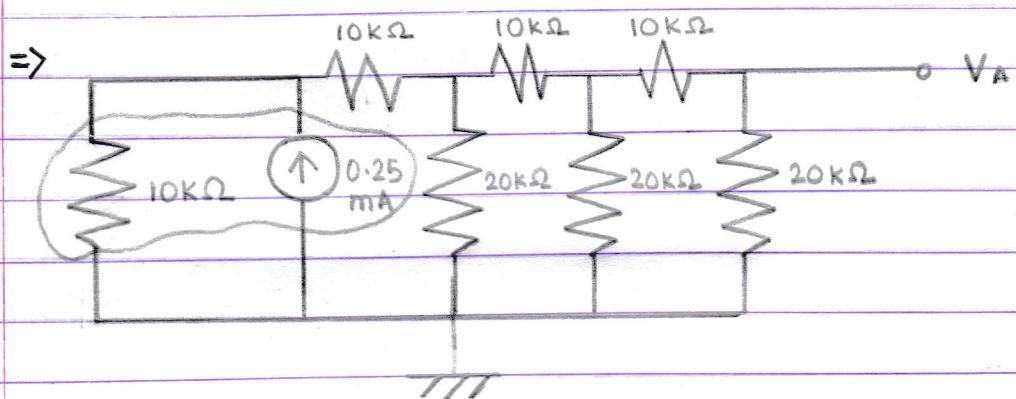
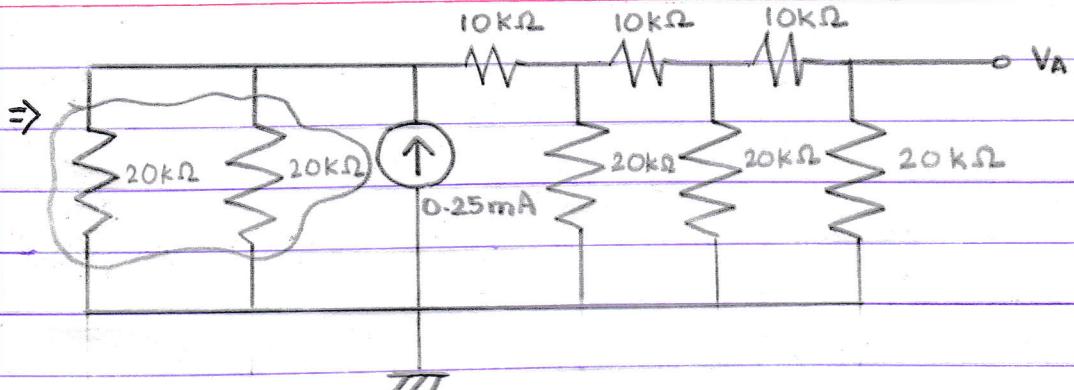
1 - MSB is least significant bit

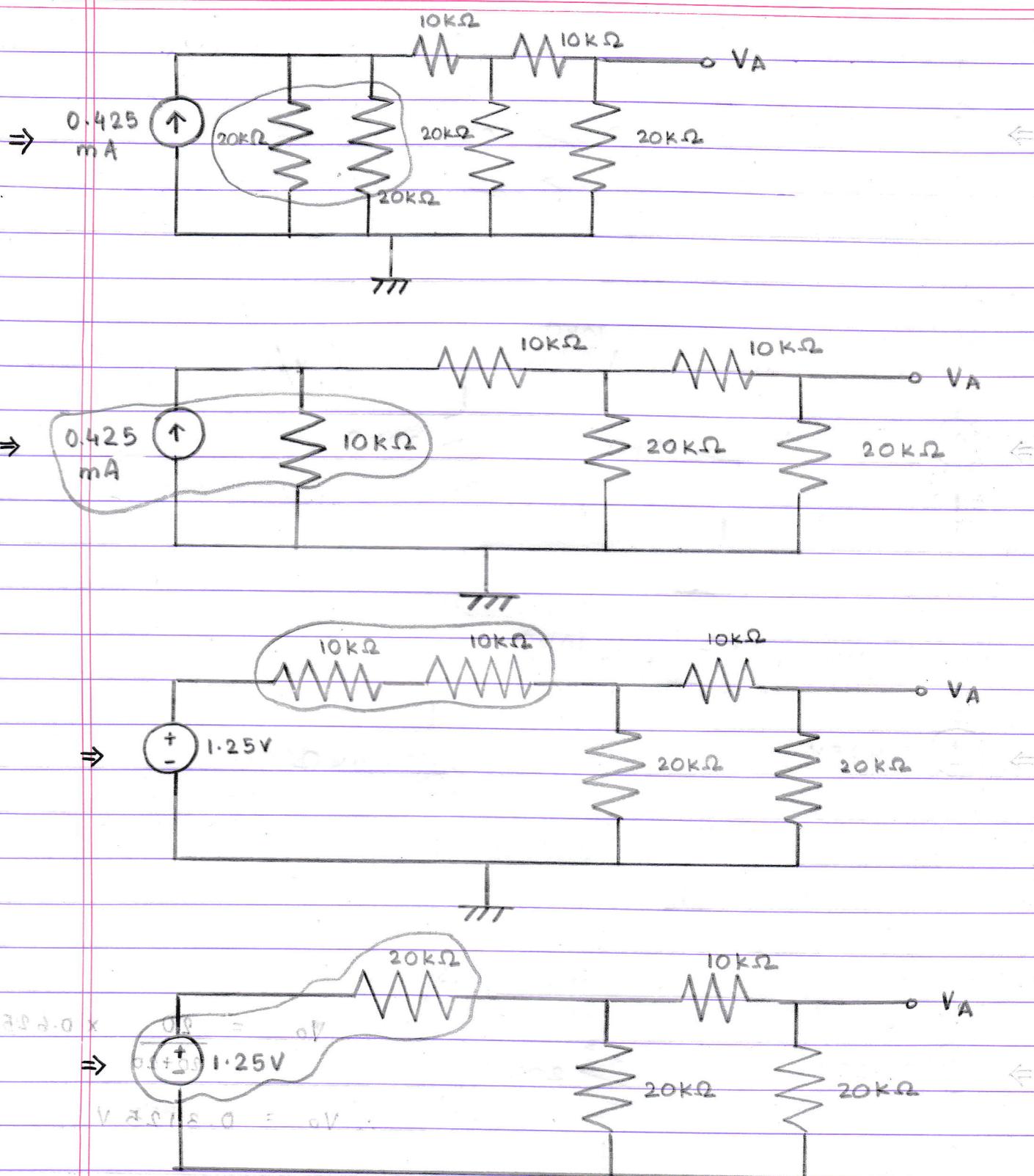
$$I = \frac{V}{R} = \frac{1}{20k\Omega}$$

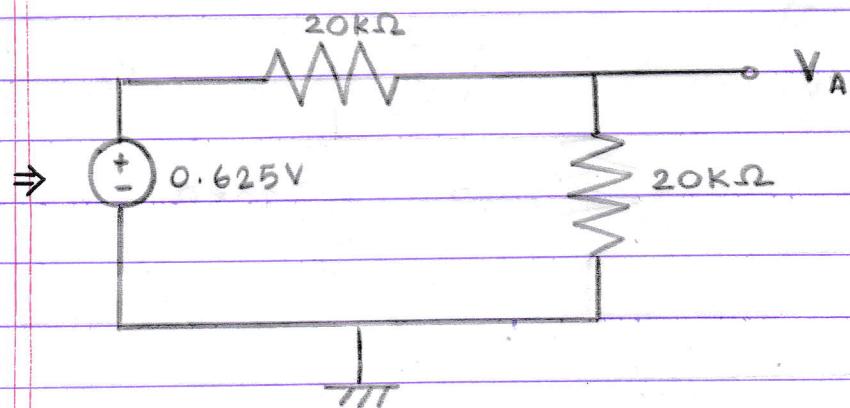
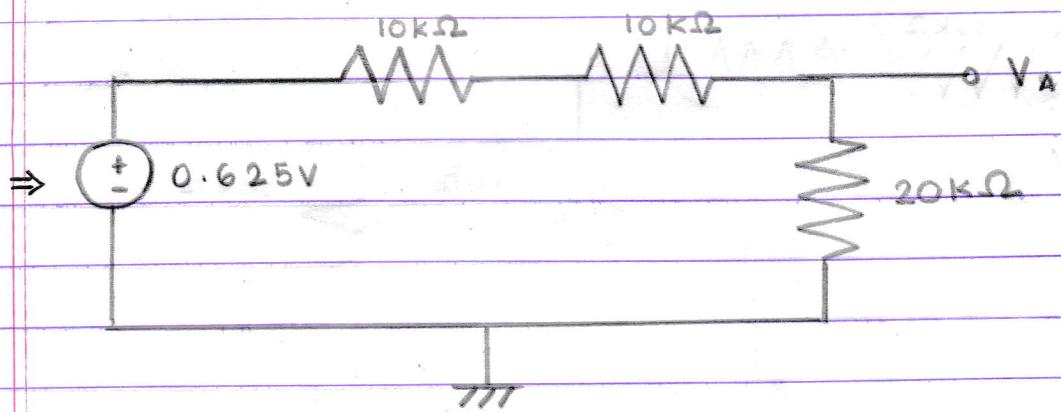
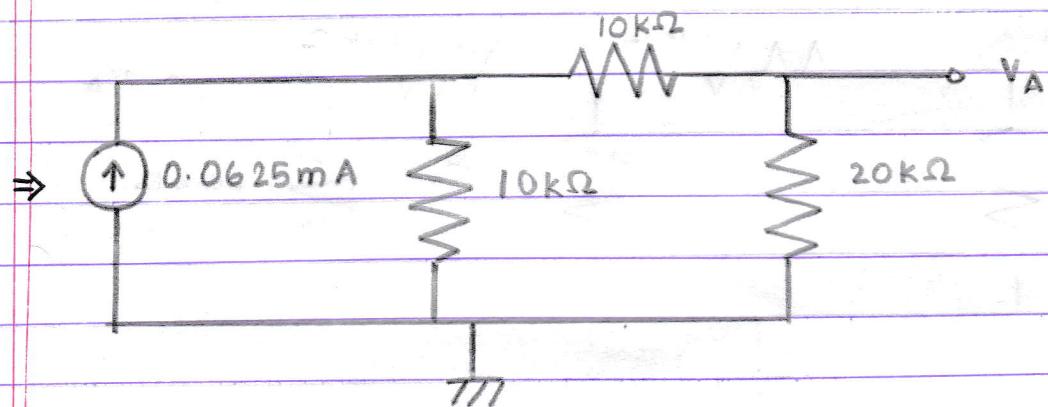
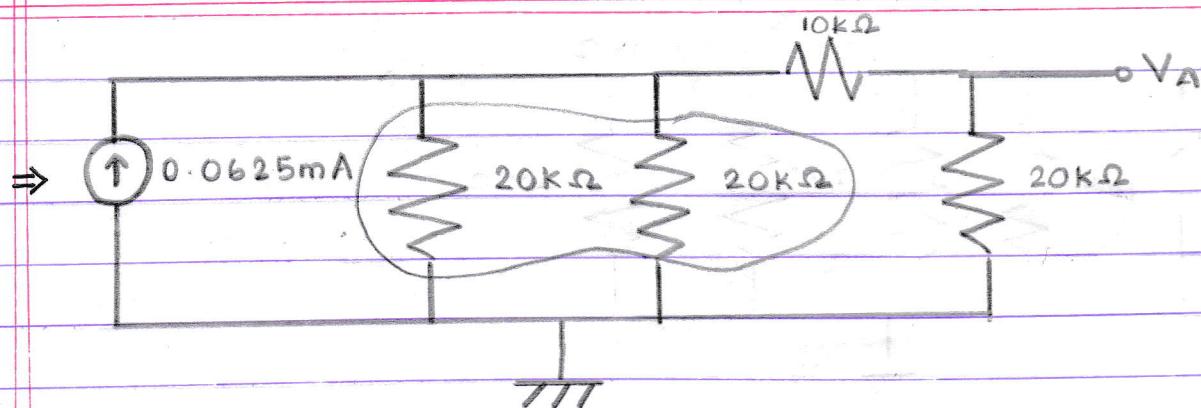
A = 5V, B = 0V, C = 30V, D = 0V

using source transformation - 3 bit digital word









$$V_A = \frac{20}{20+20} \times 0.625 = 0.3125 V$$

$$V_B = 0 V$$

$$V_O = - \left(\frac{20}{20} \times 0.625 + \frac{20}{20} \times 0 \right)$$

0 V is not attainable

$$\therefore V_O = -0.625 V$$

Validating the data,

In Proteus, we get $V_O = -0.620026 V$ when
 $D = 0 V$, $C = 0 V$, $B = 0 V$ and $A = 5 V$. Hence, validated.

4> ID = 21101098

Data = 38.00000 <=

high input voltage = $1.99 + 8.00 = 17 \text{ V}$ and gateV_{TJ} = 8

Datasheet for circuit 1, using high input voltage = 17 V

Data = 38.00000

input configuration	D (P01C00B0)	C (V)	V (V)	A180 output voltage, V _O
1	0	0	0	0.00272279
2	0	0	0	-1.69721
3	0	0	17	-3.39712
4	0	0	17	-5.09705
5	0	17	0	-6.79682
6	0	17	0	-8.49676
7	0	17	17	-10.1967
8	0	17	17	-11.8966
9	17	0	0	-13.4956
10	17	0	0	-13.4959
11	17	0	17	-13.4950
12	17	0	17	-13.4940
13	17	17	0	-13.4929
14	17	17	0	-13.4918
15	17	17	17	-13.4907
16	17	17	17	-13.4895

5) when $R_F = 1\text{ k}\Omega$,

$$\text{step size} = \frac{V_{FL}}{R_F} = \frac{9}{1000} = 0.009\text{ V}$$

$$\text{step size} = -1.69993279\text{ V}$$

$$\approx -1.7\text{ V}$$

V_{FL} = option_tugai_did pada 1 titik di setiap iterasi

when $R_F = 3\text{ k}\Omega$,

$$\text{step size} = -5.09361 - (0.00606164)$$

$$(V) = -5.09966164\text{ V}$$

$$\approx -5.1\text{ V}$$

PERSENKO	0	0	0	0	1
-5.09361 - 0.00606164	0	0	0	0	1
-5.1	0	0	0	0	1

as R_F increase $\times 3$ times, step size also increases $\times 3$ times. Hence,

$$\text{step size} = \frac{V_{FL}}{R_F} \propto \text{step size}$$

$$\text{step size} = \frac{V_{FL}}{R_F} = \frac{V_{FL}}{3R_F}$$

$$\text{step size} = \frac{0}{3R_F} = \frac{0}{3} = 0$$

$$\text{step size} = \frac{0}{3R_F} = \frac{0}{3} = 0$$