CSE260 Lab Report

Experiment Name: DESIGN AND IMPLEMENTATION OF 4-BIT

PARALLEL BINARY ADDER

Submitted by

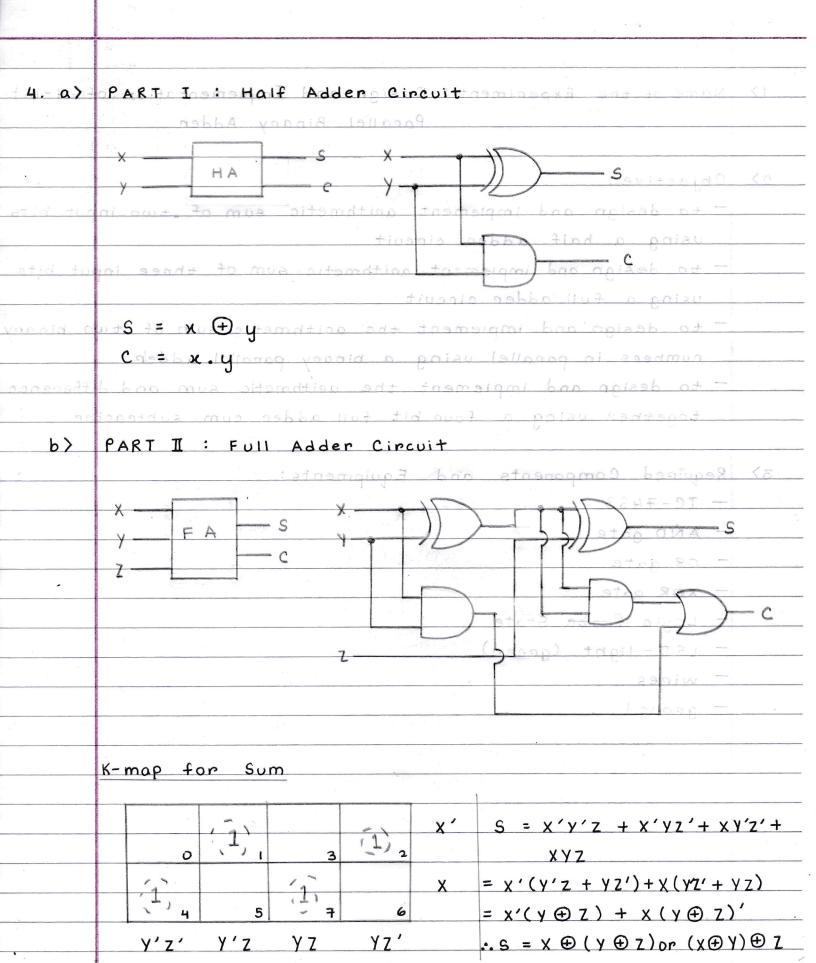
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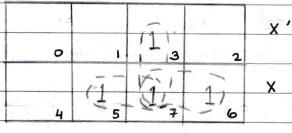
Section: 05

Date: 7 / 12 / 2020

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1>	Name of the Experiment: Design and Implementation of 4-bit												
	Parallel Binary Adder												
2>	Objective:												
	to design and implement arithmetic sum of two input bits												
	using a half adder circuit												
	to design and implement arithmetic sum of three input bits												
	using a full adder circuit												
	to design and implement the arithmetic sum of two binary numbers in parallel using a binary parallel adder												
	- to design and implement the arithmetic sum and difference												
	together using a four bit full adder cum subtractor												
	tivous adder Circuit												
3>	Required Components and Equipments:												
	- IC-7483												
	- AND gate												
	- OR gate												
	- XOR gate												
-	- Logic Probe State												
	- LED-light (green)												
	- wires												
	- ground												
	8-map 4an 5um												
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K-map for carry



Y'Z' Y'Z YZ YZ'

$$c = XY + XZ + YZ$$

$$= XY + (X + Y)Z$$

$$= XY + ((X \oplus Y) + XY)Z$$

$$= XY + (X \oplus Y)Z + XYZ$$

$$\therefore C = XY + (X \oplus Y)Z$$

$$= (x + y)(y + y')$$

$$= XY + XY' + YY + YY'$$

$$= XY + XY' + Y$$

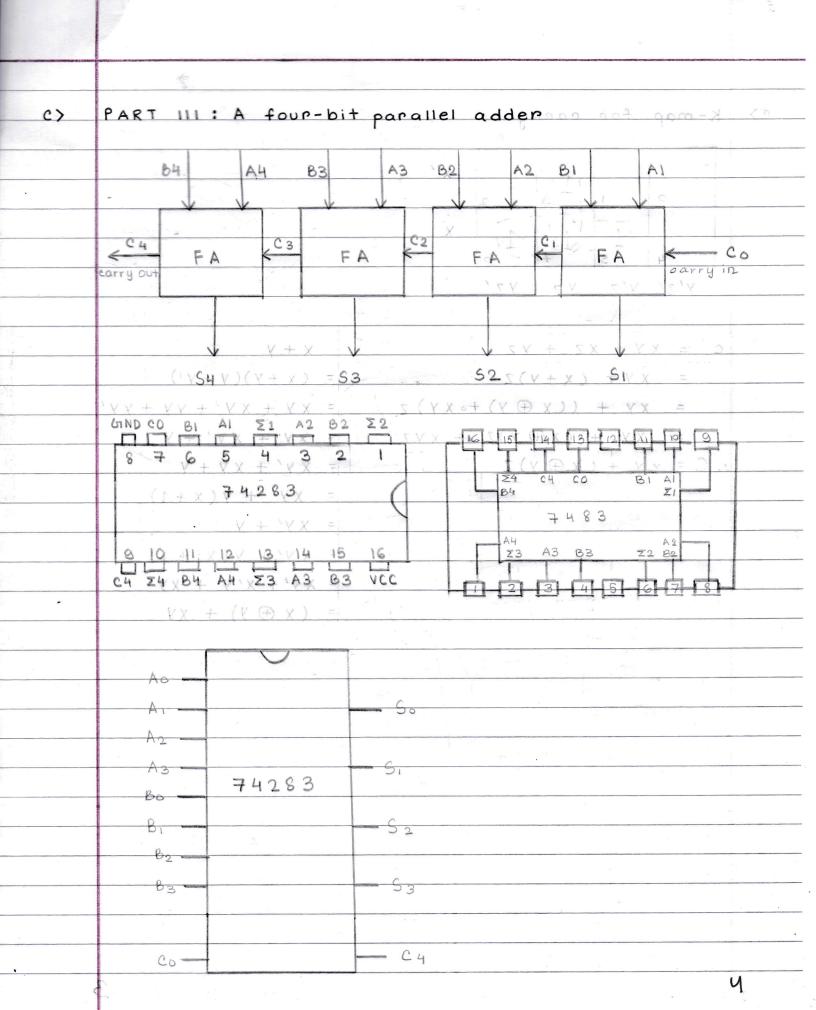
$$= xy' + xy + y$$

$$= XY' + Y(X+1)$$

$$= xy' + y(x' + x)$$

$$= xy' + x'y + xy$$

$$= (x \oplus y) + \chi y$$



0> PART IV: 4-Bit Parallel Adder cum Subtractor B3 A 4 FA FA FA Co (carry in Kearry out 52 Part II : Foll Adda A2 Ay 7463 BI Co -- C4

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	Discussion
	In this experiment, we had learnt how to implement and design different types of adders. There was one particular problem which I faced in Proteus was that despite of my circuit being accurate and correct, the LED light (green) would malfunction and give different results for the same circuit. Otherwise, the experiment was
	quite easy to conduct.
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