

CSE260 Lab Report

Experiment Name: DESIGN AND IMPLEMENTATION OF 4-BIT
PARALLEL BINARY ADDER

Submitted by

Name: Shaiane Prema Baroi

ID: 19241019

Section: 05

Date: 7 / 12 / 2020

1> Name of the Experiment: Design and Implementation of 4-bit Parallel Binary Adder

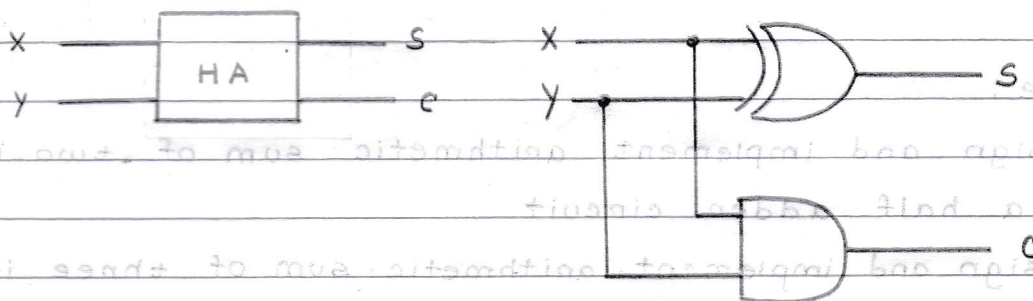
2> Objective:

- to design and implement arithmetic sum of two input bits using a half adder circuit
- to design and implement arithmetic sum of three input bits using a full adder circuit
- to design and implement the arithmetic sum of two binary numbers in parallel using a binary parallel adder
- to design and implement the arithmetic sum and difference together using a four bit full adder cum subtractor

3> Required Components and Equipments:

- IC-7483
- AND gate
- OR gate
- XOR gate
- Logic Probe State
- LED-light (green)
- wires
- ground

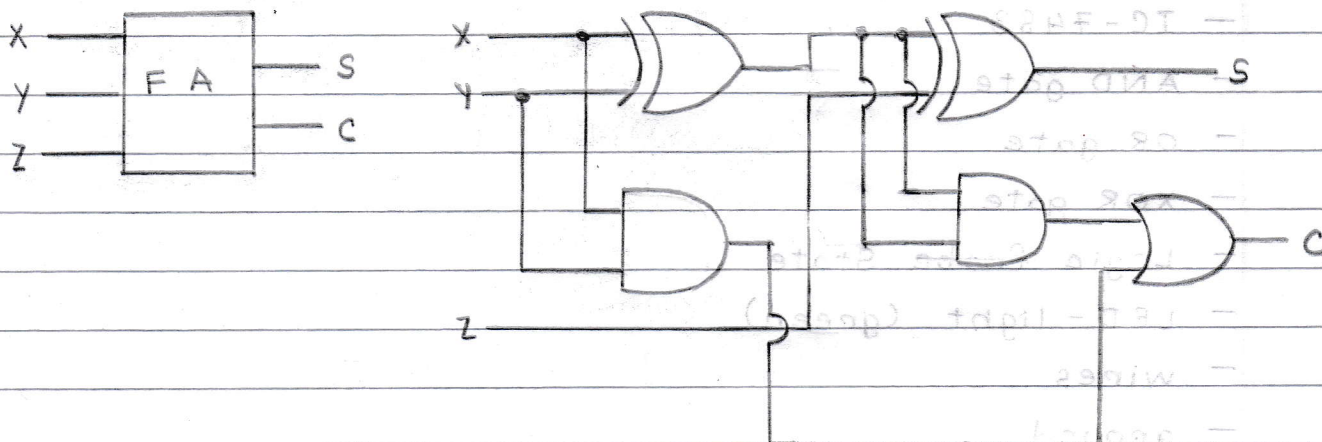
4. a) PART I : Half Adder Circuit



$$S = x \oplus y$$

$$c = x \cdot y$$

b) PART II : Full Adder Circuit



K-map for Sum

	(1) ₀		(1) ₂
	0	1	3
(1) ₄			(1) ₇
5		6	
$y'z'$	$y'z$	yz	yz'

x'

$$S = x'y'z + x'yz' + xy'z' + xyz$$

x

$$= x'(y'z + yz') + x(yz' + yz)$$

$$= x'(y \oplus z) + x(y \oplus z)'$$

$$\therefore S = x \oplus (y \oplus z) \text{ or } (x \oplus y) \oplus z$$

K-map for carry

		1			X'
0	1	3	2		
	1	1	1		X
4	5	7	6		
$Y'Z'$	$Y'Z$	YZ	YZ'		

$$C = XY + XZ + YZ$$

$$= XY + (X+Y)Z$$

$$= XY + ((X \oplus Y) + XY)Z$$

$$= XY + (X \oplus Y)Z + XYZ$$

$$\therefore C = XY + (X \oplus Y)Z$$

$$X + Y$$

$$= (X+Y)(Y+Y')$$

$$= XY + XY' + YY + YY'$$

$$= XY + XY' + Y$$

$$= XY' + XY + Y$$

$$= XY' + Y(X+1)$$

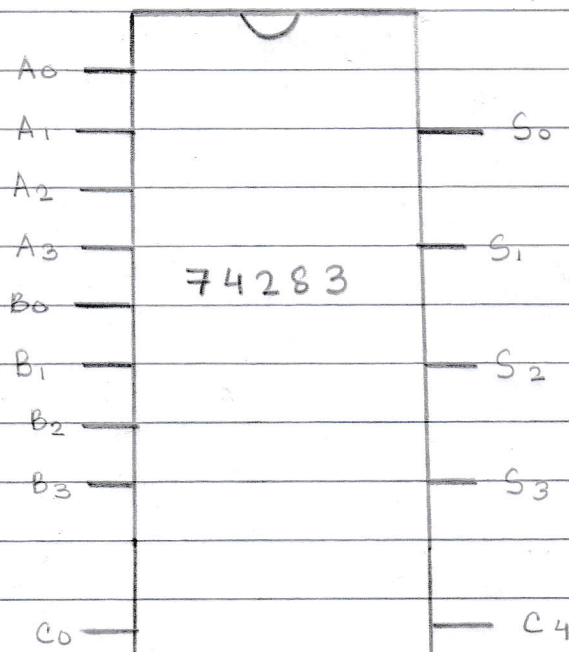
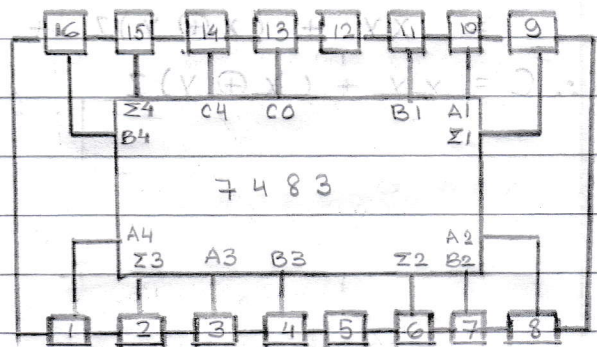
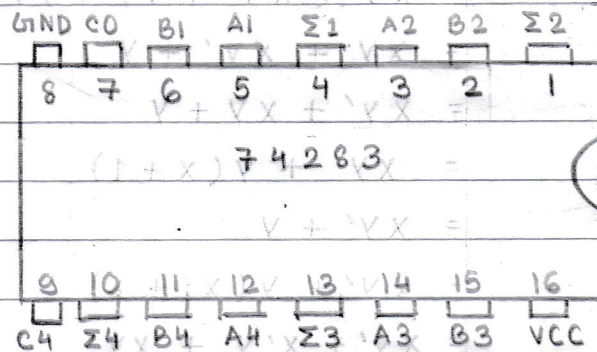
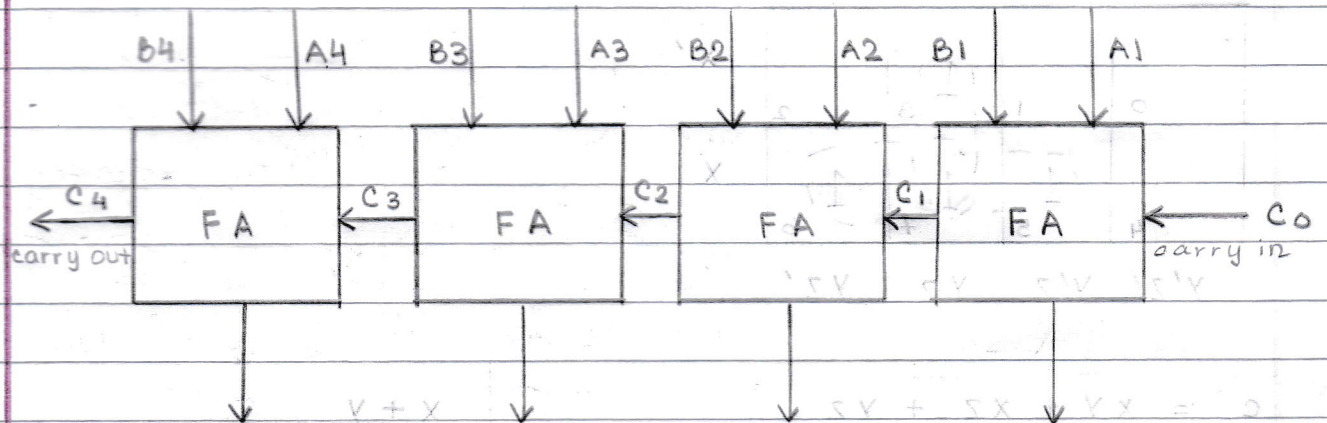
$$= XY' + Y$$

$$= XY' + Y(X' + X)$$

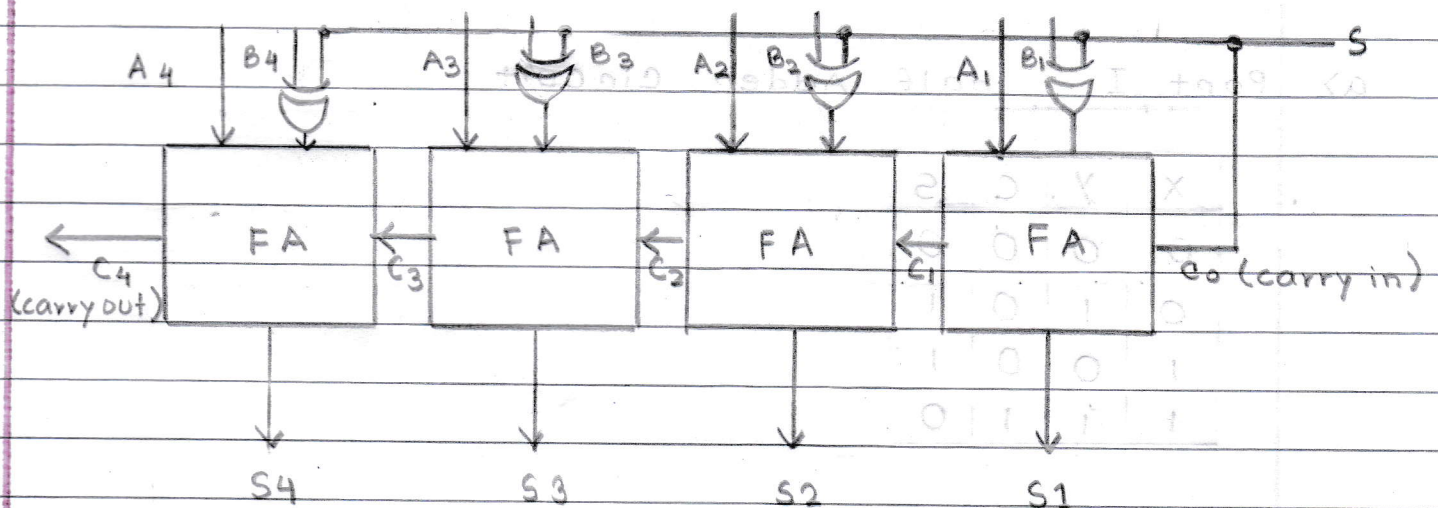
$$= XY' + X'Y + XY$$

$$= (X \oplus Y) + XY$$

c) PART III: A four-bit parallel adder



d) PART IV : 4-Bit Parallel Adder cum Subtractor



			2	3	5	7	8
A ₁			0	0	0	0	0
A ₂		S ₁	0	0	0	0	0
A ₃			1	0	1	0	0
A ₄		S ₂	1	0	0	1	0
B ₁	7463		0	1	1	1	0
B ₂		S ₃	1	0	0	0	1
B ₃			0	1	1	0	1
B ₄		S ₄	0	1	0	1	1
C ₀		C ₄	1	1	1	1	1

5> Results (Truth Table)

a> Part I : Half Adder Circuit

X	Y	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

b> Part II : Full Adder Circuit

X	Y	Z	C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

Discussion

In this experiment, we had learnt how to implement and design different types of adders. There was one particular problem which I faced in Proteus was that despite of my circuit being accurate and correct, the LED light (green) would malfunction and give different results for the same circuit. Otherwise, the experiment was quite easy to conduct.