## **CSE260 Lab Report**

Experiment Name: PARITY GENERATOR AND CHECKER

## Submitted by

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Section: 05

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## 6> Discussions

In this experiment, we had learnt about the Parity Generator and Papity Checker. The Papity Checker generates an extra bit according to the data which is then transmitted to the receiver. The data along with the parity bit is then checked by the Parity Checker which validates if the transmission has been done properly or not. In the first part of the experiment, we observed the process which takes place on the sender's end. We constructed an Fren Parity using a combination of three XOR gates and used the different values as inputs (according to the question) and obtained the corresponding bits. We noticed how the parity bit changed each time the input was changed in order to ensure that there was an even number of 1's in the entire series of bits. In the second part of the experiment, we saw the process which takes place on the neceiver's end. Once a series of bit is neceived, the Parity Checker checks if the number of 1's is even or odd as per the Parity used. Since, we used Even Parity in our experiment, the Parity Checker checked if the number of 1's necesived were even on not. If they were not even, an eppop was generated and otherwise, no eppop. At this point, we realised that there were some limitations in the Parity Checker: If a series of data, such that 1001 is being transmitted, the parity bit would be O. Hence, the transmitted bits would be 01001. Then, if by any chance, the data gets altered to 1001, in which case, the parity bit would still be 0 and the Papity Checker wouldn't produce any error even though the data is corrupt. Hence, the Parity

Checken has these limitations.