CSE350

DIGITAL ELECTRONICS AND PULSE TECHNIQUES

LAB ASSIGNMENT 05

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SECTION: 10

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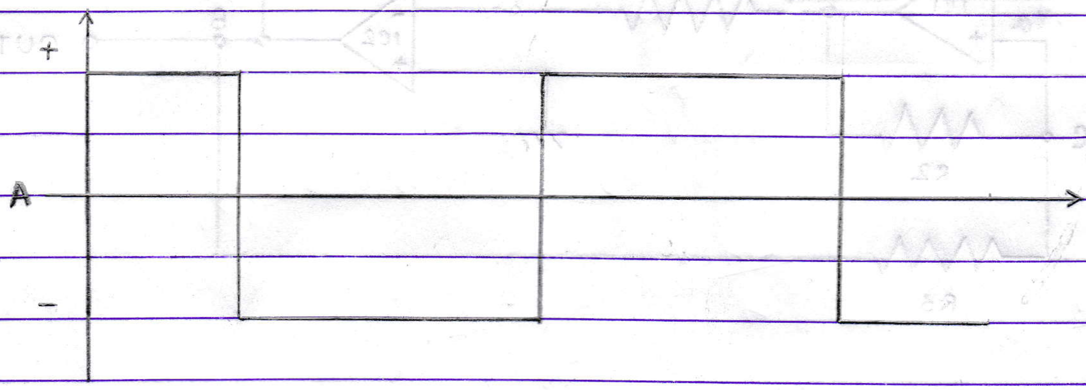
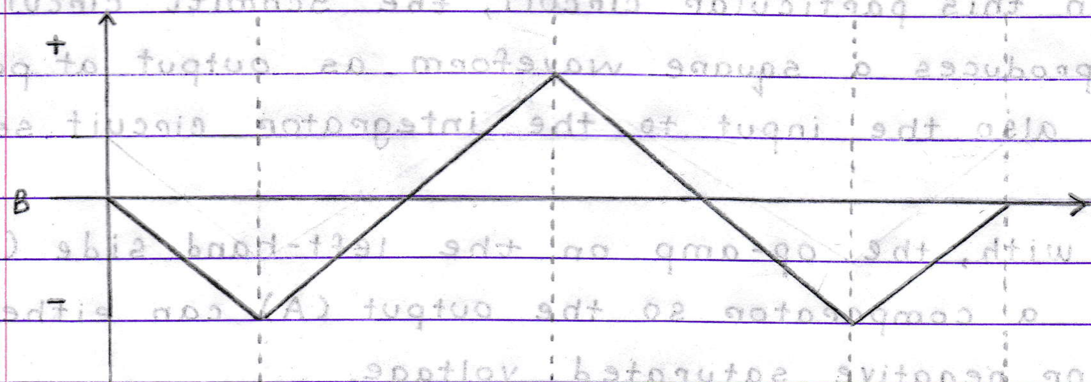
Report

1. Output wave shape at point A



Output wave shape at point B



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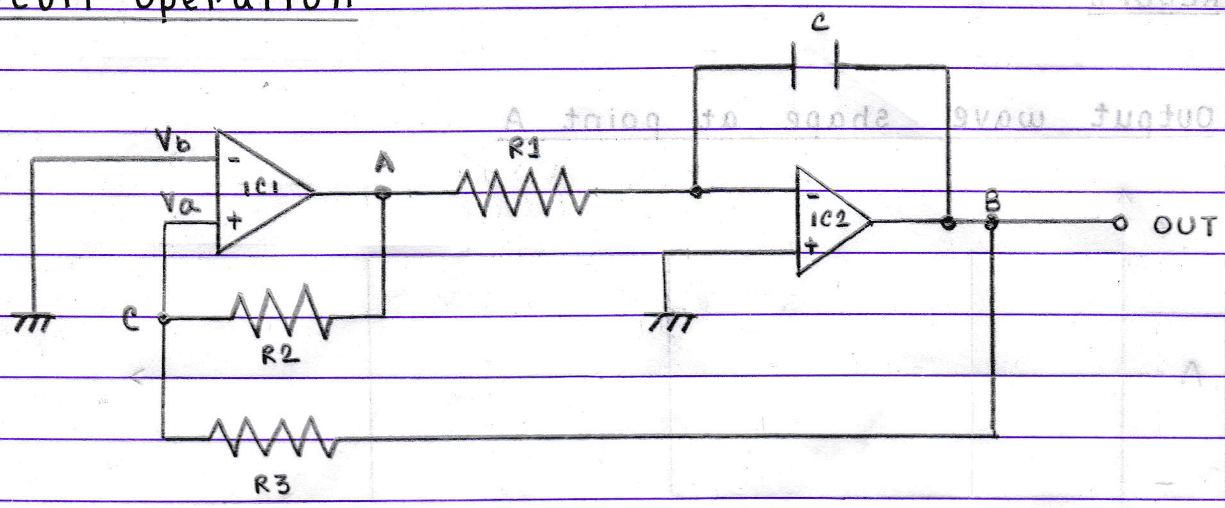
2. Circuit Operation



The triangular wave oscillator consists of two sections: a comparator circuit (Schmitt circuit) and an integrator circuit. In this particular circuit, the Schmitt circuit section produces a square waveform as output at point A which is also the input to the integrator circuit section.

To begin with, the op-amp on the left-hand side (IC_1) acts as a comparator so the output (A) can either be positive or negative saturated voltage.

$$A \rightarrow V_{SAT} \text{ or } -V_{SAT}$$

The difference between the voltage at the non-inverting terminal and the voltage at the inverting terminal can be defined as -

$$V_{id} = V_a - V_b$$

The voltage at the inverting terminal is connected to the ground, therefore -

$$V_b = 0$$

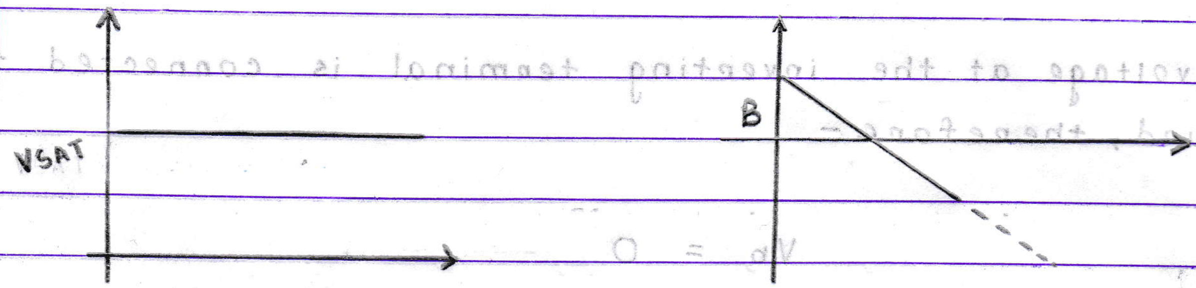
$$\Rightarrow V_{id} = V_a - 0$$

$$\therefore V_{id} = V_a$$

So, when $V_a > 0$, then $V_{id} > 0$ and so $A = V_{sat}$
when $V_a < 0$, then $V_{id} < 0$ and so $B = -V_{sat}$

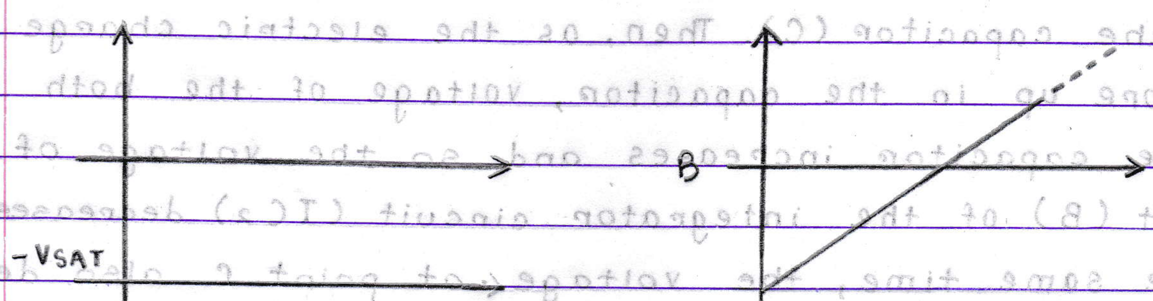
Hence, this is how a square waveform is produced at the output of the Schmitt circuit (A).

As mentioned before, the output (A) produced at the Schmitt circuit (IC_1) is the input to the integrator circuit (IC_2). So, when A is positive saturated voltage ($A = V_{SAT}$) then B is negative-going ramp. This is because the electric current flows through the resistor (R1) and into the capacitor (C). Then, as the electric charge begins to store up in the capacitor, voltage of the both edges of the capacitor increases and so the voltage of the output (B) of the integrator circuit (IC_2) decreases gradually At the same time, the voltage at point C also decreases when the voltage at point B also decreases.



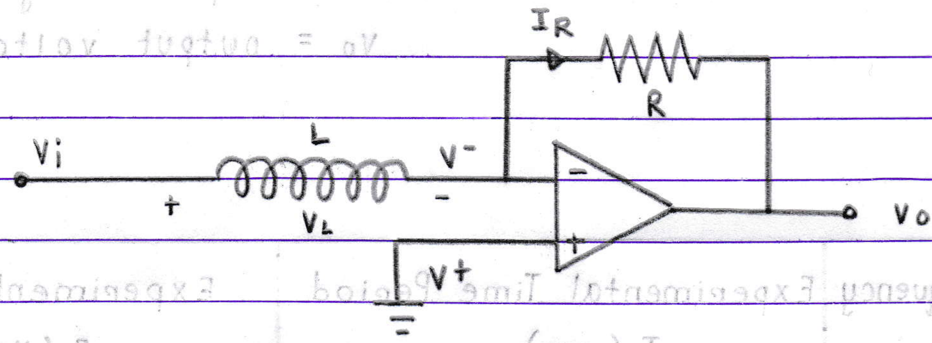
if A = VSAT then B = -ve going ramp

When the voltage at point C falls below 0V, the voltage of the output of Schmitt circuit (A) changes into minus rapidly. When A is negative saturated (A = -VSAT), then B is positive-going ramp. This is because the electric current flow to the capacitor (C) reverses and the electric current flows through the direction of point A through the resistor (R1), the voltage of point B increases. When the voltage of point C exceeds 0V, the output (A) of the Schmitt circuit changes into the plus rapidly. This process ~~rea~~ repeats and therefore, a square waveform is produced at the output of the Schmitt circuit (A) and a triangular waveform is produced at the output of the integrator circuit (B).



if A = VSAT then B = +ve going ramp

3. Yes, the integrator circuit can be implemented with an inductor.



$$I_R = \frac{0 - V_o}{R} = \frac{-V_o}{R} \quad ; \quad \left.\begin{aligned} V^- &= 0V \\ V^+ &= 0V \end{aligned}\right\} \text{virtual ground concept}$$

KCL $I_L = 0 + I_R$ $\quad V_L = V_i - 0$ $\quad V_L = L \dfrac{dI_L}{dt}$

$\therefore I_L = I_R$ $\quad \therefore V_L = V_i$

$$\therefore V_L = L \frac{dI_L}{dt} = L \frac{dI_R}{dt}$$

$$\therefore V_i = V_L = -\frac{L}{R} \times \frac{dV_o}{dt}$$

$$\Rightarrow \frac{-R}{L} V_i = \frac{dV_o}{dt}$$

$$\Rightarrow \int \frac{dV_o}{dt} \times dt = -\int \frac{R}{L} V_i \, dt$$

$$V_o = -\int \frac{R}{L} V_i \, dt$$

where, R = negative feedback resistance
L = inductence
Vi = input voltage
Vo = output voltage

Data Table

Theoretical Frequency	Experimental Time Period T (ms)	Experimental Frequency F (Hz)
156.25	6.50	154

Theoretical frequency, $f = \frac{1}{4R_1C} \times \frac{R_2}{R_3}$

$= \frac{1}{(4 \times 10 \times 10^3 \times 0.4 \times 10^{-6})} \times \frac{10}{4}$

$= 156.25 \text{ Hz}$

Experimental Time Period, $t = (6.48 \times 10^{-3}) - (12.98 \times 10^{-3})$

$= 6.50 \times 10^{-3} \text{ s}$

$= 6.50 \text{ ms}$

Experimental frequency $= \frac{1}{t} = \frac{1}{6.50 \times 10^{-3}} = 153.8 \text{ Hz} \approx 154 \text{ Hz}$

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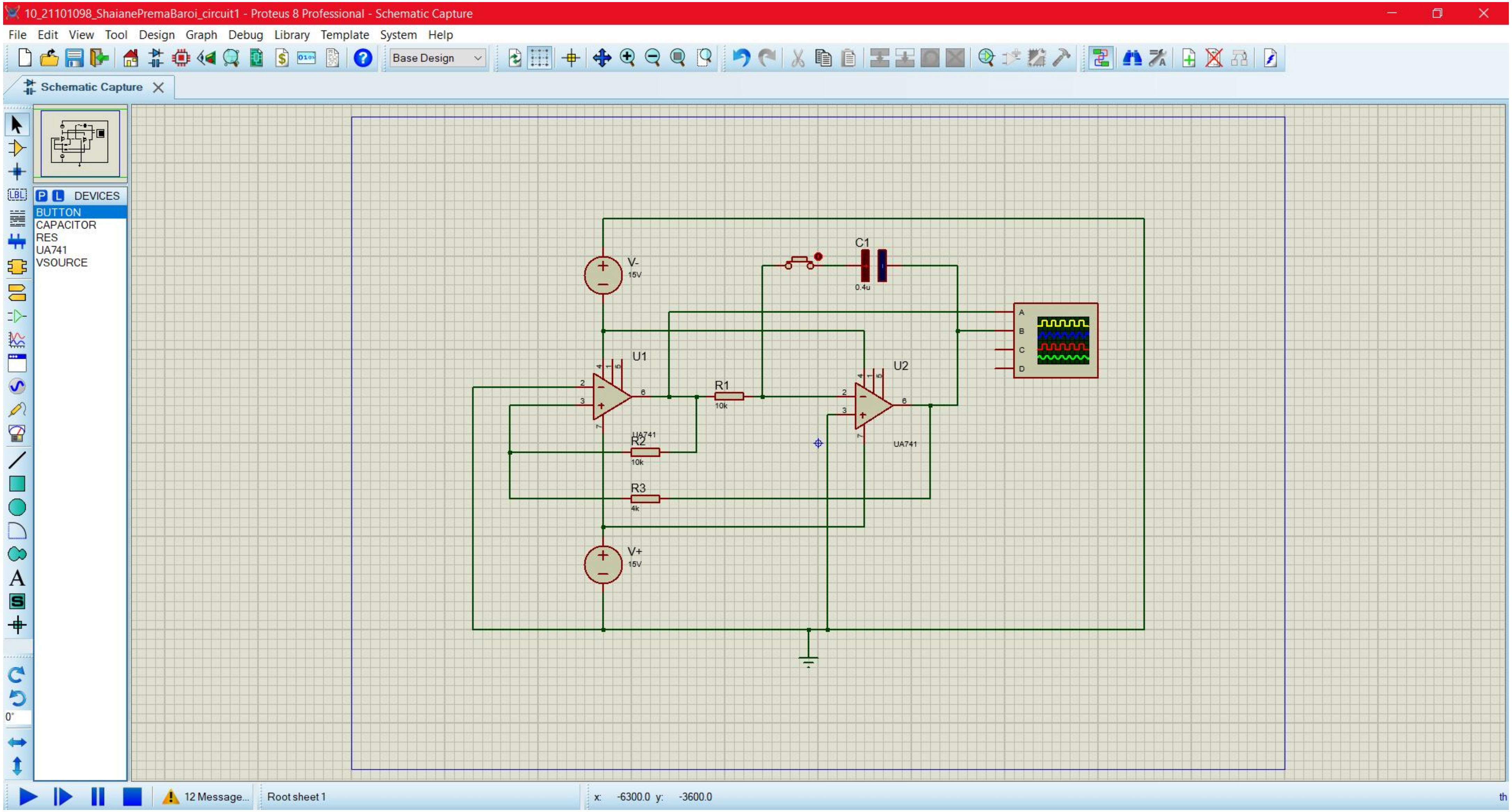
10_21101098_ShaianePremaBaroi_circuit1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
BUTTON
CAPACITOR
RES
UA741
VSOURCE
V-
15V
C1
0.4u
U1
U2
R1
10k
R2
10k
UA741
R3
4k
V+
15V
A
B
C
D
12 Message...
Root sheet 1
x: -6300.0 y: -3600.0

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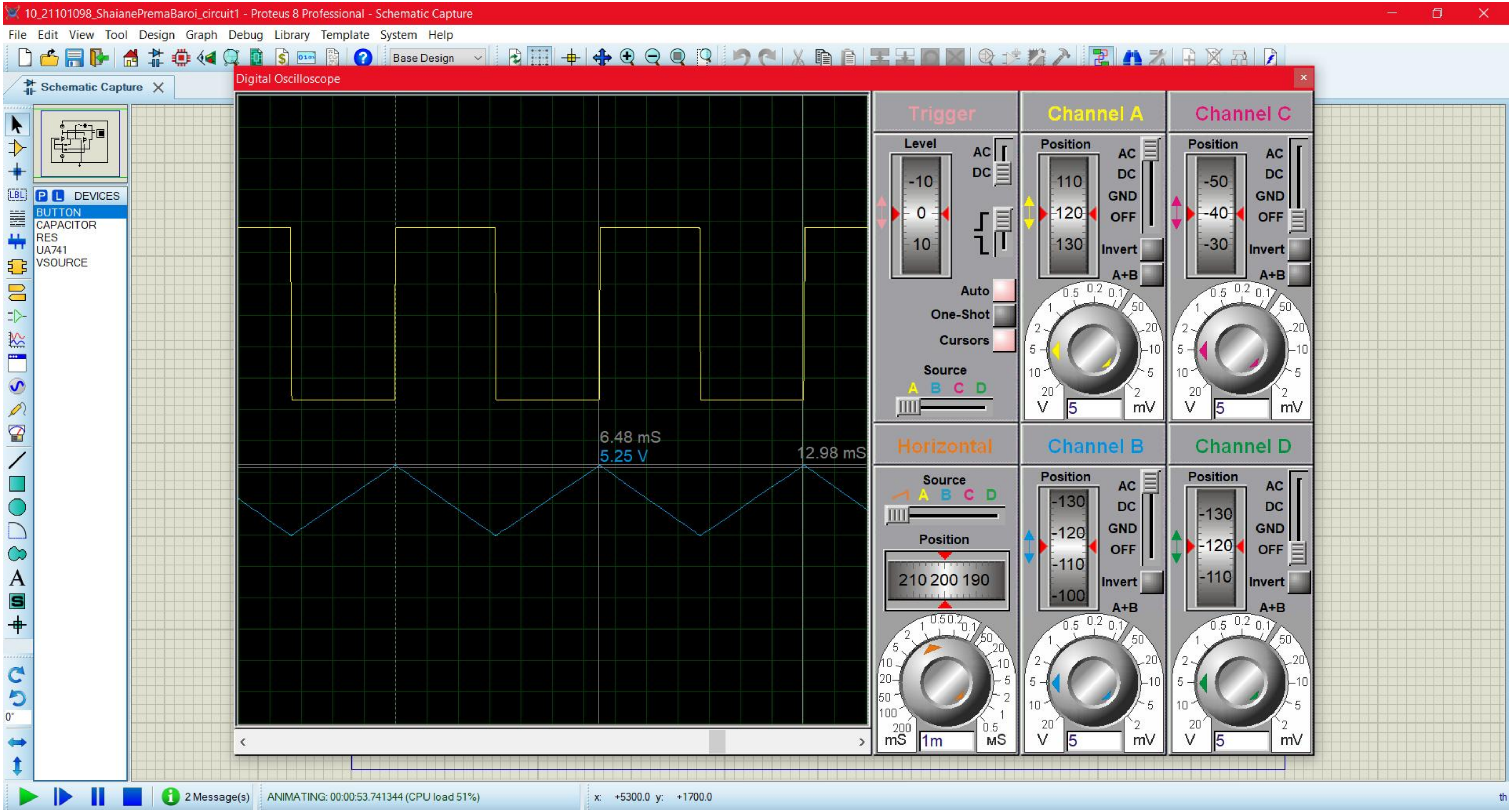
10_21101098_ShaianePremaBaroi_circuit1 - Proteus 8 Professional - Schematic Capture
Digital Oscilloscope
6.48 mS
5.25 V
12.98 mS
Trigger
Channel A
Channel C
Horizontal
Channel B
Channel D
ANIMATING: 00:00:53.741344 (CPU load 51%)