CSE350

DIGITAL ELECTRONICS AND PULSE TECHNIQUES

LAB ASSIGNMENT 02

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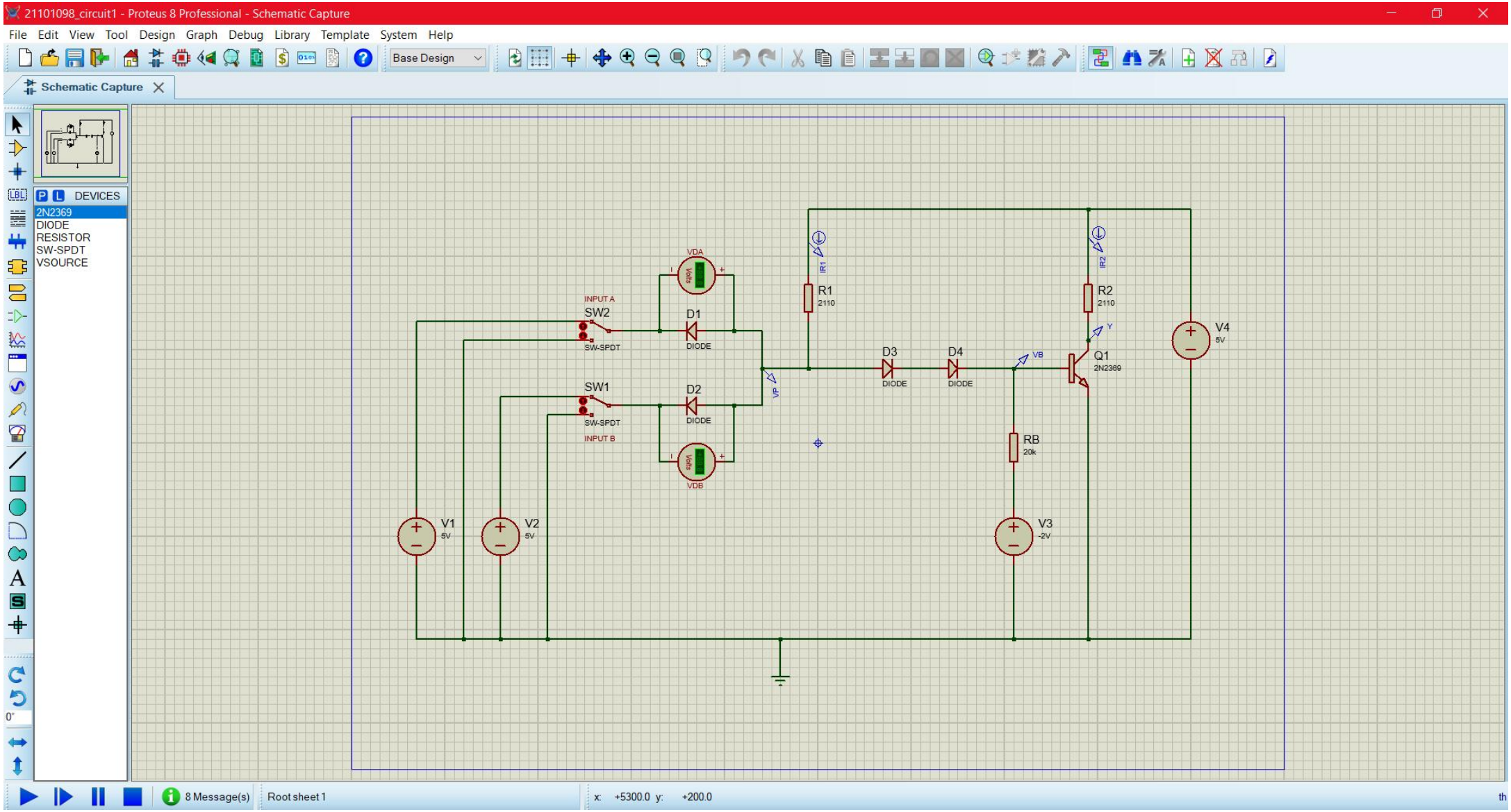
SECTION: 10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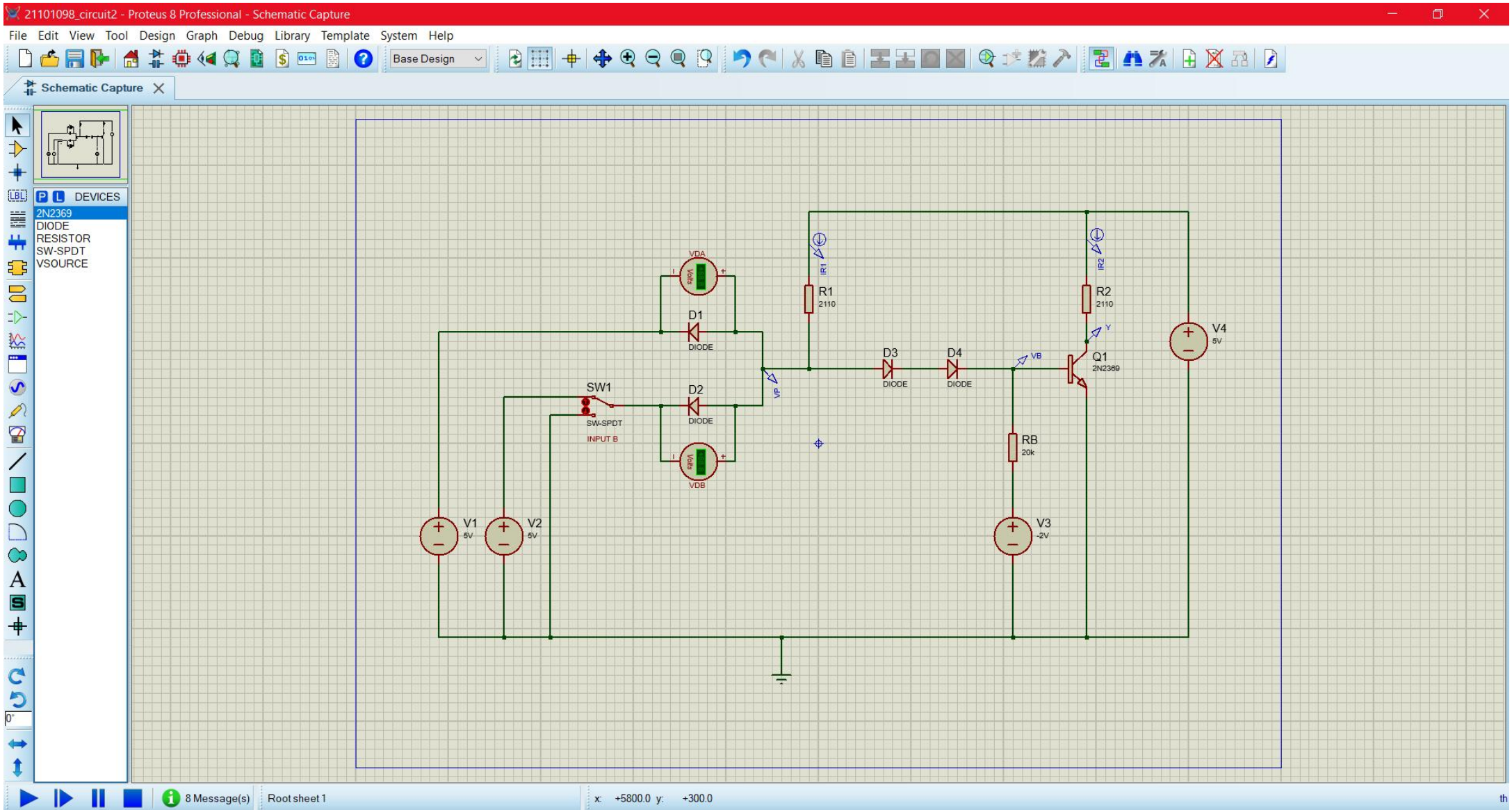
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
2N2369
DIODE
RESISTOR
SW-SPDT
VSOURCE
VDA
INPUT A
SW2
SW-SPDT
D1
DIODE
SW1
SW-SPDT
INPUT B
D2
DIODE
VDB
IR1
R1
2110
IR2
R2
2110
D3
DIODE
D4
DIODE
VB
VF
Y
Q1
2N2369
RB
20k
V1
5V
V2
5V
V3
-2V
V4
5V
8 Message(s)
Root sheet 1
x: +5300.0 y: +200.0


21101098_circuit2 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
2N2369
DIODE
RESISTOR
SW-SPDT
VSOURCE
VDA
VDB
D1
D2
D3
D4
DIODE
SW1
SW-SPDT
INPUT B
R1
2110
R2
2110
RB
20k
Q1
2N2369
V1
5V
V2
5V
V3
-2V
V4
5V
IR1
IR2
VA
VB
Y
8 Message(s)
Root sheet 1
x: +5800.0 y: +300.0

Laboratory Tasks

3.

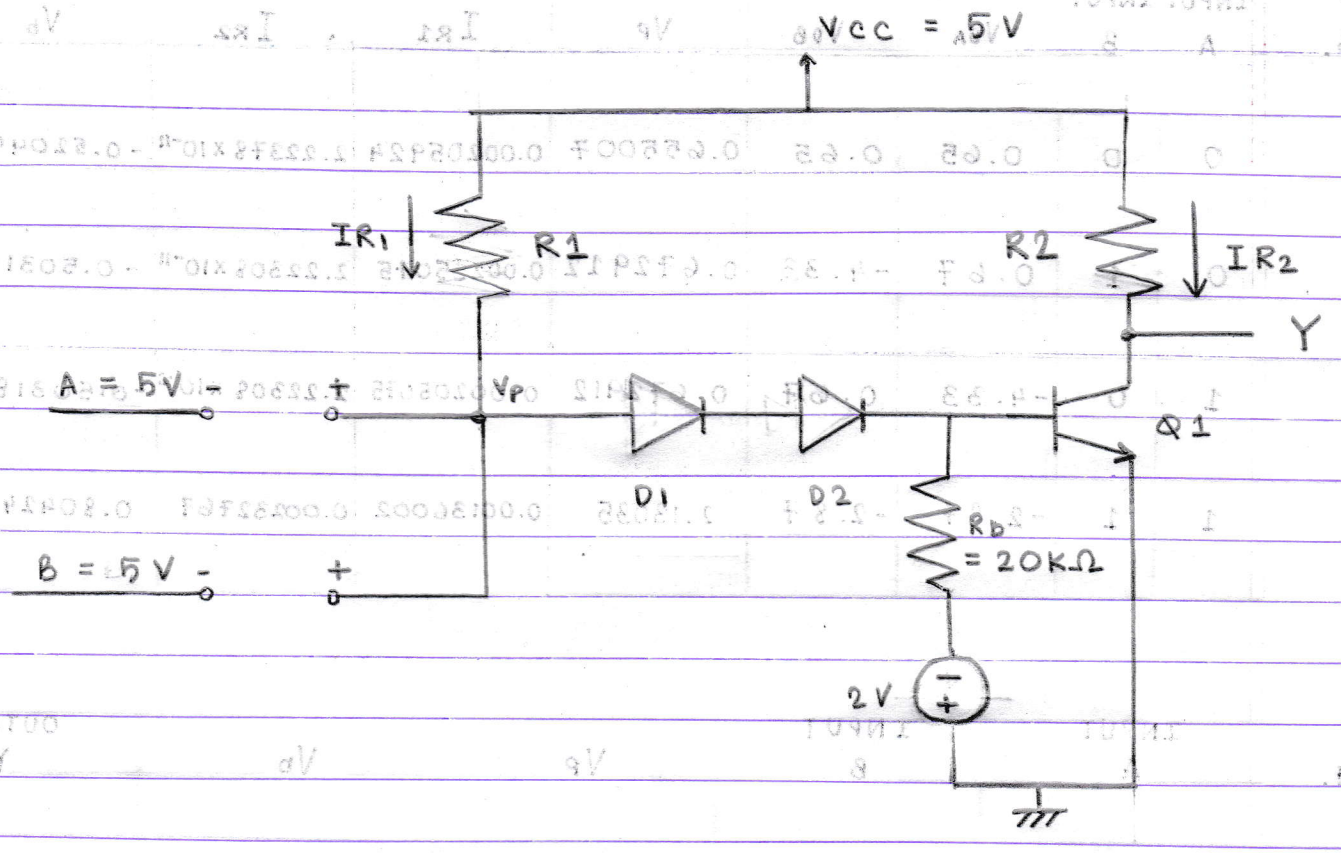
INPUT A	INPUT B	V_{DA}	V_{DB}	V_P	I_{R1}	I_{R2}	V_b	OUTPUT Y
0	0	0.65	0.65	0.655007	0.00205924	2.22378×10^{-11}	-0.52049	5
0	1	0.67	-4.33	0.672912	0.00205075	2.22308×10^{-11}	-0.503187	5
1	0	-4.33	0.67	0.672912	0.00205075	2.22308×10^{-11}	-0.503187	5
1	1	-2.87	-2.87	2.13035	0.00136002	0.00232767	0.804241	0.08862

4.

INPUT A	INPUT B	V_P	V_D	OUTPUT Y
1	0	0.672912	-0.503187	5
1	1	2.13035	0.804241	0.0886165

Report

1.



2. In table 2, we can observe the logical operation of a NOT gate. In this circuit, we have fixed input A to HIGH and can only change input B to HIGH or LOW. Then, when input B is HIGH, the output Y is low, and vice-versa, when input B is LOW, output Y is HIGH.

We reached this logical operation by manipulating the circuit from NAND operation of figure 1. We did

so by setting the values of input A fixed at HIGH. In this way, input A acts as if it is OFF and so only input B simply gets inverted.

3. A NAND operation ~~sos~~ consists of an AND gate and a NOT gate combined in the circuit. At first, the inputs go through an AND gate for which we get the following outputs -

A	B	OUTPUT
0	0	0
0	1	0
1	0	0
1	1	1

This means that we obtain a logical HIGH value only when both the inputs, A and B are HIGH. When this output goes through the NOT gate, the values get inverted, such that -

Ø

Input	Output
0	1
1	0

So, for every logical HIGH, we obtain a logical LOW, and vice-versa. Together, the AND gate and NOT gate operates to be a NAND gate

A	B	Output
0	0	1
0	1	1
1	0	1
1	1	0

4. when one of the inputs is HIGH and the other one is LOW, Q1 ~~was~~ operates in the CUT-OFF State.

CUT-OFF $I_B, I_C, I_E = 0$

$V_{BE} < 0.5\,V$

$I_B = -2.84667 \times 10^{-12}\,A \approx 0\,A$

$I_C = 1.72308 \times 10^{-11}\,A \approx 0\,A$

$I_E = 5.39052 \times 10^{-12}\,A \approx 0\,A$

[PROVED]

$V_B = -0.503187\,V$

$V_E = 0\,V$

$\therefore V_{BE} = V_B - V_E$

$= -0.503187 - 0$

$= -0.503187\,V < 0.5\,V$

[PROVED]

5. The maximum value of inputs A, B to keep the output HIGH are -

$V_A = 1.2\,V$

$V_B = 1.2\,V$