CSE350

DIGITAL ELECTRONICS AND PULSE TECHNIQUES

LAB ASSIGNMENT 01

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SECTION: 10

Simulation Tasks

Table for OR Gate

V_A	V_B	V_{R1}	V_{R2}	I_{R1}	I_{R2}	$V_R = Y$
0V	0V	0V	0V	1.193×10^{-20} A	1.193×10^{-20} A	1.387×10^{-5} V
0V	5V	0V	4.33mV	-4.431×10^{-12} A	4.421×10^{-5} A	4.42123 V
5V	0V	4.33mV	0V	4.421×10^{-5} A	-4.431×10^{-12} A	4.42123 V
5V	5V	2.18mV	2.18mV	2.220×10^{-5} A	2.220×10^{-5} A	4.4412 V

Table for AND Gate

V_A	V_B	V_{R1}	V_{R2}	I_{R1}	I_{R2}	$V_R = Y$
0V	0V	2.18mV	2.18mV	2.220×10^{-5} A	2.220×10^{-5} A	0.558803 V
0V	5V	4.33mV	0V	4.421×10^{-5} A	9.431×10^{-12} A	0.578773 V
5V	0V	0V	4.33mV	-9.431×10^{-12} A	4.421×10^{-5} A	0.578773 V
5V	5V	0V	0V	-5×10^{-12} A	-5×10^{-12} A	5V

Inverter

V_i	V_{R1}	V_{R2}	V_{RC}	I_1	I_2	I_B	I_C	Y
0V	0.65V	4.35V	5V	4.35	4.351×10^{-5}A	-3.19×10^{-12}A	1.729×10^{-11}A	5V
5V	4.32V	5.68V	0.034V	0.0002878 A	5.68×10^{-5}A	0.000231A	0.000496A	0.034V

Report

1. When both the inputs are low, then both the diodes will be ON and the output will be low. Other wise, when either of the input is high, the corresponding diode will be ON, and the output will be low. Only when both the inputs are high, both the diodes will be OFF and the output will be high.

2. The diodes work fine under the conditions $V_A = V_B = 6V$ and $V_R = 5V$.

3. The $R_2 = 100K$ at the base of the inverter controls the base current.

4. Saturation

$V_{BE} = 0.8V$, $V_{CE} = 0.2V$ $\quad I_C = 0.0022$

$V_i = 5V$ $\quad I_B = 0.0002$

$V_C = 0.108 \approx 0.2$, $\quad V_B = 0.703 \approx 0.8$

$V_E = 0$

$\therefore V_{BE} = 0.8V$ and $V_{CE} = 0.2V$

Cutoff

$V_i = 0\,V$, $V_O = 5\,V$, $V_{BE} < 0.7\,V$ and $V_{BC} < 0.5\,V$

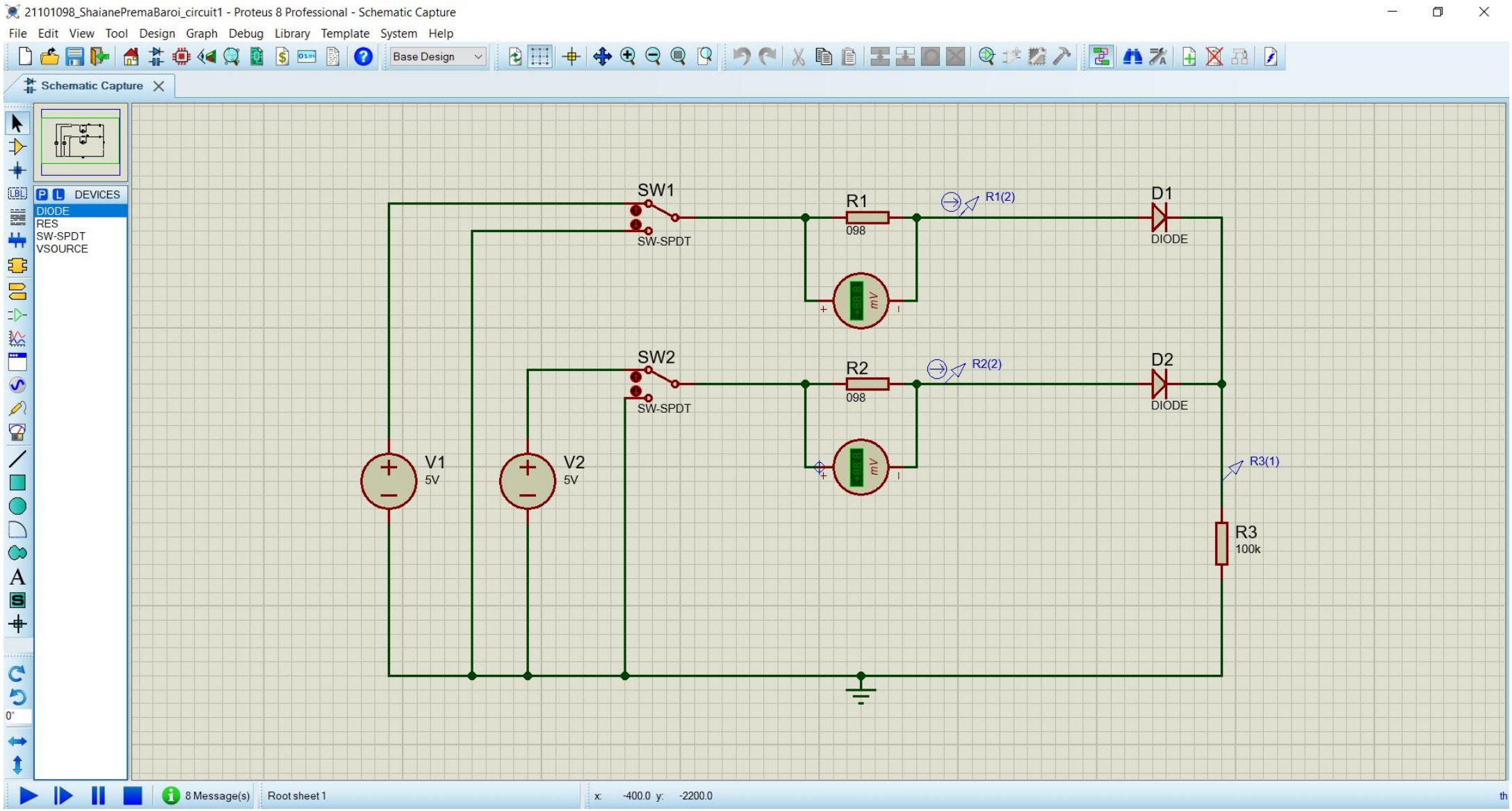
$I_B = I_C = I_E = 0\,A$

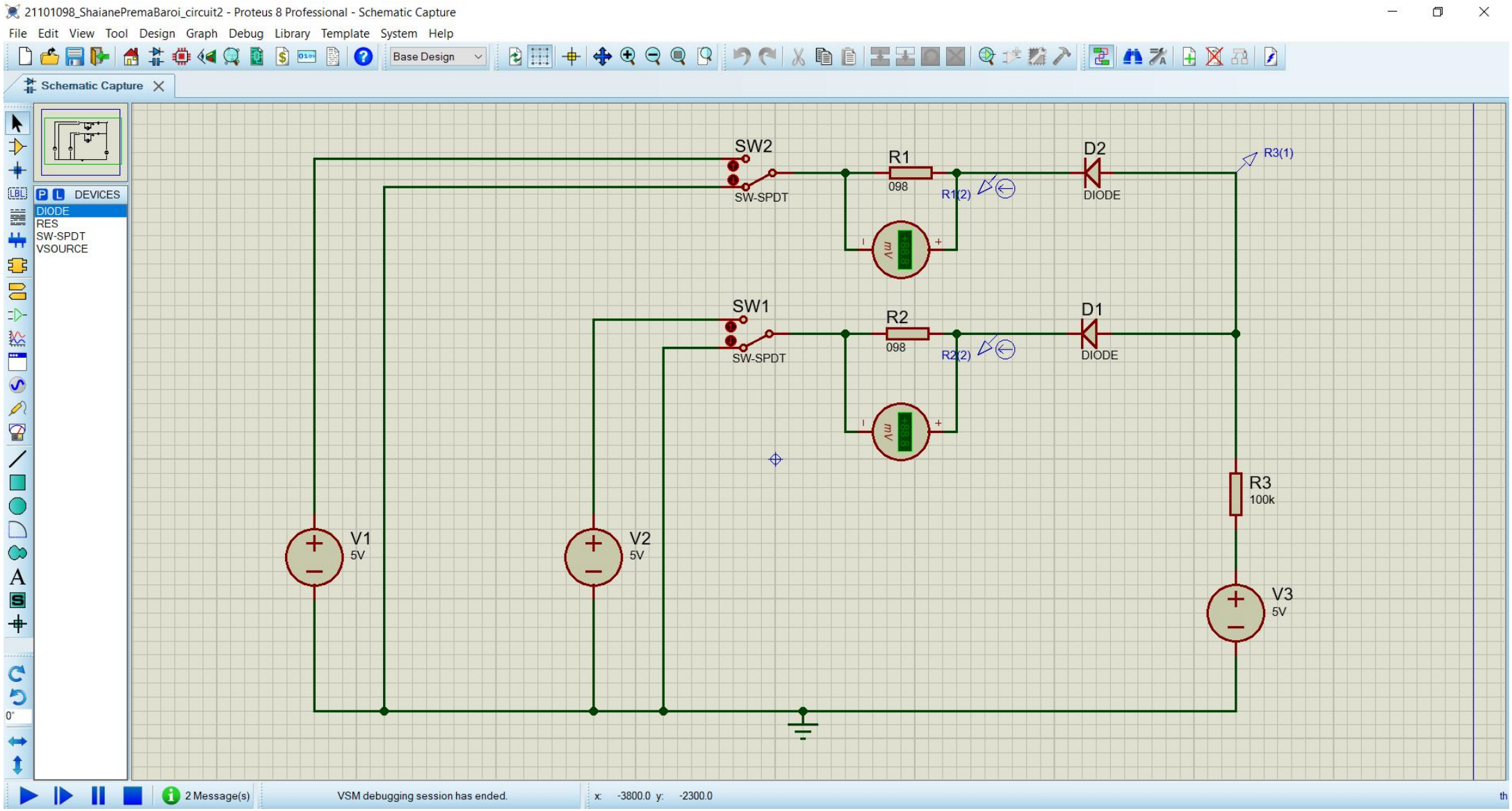
$V_B = 0.65\,V$, $V_C = 5\,V$, $V_E = 0V$

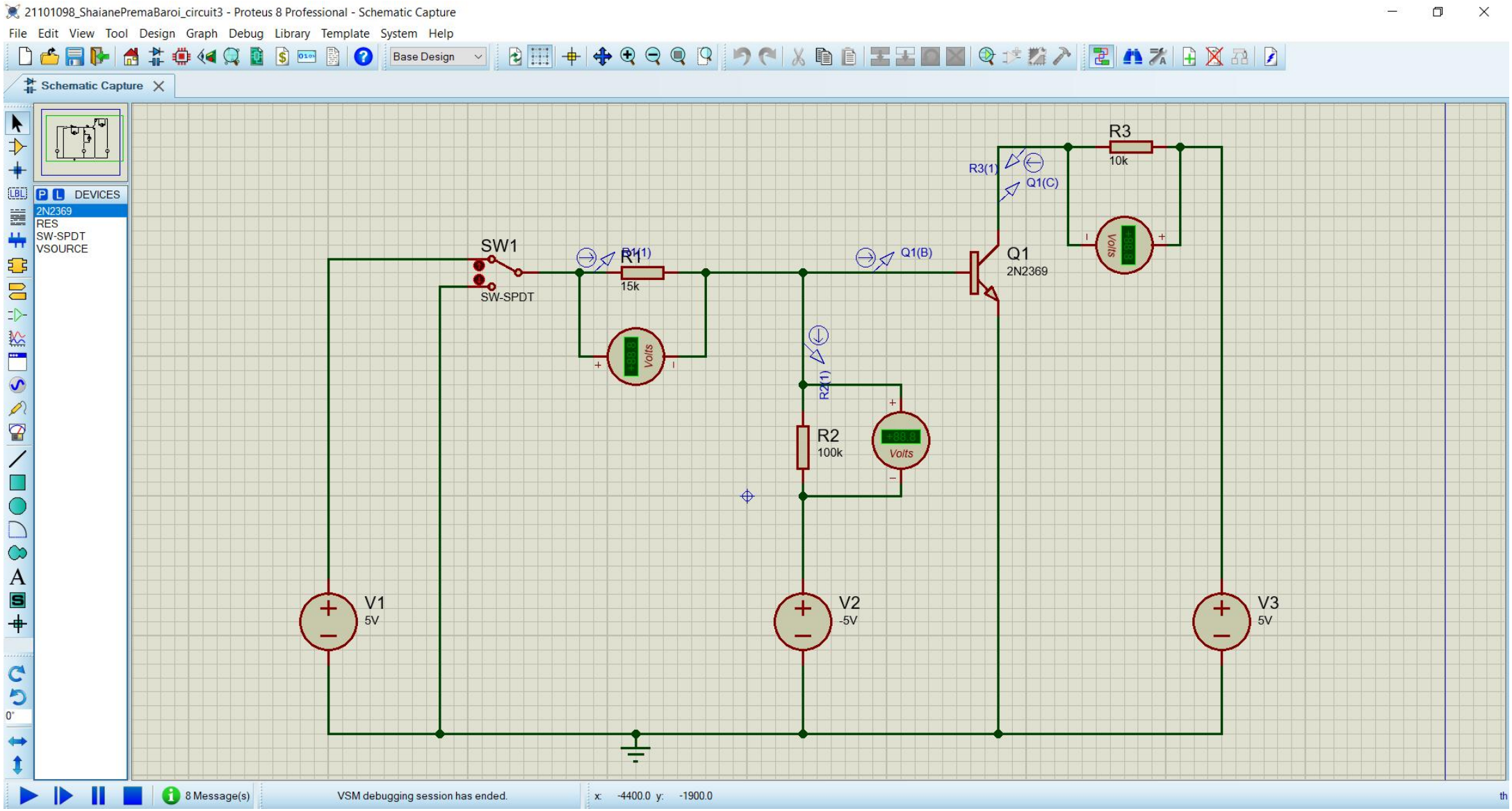
$V_{BC} = V_B - V_C = 0.65 - 5 < 0.5\,V$

$V_{BE} = V_B - V_E = 0.65 - 0 < 0.7\,V$

Verified.


21101098_ShaianePremaBaroi_circuit1 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
DIODE
RES
SW-SPDT
VSOURCE
SW1
SW-SPDT
R1
098
R1(2)
D1
DIODE
SW2
SW-SPDT
R2
098
R2(2)
D2
DIODE
V1
5V
V2
5V
R3(1)
R3
100k
8 Message(s)
Root sheet 1
x: -400.0 y: -2200.0


21101098_ShaianePremaBaroi_circuit2 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
DIODE
RES
SW-SPDT
VSOURCE
SW2
SW-SPDT
R1
098
R1(2)
D2
DIODE
R3(1)
SW1
SW-SPDT
R2
098
R2(2)
D1
DIODE
R3
100k
V1
5V
V2
5V
V3
5V
2 Message(s)
VSM debugging session has ended.
x: -3800.0 y: -2300.0


21101098_ShaianePremaBaroi_circuit3 - Proteus 8 Professional - Schematic Capture
File Edit View Tool Design Graph Debug Library Template System Help
Base Design
Schematic Capture
DEVICES
2N2369
RES
SW-SPDT
VSOURCE
SW1
SW-SPDT
R1
15k
R1(1)
Q1(B)
Q1
2N2369
R3
10k
R3(1)
Q1(C)
R2
100k
R2(1)
Volts
V1
5V
V2
-5V
V3
5V
8 Message(s)
VSM debugging session has ended.
x: -4400.0 y: -1900.0