Power efficient 4-bit flash ADC using Cadence Vistuoso

Abstract*— Analog-to-Digital Converters (ADCs) are useful building blocks in a variety of applications, including biomedical, data storage read channels, and optical receivers, because they serve as the interface between important world analog signals and, as a result, digital signal processors. In this study, an attempt is made to design a power efficient 4-bit Flash Analog to Digital Converter [ADC] for biomedical applications. Furthermore, this work examines the sample and hold circuit, comparator, and encoder in a 4-bit Flash Analog to Digital Converter (ADC) to achieve a power efficient ADC. In this work, the R-2R ladder is replaced with a sample and hold circuit to lower power consumption, the traditional comparator is replaced with a simple comparator, and the priority encoder is used as an alternative to the traditional encoder. It is implemented utilizing 0.18µm CMOS technology. In general, CADENCE VIRTUOSO tools are used to develop schematics and run simulations. The simulation results include a 1.8V analog input range with a frequency of 33.20MHz.

***Keywords*— Flash ADC, CADENCE VIRTUOSO, gpdk90/gdk180, Resolution**

I. INTRODUCTION

Analog signals are continuous, whereas digital signals are discrete. ADCs convert analog signals into digital signals, enabling processing by computers or microcontrollers.

ADC Principles:
- Sampling and quantization
- Resolution and sampling rate
- Quantization error and conversion time

Types of ADC:
- Flash ADC
- SAR ADC
- Delta-Sigma ADC

Applications:
- Data acquisition systems
- Audio and video processing
- Medical devices
- Industrial control systems
- Scientific instruments

Conclusion:

ADCs play a vital role in electronic systems, enabling the conversion of analog signals into digital signals. Understanding ADC fundamentals is essential for designing and implementing effective electronic systems.

Flash ADC (FADC) is a type of Analog-to-Digital Converter (ADC) that uses a parallel architecture to convert analog signals into digital signals. It is called "Flash" because it provides very high-speed conversions, typically in the range of nanoseconds.

Here are some key characteristics of Flash ADCs:
1. Parallel architecture: FADCs use a parallel architecture, where multiple comparators and encoders work together to convert the analog signal into a digital signal.
2. High-speed conversions: FADCs are designed for high-speed applications, with conversion times typically in the range of nanoseconds.
3. Low latency: FADCs have low latency, making them suitable for real-time applications.
4. High-resolution: FADCs can provide high resolution, typically up to 8-10 bits.
5. Power consumption: FADCs consume more power compared to other ADC types, due to their parallel architecture.

Applications of Flash ADCs:
1. High-speed data acquisition
2. Digital oscilloscopes
3. High-speed communication systems
4. Radar and electronic warfare systems
5. Medical imaging

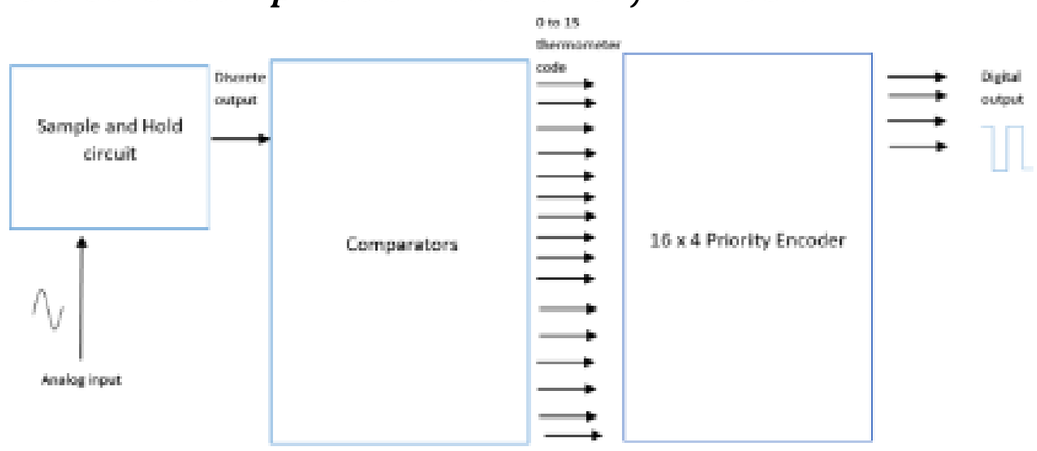
Advantages of Flash ADCs:
1. High-speed conversions
2. Low latency
3. High-resolution
4. Parallel architecture

Disadvantages of Flash ADCs:
1. High power consumption
2. Complex design
3. Expensive

In summary, Flash ADCs are high-speed ADCs that use a parallel architecture to provide fast conversions, low latency, and high resolution. They are suitable for high-speed applications but consume more power and are more complex to design.

II. DIFFERENT BLOCKS OF ADC

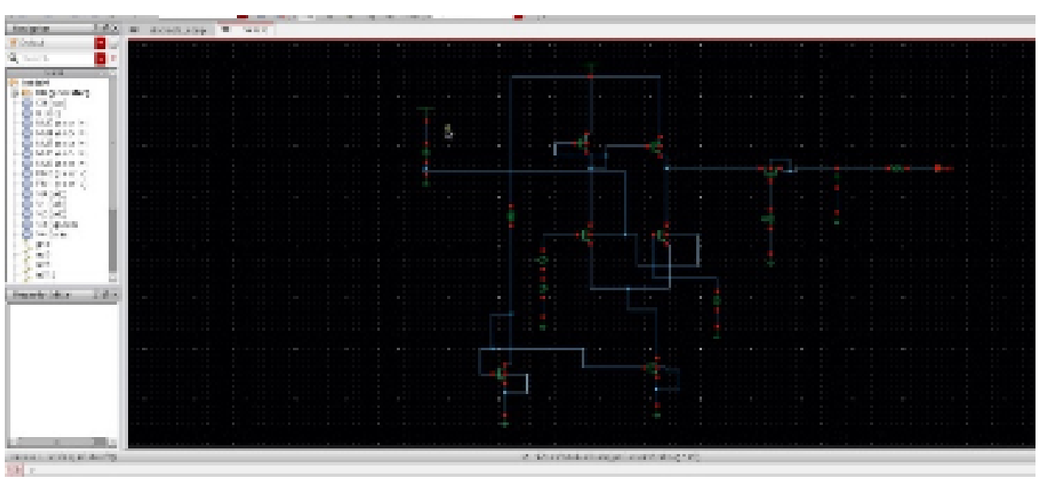
The analog signal is first applied to the ‘ sample’ block where it's sampled at a selected frequency. The sample amplitude value is maintained and held within the ‘ hold’ block. It's an analog value. The hold sample is quantized into discrete value by the ‘ quantize’ block. At last, the ‘ encoder’ converts the discrete amplitude into a binary number.



1) Sample and Hold

The input signal is sampled and the capacitor is charged to input level during the sampling phase when the clock hits high. The sampled signal is kept constant and the capacitor discharges along the same way when the clock is low in hold mode.

So, if clk is high MOS gets on => Vout can track Vin.

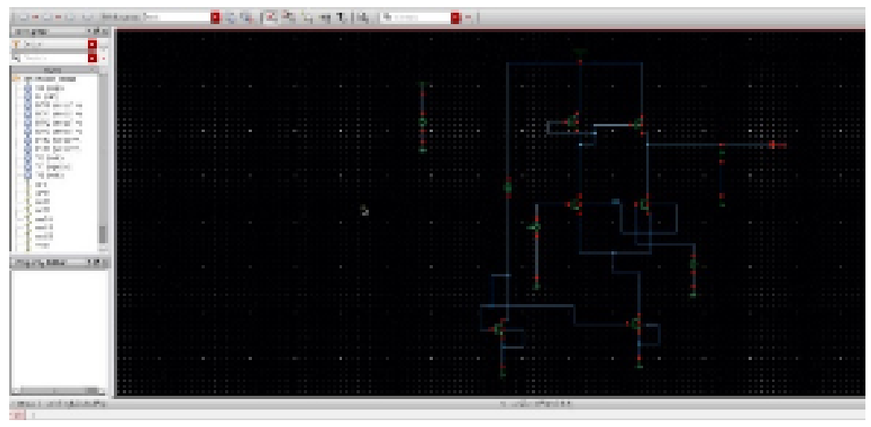


2) Discrete Comparator:

A discrete comparator is an electronic circuit that compares two analog voltages and produces a digital output indicating which voltage is higher. It is a basic building block in analog-to-digital conversion and is used in various applications, including:

1. Analog-to-digital converters (ADCs)
2. Digital-to-analog converters (DACs)
3. Audio and video processing
4. Medical devices
5. Industrial control systems

A comparator is normally used in applications where some varying signal level is compared to a fixed voltage level (usually a voltage reference). Since it is, in effect, a 1-bit analog-to-digital converter (ADC), the comparator is a basic element in all ADCs.

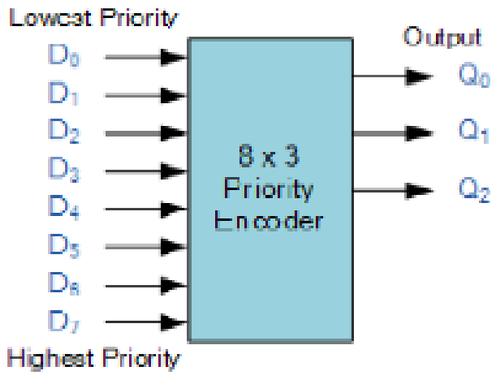


3) Priority Encoder:

A Priority Encoder is a digital circuit that converts multiple input signals into a single output signal, prioritizing the inputs based on their importance or urgency. It's a crucial component in digital systems, ensuring that critical signals are processed first.

So, for 16 to 4 priority encoder the output equations are:

O1= D1+D3+D5+D7+D9+D11+D13+D15.
O2=D2+D3+D6+D7+D10+D11+D14+D15.
O3= D4+D5+D6+D7+D12+D113+D14+D15.
O4= D8+D9+D10+D11+D12+D13+D14+D15.
Where O1, O2, O3, O4 are the output pins and D1, D2, ..., D15 are the input pins.



Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

III. PARAMETERS

.

1. Power Dissipation

The process in which an electric or electronic device produces heat or other waste energy as an unwanted byproduct of its primary action. Measured by doing DC analysis and then multiplying the output Voltage and Current we will get the amount of power which is dissipated.

2. Delay

The propagation delay of a signal path is the time taken between the change in input and the change in output for that signal. If it is not managed properly, propagation delays can result in logic circuits that run too slowly to meet their requirements, or that fail altogether. Measured by doing Transient analysis.

3. Gain Error

Defines the difference between the slopes of the actual and ideal output values. Expressed as a percentage. The total system gain error includes any gain errors from preamplifiers, attenuators, or signal transducers.

Gain error (%) = (actual value − ideal value) %
Here, gain error = 1.8-1.6 = 0.2% error is present over here.

4. SNR (Signal to Noise Ratio)

Signal-to-Noise Ratio (SNR) is the ratio of the power of a signal to the power of background noise, indicating the clarity of the signal. The noise spectrum includes all non-fundamental spectral components in the Nyquist frequency range (sampling frequency / 2) without the DC component, the fundamental itself and the harmonics:

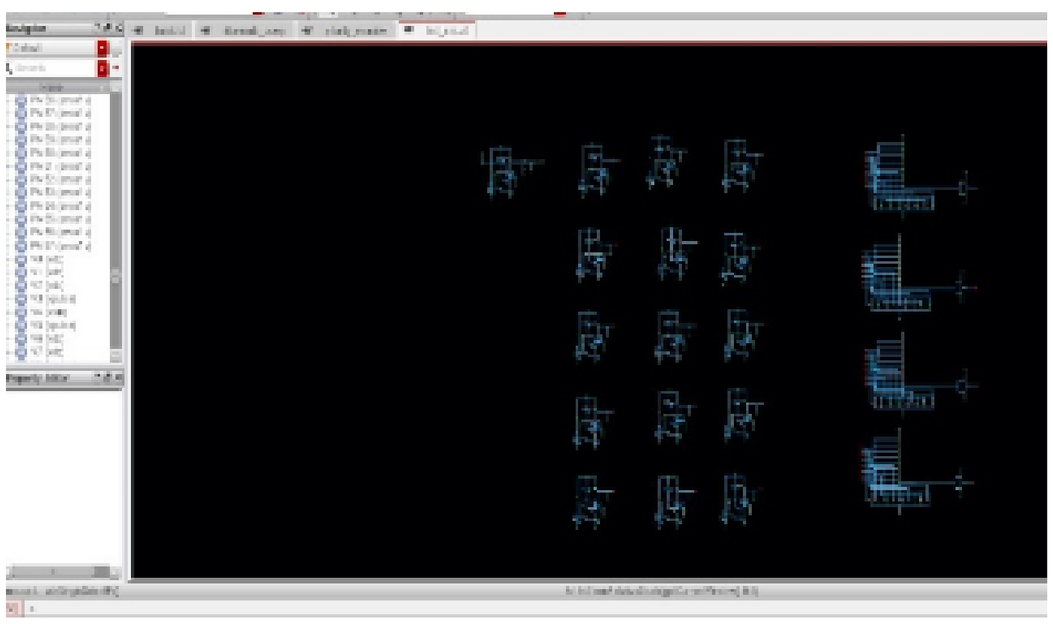
*SNR = 20 * log([Fundamental]/√(SUM(SQR[Noise])))*

Also, SNR= 6.02N + 1.76 db.

By doing theoretical calculation as to put the value of N in
above equation we will get the value of SNR. Moreover, by
doing transient analysis and then FFT one can calculate the
value of SNR.

IV. IMPLEMENTED DESIGN

The suggested ADC architecture has a 4-bit, low-power Flash
ADC structure. The design works at a frequency of 33.20MHz and 1.8V input, with a sample and hold circuit at the beginning to alleviate the problem of power consumption by the R-2R ladder. Furthermore, it is coupled to a discrete comparator, which produces discrete output, which is sent into the priority encoder as an input. Essentially, the architecture of a priority encoder is constructed with OR gates rather than MUX employing XOR gates to minimize complexity and address the problem of power loss. This circuit also includes a Low-Pass Filter (LPF),which attenuates information over a cutoff frequency while allowing lower frequencies to pass through. Furthermore, an
amplifier is retained at the beginning to amplify or strengthen the signal, reducing the quantity of noise, and then this AC signal is transmitted to the S/H circuit for further processing. A n-bit ADC requires (2^n)-1 comparators, while a 4-bit ADC requires15 comparators. The output of the sample and hold circuit is fed into the 8 input OR gate to obtain the digital output from the discrete input.



IV. RESULT

Here, a 4-bit ADC is being constructed with an input voltage of 1.8V, and the frequency is set to 33.20MHz, which will meet the requirements of the biomedical application. The power dissipation is relatively low compared to, at 2.88mW, due to the use of a sample and hold circuit instead of an R-2R ladder, as well as the use of an OR gate instead of a MUX in the encoder. SNR

have value of 25.846 , respectively. The SNR value are high because a low pass filter is used in this prepared circuit instead of a normal circuit, so the signal has less distortion. Due to the low pass filter and OR gates in the circuit, and the noise is very low. However, this comes at the expense of speed, since the delay in maintaining other features rises by 12.9ns. Furthermore, taking each block into account, the power consumption of the S/H circuit, comparator, and priority encoder is 2.78mW, 90uW, and 124.9pW, respectively. The INL and DNL are both +/- 0.133LSB, with a gain error of 0.2%.

The R-2R ladder is employed, which is the primary source of power dissipation. The R-2R ladder is substituted with the sample and hold circuit, which is employed here because the R-2R ladder consumes more power and causes delays; to address this issue, the sample and hold circuit is used. So, instead of an R-2R ladder, a sample and hold circuit is employed. Furthermore, instead of utilizing a sophisticated priority encoder with MUX and gates as in the study, simple OR gates are employed here, which contributes significantly to power consumption reduction.

CONCLUSION

The proposed work proposes a highly digital 4-bit flash ADC whose key components may be synthesized, minimizing design difficulties, time-to-market, and power requirements. It is also scalable with the technology. A biomedical application with a frequency range of 100KHz to 5.8GHz. The frequency is set at 33.2MHz since it falls within the range of biomedical applications for which this ADC is designed. The SNDR, SNR are capable of 25.842 dB and 25.246 dB respectively. This 4-bit flash ADC has a DNL and INL of ±0.133 LSB. The sample and hold circuit, comparator, and Thermometer to code converter is designed and simulated in CADENCE virtuoso tool utilizing 180 nm CMOS technology. Various analyses, such as DC and transient analyses, are conducted on the aforementioned functional blocks using the CADENCE program. The suggested circuit has an overall propagation latency of 12.9 ns and a power dissipation of 2.88 mW. The Gain Error is 0.2%, and the power consumption of each block (Sample and Hold circuit, Comparator, Priority Encoder) is 2.78mW, 90uW, and 1.249*10^(-10) W, respectively. The flash ADC is operating according to the specs. Furthermore, alternative comparator approaches, such as the TIQ comparator-based ADC, can be employed to do further analyses. Another alternative is to apply digital signal processing on the ADC output to fix the offset, gain, and linearity. In flash ADC there is a thermometer code-to-binary code encoder, one can even use another technique known as quantum voltage (QV). With the help of some above mentioned techniques ADC can be implemented again for better results.

REFERENCES

[1] Ashima Gupta, Anil Singh, Alpana Agarwal, " Highly-digital voltage scalable 4-bit flash ADC" , IET Circuits, Devices & Systems, Volume: 13, Issue: 1, 1 2019.

[2] Disha Gaude, Bathini Poornima, K.M. Sudharshan and Prashant V. Joshi, " Design and Simulation of 4-Bit Flash Analog to Digital Converter (ADC) for High Speed Applications" , Indian Journal of Science and Technology, Vol 12(36), September 2019.

[3] Piyush Kumar, " Low-Power Heterogeneous Encoder Based 4-Bit Flash ADC Using TIQ" , International

[4] Journal of Electrical and Electronics Research, ISSN 2348-6988 (online) Vol. 3, Issue 2, pp: (662-669), Month: April - June 2015.

[5] Marcel Siadjine Njinowa, Hung Tien Bui, François-Raymond Boyer, " Design of low power 4-bit flash ADC based on standard cells" , New Circuits and Systems Conference (NEWCAS), DOI: 10.1109/NEWCAS.2013.6573626, IEEE 2013.

[6] Panchal S D1, Dr. S S Gajre2, Prof. V P Ghanwat, " Design and implementation of 4-bit flash ADC using folding technique in cadence tool" , International Journal of Advanced Research in Computer and Communication Engineering, Vol. 1, Issue 4, June 2012