



United International University

Fall-2023

Digital Electronics Laboratory- 224 (A)

Lab Report: 01

Submitted to

Md. Zubair Alam Emon

Lecturer, Department of
Electrical and Electronics Engineering, UIU

Submitted by: Md. Milkan Ahmed Shahed

Group 1

Sl	Name	Id
1	Md. Sadakat Rahman	021 221 037
2	Md. Julkar Naim Antar	021 221 056
3	Sadia Islam Nupur	021 221 060
4	<u>Md. Milkan Ahmed Shahed</u>	<u>021 221 063</u>

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Part 1

❖ Constructing truth table using 74LS10 Triple 3-input NAND gates:

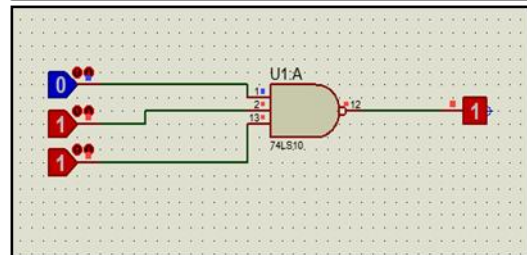
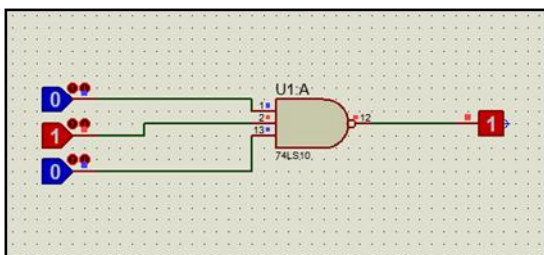
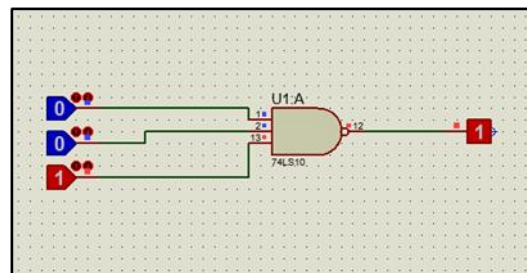
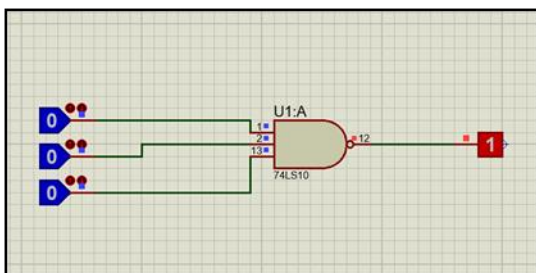
Description:

NAND gate is a combination of AND gate and NOT gate. It processes the inputs like a AND gate and inverse the result and shows it as output. It gives output '0' when all the inputs are 1. Other than this situation, the output is always 1. Our Software simulation and hardware implementation indicates the same result.

Truth Table

X	Y	Z	F
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Software Simulation & Hardware Implementation



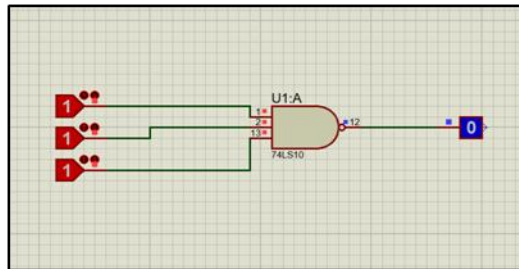
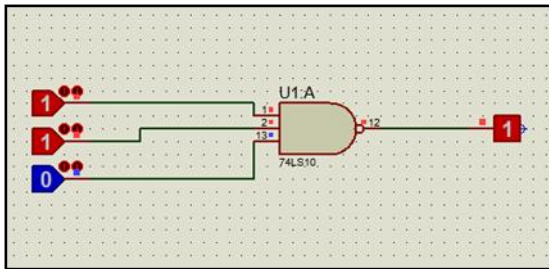
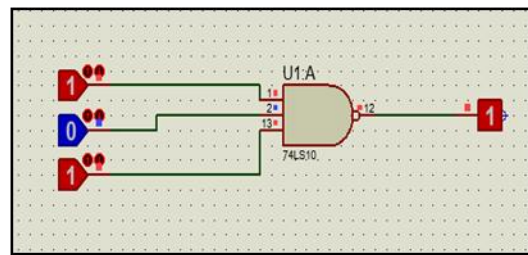
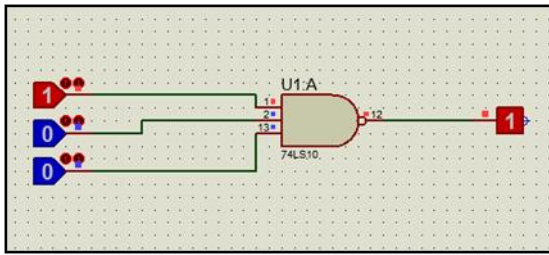


Fig: Software Simulations of 3 input NAND gate

Hardware implementation of 3 input NAND gate

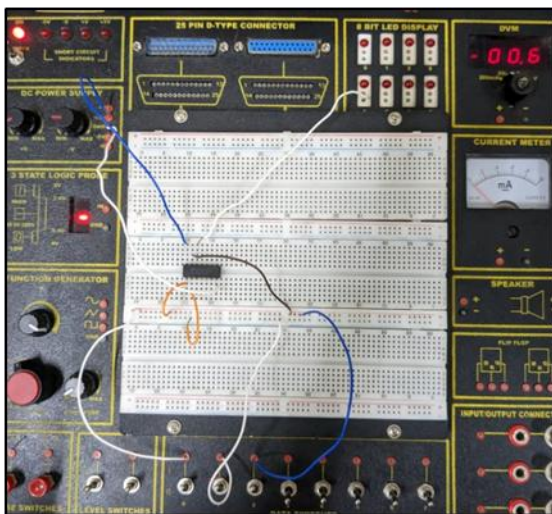


Fig: When 3 inputs are logic 1

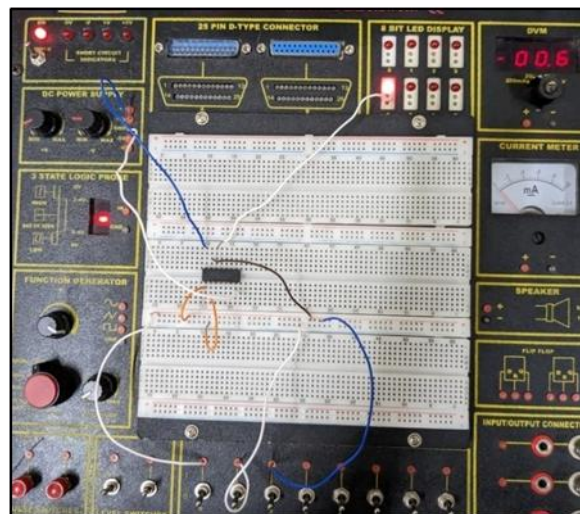


Fig: When 3 inputs are logic 0

Part 2

❖ Finding propagation delay for 75LS04

Description:

All physical circuits takes some time for transition between an input and provide an output. This is called propagation delay. From the oscilloscope we get the t_{pLH} and t_{pHL} delay for 6 NOT gates **158ns** and **156ns** respectively. Which turns into **26.33ns** and **26ns** for a single NOT gate.

Probable source of error:

There is a slight error in our experimental data compared to the specification the t_{pLH} and t_{pHL} to be **9ns** and **10ns**. Propagation delay errors or discrepancies in a 74LS04 integrated circuit (IC) can occur for various reasons. Some of them are:

- **Manufacturing defect:** there can be variations in manufacturing processes. Different batches or lots of ICs may exhibit slightly different characteristics, including propagation delay.
- **Temperature sensitivity:** The propagation delay of ICs can be temperature-sensitive. Variations in operating temperature can cause discrepancies in delay times.
- **Power supply voltage:** The propagation delay of ICs can also be sensitive to variations in the power supply voltage.
- **Non Ideal RC load:** Values of standard RC load are being considered while calculation the propagation delay, as we do not have standard RC load so the experimental result may contain some errors.

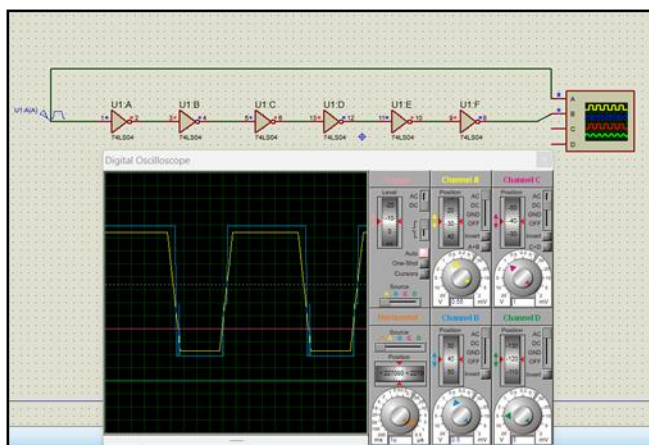


Fig: Software simulation

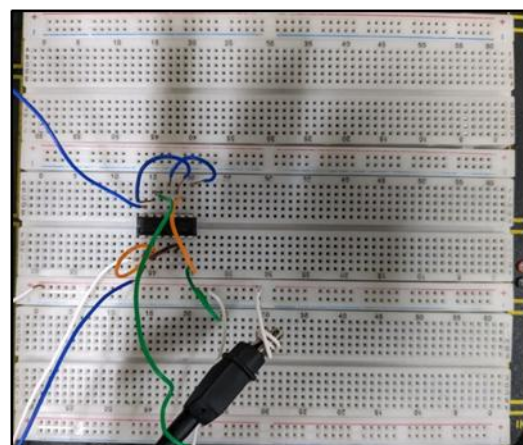


Fig: Hardware Implementation

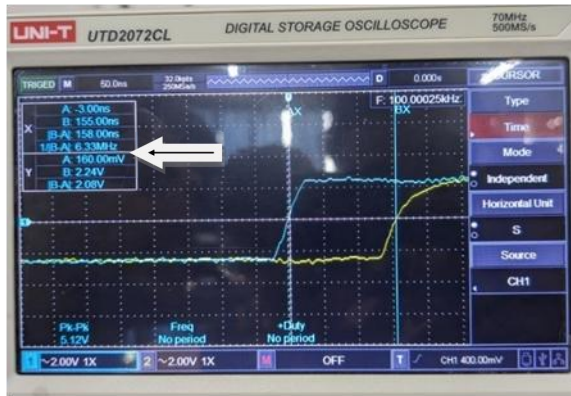


Fig: Oscilloscope reading of t_{pLH}

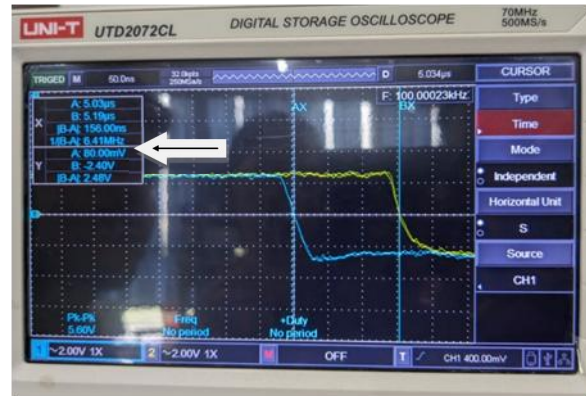


Fig: Oscilloscope reading of t_{pHL}

Part 3

❖ Problem with floating input and effect of Pull-up resistor

- When an input is left unconnected, and there is no high voltage applied to the input, it can result in an undefined state. Even a small amount of noise or voltage from the surrounding environment can cause the logic gate to toggle on or off
- By using a pull-up resistor, we can connect the input to the V_{cc} (positive power supply). We do this to make sure the input has a stable and known high voltage level, like a light switch turned on, even when nothing else is actively controlling it. This helps prevent the input from floating around and accidentally turning on or off due to electrical noise or other factors, which could cause errors in our electronic circuits. So, the pull-up resistor ensures that the input has a clear and steady "on" signal when it's not being specifically turned off by something else.

Conclusion:

This lab provided valuable hands-on experience in working with digital logic circuits and TTL gates. We learned about the importance of verifying voltage levels, the behavior of various logic gates, the impact of floating inputs in the LS TTL logic family, and how to measure propagation delays in cascaded inverters.