PSPICE Project 2023

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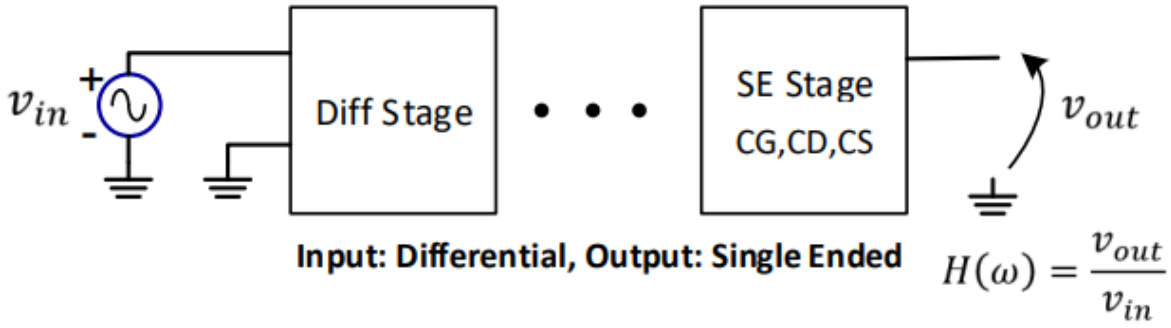
1. IDs & Summation

ID1	3	4	3	8	8	3	2	7	8
ID2	3	3	0	0	6	5	5	4	1
Sum	6	7	3	9	4	8	8	1	9
	A	B	C	D	E	F	G	H	I

Therefore:

$$A = 35 + 2 \cdot 9 = 53\ [dB]$$
$$f_1 = (8+1) = 9[kHz]$$
$$f_2 = 900\ [kHz]$$
$$C = 3 \Rightarrow M_1 = 20\ \left[\frac{dB}{dec}\right], M_2 = -40\ \left[\frac{dB}{dec}\right]$$
$$F = 8 \Rightarrow R_{out} = 13[k\Omega]$$

A=6, D=9, therefore we use:

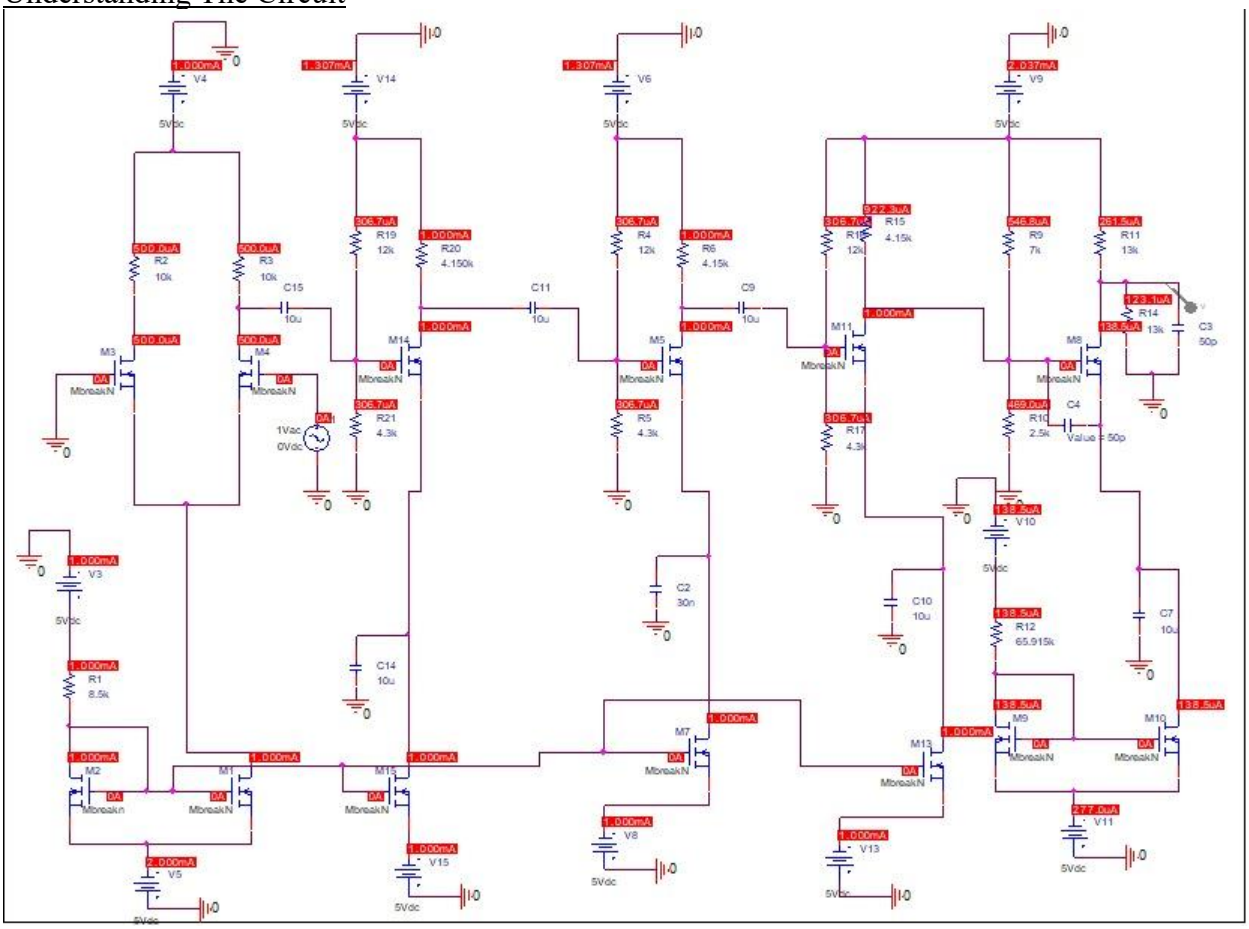


Requirements:

1. Sum of resistances=191.26KΩ<1MΩ
2. Sum of capacitances≈ $60\mu F < 1mF$

6. DC power dissipation<0.1W(check graph)

Understanding The Circuit



- "Raw" schematic of the circuit-

Essentially, the circuit is broken down into:

A. Differential Amplifier – Single Ended output; used to meet requirement demands.

B. 3 Common source – used for gain amplification.

C. Last common source– used for requirements of output resistance. We chose to have three common source amplifiers in between the input and output stage in order to ensure that the transfer function overall had enough gain. Common sources need a high drain resistance or high current to ensure high gain. Therefore, cascading stages allowed for the correct gain, without using too big resistors or current, which would yield a high DC power dissipation.

D. Current Mirrors used to bias the first 4 stages.

E. Current Mirror used to bias final stage.

Before analysis, we note that the DC analysis is verified in Figure 1, whereas the AC analysis is verified in Figure 2 .

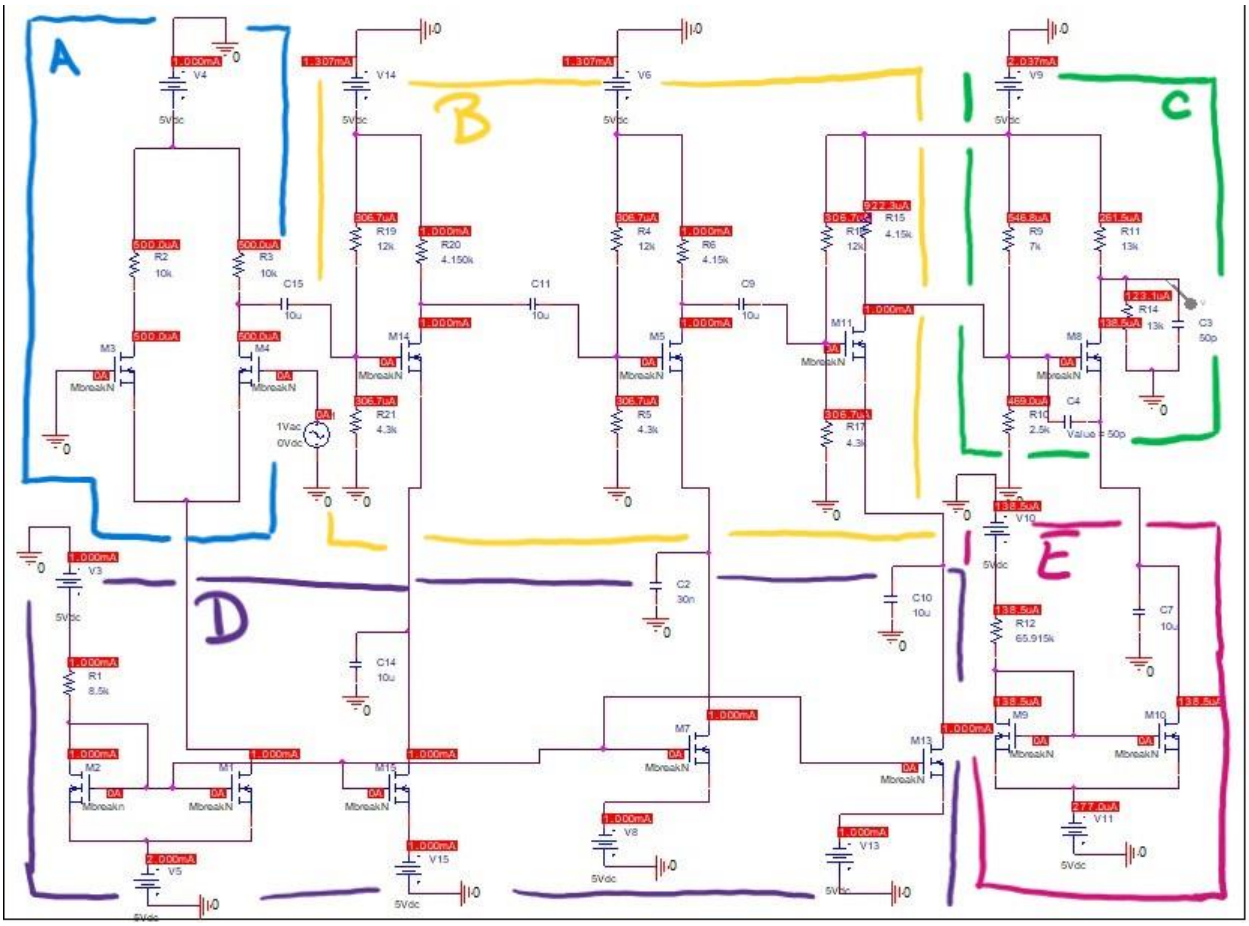


Figure 1:labels with DC currents

❖ *Circuit Analysis*

We now provide an in depth analysis of each section.

A. Differential Amplifier: The intention of the differential amplifier was mainly because we were required to do so. However, this gave a good option for use and understanding of differential amplifiers. Since we decided to use a single-ended output, the gain was sliced in half. Essentially, the gain at this output of the stage would be:

$$\frac{V_x}{V_g} = \frac{-g_m R_D}{2}$$

We know this occurs due to small signal considerations which we saw throughout the course. Now, as we know, $g_m$is calculated as follows: $g_m = 2\sqrt{k \cdot I_{DS}}$. We chose to use a current of $1\ [mA]$ such that each branch gets $.5[mA]$:

$$g_m = 2\sqrt{10^{-3} \cdot .5 \cdot 10^{-3}} = 1.41 \times 10^{-3}$$

Such that the gain is:

$$-\frac{1.41 \times 10^{-3} \cdot 10{,}000}{2} = -7.05\ \left[\frac{V}{V}\right] \rightarrow 20\log(7.05) = 16.96 \approx 17\ [dB]$$

At this point we diverge into section D, which is the current mirror.

D. Current Mirror #1: The purpose of the current is to supply a total of 1 $[mA]$ to the differential amplifier, which will then split evenly due to symmetry of the amplifier. The way it works is as follows: we **defined** that the current would be 1 $[mA]$, and then had to solve the following two equations in order to find the correct value of R_1 – the biasing resistor. We have:

$$\begin{cases} V_D = V_{DD} - I_{mirror} \cdot R_1 \\ I_{mirror} = k \cdot (V_{GS} - V_T)^2 \end{cases} \Rightarrow \begin{cases} V_D = 5 - 10^{-3} \cdot R_1 \ \ (1) \\ 10^{-3} = 10^{-3} \cdot (V_D - (-5) - 1)^2 \ \ (2) \end{cases}$$

Thus, equation (2) becomes:

$$1 = (5 - 10^{-3} \cdot R_1 + 5 - .5)^2$$
$$1 = (9.5 - 10^{-3} \cdot R_1)^2$$
$$\rightarrow 1 = (90.25 - .019 \cdot R_1 + 10^{-6} R_1^2)$$

Note that: $9.5 \cdot 2 \cdot 10^{-3} = .019$

We continue:

$$10^{-6} \cdot R_1^2 - .019\, R_1 + 89.25 = 0$$
$$\rightarrow R_1 = \begin{cases} 10.5\ [k\Omega] \rightarrow V_D = 5 - 10^{-3} \cdot 10.5k = -5.5 < -V_{DD} \ \times \\ 8.5\ [k\Omega] \end{cases}$$
$$\Rightarrow \boxed{R_1 = 8.5\ [k\Omega]}$$

This current is then "brought" to the next amplification stages – "section B" – via the MOS's. Now, we analyze section B.

B. Cascading Common Sources: We know that the amplification of a common source is:

$$-\frac{g_m R_D}{1 + g_m R_s}$$

We use the capacitors to short the source resistance such that R_s is zero, since $r_{ds} \rightarrow \infty$ and this would kill our gain. We also use coupling capacitors to differentiate between DC and AC analysis. Finally, we used voltage dividers in order to set the base voltage:

$$V_G = V_{DD} \cdot \frac{4.3k}{4.3k + 12k} = 5 \cdot .26 = 1.3\ [V]$$

Therefore:

$$5 - 10^{-3} \cdot 4.15k = .85 = V_D > V_{GS} - V_T = 1.3 - .5 = .8$$

So, we are indeed in saturation.

With this, $g_m = 2\sqrt{10^{-3} \cdot 10^{-3}} = 2 \times 10^{-3} \rightarrow A_v = -g_m R_D = -2 \cdot 10^{-3} \cdot 4.15k = -8.3\ \left[\frac{V}{V}\right]$

$$8.3\ \left[\frac{V}{V}\right] \rightarrow 20 \log(8.3) = 18.3$$

Thus, the total amplification in section B is: $-24.9\ \left[\frac{V}{V}\right]$.

This brings us to the last stage, Stage C.

C. "Output" Stage: The reason this is in "" is because output stages refer really to Class A, B, AB, but we did not cover that in this course. It's name comes from the fact that it is where the output is. The current flowing through this MOS is: $.1385\ [mA]$

$$\rightarrow g_m = 2\sqrt{10^{-3} \cdot .1385 \cdot 10^{-3}} = 7.44 \cdot 10^{-4}$$

Therefore, the gain is:

$$-g_m R_D = 7.44 \cdot 10^{-4} \cdot 13 \cdot 10^3 = -9.672\ \left[\frac{V}{V}\right] \rightarrow 19.7\ [dB]$$

E. Current Mirror of "Output" Stage: The values and equations follow the same as in section D and therefore the analysis is not brought again.

Thus, summing all gain stages in dB we get that: $A_v = \frac{V_{out}}{V_{in}} \approx 53dB$, as is shown below in Figure 2:

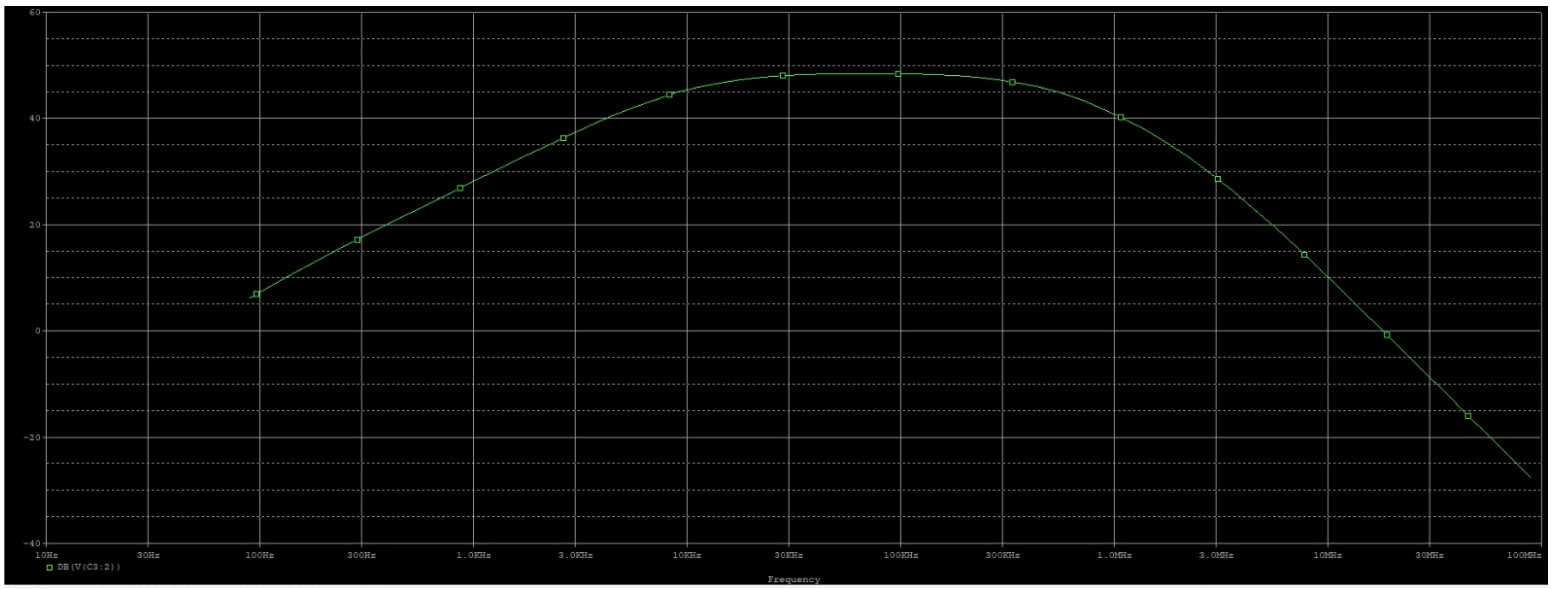


Figure 2: bode plot showing gain of the system[dB]

Finding the poles:

f_h:

$$f_h = 900kHz$$

Using time constants:

$$R_{c4} = \frac{1}{2}\left(R_{10}||R_9||R_{15}\right) = 0.64k\Omega$$
$$\therefore \tau_{c4} = 50 * 0.64 * 10^{-12} * 10^3 = 32 * 10^{-9}$$
$$R_{c3} = \frac{1}{2}(R_{11}||R_L) = 3.25k\Omega$$
$$\therefore \tau_{c3} = 50 * 3.23 * 10^{-12} * 10^3 = 161.5 * 10^{-9}$$
$$\therefore \omega_h = \frac{1}{\tau_{c4} + \tau_{c3}}, f_h = \frac{\omega_h}{2\pi} = \frac{(0.00516 * 10^9)}{2\pi} = 820kHz \approx 900\ [kHz]$$

f_L:

We require that $f_L = 9\ [kHz] = \sum \frac{1}{\tau}$:

We will start with the largest contributor and show that even with this alone we are approximately at our frequency:

$$\tau_{MostSig} = C_2 * \frac{1}{g_{m_5}} = 30 \cdot 10^{-9} \cdot \frac{1}{2 \cdot 10^{-3}} = 1.5 \cdot 10^{-5}$$
$$\omega_{L_{approx}} = \frac{1}{\tau_{MostSig}} = 66.7\ \left[\frac{krad}{s}\right]$$
$$\rightarrow f_{L_{approx}} = \frac{\omega_{L_{approx}}}{2\pi} = 10.6\ [kHz] \approx 9\ [kHz]$$

The other time constants are considerably negligibly in comparison and are therefore not brought in the calculation.

❖ R_{in} & R_{out}

Lastly, it is important that we note and explain the input and output resistances. The voltage input is sent into the **gate** of the MOS in the differential amplifier, and therefore the input resistance will be infinite, from small signal model considerations.
As required, we have set $R_{out} = 13\ [k\Omega]$. The way that this was done was by setting the drain resistor of the output stage MOS as $13\ [k\Omega]$. It was given in the PDF that $r_0 \to \infty$ and therefore, the load resistor will "see":

$$(looking\ up\ from\ the\ drain)||(looking\ into\ the\ drain)$$
$$= 13{,}000||\infty \Rightarrow R_{out} = 13\ [k\Omega]$$

This output resistance is independent of frequencies, and thus if graphed[1] against frequency, it should be a constant line.

❖ *Power Dissipation*

Finally, we show the power dissipation requirement is met:

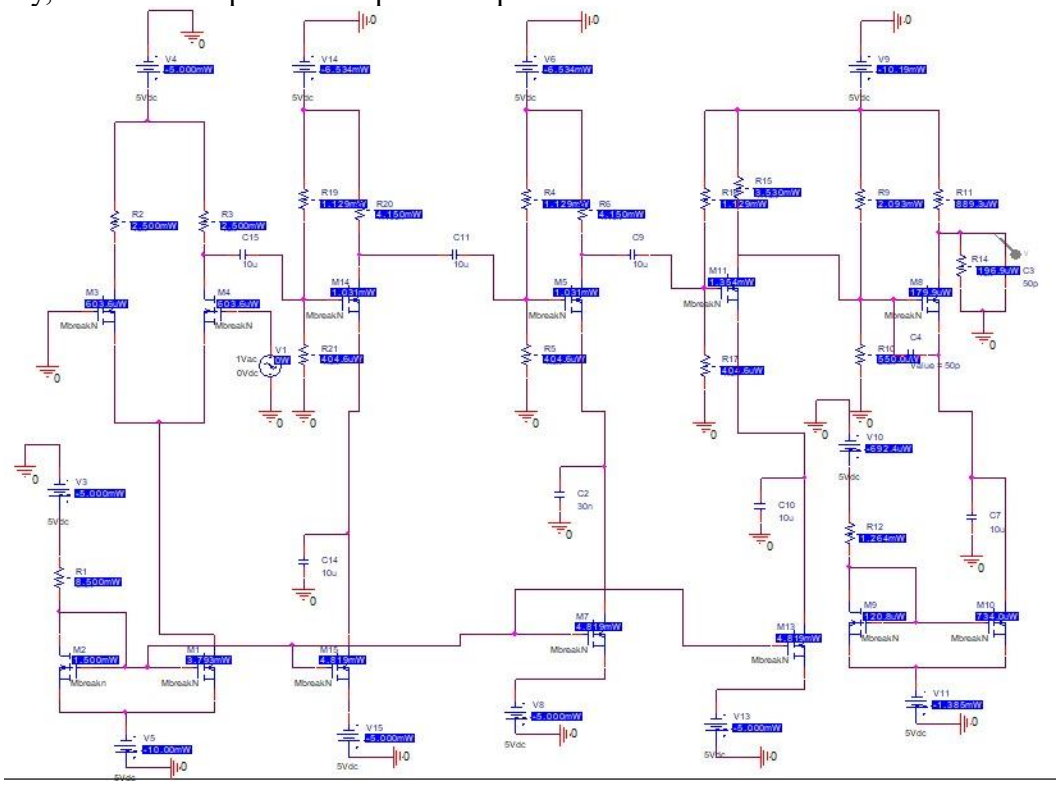


Figure 3: Labels for static power dissipation

[1] Please note that a graph of $R_{out}\ vs.\ freq.$ was not given due to technical issues. An inquiry about this was sent to the staff but we received no response and therefore had to submit without it. Thus, we have explained what we - *would* have seen on the simulation, and hope this will suffice.