WARP Clock Board
Rev 1.0 - October 2006
Charles Camp

Schematic Pages:

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VCC_RADIO

VCC_LOGIC

R60 4.75K R59 4.75K R58 4.75K R57 4.75K R50 215 D1 LED

R56 4.75K R55 4.75K R54 4.75K R53 4.75K R49 215 D2 LED

In FPGA I/O banks 4/5, the GCLK
xP pins are CLK+, xS are CLK-

VCC

J1
1 VDD
2 GND
3 GCLK0P
4 GCLK1S
5 GND
6 GND
7 GCLK6P
8 GCLK7S
9 GND
10 VDD

CONTROL0 11
CONTROL1 12
CONTROL2 13
GND 14
CONTROL3 15
CONTROL4 16
GND 17
CONTROL5 18
CONTROL6 19
CONTROL7 20
MHOLE 21

Clock Board Header

CK_LOGIC_FPGA0_P
CK_LOGIC_FPGA0_N

CK_LOGIC_FPGA1_P
CK_LOGIC_FPGA1_N

GND

GND

R1 100
R2 100
R3 100

R4 100
R5 100

R6 100
R7 100
R8 100

CTL_RADIO_EN
CTL_RADIO_CSB
CTL_RADIO_SDIO

CTL_RADIO_CLK
CTL_LOGIC_EN

CTL_LOGIC_CSB
CTL_LOGIC_SDIO
CTL_LOGIC_CLK

C14 220pF C15 220pF C16 220pF C17 220pF T4 NTS4001N

C18 220pF C19 220pF C20 220pF C21 220pF T3 NTS4001N

GND

GND

VCC_LOGIC

L6 HZ0805E601R-00
L5 HZ0805E601R-00
L4 NM - HZ0805E601R-00

C13 1.0uF C8 10uF

GND

C3 0.01uF C2 0.01uF C4 0.01uF C5 0.01uF C1 1.0uF C6 1.0uF C9 10uF

TP1 1

GND

L1 HZ0805E601R-00
L2 HZ0805E601R-00
L3 NM - HZ0805E601R-00

C12 1.0uF C7 10uF

TP2 1

VCC_RADIO

WARP Clock Board schematic (Sheet 3 of 4), Rice University - CMC. AD9510 clock distribution circuit with MMCX connectors, 1X LVPECL (AC) and 4X LVCMOS (AC, 33.3% FULL-SCALE SWING) outputs.

VCC_LOGIC

R14 · NM - 0

U2A — AD9510

Pin	Signal	Pin	Signal
63	CPRSET	5	VCP
61	RSET	6	CP
16	FUNC	17	STATUS
1	REFIN	58	OUT0
2	REFINB	57	OUT0B
14	CLK1	54	OUT1
15	CLK1B	53	OUT1B
10	CLK2	35	OUT2
11	CLK2B	34	OUT2B
18	SCLK	29	OUT3
19	SDIO	28	OUT3B
20	SDO	47	OUT4
21	CSB	46	OUT4B
		43	OUT5
		42	OUT5B
		39	OUT6
		38	OUT6B
		25	OUT7
		24	OUT7B

CTL_LOGIC_EN
CTL_LOGIC_CLK
CTL_LOGIC_SDIO
CTL_LOGIC_CSB

4X DIFF. LVPECL (AC)

R76 215, R25 0, C34 0.1uF — Jumper-4 J8 — CK_LOGIC_DC0_P / CK_LOGIC_DC0_N
R78 215, R27 0, C36 0.1uF
R80 215, R29 0, C38 0.1uF — Jumper-4 J7 — CK_LOGIC_DC1_P / CK_LOGIC_DC1_N
R82 215, R31 0, C41 0.1uF
R90 215, R40 0, C51 0.1uF — Jumper-4 J9 — CK_LOGIC_DC2_P / CK_LOGIC_DC2_N
R91 215, R39 0, C50 0.1uF
R83 215, R32 0, C42 0.1uF — Jumper-4 J13 — CK_LOGIC_DC3_P / CK_LOGIC_DC3_N
R81 215, R30 0, C40 0.1uF

LVDS (3.3V)

R44 0, R48 NM - 215 — CK_LOGIC_FPGA0_P
R43 0, R47 NM - 215 — CK_LOGIC_FPGA0_N
R46 NM - 215

LVCMOS

R42 10, R45 NM - 215 — CK_LOGIC_FPGA1_P
R41 10 — CK_LOGIC_FPGA1_N

1X LVCMOS (AC, 33% FULL-SCALE SWING INTO Rt = 50 OHMS)

R28 60, C37 0.1uF, R79 NM - 100 — CK_LOGIC_EXT_P — J5 MMCX Conn.
R26 60, C35 0.1uF, R75 NM - 100
R77 50

J3 MMCX Conn.
2 GND, 3 GND PIN, 4 GND, 5 GND

R63 NM - 50
T2 · TC1-1T
R65 NM - 0
R66 NM - 0
R13 25, C28 0.1uF
R12 25, C27 0.1uF
C61 0.1uF

GND

VCC_LOGIC
R52 NM - 1K
Y3 NM - 40 MHz (VC VCC GND OUT)
Y2 NM - 40 MHz (OE VDD GND OUT)
R62 NM - 1K
C59 NM - 0.1uF
C52 NM - 0.01uF
C56 0.01uF
C57 0.1uF

R20 NM - 5.1K
R23 4.12K
C74 0.1uF
R24 NM - 4.75K

VCC_LOGIC
C111 0.01uF
C113 0.01uF
C110 0.01uF
C112 0.01uF
C10 0.01uF
C11 0.01uF
C62 0.01uF

U2B — AD9510

Pin	Signal	Pin	Signal
3	GND	4	VS
7	GND	9	VS
8	GND	13	VS
12	GND	23	VS
22	GND	26	VS
27	GND	30	VS
32	GND	31	VS
49	GND	33	VS
50	GND	36	VS
55	GND	37	VS
62	GND	40	VS
		41	VS
		44	VS
		45	VS
		48	VS
		51	VS
		56	VS
		59	VS
		60	VS
		64	VS

VCC_LOGIC

C85 0.01uF, C104 0.01uF, C109 0.01uF, C105 0.01uF, C78 0.01uF, C94 0.01uF, C88 0.01uF, C75 0.01uF, C73 0.01uF, C72 0.01uF, C93 0.01uF, C103 0.01uF, C106 0.01uF, C107 0.01uF, C108 0.01uF, C92 0.1uF, C102 0.1uF, C101 0.1uF, C89 0.1uF, C95 0.1uF, C84 0.1uF, C82 0.1uF, C29 1.0uF, C43 1.0uF, C24 1.0uF

GND