TAP Radio Board

MAX2829 Version - Rev x1

Schematic Pages:

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2 - MAX2829 RF Transceiver
3 - Rx A/D Converter
4 - Tx D/A Converter
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SiGe Semiconductor: SE2542A dual-band front end module
  requested docs/samples 2005-01-17

SkyWorks: SKY65200 dual-band front end module
  requested docs/samples 2005-01-18

Epcos: R005, R012 dual-band front end module
  requested docs/samples 2005-01-19

Johanson parts
Requested samples 2005-01-29
2450BP15B100
2450DP15D5400
2450DP15E5400
5515BP15C975

Ant Switch:
CEL UPG2035T5F-A
Mouser: 551-UPG2035T5F-A
Arrow: available min 1

Dualband PA (IRM046U):
Sharp sales: 408-436-4900
ION assoc: 281-376-2000

CMC - Rice University	
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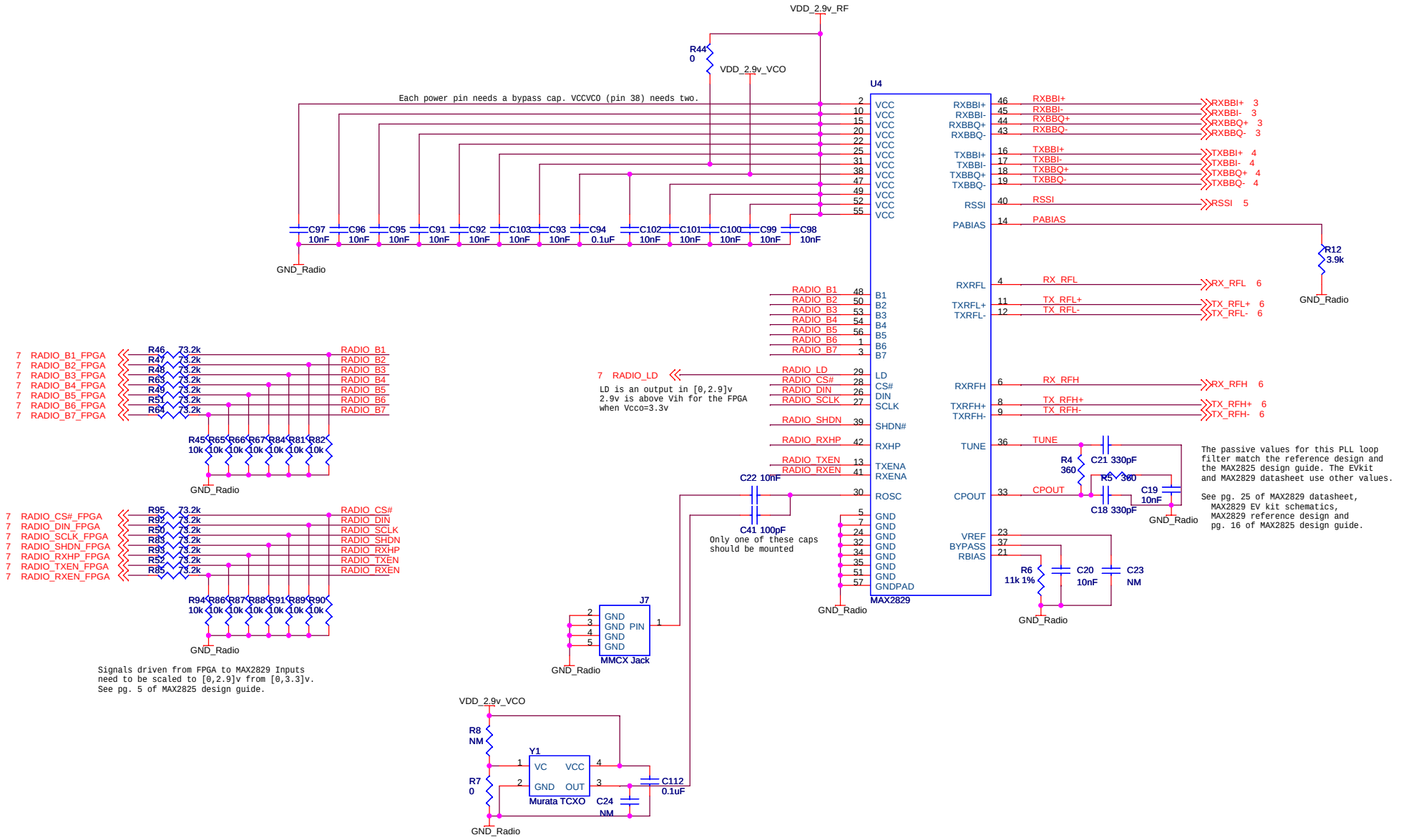
VDD_2.9v_RF
R44 0
VDD_2.9v_VCO
Each power pin needs a bypass cap. VCCVCO (pin 38) needs two.
U4
C97 10nF
C96 10nF
C95 10nF
C91 10nF
C92 10nF
C103 10nF
C93 10nF
C94 0.1uF
C102 10nF
C101 10nF
C100 10nF
C99 10nF
C98 10nF
GND_Radio
RXBBI+
RXBBI-
RXBBQ+
RXBBQ-
TXBBI+
TXBBI-
TXBBQ+
TXBBQ-
RSSI
PABIAS
R12 3.9k
RXRFL
TXRFL+
TXRFL-
RXRFH
TXRFH+
TXRFH-
TUNE
CPOUT
VREF
BYPASS
RBIAS
R4 360
C21 330pF
R5 360
C19 10nF
C18 330pF
R6 11k 1%
C20 10nF
C23 NM
The passive values for this PLL loop filter match the reference design and the MAX2825 design guide. The EVkit and MAX2829 datasheet use other values.
See pg. 25 of MAX2829 datasheet, MAX2829 EV kit schematics, MAX2829 reference design and pg. 16 of MAX2825 design guide.
RADIO_B1
RADIO_B2
RADIO_B3
RADIO_B4
RADIO_B5
RADIO_B6
RADIO_B7
RADIO_LD
RADIO_CS#
RADIO_DIN
RADIO_SCLK
RADIO_SHDN
RADIO_RXHP
RADIO_TXEN
RADIO_RXEN
LD is an output in [0,2.9]v
2.9v is above Vih for the FPGA
when Vcco=3.3v
C22 10nF
C41 100pF
Only one of these caps
should be mounted
MAX2829
R46 R47 R48 R63 R49 R51 R64 73.2k
R45 R65 R66 R67 R84 R81 R82 10k
RADIO_B1_FPGA
RADIO_B2_FPGA
RADIO_B3_FPGA
RADIO_B4_FPGA
RADIO_B5_FPGA
RADIO_B6_FPGA
RADIO_B7_FPGA
R95 R92 R50 R83 R93 R52 R85 73.2k
R94 R86 R87 R88 R91 R89 R90 10k
RADIO_CS#_FPGA
RADIO_DIN_FPGA
RADIO_SCLK_FPGA
RADIO_SHDN_FPGA
RADIO_RXHP_FPGA
RADIO_TXEN_FPGA
RADIO_RXEN_FPGA
Signals driven from FPGA to MAX2829 Inputs
need to be scaled to [0,2.9]v from [0,3.3]v.
See pg. 5 of MAX2825 design guide.
J7
GND
GND PIN
MMCX Jack
VDD_2.9v_VCO
R8 NM
R7 0
Y1
VC
VCC
GND
OUT
Murata TCXO
C24 NM
C112 0.1uF
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DVDD_3.3v

AVDD_3.3v

C161+ 10uF — Bypass for DRVDD pins

C172 0.1uF, C171 0.1uF, C170 0.1uF

C153 1.0nF, C160 1.0nF, C156 1.0nF

DGND

C163+ 10uF — Bypass for AVDD pins

C175 0.1uF, C173 0.1uF, C176 0.1uF

C157 1.0nF, C162 1.0nF, C158 1.0nF, C159 1.0nF

DGND

DVDD_3.3v

AVDD_3.3v

U5

29	DRVDD	AVDD	64
41	DRVDD	AVDD	17
52	DRVDD	AVDD	12
		AVDD	5

ADC_RX_DA0 … ADC_RX_DA13 — 7 ADC_RX_DA[0:13]

42	DA_0	
43	DA_1	
44	DA_2	
45	DA_3	
46	DA_4	
47	DA_5	
48	DA_6	
49	DA_7	
50	DA_8	
51	DA_9	
54	DA_10	
55	DA_11	
56	DA_12	
57	DA_13	

ADC_RX_DB0 … ADC_RX_DB13 — 7 ADC_RX_DB[0:13]

23	DB_0	
24	DB_1	
25	DB_2	
26	DB_3	
27	DB_4	
30	DB_5	
31	DB_6	
32	DB_7	
33	DB_8	
34	DB_9	
35	DB_10	
36	DB_11	
37	DB_12	
38	DB_13	

7 ADC_RX_OTRA, 7 ADC_RX_OTRB — ADC_RX_OTRA, ADC_RX_OTRB

58	OTR_A	
39	OTR_B	

7 ADC_RX_DCS, 7 ADC_RX_DFS — ADC_RX_DCS, ADC_RX_DFS

19	DCS	
20	DFS	

7 ADC_RX_PWDNA, 7 ADC_RX_PWDNB — ADC_RX_PWDNA, ADC_RX_PWDNB

60	PDWN_A	
21	PDWN_B	

59	OEB_A	
22	OEB_B	
28	DRGND	
40	DRGND	
53	DRGND	

R23 0, R24 0

DGND

2	VIN_A+	RXBBI+
3	VIN_A-	RXBBI-
15	VIN_B+	RXBBQ+
14	VIN_B-	RXBBQ-

RXBBI+ 2, RXBBI- 2, RXBBQ+ 2, RXBBQ- 2

DC coupled signals from MAX2829 baseband output
Vdm = 1.76Vp-p, Vcm = 0.96v, which is in the allowed range for the AD9238

See pg. 6 of the MAX2825 design guide and pg. 13 of AD9238 datasheet

6	REFT_A	C38 0.1uF, + C165 10uF, C35 0.1uF
7	REFB_A	R19 0, R20 0, C39 0.1uF
11	REFT_B	C36 0.1uF, + C166 10uF, C34 0.1uF
10	REFB_B	C37 0.1uF
8	VREF	+ C167 10uF, C30 0.1uF
9	SENSE	R17 1.07k 0.1%, R18 1.4k 0.1%

AGND

ADCs are configured to share a reference
=> REFx_A = REFx_B
See pg. 15 of AD9238 datasheet

MAX2829 Rx outputs swing 1.76Vp-p
AD9248 input span is 2 x Vref
Vref=0.5x(1 + R2/R1)
=> Span = 1 + (1.07k/1.4k) = 1.764Vp-p

See pg. 6 of MAX2825 design guide and pg. 15 of AD9238 datasheet

(1.4k - DigiKey RR08P1.4KBCT-ND)

63	CLK_A	ADC_RX_CLKA	ADC_RX_CLKA 8
18	CLK_B	ADC_RX_CLKB	ADC_RX_CLKB 8

Parallel termination for the clock signals
(just in case; probably won't be used)

AVDD_3.3v

61	MUX_SEL	R21 0
62	SHARED_REF	R22 NM

16	AGND	
13	AGND	
4	AGND	
1	AGND	

AGND

AD9248

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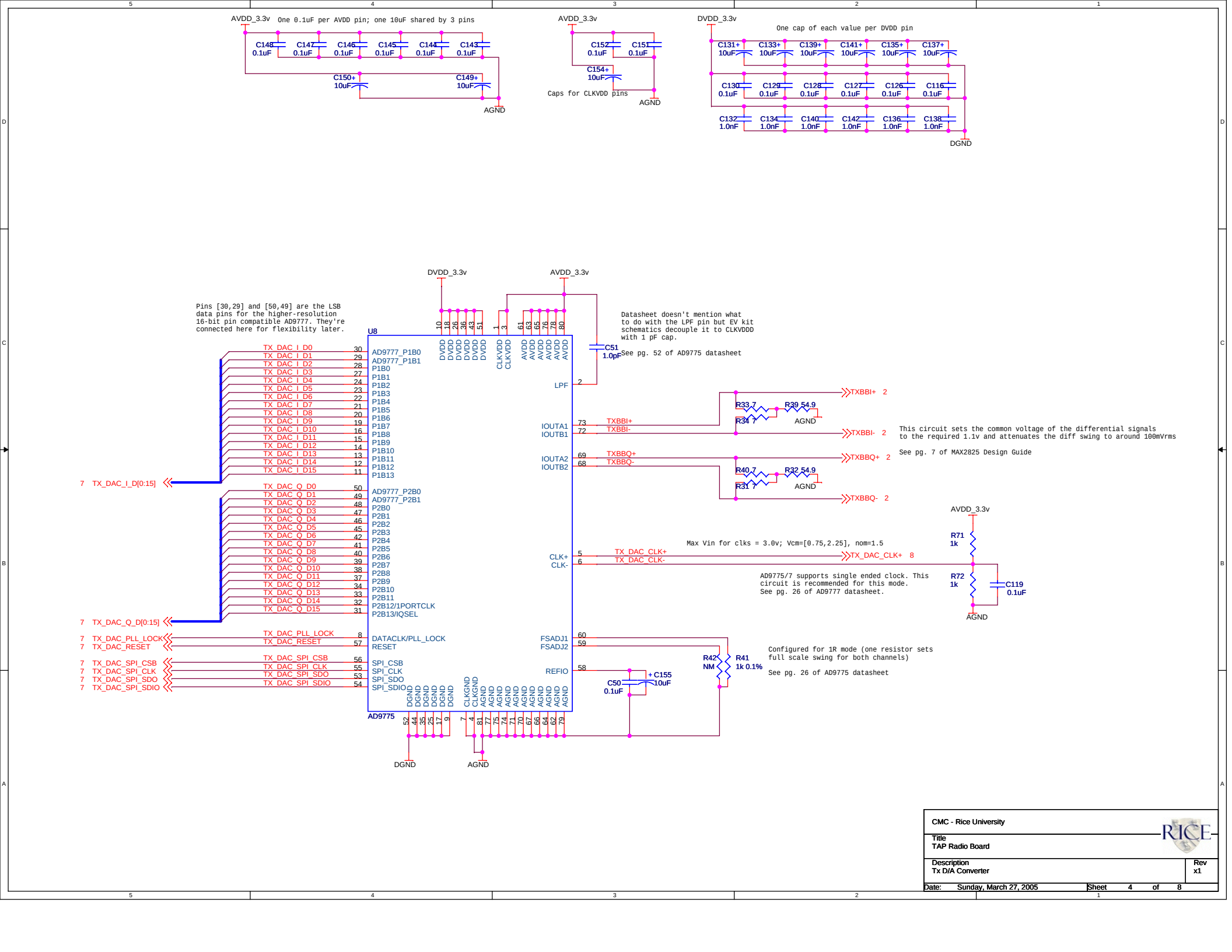
AVDD_3.3v
One 0.1uF per AVDD pin; one 10uF shared by 3 pins
C148 0.1uF
C147 0.1uF
C146 0.1uF
C145 0.1uF
C144 0.1uF
C143 0.1uF
C150+ 10uF
C149+ 10uF
AGND
AVDD_3.3v
C152 0.1uF
C151 0.1uF
C154+ 10uF
Caps for CLKVDD pins
AGND
DVDD_3.3v
One cap of each value per DVDD pin
C131+ 10uF
C133+ 10uF
C139+ 10uF
C141+ 10uF
C135+ 10uF
C137+ 10uF
C130 0.1uF
C129 0.1uF
C128 0.1uF
C127 0.1uF
C126 0.1uF
C116 0.1uF
C132 1.0nF
C134 1.0nF
C140 1.0nF
C142 1.0nF
C136 1.0nF
C138 1.0nF
DGND
DVDD_3.3v
AVDD_3.3v
Pins [30,29] and [50,49] are the LSB data pins for the higher-resolution 16-bit pin compatible AD9777. They're connected here for flexibility later.
U8
AD9777
DVDD
CLKVDD
AVDD
Datasheet doesn't mention what to do with the LPF pin but EV kit schematics decouple it to CLKVDDD with 1 pF cap.
C51 1.0pF
See pg. 52 of AD9775 datasheet
LPF
TX_DAC_I_D0
TX_DAC_I_D1
TX_DAC_I_D2
TX_DAC_I_D3
TX_DAC_I_D4
TX_DAC_I_D5
TX_DAC_I_D6
TX_DAC_I_D7
TX_DAC_I_D8
TX_DAC_I_D9
TX_DAC_I_D10
TX_DAC_I_D11
TX_DAC_I_D12
TX_DAC_I_D13
TX_DAC_I_D14
TX_DAC_I_D15
7 TX_DAC_I_D[0:15]
AD9777_P1B0
AD9777_P1B1
P1B0
P1B1
P1B2
P1B3
P1B4
P1B5
P1B6
P1B7
P1B8
P1B9
P1B10
P1B11
P1B12
P1B13
IOUTA1
IOUTB1
IOUTA2
IOUTB2
TXBBI+
TXBBI-
TXBBQ+
TXBBQ-
R33 7
R34 7
R39 54.9
R40 7
R31 7
R32 54.9
AGND
TXBBI+ 2
TXBBI- 2
TXBBQ+ 2
TXBBQ- 2
This circuit sets the common voltage of the differential signals to the required 1.1v and attenuates the diff swing to around 100mVrms
See pg. 7 of MAX2825 Design Guide
TX_DAC_Q_D0
TX_DAC_Q_D1
TX_DAC_Q_D2
TX_DAC_Q_D3
TX_DAC_Q_D4
TX_DAC_Q_D5
TX_DAC_Q_D6
TX_DAC_Q_D7
TX_DAC_Q_D8
TX_DAC_Q_D9
TX_DAC_Q_D10
TX_DAC_Q_D11
TX_DAC_Q_D12
TX_DAC_Q_D13
TX_DAC_Q_D14
TX_DAC_Q_D15
7 TX_DAC_Q_D[0:15]
AD9777_P2B0
AD9777_P2B1
P2B0
P2B1
P2B2
P2B3
P2B4
P2B5
P2B6
P2B7
P2B8
P2B9
P2B10
P2B11
P2B12/1PORTCLK
P2B13/IQSEL
CLK+
CLK-
TX_DAC_CLK+
TX_DAC_CLK-
Max Vin for clks = 3.0v; Vcm=[0.75,2.25], nom=1.5
AD9775/7 supports single ended clock. This circuit is recommended for this mode.
See pg. 26 of AD9777 datasheet.
R71 1k
R72 1k
C119 0.1uF
AVDD_3.3v
AGND
7 TX_DAC_PLL_LOCK
7 TX_DAC_RESET
TX_DAC_PLL_LOCK
TX_DAC_RESET
DATACLK/PLL_LOCK
RESET
7 TX_DAC_SPI_CSB
7 TX_DAC_SPI_CLK
7 TX_DAC_SPI_SDO
7 TX_DAC_SPI_SDIO
TX_DAC_SPI_CSB
TX_DAC_SPI_CLK
TX_DAC_SPI_SDO
TX_DAC_SPI_SDIO
SPI_CSB
SPI_CLK
SPI_SDO
SPI_SDIO
FSADJ1
FSADJ2
REFIO
R42 NM
R41 1k 0.1%
Configured for 1R mode (one resistor sets full scale swing for both channels)
See pg. 26 of AD9775 datasheet
C50 0.1uF
+ C155 10uF
DGND
AGND
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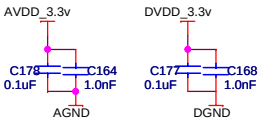

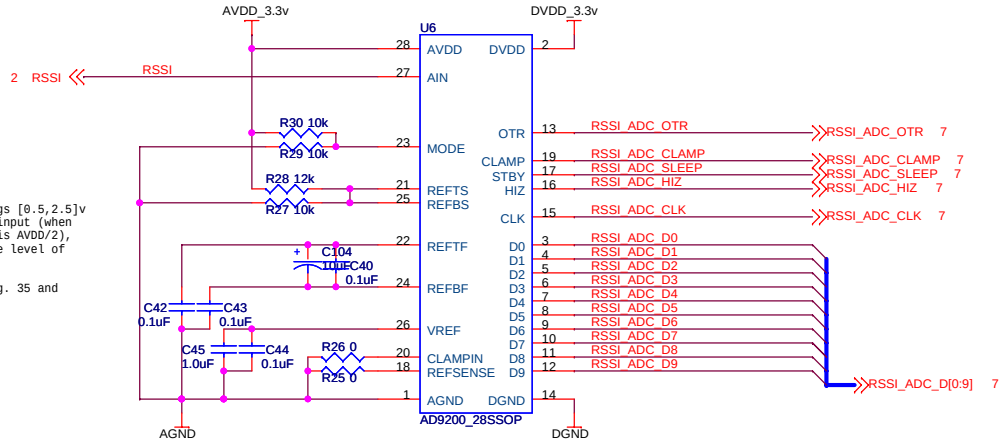

MAX2829 RSSI signal swings [0.5,2.5]v
AD9200 supports a 2Vp-p input (when
REFSENSE is 0v and MODE is AVDD/2),
so this needs a mid-range level of
1.5v=REFTS=REFBS.

See MAX2829 datasheet, pg. 35 and
AD9200 datasheet, pg. 11

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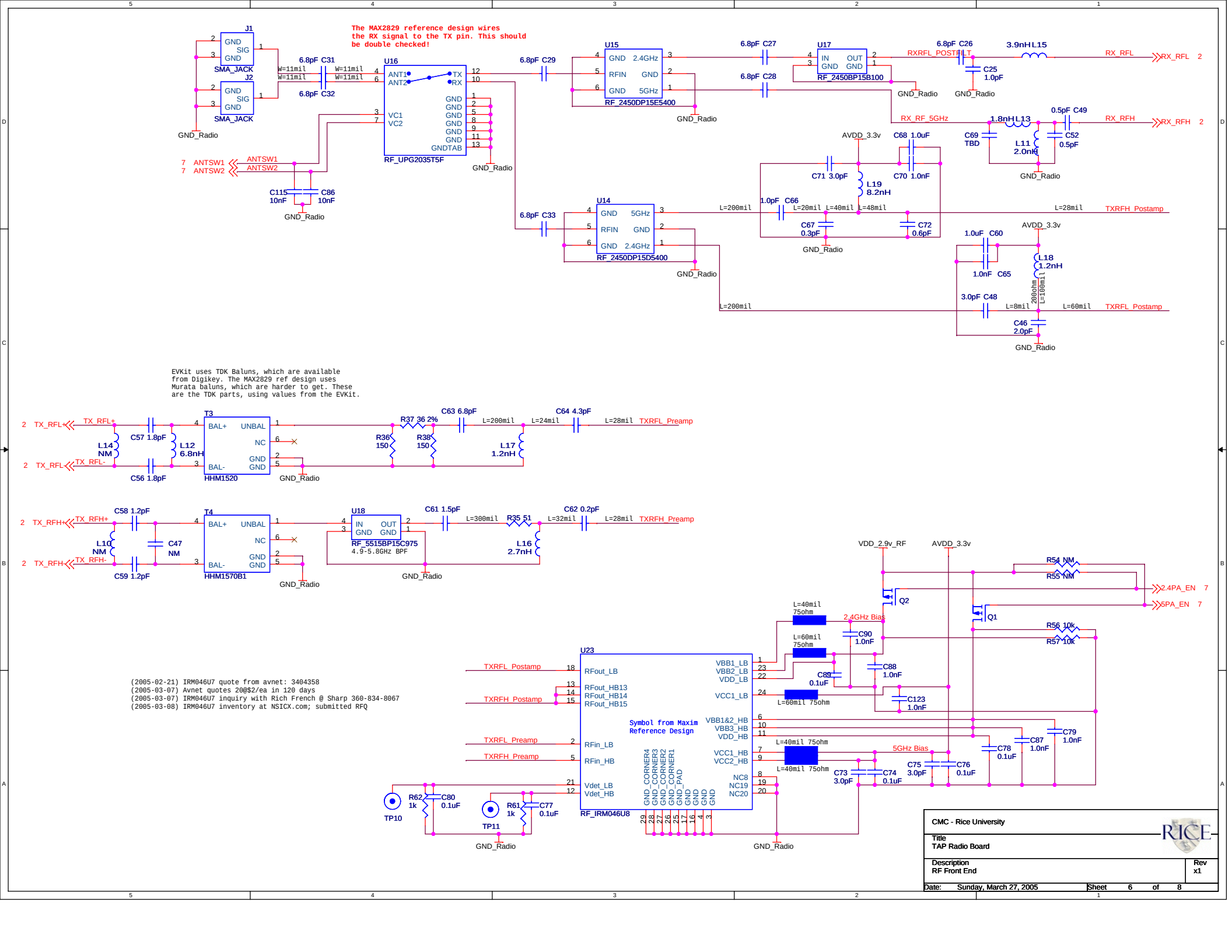
The MAX2829 reference design wires the RX signal to the TX pin. This should be double checked!
J1
SMA_JACK
J2
SMA_JACK
GND_Radio
6.8pF C31
6.8pF C32
W=11mil
U16
ANT1
ANT2
TX
RX
VC1
VC2
GND
GNDTAB
RF_UPG2035T5F
ANTSW1
ANTSW2
C115 10nF
C86 10nF
6.8pF C29
U15
GND 2.4GHz
RFIN
GND 5GHz
RF_2450DP15E5400
6.8pF C27
6.8pF C28
U17
IN OUT
GND GND
RF_2450BP15B100
6.8pF C26
RXRFL_POSTFILT
C25 1.0pF
3.9nH L15
RX_RFL
RX_RFL 2
RX_RF_5GHz
1.8nH L13
0.5pF C49
RX_RFH
RX_RFH 2
C69 TBD
L11 2.0nH
C52 0.5pF
AVDD_3.3v
C68 1.0uF
C70 1.0nF
C71 3.0pF
L19 8.2nH
6.8pF C33
U14
RF_2450DP15D5400
L=200mil
1.0pF C66
L=20mil
L=40mil
L=48mil
L=28mil
TXRFH_Postamp
C67 0.3pF
C72 0.6pF
1.0uF C60
1.0nF C65
L18 1.2nH
200ohm L=100mil
3.0pF C48
L=8mil
L=60mil
TXRFL_Postamp
C46 2.0pF
EVKit uses TDK Baluns, which are available from Digikey. The MAX2829 ref design uses Murata baluns, which are harder to get. These are the TDK parts, using values from the EVKit.
TX_RFL+
TX_RFL-
T3
BAL+
BAL-
UNBAL
NC
GND
HHM1520
L14 NM
C57 1.8pF
L12 6.8nH
C56 1.8pF
C63 6.8pF
R37 36 2%
R36 150
R38 150
L17 1.2nH
C64 4.3pF
L=24mil
TXRFL_Preamp
TX_RFH+
TX_RFH-
T4
HHM1570B1
C58 1.2pF
L10 NM
C47 NM
C59 1.2pF
U18
IN OUT
GND GND
RF_5515BP15C975
4.9-5.8GHz BPF
C61 1.5pF
L=300mil
R35 51
L=32mil
L16 2.7nH
C62 0.2pF
TXRFH_Preamp
(2005-02-21) IRM046U7 quote from avnet: 3404358
(2005-03-07) Avnet quotes 20@$2/ea in 120 days
(2005-03-07) IRM046U7 inquiry with Rich French @ Sharp 360-834-8067
(2005-03-08) IRM046U7 inventory at NSICX.com; submitted RFQ
U23
RFout_LB
RFout_HB13
RFout_HB14
RFout_HB15
RFin_LB
RFin_HB
Vdet_LB
Vdet_HB
VBB1_LB
VBB2_LB
VDD_LB
VCC1_LB
VBB1&2_HB
VBB3_HB
VDD_HB
VCC1_HB
VCC2_HB
NC8
NC19
NC20
GND_CORNER4
GND_CORNER3
GND_CORNER2
GND_CORNER1
GND_PAD
Symbol from Maxim Reference Design
RF_IRM046U8
TXRFL_Postamp
TXRFH_Postamp
TXRFL_Preamp
TXRFH_Preamp
TP10
TP11
R62 1k
C80 0.1uF
R61 1k
C77 0.1uF
VDD_2.9v_RF
AVDD_3.3v
Q2
Q1
R54 NM
R55 NM
2.4PA_EN 7
5PA_EN 7
R56 10k
R57 10k
L=40mil 75ohm
2.4GHz Bias
C90 1.0nF
L=60mil 75ohm
C88 1.0nF
C89 0.1uF
C123 1.0nF
L=40mil 75ohm
5GHz Bias
C73 3.0pF
C74 0.1uF
C75 3.0pF
C76 0.1uF
C78 0.1uF
C87 1.0nF
C79 1.0nF
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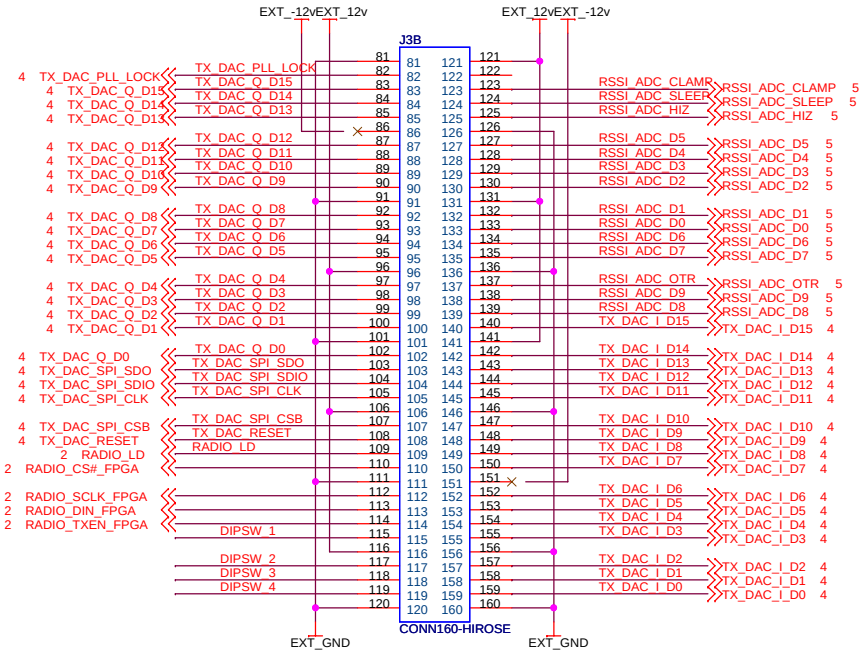

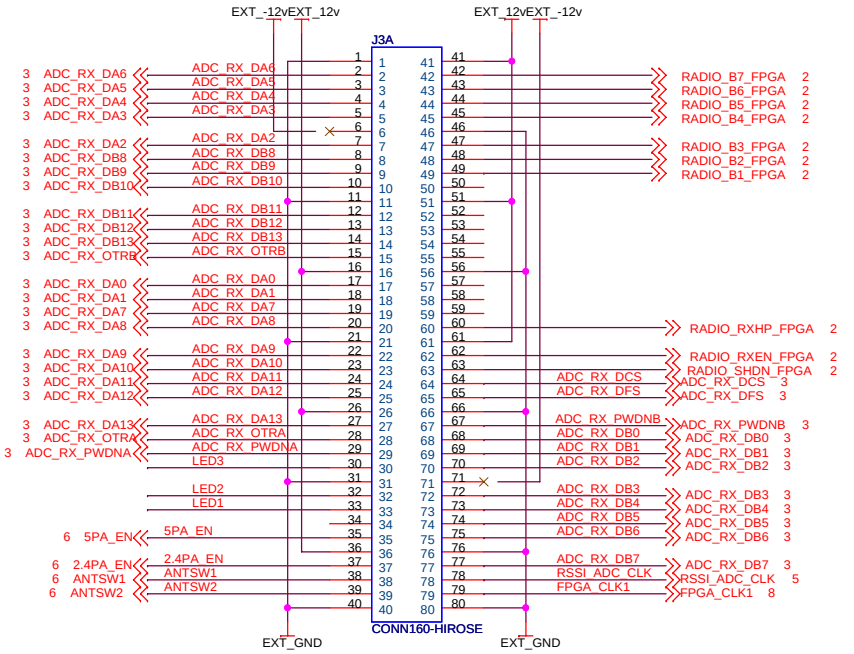

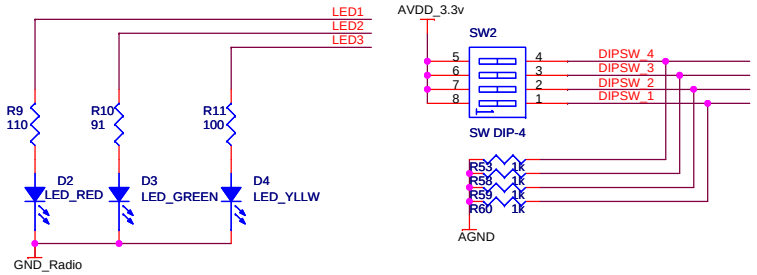

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FPGA Board Headers

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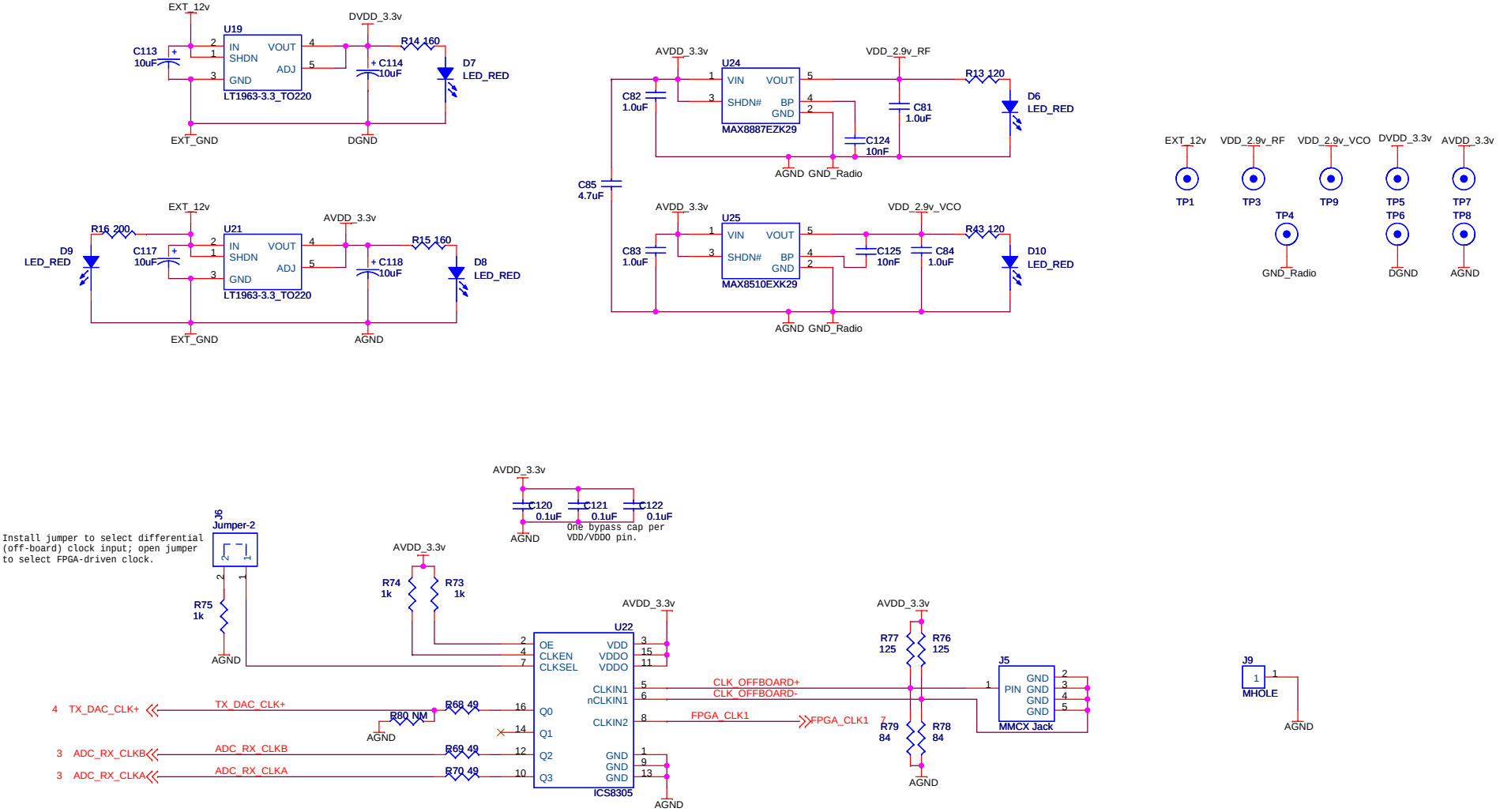

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